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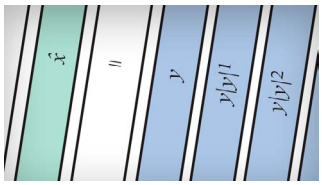
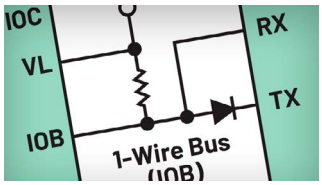


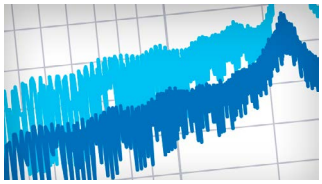
5 Digital Predistortion for RF Communications: From Equations to Implementation

Digital predistortion (DPD) is an acronym that will be familiar to many RF (radio frequency) engineers, signal processing enthusiasts, and embedded software developers. When an RF signal is outputted from a base station radio, it needs to be amplified before it is transmitted through the antenna. In an ideal world, an RF power amplifier would just amplify the input signal. But this isn't an ideal world. PAs are nonlinear.



10 Simplifying TWS Earbud Designs with 1-Wire Connectivity

Since mainstream mobile phone manufacturers are gradually removing the headphone jack, true wireless stereo (TWS) earbud technology has developed rapidly and continues to gain popularity, even surpassing conventional Bluetooth® earbuds. This article demonstrates a design that applies a unique 1 Wire® technology to the TWS solution while overcoming challenges such as cost, power, accuracy, size, and high efficiency.

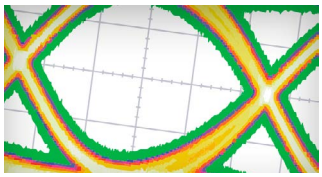


19 Low Noise Silent Switcher µModule and LDO Regulators Improve Ultrasound Noise and Image Quality

In the field of medical diagnostics, there is an ever increasing demand for higher image quality from ultrasound imaging systems. One of the key techniques for image quality improvement is to enhance the signal-to-noise ratio of the system. This article presents a brief introduction to the ultrasound system and a detailed analysis of power management design within this system.

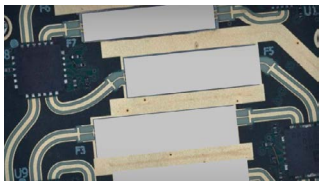
24 Rarely Asked Questions—Issue 200: Practical Tips for Measuring Ultralow Bias Current Using Commercial-Grade Lab Equipment

The next article will discuss practical tips for measuring ultralow bias current. In applications where low leakage current is required, it is important to select a low input bias current (I_B) operational amplifier. This article explains how to use commercial-grade lab equipment, jigs, and materials that are commonly available and some workarounds to improve and simplify the femtoampere measuring process.



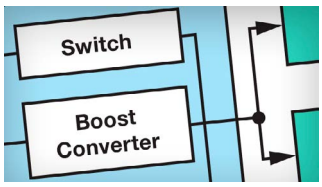
28 Accelerate Your Test Capability and System Productivity with New MEMS Switches

This article covers advancements in MEMS technology. Advanced digital processor chips require separate DC parametric and high speed digital automatic test equipment (ATE) passes for quality assurance. One additional critical aspect is the increasing number of transmission (Tx)/receiver (Rx) channels that require both high speed digital and DC parametric testing.



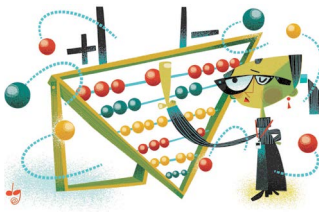
32 High IF Sampling Puts Wideband Software-Defined Radio Within Reach

This article explains the technology advancements enabled by the new ICs of wideband software-defined radio that are expected to change and enhance multiband radar architectures. In the past, high performance integrated frequency translation ICs employing suboctave RF filtering and gain control were hard to define because everybody's use case, frequency plan, and resulting RF/IF filtering was different.



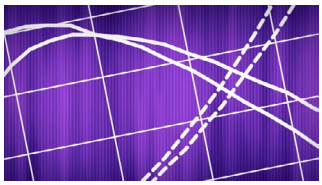
37 What Are the Best Applications for IoT in the New World of IC Power Management?

With the growth of IoT devices used in industrial equipment, home automation, and medical applications, there is increasing pressure to optimize power management. This article explores IoT battery technology, describes some of the problems that designers face with power sourcing, and presents highly efficient solutions.



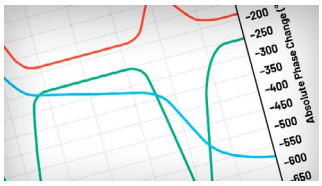
42 Rarely Asked Questions—Issue 201: How to Measure Op Amp Input Capacitance to Minimize Noise

Operational amplifiers are used in a wide variety of electronic circuits. Their task is to amplify (very small) electrical voltages for further signal processing. To maximize the accuracy of a corresponding circuit, it is necessary to know the input capacitance of the op amp.



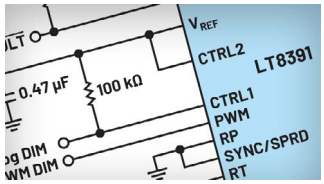
44 How Monolithic Driver + MOSFET (DrMOS) Technology Improves Power System Design

This article covers the latest DrMOS technology and its advantages in voltage regulator module applications. Monolithic DrMOS devices improve power density, efficiency, and thermal performance, which can enhance the overall performance of end applications. An excellent solution for an optimized high speed power converter includes an advanced switching MOSFET—a major building block of voltage regulators—and its corresponding driver in a single, monolithic package.



50 How Digitally Tunable Filters Enable Wideband Receiver Applications

In today's multichannel, wideband multioctave tuning RF receivers, it is often necessary to eliminate unwanted blockers to preserve the fidelity of signals of interest. Filters have played an essential role in reducing these unwanted signals, particularly in the receiver RF front end and local oscillator portions of these systems. This article discusses filters within RF signal chains, the concept of blocker signals, traditional filtering technologies, and the latest product solutions for optimizing signal chain performance.



58 Automotive LED Driver Power Conversion Topology Guide

In many systems, including the myriad of regulators deployed in automotive power-delivery systems, the design of power-conversion regulators is often a difficult and complex task. Driving LED strings can make the selection of power-conversion methods even more complex. To simplify the selection process, this article explains the benefits, trade-offs, and applications for different switching topologies used for LED drivers in automotive lighting.

62 Rarely Asked Questions—Issue 202: RF Demystified: Scattering Parameters and Their Types

This article continues our series about how to solve much of the RF mystery for non-RF engineers. This time we will talk about the most basic term one needs to know to describe any RF component—the scattering parameters (or S-parameters). Previous topics include: "RF Demystified—Understanding Wave Reflections" and "How to Easily Select the Right Frequency Generation Component."

Bernhard Siegel,
Editor in Chief

Bernhard became editor in chief of *Analog Dialogue* in March 2017. He has been with Analog Devices for over 30 years, starting at the ADI Munich office in Germany. In his current role as the editor in chief, he is responsible for the worldwide technical article program within Analog Devices.

Bernhard has worked in various engineering roles including sales, field applications, and product engineering, as well as in technical support and marketing roles.

Residing near Munich, Germany, Bernhard enjoys spending time with his family and playing trombone and euphonium in both a brass band and a symphony orchestra.

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AnalogDialogue

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Digital Predistortion for RF Communications: From Equations to Implementation

Claire Masterson, Systems Engineer

Abstract

This article covers the mathematical fundamentals of digital predistortion (DPD) and how it is implemented in a transceiver's microprocessor and hardware. It addresses why DPD is needed in modern communication systems and explores how the mathematical model captures real-world signal distortion.

Introduction

DPD is an acronym that will be familiar to many RF (radio frequency) engineers, signal processing enthusiasts, and embedded software developers. DPD is ubiquitous in our cellular communications systems, enabling power amplifiers (PAs) to efficiently deliver maximum power to an antenna. As 5G drives up the antenna count in base stations and our spectrum becomes ever more congested, DPD has emerged as a key technology to allow for the development of efficient, cost-effective, and specification compliant cellular systems.

Many of us have a unique understanding of DPD based on our own perspectives, be that from the purely mathematical viewpoint or the more constrained implementation on a microprocessor. Perhaps you're an engineer evaluating the performance of DPD in your RF base station product or an algorithm developer who is curious as to how mathematical modeling techniques are implemented in real world-systems. This article aims to broaden your knowledge and empower you to fully grasp the topic from all angles.

What Is DPD and Why Is It Used?

When an RF signal is outputted from a base station radio (see Figure 1), it needs to be amplified before it is transmitted through the antenna. An RF PA is used to do this. In an ideal world, the PA takes an input signal and outputs a higher power signal that is proportional to its input. It also does this in the most power efficient way possible so that most of the DC power supply provided to the amplifier is converted into signal output power.

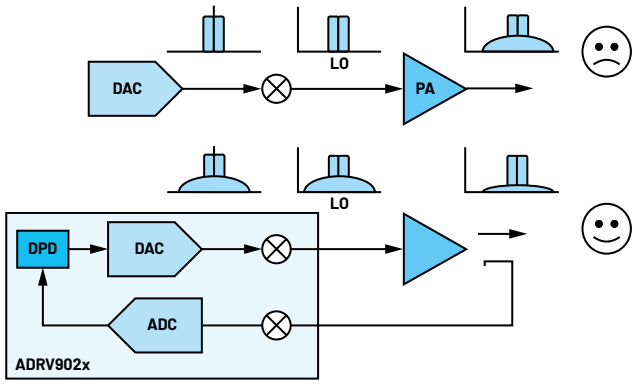


Figure 1. Block diagram of a simplified radio structure with and without DPD.

However, this isn't an ideal world. PAs are made from transistors, which are active devices and inherently nonlinear. Now if we use PAs in their "linear" region (linear here is a relative term; hence, the quotation marks) as shown in Figure 2, then the output power is relatively proportional to the input power. The downside of this approach is that the PA is generally used in a very inefficient state with most of the power provided being lost as heat. We often want to use PAs at the point where they are beginning to compress. That means if the input signal is increased by a set amount (say 3 dB), the PA output does not increase by the same amount (maybe only by 1 dB). Obviously, the signal is being significantly distorted at this point by the amplifier.

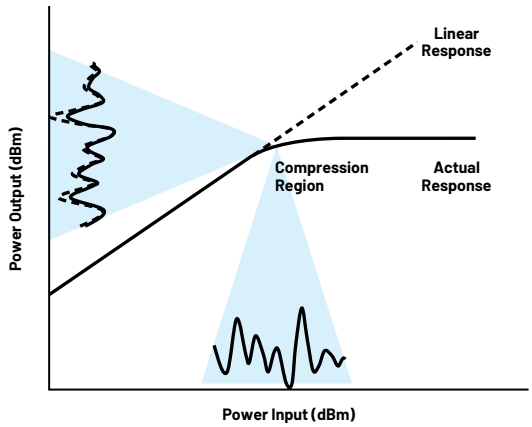


Figure 2. PA input power vs. output power plot (shows projection of sample input/output signals).

This distortion happens at known places in the frequency domain dependent on the input signal. Figure 3 shows these locations and the relationship between the fundamental frequencies and these distortion products. In RF systems, the only distortions we need to compensate for are those close to the fundamental signal, which are the odd order intermodulation products. Filtering in the system takes care of the out of band products (harmonics and even order intermodulation products). Figure 4 shows the output of an RF PA run near its compression point. The intermodulation products (especially the third order) are clearly visible. They look like "skirts" around the desired signal.

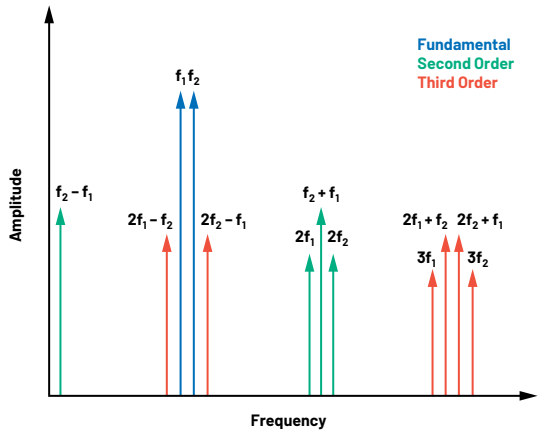


Figure 3. Location of intermodulation and harmonic distortion for 2 tone input.

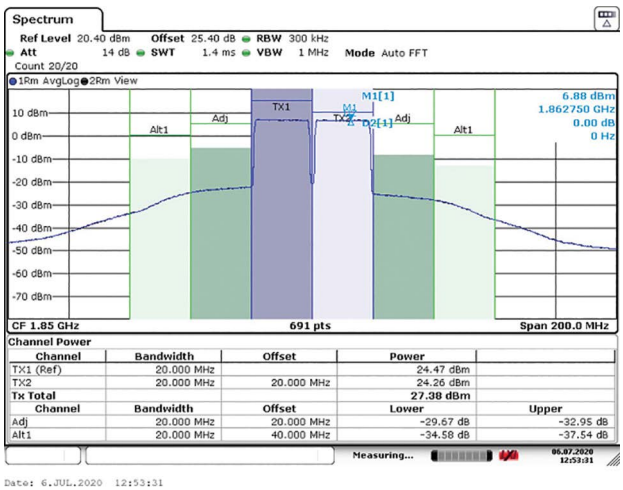


Figure 4. 2× 20 MHz carriers passed through SKY66391-12 RF PA. The center frequency = 1850 MHz.

DPD aims to characterize this distortion by observing the PA output and, knowing the wanted output signal, altering the input signal so that the PA output is closer to the ideal. This can only be done effectively in fairly specific circumstances. We need to have the amplifier and input signal configured such that the amplifier is compressing somewhat but not completely saturating.

The Math Behind Modeling PA Distortion

Do the sight of Greek letters and other mathematical symbols tend to bring on terrifying flashbacks of college exams of yesteryear? You're not alone! People can be unnecessarily put off by the fundamentals when one of the first references they are given is a math heavy academic paper. The paper "A Generalized Memory Polynomial Model for Digital Predistortion of RF Power Amplifiers"[1] is a seminal work that introduces the widely adopted generalized memory polynomial (GMP) approach to DPD. If you just dabble in the signal processing side of things, it may be a little heavy for an introduction to the subject. So, as a start, let's try and break down the GMP approach and reach a more intuitive understanding of what the math is doing.

The Volterra series is the mathematical backbone of DPD. It is used to model nonlinear systems with memory. *Memory* simply means that the present output of the system can depend on the current and past inputs. Volterra series is very general (and, hence, powerful) and is used in many fields outside of electrical engineering. For PA DPD, the Volterra series can be slimmed down and made such that it is more implementable and stable in real-time digital systems. GMP is one such slimmed down approach.

Figure 5 describes how GMP is used to model the relationship between the input, x, of the PA and its output, y. You'll see the three separate summation blocks of the equation are very similar to each other. Let's focus on the first one for now highlighted in red below. The $|x(...)|^k$ term is referred to as the envelope of the input signal, where k is the polynomial order. l incorporates memory into the system. If $L_a = \{0,1,2\}$, then the model allows the output $y_{GMP}(n)$ to depend on the current input x(n) and past inputs x(n – 1) and x(n – 2). Figure 6 examines the effect of the polynomial order k on a sample vector. The vector, x, is a single 20 MHz carrier and is plotted at complex baseband. The GMP modeling equation is simplified by removing the memory component. The plots of $x|x|^k$ show a clear similarity to the real-world distortion visible in Figure 4.

Each polynomial order (k) and memory lag (l) has an associated complex weight (a_{kl}). When the complexity of the model has been chosen (which values of k and l will be included), it is then necessary to solve for these weights based on real-world observations of the PAs output for a known input signal. Figure 7 converts the simplified equation into matrix form. The mathematical notation used allows for a concise representation of the model. However, for the actual implementation of DPD on buffers of digital data, it is easiest and more representative to view things in matrix notation.

Let's briefly look at the second and third lines of the equation in Figure 6 that were ignored for simplicity. Note that if m is set to zero, then these lines become identical to the first one. These lines allow for delays (both positive and negative) to be added between the envelope term and the complex baseband signal. These are called lagging and leading crossterms and can improve the modeling accuracy of DPD significantly. They offer an extra level of freedom in our attempts to model the amplifier's behavior. Note that M_b, M_c, K_b, and K_c do not contain zero; otherwise, we would be repeating terms from the first line.

$$y_{GMP}(n) = \sum_{l \varepsilon L_a} \sum_{k \varepsilon K_a} a_{kl} x(n-l)|x(n-l)|^k + \sum_{k \varepsilon K_b} \sum_{l \varepsilon L_b} \sum_{m \varepsilon M_b} b_{klm} x(n-l)|x(n-l-m)|^k + \sum_{k \varepsilon K_c} \sum_{l \varepsilon L_c} \sum_{m \varepsilon M_c} c_{klm} x(n-l)|x(n-l+m)|^k$$

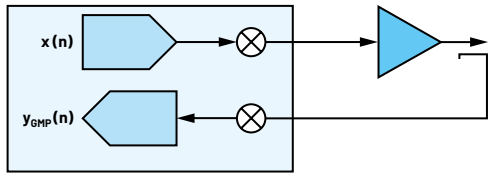


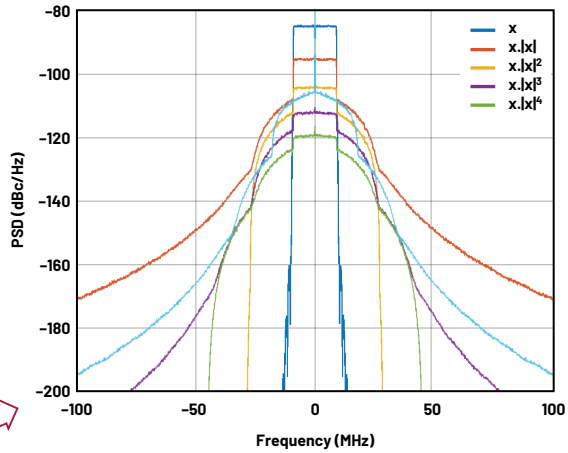
Figure 5. GMP for modeling PA distortion.[1]

$$y_{GMP}(n) = \boxed{\sum_{l \varepsilon L_a} \sum_{k \varepsilon K_a} a_{kl} x(n-l)|x(n-l)|^k} + \sum_{k \varepsilon K_b} \sum_{l \varepsilon L_b} \sum_{m \varepsilon M_b} b_{klm} x(n-l)|x(n-l-m)|^k + \sum_{k \varepsilon K_c} \sum_{l \varepsilon L_c} \sum_{m \varepsilon M_c} c_{klm} x(n-l)|x(n-l+m)|^k$$

Simplify

- $K_a = \{0, 1, 2, 3, 4\}$
- $L_a = 0$

$$y_{GMP}(n) = \sum_{k \varepsilon K_a} a_{kl} \boxed{x(n)|x(n)|^k}$$



Plot Highlighted Element for Each Value of k
$y_{GMP}(n)$ Is the Sum of These Elements, Each Multiplied by a Complex Weight, a_{kl}

Figure 6. Plot of effect of order (k) on signal in frequency domain of a signal x.

Convert From Equations to Matrix Operations on Vectors/Buffers of Data

$$y_{GMP}(n) = \sum_{k \varepsilon K_a} a_{kl} x(n)|x(n)|^k$$

- $K_a = \{0, 1, 2, 3, 4\}$
- $L_a = 0$

$$\begin{bmatrix} y_{GMP} \end{bmatrix} = \begin{bmatrix} x & x|x|^1 & x|x|^2 & x|x|^3 & x|x|^4 \end{bmatrix} \begin{bmatrix} a_{00} \\ a_{10} \\ a_{20} \\ a_{30} \\ a_{40} \end{bmatrix} \Rightarrow \hat{y} = Xw$$

Figure 7. Convert the simplified equation to matrix operation on data buffers (closer to how it is implemented digitally).

So how do we settle on the order of the model, the number of memory terms, and what crossterms we should add? This is where a certain amount of "black magic" comes into things. It is possible to be guided to some degree by our knowledge of the physics of the distortion. The type of amplifier and the material it is manufactured out of and the bandwidth of the signal being played through it all impact on the modeling terms and allow an engineer experienced in the area to put bounds on what model should be used. However, there is also a degree of trial and error involved on top of this.

The last aspect of the problem to be addressed from a mathematical viewpoint, now that a modeling structure is available, is how to solve for the weighting coefficients. In a practical scenario, there is a tendency to solve for the inverse of the model described above. It turns out that there is a nice reciprocity with these model coefficients, in that the same weights can be used to postdistort the captured PA output vector to remove nonlinearities and to predistort the transmitted signal sent through the PA so that the PA output appears as linear as possible. Figure 8 shows a block diagram of how the weight coefficient estimation and predistortion are carried out.

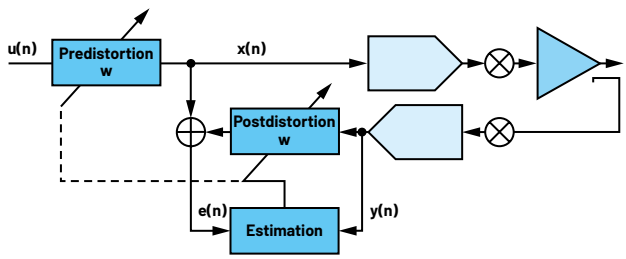


Figure 8. Block diagram describing indirect implementation of modeling and predistortion.

For the inverse model, the matrix equation given in Figure 7 is swapped around to give $\hat{x} = Yw$. Here the matrix Y is formed in the same way as X was in the other case, as shown in Figure 9. For this example, a memory term has been included and the number of polynomial orders included has been reduced. To solve for w, we need to get the inverse of Y. Y is not square (it's a tall, slim matrix) so this is achieved using the matrix "pseudo inverse" (see Equation 1). This solves for w in a least squares sense, that is, it minimizes the square of the difference between $\hat{x}$ and Yw, which is what we want!

$$w = (Y^H Y)^{-1} Y^H x \tag{1}$$

This can be refined a bit further to take into account that it's being applied in a live environment with varying signals. Here the coefficients are constrained by being updated from their previous value. μ is a constant value between 0 and 1 that controls how much the weights can change per iteration. If μ = 1 and $w_0 = 0$, then this equation reverts to the basic least squares solution immediately. If μ is set to a value less than 1, then it will take a number of iterations for the coefficients to converge.

$$w_{i+1} = w_i + \mu(Y^H Y)^{-1} Y^H e,\ e = x - \hat{x} \tag{2}$$

Note that the modeling and estimation techniques described here are not the only way to do DPD. Techniques such as dynamic deviation reduction (DDR)-based modeling can also be used instead of or in addition to it. The estimation techniques described for solving for the coefficients can also be done in numerous ways. Given this is a short article and not a book, let's leave it there.

How Do We Implement This in a Microprocessor?

Okay, so the math has been thoroughly covered. The next question is how is it applied in real-world communication systems? It is implemented in the digital baseband, generally in a microprocessor or an FPGA. ADI's RadioVerse® transceiver products such as the ADRV902x family have built-in microprocessor cores, with a structure specifically put in place to allow for easy DPD implementation.

There are two distinct aspects to DPD implementation in embedded software. The first is the DPD actuator, which is where the predistortion of the live transmitted data is performed in real time, and the second is the DPD adaption engine, which is where the DPD coefficients are updated based on observations of the PA output.

The key to how DPD and many other signal processing concepts are implemented in real time in a microprocessor or similar is through the use of lookup tables (LUTs). LUTs allow for expensive run-time calculations to be replaced with a simpler array indexing operation. Let's consider how the DPD actuator applies predistortion to a transmitted sample of data. The notation is as shown in Figure 8, where u(n) is the raw sample of data to be transmitted and x(n) is the predistorted version. Figure 10 shows the calculations required to obtain one predistorted sample for a given scenario. This is a relatively limited example with the highest polynomial order being third order and only one memory tap and a single crossterm. Even for this case, there are clearly a lot of multiplication, power of, and addition calculations needed to gain this one sample of data.

This is where LUTs come into play to ease the real-time computation burden. Figure 10 can be rewritten as Figure 11 where the data that will be entered in the LUTs become more evident. Each LUT contains the result of the highlighted element of the equation for a large number of possible values for |u(n)|. The resolution depends on the size of the LUT that can be implemented in the available hardware. The magnitude of the current input sample is quantized depending on the resolution of the LUT and used as an index to access the correct LUT element for that given input.

$$\begin{aligned} x(n) = u(n)&\left[a_{00} + a_{10}|u(n)|^1 + a_{20}|u(n)|^2\right] + \\ u(n-1)&\left[a_{01} + a_{11}|u(n-1)|^1 + a_{21}|u(n-1)|^2\right] + \\ u(n)&\left[b_{201}|u(n-1)|^2\right] \end{aligned}$$

LUT1
LUT2
LUT3

Figure 11. Regrouping equation elements to show LUT's structure.

$$\hat{x} = Yw$$

- $K_a = \{0, 1, 2\}$
- $L_a = \{0, 1\}$
- $y_{delay} = [0, y\,(1{:}\,end-1)]$

$$\begin{bmatrix} \hat{x} \end{bmatrix} = \begin{bmatrix} y & y|y|^1 & y|y|^2 & y_{delay} & y_{delay}|y_{delay}|^1 & y_{delay}|y_{delay}|^2 \end{bmatrix} \begin{bmatrix} a_{00} \\ a_{10} \\ a_{20} \\ a_{01} \\ a_{11} \\ a_{21} \end{bmatrix}$$

Figure 9. Inverse approach equation in matrix form. Some memory has been included here.

- $K_a = \{0, 1, 2\}$
- $L_a = \{0, 1\}$
- $K_b = \{2\}$
- $L_b = \{0\}$
- $M_a = \{1\}$

$$\begin{aligned} x(n) = {} & a_{00}u(n) + a_{10}u(n)|u(n)|^1 + a_{20}u(n)|u(n)|^2 + a_{01}u(n-1) \\ & + a_{11}u(n-1)|u(n-1)|^1 + a_{21}u(n-1)|u(n-1)|^2 + b_{201}u(n\,)|u(n-1)|^2 \end{aligned}$$

Figure 10. Predistortion calculation for third-order case with one memory tap and one third-order crossterm element.

Figure 12 shows how the LUTs are incorporated into the full predisortion actuator implementation for our example case. Note that this is just one possible implementation out of many. One example of a change that could be made while still maintaining the same output is that the delay element, z^{-1}, could be moved to the right of LUT2.

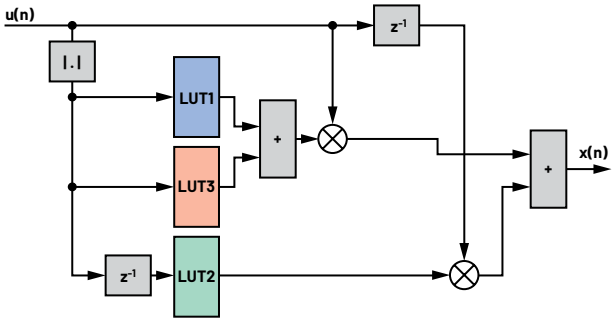


Figure 12. Block diagram of possible implementation of DPD using LUTs.

The adaption engine is tasked with solving for the coefficients that are used to calculate the LUT values in the actuator. This involves solving for the w vector described in equations 1 and 2. The pseudoinverse matrix operation, $(Y^H Y)^{-1} Y^H$, is computationally hungry. Equation 1 can be rewritten as

$$Y^H Y w = Y^H x \tag{3}$$

If $C_{YY} = Y^H Y$ and $C_{Yx} = Y^H x$, then Equation 3 becomes

$$C_{YY} w = C_{Yx} \tag{4}$$

C_{YY} is a square matrix and can be decomposed into the product of an upper triangular matrix, L, and its conjugate transpose ($C_{YY} = L^H L$) using Cholesky decomposition. This allows us to solve for w by introducing a dummy variable z and solving for it as shown:

$$L^H z = C_{Yx} \tag{5}$$

Then substitute this dummy variable back in to solve for

$$L w = C_{Yx} \tag{6}$$

Because L and L^H are upper and lower triangular matrices, respectively, Equation 5 and Equation 6 are easy to solve with minimal computational expense to give w. Every time the adaption engine is run and new values for w are found, it is necessary to update the actuator LUTs to reflect them. The adaption engine may be performed at set regular intervals or at more irregular intervals based on the observation of the PA output or the operator's knowledge of changes to the signal to be transmitted.

The implementation of DPD in an embedded system requires a lot of checks and balances to ensure the stability of the system. It is of utmost importance that the transmitted data buffer and capture buffer data are time aligned to ensure the mathematical relationship established between them is correct and holds true as it is applied over time. If this alignment is lost, then the coefficients returned by the adaption engine will not predistort the system correctly and may lead to instability in the system. The predistorted actuator output should also be checked to ensure that the signal will not saturate the DAC.

Conclusion

Hopefully, this article has cleared up some of the mystery around DPD by examining the underlying mathematics and its implementation in hardware. This is just the tip of the iceberg on this fascinating topic and may prompt the reader to look further into the application of signal processing techniques in communications systems. The study of Pratt and Kearney is a good source about DPD applied to an ultrawide bandwidth use case in a wired communications system.[2] ADI's RadioVerse transceiver products are uniquely placed to incorporate algorithms such as DPD as they provide highly integrated RF hardware and configurable software tools to customers.

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About the Author

Claire Masterson is a systems engineer in the Wireless Systems Group at Analog Devices Limerick working on systems implementation, software development, and algorithm development and verification. She received a B.A.I. and Ph.D. from Trinity College Dublin and joined ADI in 2011 after graduating. She is particularly interested in the application of digital signal processing in real-world systems, particularly in 5G and 6G system development and next-generation DPD implementations.

Simplifying TWS Earbud Designs with 1-Wire Connectivity

Yi Xin, Applications Engineer

Abstract

This article demonstrates a design that applies ADI's unique 1-Wire® technology to a true wireless stereo (TWS) earbud solution for the first time. The design utilizes the DS2488 1-Wire dual-port link, and features many merits, such as low cost, low power, high accuracy, small size, and high efficiency, based on meeting the requirements of power transfer and data communication. The design is an ideal solution for TWS earbud applications.

Introduction

The most attractive feature of TWS earbuds is the convenience of wireless wear. Compared to conventional Bluetooth® earbuds, TWS earbuds have many merits such as small size, good sound quality, and high stability, as well as a certain degree of water resistance and intelligence, which have quickly caught the interest of consumers. Shipment volume and total market size for TWS earbuds are continuously expanding in tandem with research and development of this technology in the field of consumer electronics.

System Architecture

The 1-Wire TWS earbud solution presented in this article, the MAXREFDES1302, includes two parts: the charging cradle and the earbuds. The overall system hardware architecture is shown in Figure 1.

The charging cradle uses a single-cell Li-Ion battery of 3.7 V, 1500 mAh to power the system, and uses the MAX77651 charger supporting the USB Type-C protocol to charge the battery. Users can charge the whole system by using one USB Type-C cable. For power rails, the charging cradle uses the MAX17224 boost module to boost the system voltage of the MAX77651 to 5 V, and the MAX38640 buck module generates 3.3 V from this 5 V to power the MAX32655 microcontroller. The 5 V is also transferred to the earbud side through the 1-Wire control circuit as the power supply that charges the earbud system. The charging cradle uses the MAX17262 fuel gauge with internal current sensing resistor to monitor the battery. The MAX17262 combines the traditional coulometer with the novel ModelGauge™ m5 EZ algorithm; it features flexible configuration and ease of use, and no battery characterization. The charging cradle uses the MAX32655 with a Bluetooth 5.2 module and an internal SIMO power module as the microcontroller. In addition to common communication interfaces, some GPIOs can be configured as a 1-Wire interface to control the DS2488 of the earbuds, providing great convenience for 1-Wire communication and charging. The SWD interface of the charging cradle can be connected to the MAX32625PICO programming platform, which can update the firmware of the MAX32655 of the charging cradle, and also display battery information on the computer through the virtual serial port. Battery information can also be displayed on the OLED screen of the charging cradle.

The earbud uses a single-cell Li-Ion battery of 3.7 V, 130 mAh to power the system, and it uses the DS2488 1-Wire dual-port link to implement the data communication between the earbud and the charging cradle, and at the same time controls the 5 V charging power supply, which comes from the charging cradle. The earbud also uses the MAX32655 microcontroller, which uses the UART interface to simulate 1-Wire timing to read and write the DS2488. The MAX32655 of the earbud similarly uses the SWD interface to connect to the MAX32625PICO programming platform to flash programs. For power rails, the MAX77734 charger of the earbud comes with a 3.3 V LDO output to power the MAX32655 microcontroller. At the same time, the 3.3 V, together with the 1.8 V and 1.2 V power supplies generated by the internal SIMO module of the MAX32655, forms the power rails of the MAX98050 audio codec. The earbud also uses the MAX17262 fuel gauge to monitor the battery.

Figure 2 shows a photo of the design. The actual size of the charging cradle is 10.20 cm × 5.80 cm, and that of the earbud is 10.20 cm × 6.50 cm. Since this is a prototype to assist customers in design, testing, and research, the product size could be further diminished if the test points are simplified, to meet the size requirements of actual TWS earbud applications.

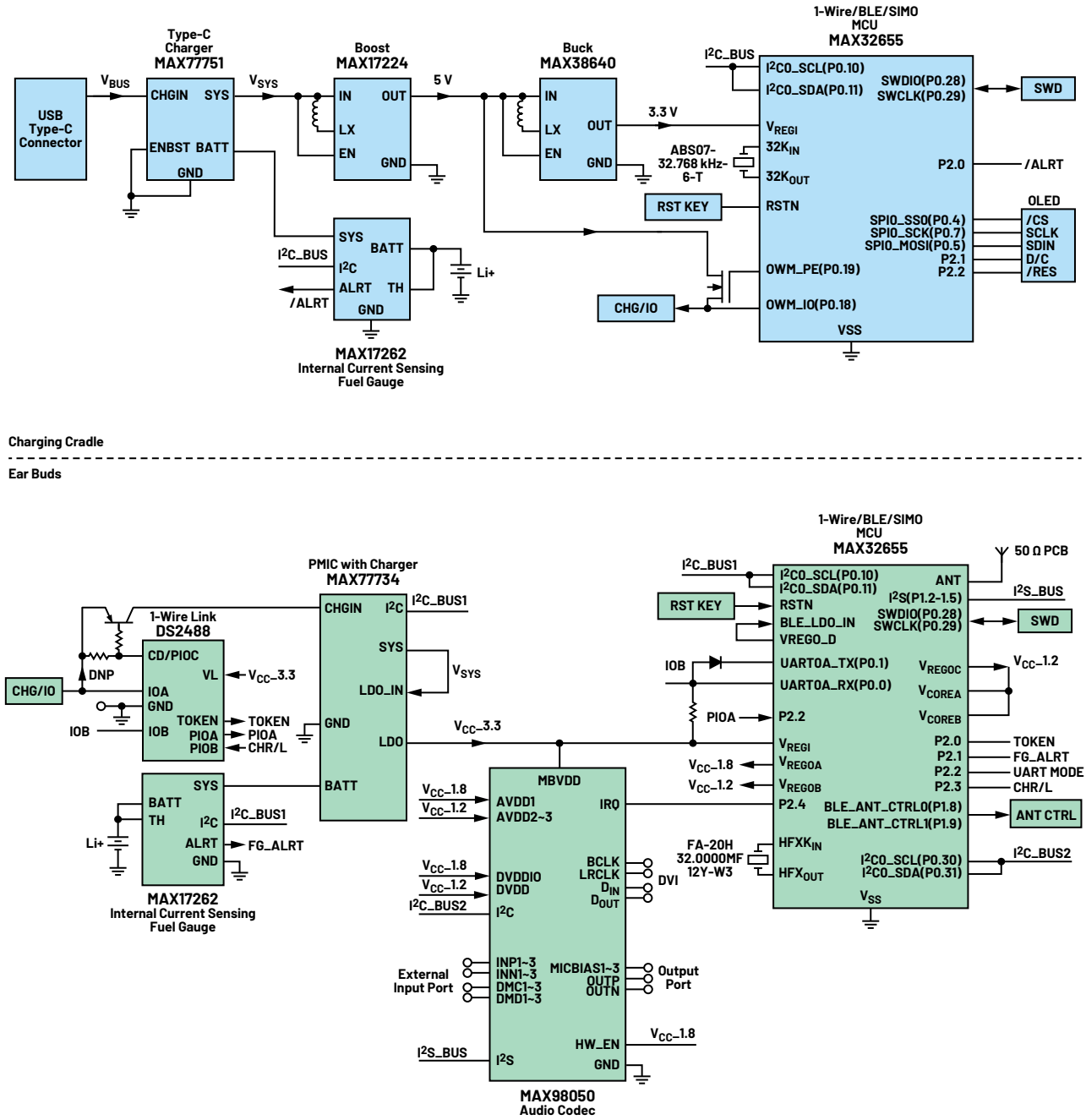

Figure 1. System architecture of 1-Wire TWS charging cradle and earbud.

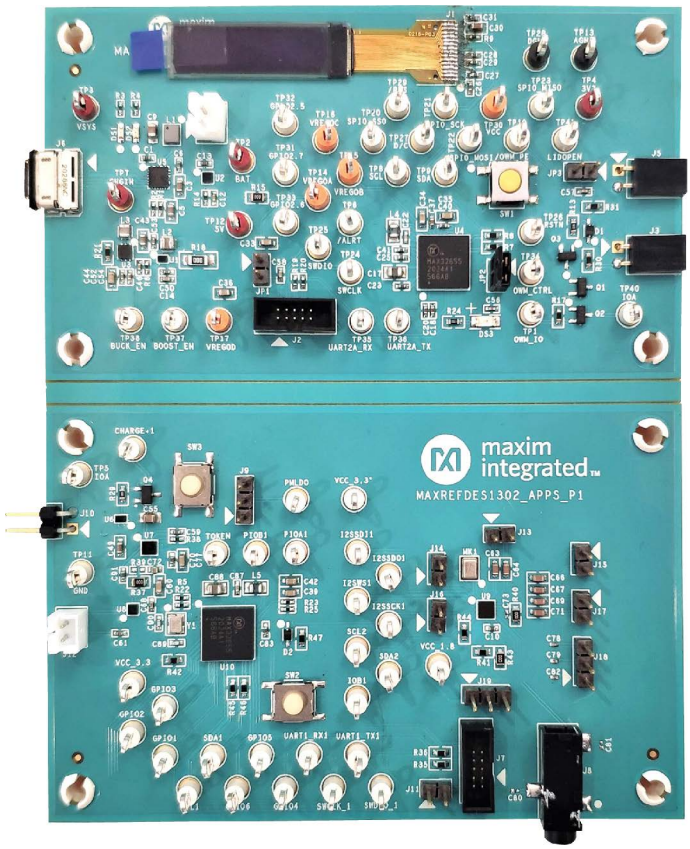

Figure 2. 1-Wire TWS charging cradle and earbud prototype PCBA photo.

1-Wire Data Communication and Power Transfer

In TWS earbud applications, it is very important to realize data communication and power transfer between the charging cradle and the earbud reliably and conveniently. Many common TWS earbuds currently on the market usually use three or more touch points to connect to the charging cradle to exchange messages and transfer power. However, having too many touch points usually contributes to higher system cost, which is extremely detrimental to low cost wearable products. In addition, more touch points usually require larger size, which is contrary to the requirement of TWS earbuds' small size. Also, more touch points tend to increase the likelihood of system failure. Faced with these difficulties, this design uses ADI's proprietary 1-Wire dual-link port, the DS2488, which is especially designed for TWS solutions to conduct power transfer and data communication between the earbud and the charging cradle. The DS2488 supports 1-Wire protocol and can exchange data and transfer power by a single wire. Since the system needs an additional touch point to connect the GND of the earbud and that of the charging cradle, the whole solution only needs two touch points, which can significantly improve the reliability and reduce the size and cost of the system. The block diagram of the 1-Wire communication and charging circuit of this design is shown in Figure 3.

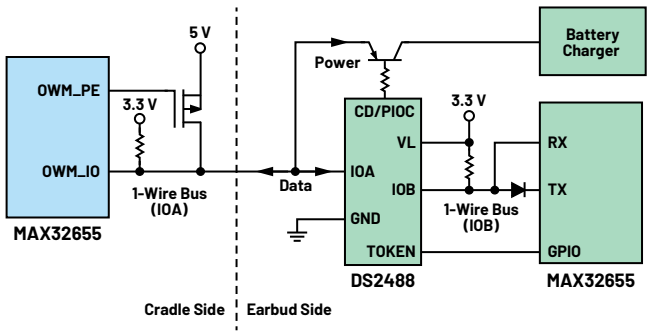

Figure 3. Block diagram of 1-Wire communication and charging.

Working Principle of the DS2488

As shown in Figure 3, the DS2488 is the 1-Wire dual-port link with two 1-Wire communication pins, IOA and IOB, which are controlled by the microcontrollers on both sides. The IOA pin is controlled by the microcontroller of the charging cradle, and the IOB pin is controlled by the microcontroller of the earbud. The IOA pin can support input voltage up to 5.5 V, and it can support different communication and charging levels on the 1-Wire bus (IOA). As a 1-Wire device, each DS2488 has a unique 64-bit ROM ID for users to identify and authenticate. The DS2488 also features an internal 8-byte buffer that can be read and written by the microcontroller to update battery information on both sides in real time. In this design, the information stored in the buffer is shown in Table 1.

Table 1. Information Stored in DS2488 Buffer

Index	Information
Bit 7	Reserved
Bit 6	Cradle battery CAP (thousands and hundreds place) (mAh)
Bit 5	Cradle battery CAP (tens and ones place) (mAh)
Bit 4	Cradle battery SOC (%)
Bit 3	Right earbud battery CAP (mAh)
Bit 2	Right earbud battery SOC (%)
Bit 1	Left earbud battery CAP (mAh)
Bit 0	Left earbud battery SOC (%)

The TOKEN pin of the DS2488 indicates the control status of the DS2488: TOKEN logic low indicates that the microcontroller on the charging cradle side has obtained the control authority of the DS2488, while TOKEN logic high indicates that the microcontroller on the earbud side has obtained the control authority of the DS2488. The CD/PIOC pin of the DS2488 controls the charging cradle to charge the earbud: when the voltage on the 1-Wire bus (IOA) is lower than 4 V, the CD/PIOC pin is high impedance, so the transistor is off and charging stops. When the voltage on the 1-Wire (IOA) is higher than 4 V, the CD/PIOC pin is logic low. The transistor is on, so the voltage on the 1-Wire bus (IOA) is directly transferred to the charger of the earbud, and charging starts. The MOSFET connected to 5 V determines when to charge and when to communicate. The turn-on and turn-off of the MOSFET is controlled by the microcontroller of the charging cradle. The usage of the earbuds and charging cradle can be roughly divided into the following three cases.

The earbud is in the cradle and the cradle cover is open

In this case, the microcontroller of the charging cradle turns off the MOSFET and obtains the control authority of the DS2488. Under the circumstances, the TOKEN pin is logic low and the CD/PIOC pin is high impedance. The charging cradle reads the 8-byte buffer of the DS2488 through the 1-Wire bus (IOA) to read the earbud battery information and writes the 8-byte buffer to update the cradle battery information. At this time, charging stops and communication starts.

The earbud is in the cradle and the cradle cover is closed

In this case, the microcontroller of the cradle turns on the MOSFET, so 5 V is directly transferred to the earbud through the 1-Wire bus (IOA). Under the circumstances, the TOKEN pin is logic high and the CD/PIOC pin is logic low. The 5 V from the cradle is transferred to the earbud side to charge the earbud battery. Meanwhile, the microcontroller of the earbud obtains the control authority of the DS2488, updates the earbud battery information, and reads the cradle battery information by reading and writing the 8-byte buffer of the DS2488 through the 1-Wire bus (IOB). At this time, communication stops and charging starts.

The earbud is not in the cradle, or the cradle battery is nearly dead

In this case, the 1-Wire bus (IOA) is high impedance, the TOKEN pin is logic high, and the CD/PIOC pin is high impedance. At this time, the microcontroller of the earbud obtains the control authority of the DS2488 and updates the earbud battery information by writing the 8-byte buffer of the DS2488 through the 1-Wire bus (IOB).

DS2488 1-Wire Data Communication

As mentioned, this design uses the DS2488 as a bridge between the microcontrollers on the charging cradle side and the earbud side to realize the message exchange on both sides. The DS2488 supports the typical 1-Wire communication protocol. The protocol includes reset and response timing and read/write timing. The read/write timing includes a write-zero slot, a write-one slot, and a read-data time slot, as shown in Figure 4 and Figure 5. Timing slot duration details are listed in the DS2488 data sheet.

All 1-Wire devices have an internal state machine and its state transition diagram is shown in Figure 6. As shown in Figure 4, when the microcontroller sends a reset signal to the DS2488, the 1-Wire bus will be pulled low for 48 µs to 80 µs, and then the bus will be released to high level by the pull-up resistor. If there is a DS2488 on the bus, the DS2488 will respond to the reset signal and pull the 1-Wire bus low again for 6 µs to 10 µs after the bus is released for 48 µs. At this time, the microcontroller can detect the level change on the bus—that is, determine whether there is a DS2488 connected to the 1-Wire bus by detecting whether the bus is pulled low again.

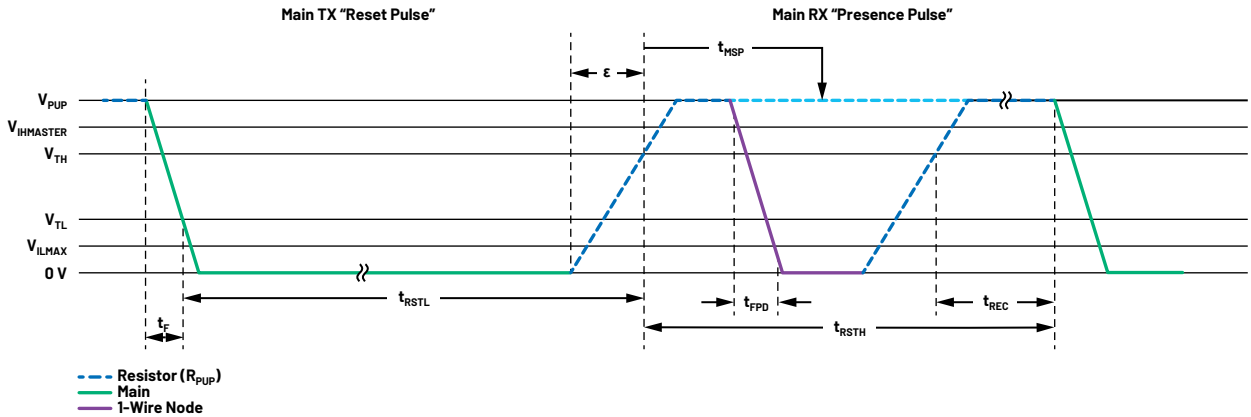

Figure 4. DS2488 1-Wire reset and presence timing.

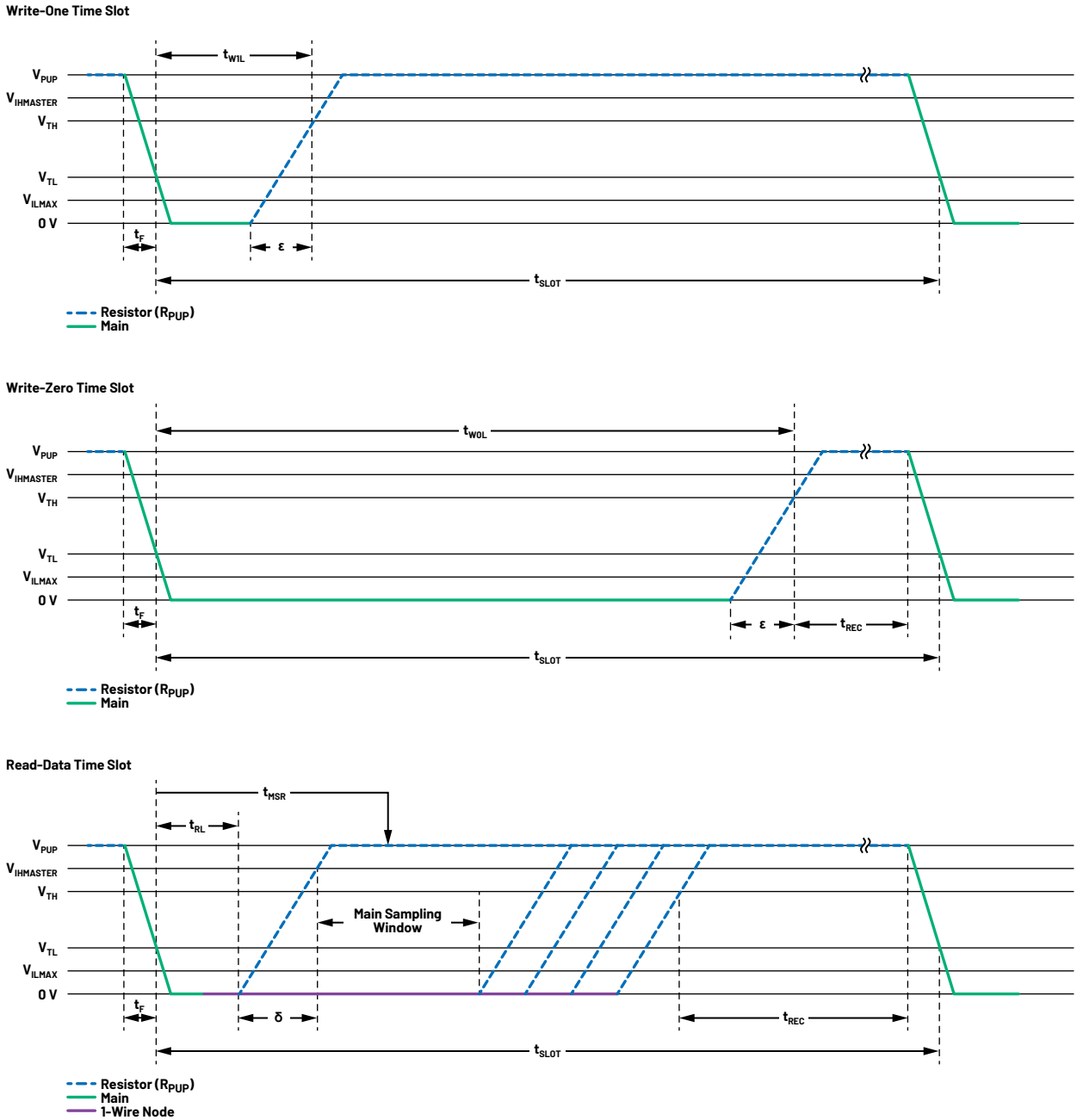

Figure 5. DS2488 1-Wire read/write timing.

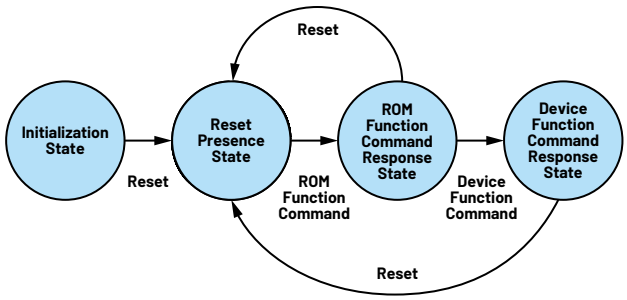

Figure 6. State transition diagram of 1-Wire devices.

Once the DS2488 has responded to the reset signal, the microcontroller will send a ROM function command. All 1-Wire devices have the same ROM function commands. Some common ROM function commands are summarized in Table 2. In the design, two DS2488s are connected to the 1-Wire bus (IOA) because there are usually two earbuds in the charging cradle. The read ROM command (0x33) and the match ROM command (0x55) are used to read the ROM IDs of the two DS2488s on the 1-Wire bus (IOA) and match the DS2488 with the specific ROM ID to implement the identification and selection of the left earbud or the right earbud.

Table 2. Common 1-Wire ROM Function Commands

ROM Function Command	Code	Description
Search ROM	0xF0	Read ROM IDs of all devices on the bus
Read ROM	0x33	Read the ROM ID of the only device on the bus
Match ROM	0x55	Select a device with a specific ROM ID
Skip ROM	0xCC	Select the only device on the bus

After sending the ROM function command, the microcontroller will send a device function command to perform further control of the device. Different 1-Wire devices have different device function commands. For the DS2488, some common device function commands are summarized in Table 3. This design uses the write buffer (0x33) and the read buffer (0x44) commands to read and write the 8-byte buffer of the DS2488 to realize battery information exchange between the charging cradle and the earbud.

Table 3. Common DS2488 Device Function Commands

Device Function Command	Code	Description
Write Configuration	0x11	Write the DS2488 configuration
Read Configuration	0x22	Read the DS2488 configuration
Write Buffer	0x33	Write the buffer of the DS2488
Read Buffer	0x44	Read the buffer of the DS2488
Read Status	0x55	Read the status of the DS2488

Two groups of GPIOs (P0.6 and P0.7, P0.18 and P0.19) of the MAX32655 microcontroller of the cradle can be configured as the OWM_IO pin and the OWM_PE pin of the 1-Wire module to realize communication to DS2488 and 5 V transfer, respectively. In this design, the OWM_IO pin of the MAX32655 is connected to the IOA pin of the DS2488 to realize 1-Wire communication function between the microcontroller of the cradle and the DS2488 of the earbud.

Differently, considering that some microcontrollers on the market do not have the 1-Wire interface, for the convenience of design, the MAX32655 microcontroller of the earbud uses the UART interface to simulate 1-Wire timing and communicates with DS2488 through the IOB pin, as shown in Figure 3. The microcontroller can realize this function by configuring a specific UART baud rate and sending a specific code pattern. Taking the reset and presence sequence shown in Figure 4 as an example, when the baud rate is 115200, the duration for the UART to send or receive 1-bit data is about 8.68 µs. Therefore, the duration for 1-byte data is approximately 69.44 µs. Since 0xE0 (11100000, LSB first) exactly corresponds to the 1-Wire reset timing, it can be sent as the 1-Wire reset signal. In this case, if the microcontroller sends 0xE0 (1-Wire reset signal) through the TX pin, the DS2488 on the 1-Wire bus (IOB) will respond to this 1-Wire reset signal and pull the bus low for 6 µs to 10 µs. At this time, the signal received by the RX pin should be 0xC0 (11000000) or 0x80 (10000000). To conclude, the microcontroller can implement the function of simulating 1-Wire timing via UART by sending and receiving different code patterns and comparing the received and sent signals.

DS2488 1-Wire Power Transfer

As shown in Figure 3, the OWM_PE pin of the MAX32655 microcontroller of the cradle controls the turn-on and turn-off of the MOSFET. When the MOSFET is off, the system conducts 1-Wire communication. When the MOSFET is on, the 5 V voltage is transferred to the earbud side through the 1-Wire bus (IOA). As soon as the DS2488 detects 5 V, the CD/PIOC pin will output low level to turn on the transistor to transfer the 5 V to the MAX77734 charger so as to charge the earbud battery.

Battery Management and Power Configuration

The battery management and power configuration system of the charging cradle consists of the MAX77751 USB Type-C charger, the MAX17262 fuel gauge, the MAX17224 boost DC-to-DC converter, and the MAX38640 buck DC-to-DC converter. Generally, the termination voltage of a single-cell Li-Ion battery is 4.2 V, so MAX77751CEFG+ is selected as the specific part number of the charger. Its charging current is configured by the resistors connected to the IFAST pin and the ITOPOFF pin. Considering the design needs, a fast charge current of 500 mA and a top-off current of 100 mA are selected, and the corresponding resistors are 2.4 kΩ and 8.06 kΩ, respectively. The MAX17262 fuel gauge features the ModelGauge m5 EZ algorithm, which can automatically measure the battery after configuring battery parameters such as battery capacity, termination current, and charging voltage threshold, without additional battery characterization. The output voltages of the MAX17224 boost DC-to-DC converter and the MAX38640 buck DC-to-DC converter are respectively configured by resistors connected to the SEL pin and the RSEL pin. In this design, 0 Ω and 56.2 kΩ resistors are selected to output 5 V and 3.3 V respectively.

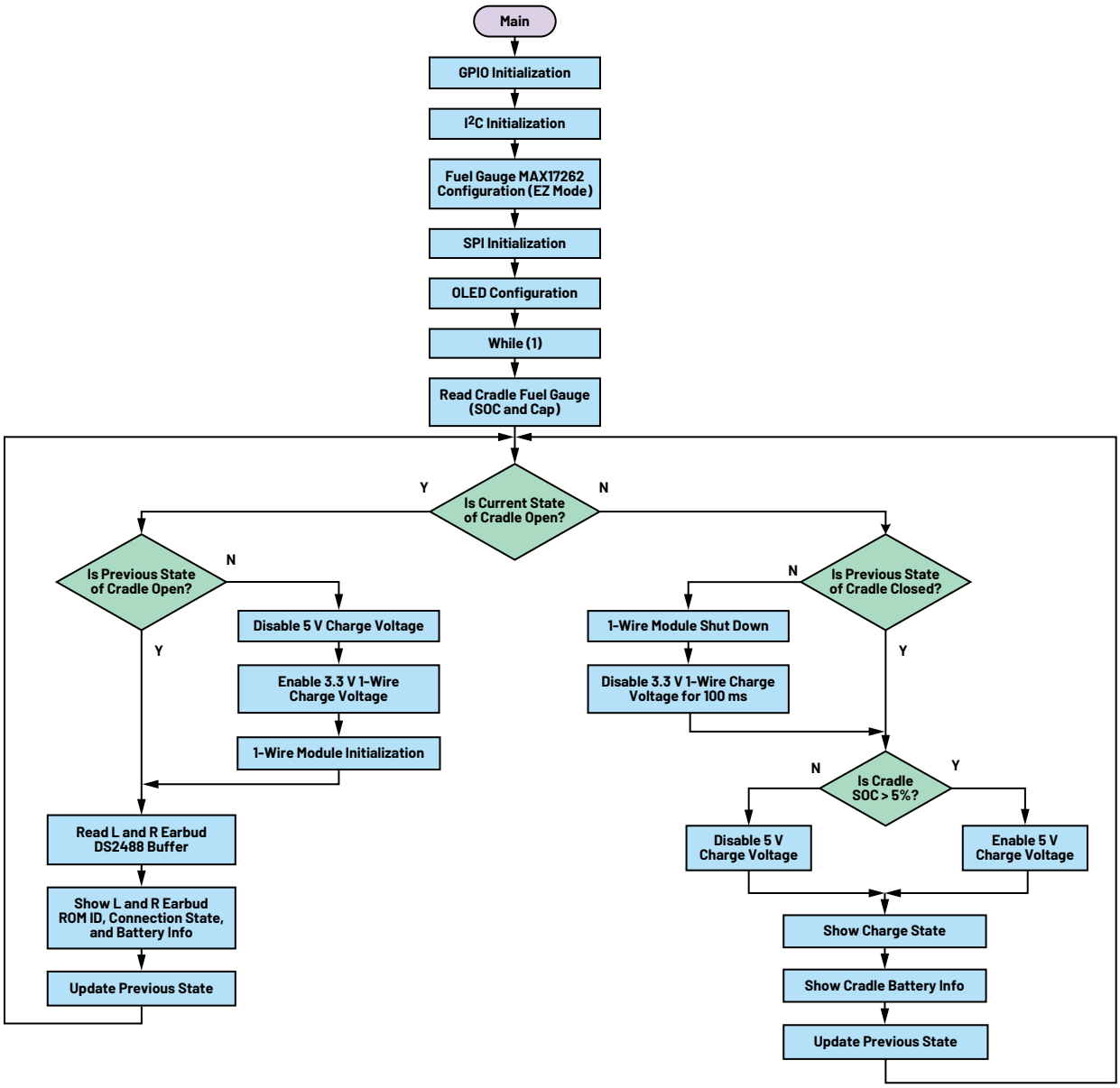

Figure 7. Flowchart of cradle firmware.

The battery management and power configuration system of the earbud consists of the MAX77734 charger and the MAX17262 fuel gauge. The output of the MAX32655 microcontroller SIMO module also provides 1.8 V and 1.2 V power rails for the system. Since only one 3.3 V LDO output is needed, the MAX77734GENP+ is selected as the specific part number of the charger. The charger can also be configured to factory-ship state, shutdown state, and standby state through I²C to extend battery life. The MAX32655 microcontroller provides four SIMO outputs, each of which can be configured to output different voltages.

Firmware Design

The flowchart of the charging cradle firmware is shown in Figure 7. After power-on, the microcontroller of the charging cradle will initialize GPIOs, and configure the MAX17262 fuel gauge and the OLED module. Then, the microcontroller polls the status of the cradle cover. If the cradle is closed, the microcontroller will disable the 1-Wire module and apply the 5 V charging voltage to the 1-Wire bus (IOA) to charge the earbud. In this case, if the microcontroller detects that the remaining power of the cradle battery is less than 5%, the charging will be stopped. If the cradle is opened, the microcontroller will disable the 5 V charging voltage and enable the 1-Wire module to read and write the DS2488 buffer. Battery information of the cradle and earbud is displayed through an OLED module or the virtual serial port.

The flowchart of the earbud firmware is shown in Figure 8. After power-on, the microcontroller of the earbud will initialize GPIOs and configure the MAX17262 fuel gauge and the MAX77734 charger. Then, the microcontroller polls whether the input voltage from the charger is valid. If the input voltage is valid and greater than 4 V, the microcontroller enables the charger and starts charging. At this time, the microcontroller polls the status of the TOKEN pin. If the TOKEN pin is logic low, the cradle has the control authority to read and write the DS2488. If the TOKEN pin is logic high, the earbud has the control authority to read and write the DS2488. Under the circumstances, the microcontroller writes the earbud battery information into the buffer of the DS2488 for the cradle to read.

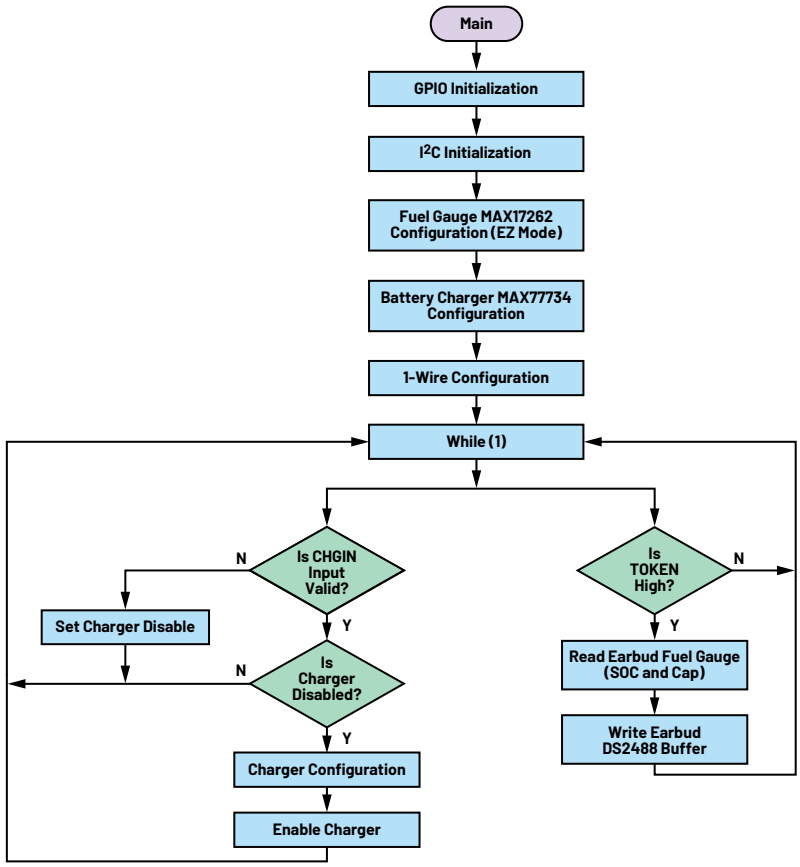

Figure 8. Flowchart of earbud firmware.

Test Result

The design requirements and test results of the power rail of the cradle and earbud are shown in Table 4 and Table 5. This design can meet the system design requirement.

Table 4. Design Requirements and Test Results of the Cradle Power Rail

Parameter	Symbol	Measured Value	Design Requirement
Battery Voltage	BAT	4.08 V	3.1 V to 4.6 V
USB Input Voltage	CHGIN	4.94 V	4.8 V to 5.2 V
5 V Output of the Boost Module	5 V	5.16 V	4.8 V to 5.2 V
3.3 V Output of the Buck Module	3V3	3.30 V	3.2 V to 3.4 V

Table 5. Design Requirements and Test Results of the Earbud Power Rail

Parameter	Symbol	Measured Value	Design Requirement
Battery Voltage	V_{BAT}	3.71 V	3.3 V to 4.6 V
3.3 V Output of the Charger	V_{CC}–3.3	3.32 V	3.2 V to 3.4 V
1.8 V Output of the Microcontroller	V_{CC}–1.8	1.82 V	1.7 V to 1.9 V
1.2 V Output of the Microcontroller	V_{CC}–1.2	1.12 V	1.1 V to 1.3 V

The test results for the open cradle and closed cradle are shown in Figure 9 and Figure 10, respectively. This design can display the information of the cradle battery and earbud battery in real time, and read and display the ROM ID of the DS2488 of the earbud.

```
******* Cradle is closed ********
1-Wire Charge
*********************************

*********************************
Cradle:
Capacity: 1360mAh
Percentage is 90%
*********************************
```

Figure 9. Test result for closed cradle.

```
******** Cradle is open *********
1-Wire Communication
*********************************

*********************************
Cradle:
Capacity: 1360mAh
Percentage: 90%

Left Earbud:
ROMID:0x59, 0x06, 0x0D, 0x02, 0x00, 0x00, 0x00, 0xA9
Capacity: 102mAh
Percentage: 78%

Right Earbud:
ROMID:0x59, 0x05, 0x0D, 0x02, 0x00, 0x00, 0x00, 0xF0
Capacity: 81mAh
Percentage: 62%
*********************************
```

Figure 10. Test result for open cradle.

Conclusion

Prototyping TWS earbud solutions is a challenge that requires the balance between ease of use, low cost, portability, and stability. The DS2488 1-Wire dual-port link paves the way for low power, high stability, high performance TWS earbud solutions in smaller form factor and at a lower cost. Building on the DS2488, the MAXREFDES1302, including hardware design and firmware design, is an easy to use TWS earbud prototype that is capable of power transfer and data communication through only two touch points.

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About the Author

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Low Noise Silent Switcher µModule and LDO Regulators Improve Ultrasound Noise and Image Quality

Yu Lu, Field Applications Engineer, and
Hugh Yu, Healthcare Systems Applications Manager

Abstract

This article presents a brief introduction to ultrasound imaging systems and provides a detailed analysis of some of challenges and solutions in ultrasound power management design. Four main design considerations are discussed: system noise level, switching noise, electromagnetic interference (EMI), and the ultrasound thermal dissipation related to its power supply. This article will also explain how the Silent Switcher® µModule® and low noise LDO technology can help solve the most common problems and improve system noise and image quality.

Introduction

The ultrasound market has grown rapidly following the introduction of the first digital ultrasound (by GE) in 2000. Ultrasound technology has shifted from static-based to dynamic and from black and white to color doppler. A growing number of ultrasound applications has led to increased component requirements such as those related to the probe, AFE, and power system.

In the field of medical diagnostics, there are ever increasing demands for higher image quality in ultrasound imaging systems. One of the key techniques for improving image quality is to enhance the signal-to-noise ratio (SNR) of the system. The different factors that affect noise will be discussed below, especially the power supplies.

How Does Ultrasound Work?

An ultrasound system is composed of transducers, transmitting circuits, receiving circuits, back-end digital processing circuits, control circuits, a display module, etc. The digital processing module usually comprises a field programmable gate array (FPGA), which generates the transmit beamformers and corresponding waveform patterns according to the configuration and control parameters of the system. The transmit circuits' driver and the high voltage circuit then generate a high voltage signal to excite the ultrasound transducers. The ultrasound transducer is usually made of PZT ceramic. It converts a voltage signal into ultrasound waves that enter into the human body while receiving the echoes produced by the tissues. The echoes are converted into a small voltage signal and passed to a transmitting/receiving (T/R) switch. The primary objective of the T/R switch is to prevent the high voltage transmit signal from damaging the low voltage receive analog front end. The analog voltage signal after signal conditioning, gaining, and filtering is passed to the integrated ADC of the AFE and then converted into digital data. The digital data is transmitted through a JESD204B or LVDS interface to the FPGA for receive beamforming and then to the back-end digital parts for further processing to create the ultrasound image.

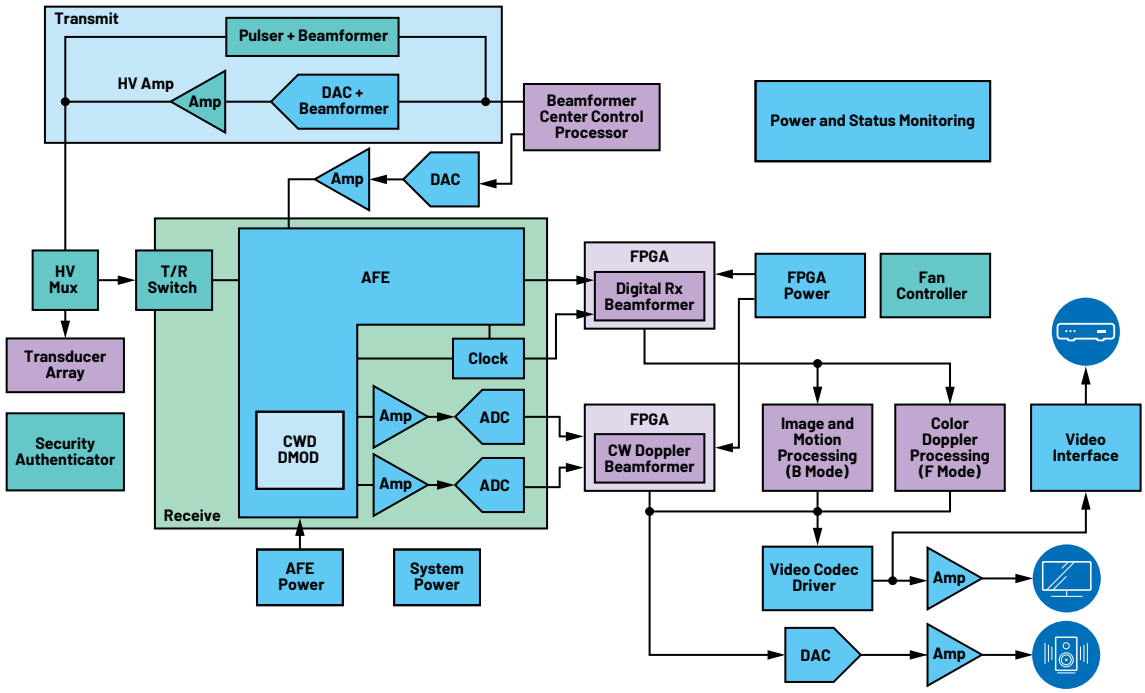

Figure 1. Ultrasound system block diagram.

How Does a Power Supply Influence Ultrasound Systems?

From the ultrasound architecture described above, system noise can be affected by many factors such as the transmit signal chain, the receive signal chain, TGC gain control, clocking, and power supplies. In this article, we will discuss how the power supply can affect noise.

There are different kinds of image modes in an ultrasound system, and each image mode has different requirements for the dynamic range. This also means that the SNR or noise requirements depend on the varying image modes. 70 dB dynamic range is required for black and white mode, 130 dB is required for pulse wave doppler (PWD) mode, and 160 dB is required for continuous wave doppler (CWD) mode. The noise floor is important for the black and white mode, and it impacts the maximum depth the smallest ultrasound echo can be seen in the far field, which is called penetration, one of the key features of black and white mode. The 1/f noise is particularly important for the PWD and CWD modes. Both PWD and CWD images include the low frequency spectrum below 1 kHz, and the phase noise impacts the doppler frequency spectrum higher than **1 kHz. As the ultrasound transducer frequency is typically from 1 MHz to 15 MHz,** it will be affected by any switching frequency noise within this range. If there are intermodulated frequencies within the PWD and CWD spectrums (from 100 Hz to 200 kHz), the obvious noise spectrums will appear in the doppler images, which is unacceptable in the ultrasound system.

On the other hand, a good power supply can improve ultrasound images by taking into account the same considerations. There are several factors a designer should understand when designing a power supply for an ultrasound application.

Switching Frequency

As mentioned, it is necessary to avoid introducing unexpected harmonic frequency into the sampling band (200 Hz to 100 kHz). It is easy to find this kind of noise in a power system.

The majority of switching regulators use a resistor to set the switching frequency. The error of this resistor introduces different switching nominal frequencies and harmonics on the PCB. For example, 1% accuracy resistors provide ±1% error and 4 kHz harmonic frequency in a 400 kHz DC-to-DC regulator. A better solution is to select power switchers with a sync function. The external clock will send a signal to all regulators via the SYNC pin so that all regulators switch at the same frequency and same phase.

Also, some regulators feature a variant switching frequency of 20% for EMI consideration or higher transient response, which leads to 0 kHz to 80 kHz harmonic frequency in a 400 kHz power supply. Switching regulators with constant frequency help avoid this issue. ADI's family of Silent Switcher voltage regulators and µModule regulators features constant frequency switching, but at the same time keep excellent EMI performance without spread spectrum on and keep excellent transient response.

White Noise

There are also many white noise sources in an ultrasound system, which leads to the background noise in ultrasound imaging. This noise mainly comes from the signal chain, clock, and power.

Adding an LDO regulator at the analog power pin of the analog processing component is common now. ADI's next-generation LDO regulators feature around 1 µV rms ultralow noise that covers current from 200 mA to 3 A. The circuit and specifications are shown in Figure 2 and Figure 3.

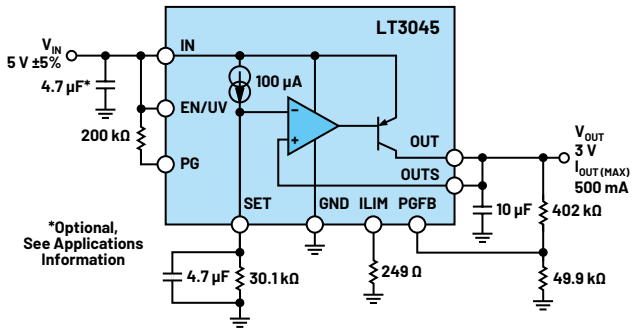

Figure 2. Next-generation low noise LDO regulator.

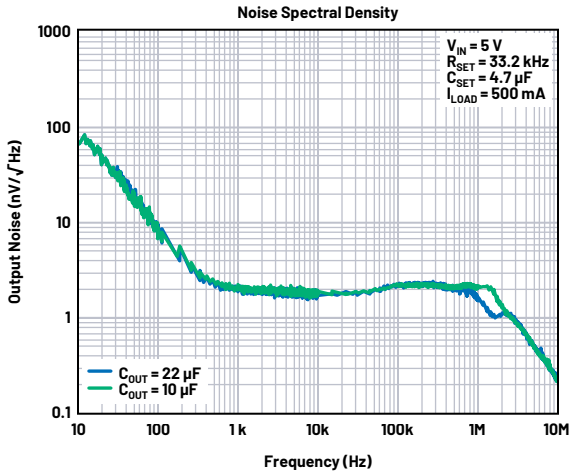

Figure 3. The low noise spectrum density in the next-generation LDO regulator: LT3045.

PCB Layout

When designing a data acquisition board in an ultrasound system, it is easy to notice the trade-off between a high current power part and a highly sensitive signal chain part. Noise from switching power supplies will easily be coupled in the signal path trace and this is not easy to remove from data processing. The switching noise is usually generated from the switching input cap (Figure 4) and the hot loop generated by the up or down side switches. Adding a snubber circuit can help manage electromagnetic emission; however, it decreases efficiency at the same time. Silent Switcher architecture can help improve EMI performance and maintain high efficiency even at a high switching frequency.

Handheld Digital Probe

In addition to heating due to the absorption of ultrasound, the temperature of tissues near a transducer is strongly influenced by the temperature of the transducer itself. Ultrasound pulses are produced by applying an electrical signal to the transducer. Some electrical energy is dissipated in the element, lens, and backing material, causing transducer heating. Electronic processing of received signals in the transducer head may also result in electrical heating. Conduction of heat from the transducer face can result in a temperature rise of several degrees Celsius in superficial tissues. The maximum allowable transducer surface temperatures (T_{SURF}) are specified in the IEC standard 60601-2-37 (Rev 2007).[1] These are 50°C when the transducer is transmitting into air and 43°C when transmitting into a suitable phantom. This latter limit implies that skin (typically at 33°C) can be heated by up to 10°C. Transducer heating is a significant design consideration in complex transducers, and, in some circumstances, these temperature limits may effectively restrict the acoustic output that can be achieved.

The safety standard IEC 60601-2-37 Rev 2007[1] limits the temperature of the transducer surface to less than 50°C when running in air and to less than 43°C when in contact with a phantom at 33°C (for externally applied transducers) or at 37°C (for internal transducers). It is often these temperature limits (rather than the limit on the maximum intensity in the beam) that restrict the acoustic output of a transducer. Silent Switcher devices have the highest efficiency converting power (with a wide switching bandwidth up to 3 MHz) to the different voltage domains of the digital probe. This means the power losses during power conversion are minimal. This helps the cooling system as there's not much additional power loss in the form of heat.

Silent Switcher µModule Regulators Help a Lot

Silent Switcher µModule regulator technology is the best choice in ultrasound power rail design. It was introduced to help improve EMI and switching frequency noise. Traditionally, we should take care of the circuit and layout design on the hot loop for each switching regulator. For a buck, as shown in Figure 4, a hot loop contains an input cap, a top side MOSFET, a bottom side MOSFET, and parasitic inductance introduced by wiring, routing, bounding, etc.

Silent Switcher modules feature two major design approaches:

Firstly, as shown in Figure 4 and Figure 5, by creating an opposite hot loop, most of the EMI will be reduced due to bidirectional emission. Nearly 20 dB will be optimized by this approach.

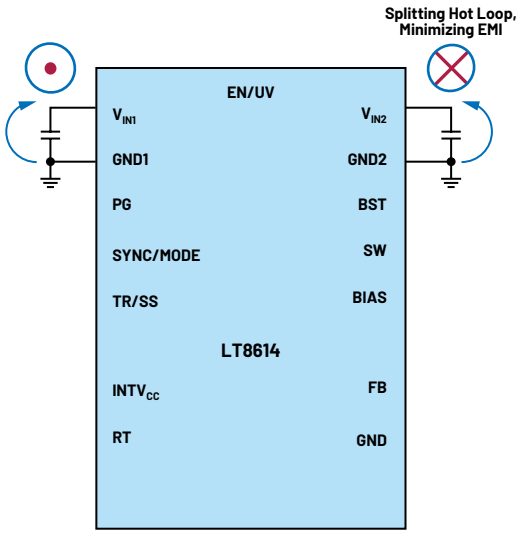

Figure 4. Splitting a hot loop's schematic.

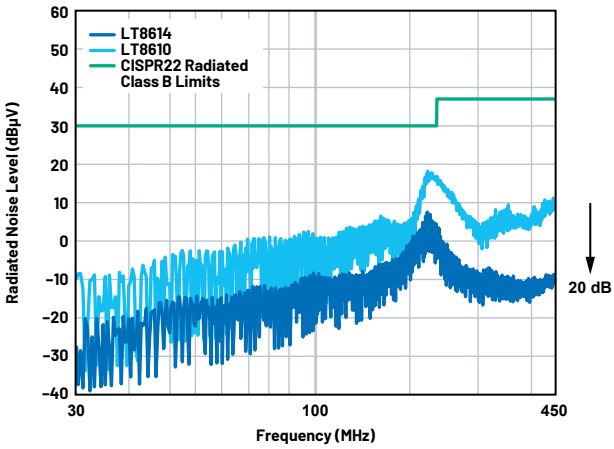

Figure 5. A comparison of silent switching and nonsilent switching EMI performance.

Secondly, as shown in Figure 6, instead of direct bonding surrounding the chip, a copper pillar flip-chip package in a Silent Switcher module helps to reduce parasite inductance and optimize spike and dead time.

In addition, as shown in Figure 7, Silent Switcher technology offers high power density design and enables large current capability in a small package, keeping low theta JA and resulting in high efficiency (for example, LTM4638 enabling 15 A in a 6.25 mm × 6.25 mm × 5.02 mm package).

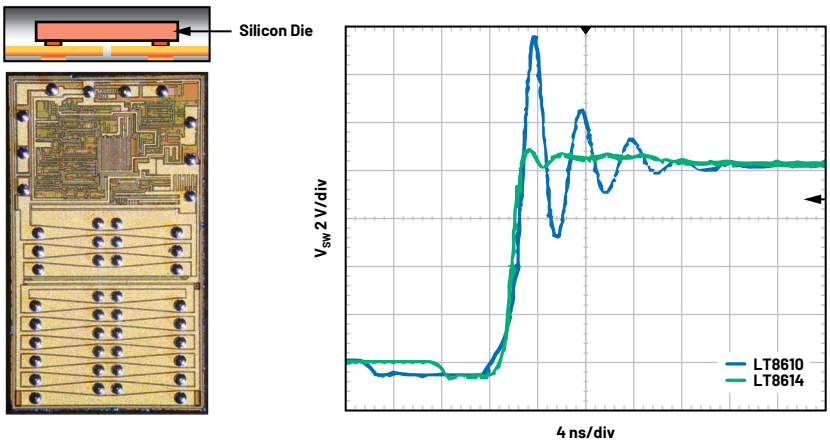

Figure 6. A copper pillar flip-chip package and its performance (LT8614) compared with a traditional bounding technique (LT8610).

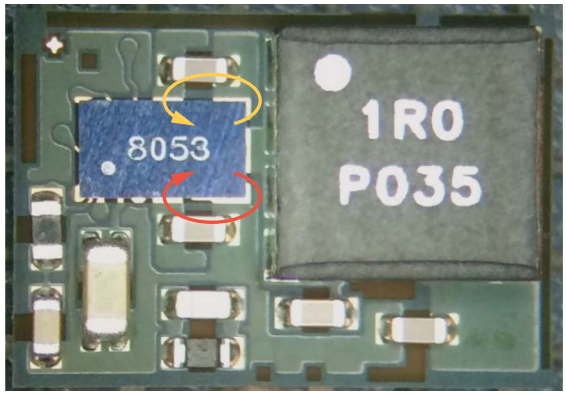

Figure 7. Silent Switcher µModule regulator in-package view.

Table 1. Silent Switcher Products Summary

	Low Frequency Noise	Switching Noise Harmonics	High Thermal Performance
Architecture	Ultralow noise reference in Silent Switcher 3 device	Silent Switcher technology plus Cu pillar package	Silent Switcher technology plus heat sink in package
Feature	Same performance as an LDO regulator in terms of low f noise	Low EMI, low switching noise Fast switching frequency, tiny dead slot	High power density Smaller thermal resistance
Benefit in Application	Removing the necessity of post-LDO regulator while keeping the same image quality	High frequency with high efficiency Higher frequency, smaller filter size	Minimize degrading for the same current level

Table 2. Popular Ultralow Noise Power Solutions with Silent Switcher Technology

	Switching Frequency	Control Mode	Switching Jitter	Power Stage Architecture	EMI	RMS Noise
LTM8053-1	200 kHz to 3 MHz	Fix frequency peak current	Small	Silent Switcher 2 module	Ultralow	0.8 µV rms (with LT3045)
LTM8060	200 kHz to 3 MHz	Fix frequency peak current	Small	Silent Switcher 2 module	Ultralow	0.8 µV rms (with LT3045)
LT8625S	300 kHz to 4 MHz	Fix frequency peak current	Small	Silent Switcher 3 converter	Ultralow	4 µV rms (without LT3045)

What's more, many Silent Switcher µModule regulators also feature fix frequency, wide frequency range, and peak current architecture, enabling low jitter and fast transient response. Popular products in this portfolio are listed in Table 2.

Conclusion

ADI's Silent Switcher power µModule regulator and LDO products provide a total solution for ultrasound power rail design, minimizing system noise levels and switching noise. This helps to improve the image quality. They are also helpful to limit temperature increase and simplify PCB layout design complexities.

Reference

[1] IEC Standard 60601-2-37. 2007.

About the Author

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About the Author

Hugh Yu earned his master's in electronic and information engineering in 2001 from the Nanjing University of Posts and Telecommunications, China. He worked as a senior ultrasound hardware engineer at GE Medical System, China, between 2002 and 2005, and worked as a research scientist at Siemens Corporate Technology China between 2005 and 2010. He is currently a healthcare systems application manager at Analog Devices, Shanghai, China.

RAQ Issue 200: Practical Tips for Measuring Ultralow Bias Current Using Commercial-Grade Lab Equipment

Aoi Ueda, Field Applications Engineer

Question:

Is there an easy way to measure ultralow bias currents in the femtoampere area?

Answer:

Yes—it just requires a careful setup.

Introduction

In applications where low leakage current is required, it is important to select a low input bias current (I_B) operational amplifier. The application note, AN-1373 describes how to measure ultralow bias current using the ADA4530-1 evaluation board. However, due to the nature of handling femtoampere (fA) level currents, the measurement environment—equipment such as jigs, shield, cable, and connectors—also affect the measurement results.

This article will introduce a trial to recreate the measurement in AN-1373 using commercial-grade lab equipment, jigs, and materials commonly available, and also includes some workarounds to improve the measurement to finally achieve 50 fA.

First, we measure the input capacitance for bias current measurement and the variation of output voltage with charging of the input capacitance under the condition of 125°C. We also attempt to derive the bias current value from the measured output voltage. Finally, we will try to improve the measurement environment based on the measurement results.

Capacitive Integration Measurement

According to AN-1373, the input capacitance (C_p) of the ADA4530-1 must be measured first in order to use the capacitance integral measurement method. We will perform this experiment using the ADA4530-1R-EBZ-BUF with the ADA4530-1 configured in buffer mode.

Next, we calculate the input current (I_{B+}). Specifically, using the circuit configuration shown in Figure 1, when the SW in the test box is turned from ON (grounded to GND) to OFF (open), I_{B+} flows into the C_p. The output voltage rises as I_{B+} charges C_p, so the value of I_{B+} can be calculated by monitoring and substituting it into Equation 1.

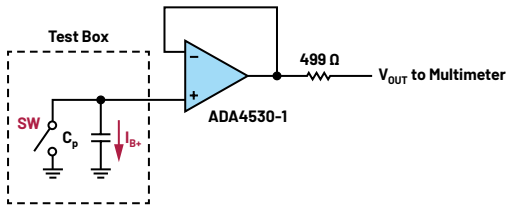

Figure 1. A diagram of the capacitive integration measurement method.

$$I_{B+} = \frac{C_p dV_{OUT}}{dt} \quad (1)$$

Measuring Total Input Capacitance with an Input Series Resistor

To calculate C_p, this experiment adopts a method using series resistance. Figure 2 shows a simple circuit diagram. The value of the series resistance is based on the measurement guidelines found on page 6 of AN-1373, and the actual value is R_S = 8.68 MΩ. An SW is also mounted in the test box for later experiments (SW is open at this time).

The frequency at which the waveform from the function generator is attenuated to –3 dB can be measured, and the input capacitance can be calculated using Equation 2.

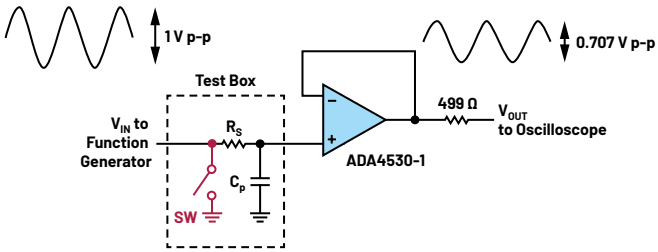

Figure 2. Calculation of C_p using series resistance of input.

$$C_p = \frac{1}{2 \times \pi \times R_S \times f_{-3\ dB}} \quad (2)$$

Figure 3 shows the setup. Since the temperature in the temperature-controlled chamber rises to 125°C in the experiment described in the section "Measuring I_{B+} with Known Input Capacitance" (page 6 of AN-1373), we use materials that can withstand such a temperature. RG-316U was used as the material for the coaxial cable. Furthermore, the noninverting inputs of the ADA4530-1 on the evaluation board are triaxial connectors. For this reason, a triax-to-coaxial conversion connector (BJ-TXP-1 from the Axis Company) was used. In this configuration, the guard terminal on the triax side was left floating.

As a result of the measurement, C_p = 73.6 pF was obtained, which is a relatively large value since the actual measurement, according to AN-1373, is about 2 pF. The reason for this is related to the cable length from the test box—which looks more like a test board—to the noninverting input.

Measuring I_{B+} with Known Input Capacitance

Finally, we start to measure the bias current. The circuit configuration is shown in Figure 1, and the mounted test box is shown in Figure 4. Note that the input resistor used in the section "Measuring Total Input Capacitive with an Input Series Resistor" is removed. As described in AN-1373 (the capacitive integration measurement method, page 7), short circuit the SW to GND, then open it and monitor the output voltage fluctuation with a digital multimeter (DMM) for a few minutes (We used the 34401A DMM from Keysight Technologies). Finally, calculate the I_{B+} by substituting V_{OUT} into Equation 1.

The results of three measurements under the same conditions are shown in Figure 5. The lower part of the figure shows the output voltage fluctuation of the ADA4530-1 measured by the DMM, and the upper part shows the current value calculated using Equation 1. The figure shows that for all three instances, there is no repeatability in the measured voltage values. Therefore, the waveform of the calculated current value also has a different shape from the result described in AN-1373 (see AN-1373 figures 13 and 14).

Figure 3. C_p measurement setup: (a) inside the temperature-controlled chamber—the evaluation board of ADA4530-1 is shown—and (b) setup of the test box side.

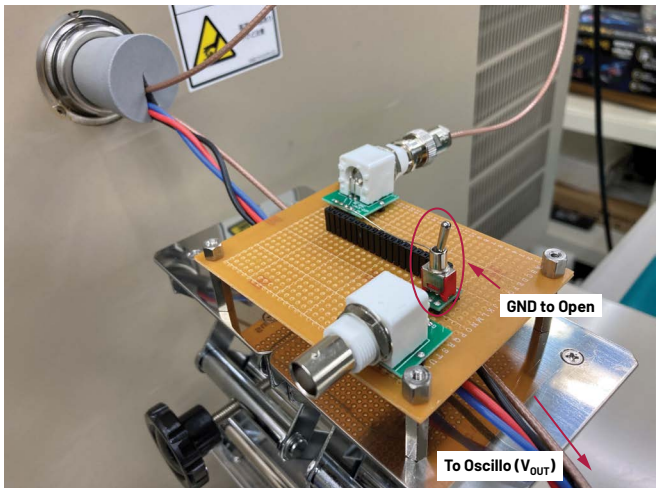

Figure 4. Setup of the capacitive integration measurement.

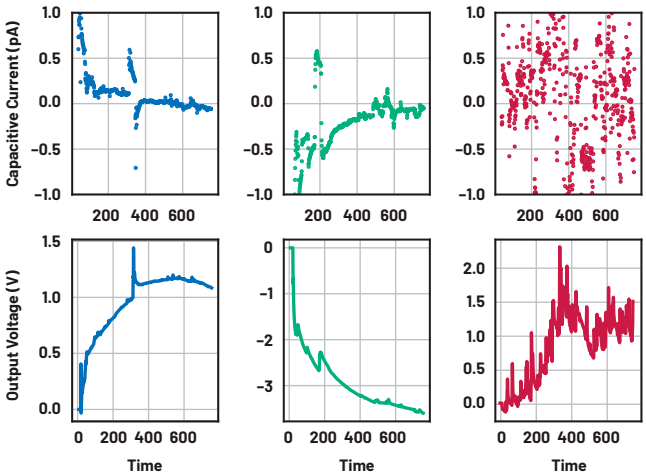

Figure 5. Measurement results. The lower side shows the output voltage of ADA4530-1 measured by the DMM, and the upper side shows the current value calculated using Equation 1. The blue line is the first measurement, the green line is the second measurement, and the red line is the third measurement.

How to Improve the Measurement Environment

In the section "Capacitive Integration Measurement," we measured I_{B+} based on the AN-1373, but the results differed. In this section, we share the steps to improve the measurement environment and thus, the accuracy of the measurements.

Mount a Shield Box and Shorten the Input Cable

First, we have made the following two improvements:

- A shield box was installed on the evaluation board inside the thermostatic chamber (see Figure 6).
- The coaxial cable connected to the noninverting input terminal was shortened to reduce the C_p (see Figure 7).

For one, we expect to reduce the effect of external noise, and for two, we expect to reduce the small leakage current in the cable (the recalculated C_p is 35.2 pF).

However, although these measures were taken and remeasured, no reproducibility was observed, similar to the results obtained in "Capacitive Integration Measurement." The waveforms differed significantly from the expected ones.

Figure 6. Installing the shield box.

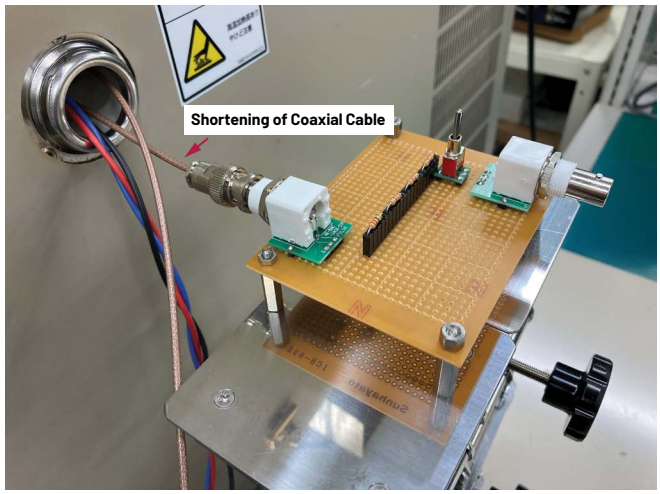

Figure 7. Shortening the coaxial cable.

Remove the Test Box

The test box used was removed and the SW was changed by directly shorting and opening the ground (see Figure 8). In other words, the conductance component called the test box was removed and the measurement was performed. As a result, we were able to obtain the waveform as shown in Figure 9.

The output voltage measured by the DMM increased with a constant slope and reached around 4.16 V in all measurements. The corresponding current shows a value of about 50 fA.

Furthermore, the red line in Figure 9 shows the waveform of the remeasurement with a shorter coaxial cable connected to the noninverting input terminal (C_p = 26.5 pF). The slope of the voltage rise is as large as the theoretical calculation.

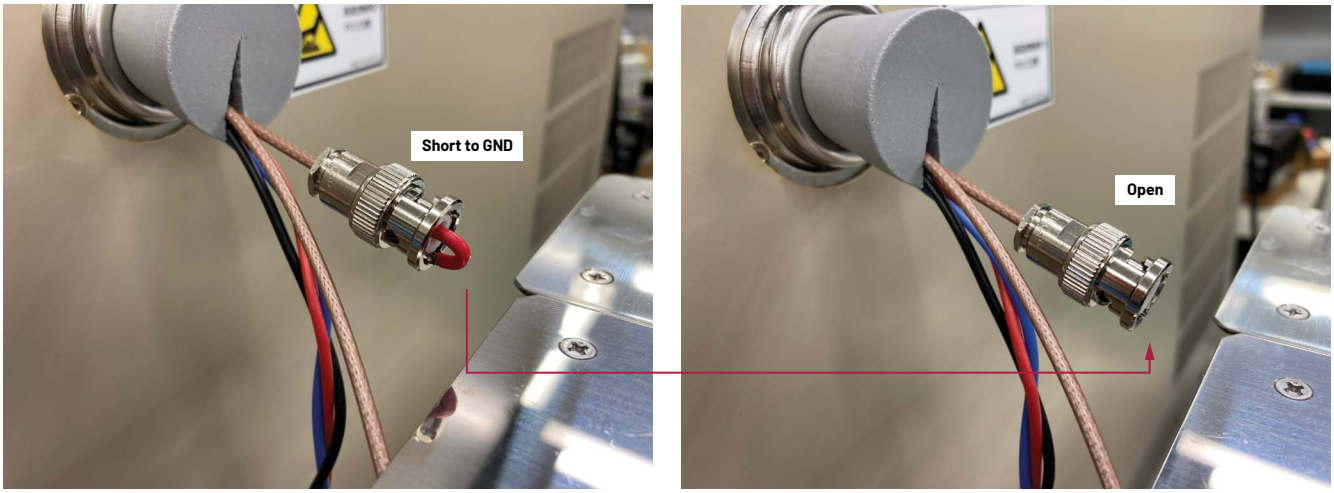

Figure 8. Measurement with test box removed. Short and open operation by hand instead of the SW.

From these measurement results, it was found that the conductance component on the input side has a significant adverse effect on the measurement accuracy.

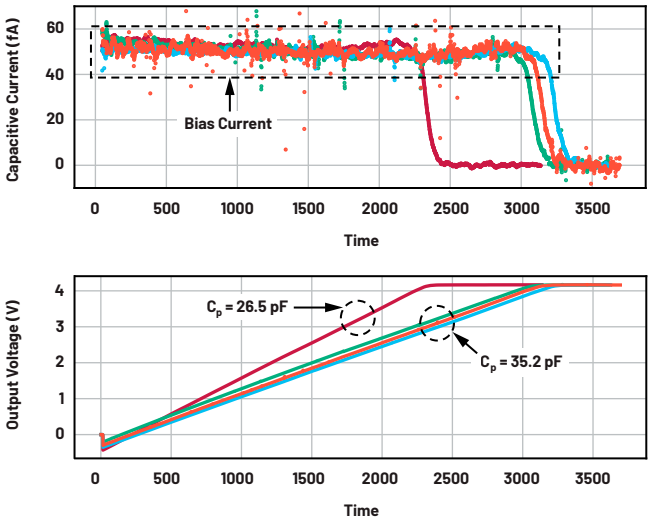

Figure 9. Measurement results after removing the test box. The blue, orange, and green lines are measurement results at C_p = 35.2 pF. The red line is the measurement result when C_p = 26.5 pF.

Conclusion

Although the fA level measurement can be performed in a general lab environment, the path of the leakage current on the input side of the operational amplifier needs to be carefully considered.

In order to improve the accuracy of the measurement, it is recommended to use a Teflon terminal block on the input side or a triaxial cable together with the evaluation board.

Acknowledgements

The author would like to thank Scott Hunt, Iku Nagai, and Jun Kakinuma for their technical advice.

Reference

Wong, Vicky. "AN-1373 Application Note: ADA4530-1 Femtoampere Level Input Bias Current Measurement." Analog Devices, Inc., October 2015.

About the Author

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Accelerate Your Test Capability and System Productivity with New MEMS Switches

Richard Houlihan, Product Marketing Manager
Naveen Dhull, Product Applications Engineer, and
Padraig Fitzgerald, Principal IC Design Engineer

Abstract

Advanced digital processor ICs require separate DC parametric and high speed digital automatic test equipment (ATE) passes for quality assurance. This creates significant cost and logistical challenges. This article explains how the ADGM1001 SPDT MEMS switch facilitates a one pass single insertion test for both DC parametric and high speed digital tests, reducing test cost and simplifying logistics for digital/RF system on chip (SoC) testing.

Figure 1. Operator mounting load board on tester for testing digital SoC.

ATE Challenges

The semiconductor market is evolving with higher speed and higher density interchip communications for advanced processors such as 5G modem ICs, graphics ICs, and central processing ICs. Assuring quality amidst this increasing complexity and demand for increased throughput is the ultimate challenge for today's ATE designers. One critical aspect is the increasing number of transmitter (Tx)/receiver (Rx) channels, which require both high speed digital and DC parametric testing. These challenges are driving complexity in semiconductor tests and not addressing them leads to increased test time, increased load board complexity, and reduction in test throughput. In turn, this will drive up operational expenses (OPEX) and reduce productivity in a modern ATE environment.

To solve these ATE challenges, a switch that is operational at DC and high frequencies is needed. ADGM1001 can pass true 0 Hz DC signals and up to 64 Gbps high speed signals. This enables an efficient single test platform (one insertion) that can be configured to test both DC parameters and high speed digital communication standards, such as PCIe Gen 4/5/6, PAM4, and USB 4.

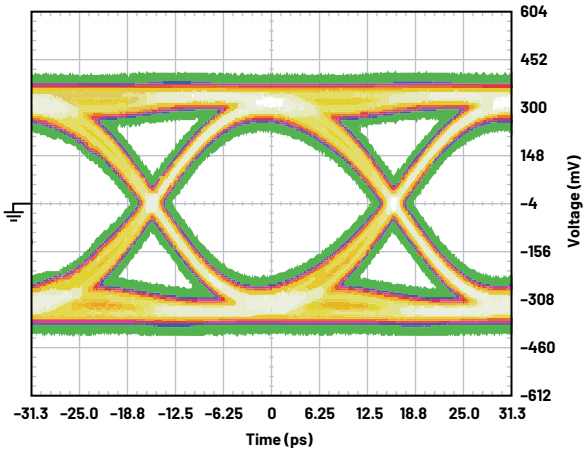

Figure 2. ADGM1001 eye diagram at 32 Gbps (RF1 to RFC with reference trace, pattern used PRBS 2^{15}-1).

How Are HSIO Pins Tested?

Testing high speed input output (HSIO) interfaces in a high volume manufacturing environment is a challenge. A common approach to validate an HSIO interface is to implement a high speed loopback test architecture. This incorporates both high speed and DC test paths in one configuration.

To perform high speed loopback testing, generally a pseudorandom bit sequence (PRBS) is transmitted at high speed from the transmitter and received at the receiver end after being looped back on the load board or test board as shown in Figure 3 (left side). At the receiver end, the sequence is analyzed to calculate the bit error rate (BER).

DC parametric tests, such as continuity and leakage tests, are performed on I/O pins to ensure device functionality. To perform these tests, pins need to be connected directly to a DC instrument where a current is forced and a voltage is measured in order to test for failures.

To perform both a high speed loopback test and a DC parametric test on the DUT I/Os, there are a few methods that can be used to test the digital SoC; for example, using MEMS switches or relays, or using two different types of load boards, one for high speed testing and the other for DC testing, which requires two insertions.

Performing high speed testing and DC parametric testing using relays becomes challenging as most relays don't operate beyond 8 GHz, so users have to compromise on signal speed and test coverage. Moreover, relays are big in size and consume a large PCB area, which impacts the solution size. Reliability is always a concern for relays as they typically only last for 10 million switching cycles, which limits system uptime and load board lifetime.

Figure 3 shows a two insertion test method to perform a high speed loopback test and a DC parametric test. In Figure 3, the left side shows the high speed digital loopback test setup, where the transmitter of the DUT is connected back to the receiver through a coupling capacitor. On the right side of Figure 3 is the DC parametric test setup where DUT pins are directly connected to the ATE tester for parametric tests. Until now, it has not been possible to have both high speed loopback and DC test functionality on the same load board due to component limitations.

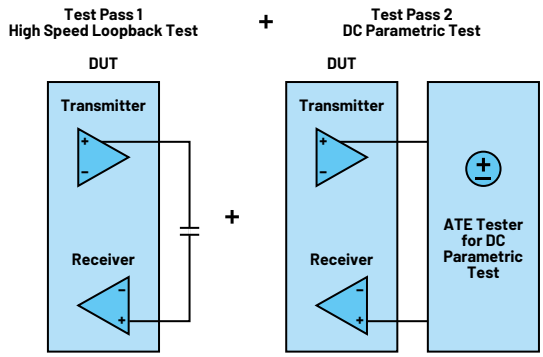

Figure 3. Illustration of a two insertion test methodology.

Challenges Associated with Two Test Insertions

- **Management of two sets of hardware:** Users must maintain and manage two sets of load boards required for DC and loopback test. This adds significant overhead, particularly when testing a high volume of parts.
- **Higher test time and higher test cost:** Two test insertion means every DUT must be tested twice, hence the indexing time during each test will be doubled, which ultimately increases the test cost and impacts the test throughput significantly.
- **Test time optimization:** Test times can't be optimized when two sets of hardware are involved. More cost will be incurred if a part fails the second insertion. The first insertion will have been wasted tester time.
- **More prone to human error:** Since every DUT is tested twice, it doubles the risk of human error.
- **Solution set up × 2:** The two test insertion approach involves two sets of hardware, which doubles the hardware setup time.
- **Logistics overhead:** The two test insertion requires more component moves. It requires moving the components between testers and potentially between test houses, creating planning and logistical challenges.

How ADI's DC to 34 GHz Switch Technology Solves the Double Insertion Problem with Superior Density

ADI's 34 GHz MEMS switch technology offers both high speed digital and DC testing capability with superior density in a small 5 mm × 4 mm × 0.9 mm LGA package, as shown in Figure 4. To perform a high speed digital test, high speed signals from a transmitter are passed through the switch and routed back to a receiver, where after decoding, the BER is analyzed. For parametric DC testing, the switch connects the pins to the DC ATE tester where parametric tests such as continuity and leakage tests are performed to ensure device functionality. During parametric DC testing, MEMS switches also provide an option to communicate with ATE at high frequency, which is required in some applications.

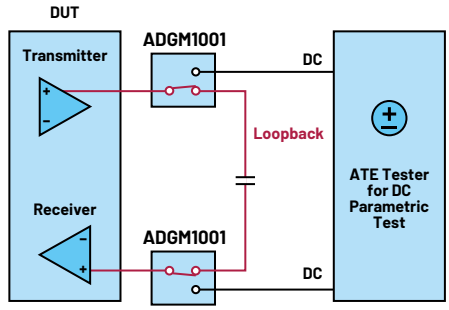

Figure 4. ADGM1001 enabling both high speed digital and DC testing (highlighting P channel only).

Figure 5 shows a high speed digital testing solution comparing the use of relays and ADGM1001 MEMS switches. The solution provided by the MEMS switches is nearly 50% smaller than the relay solution as the ADGM1001 comes in a 5 × 4 × 0.9 mm LGA package, which is 20× smaller than a typical relay. The high frequency standards such as PCIe Gen 4/5, PAM4, USB 4, and SerDes drive multiple transmitter and receiver channels, which require intense PCB densification without any layout complication to mitigate channel-to-channel variation. To meet the demand of these evolving high frequency standards, MEMS switches offer intense densification and enhanced functionality in the load board design for digital SoC testing.

Relays are typically large and have limited high frequency performance. They struggle to support higher frequency standards such as PCIe Gen 4/5, PAM4, USB 4, and SerDes with enhanced densification. The majority of the relays don't operate beyond 8 GHz and their poor insertion loss at high frequencies impacts the signal integrity and limits the test coverage.

An Introduction to ADGM1001

The ADGM1001 SPDT MEMS switch provides class-leading performance from DC to 34 GHz. Due to the ultralow parasitics and wide bandwidth of the technology, the switch has minimal impact on signals up to 64 Gbps and offers minimal channel skew, jitter, and propagation delay enabling high fidelity data transmission. It provides a low insertion loss of 1.5 dB at 34 GHz and low R_{ON} of 3 Ω typically. It offers excellent linearity of 69 dBm and can handle high RF power of 33 dBm. It comes in a small 5 mm × 4 mm × 0.95 mm plastic SMD package, with 3.3 V power supply and simple low voltage control interface. All these features make the ADGM1001 an ideal candidate for ATE applications enabling both high speed digital and DC parametric testing capability in a single test insertion, as shown in Figure 4.

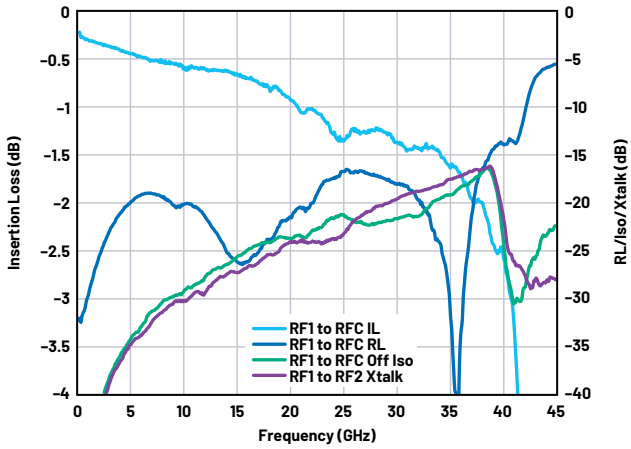

Figure 6. ADGM1001 RF performance.

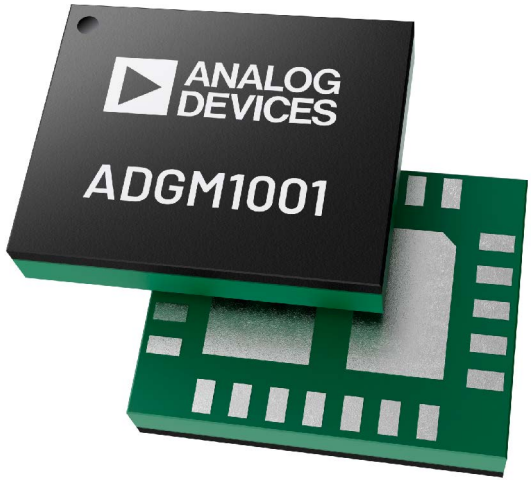

Figure 7. Package type: 5 mm × 4 mm × 0.9 mm, 24-lead LGA package.

The ADGM1001 is easy to use. It can be operated by applying V_{DD} of 3.3 V to Pin 23. However, V_{DD} can operate from 3.0 V to 3.6 V. The switches can then be controlled normally via the logic control interface (Pin 1 to Pin 4) or via the SPI interface. All the required passive components for device functionality are integrated inside the package for ease of use and board space saving. Figure 8 shows the functional block diagram of the ADGM1001.

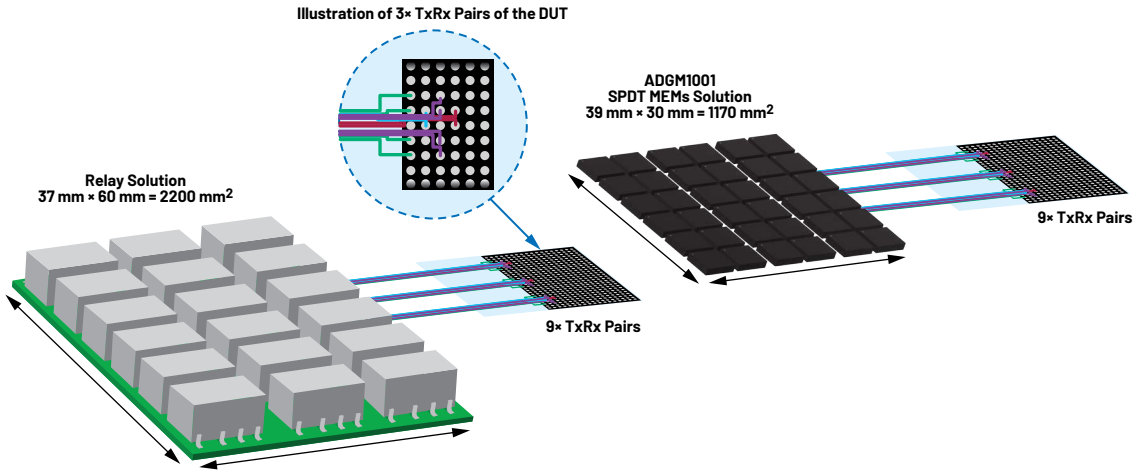

Figure 5. Comparing the loopback solution provided by relays vs. the ADGM1001.

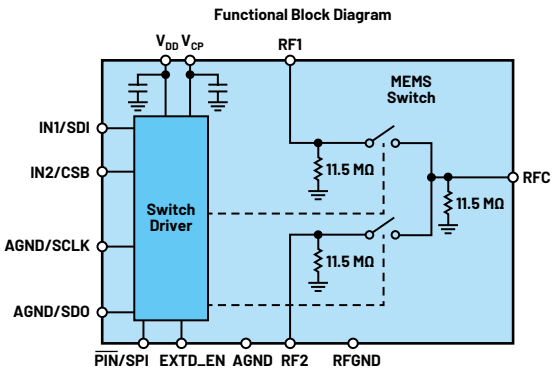

Figure 8. ADGM1001 functional block diagram.

Benefits of the ADGM1001 in Enabling a Single Insertion Test

- **Superior high speed and DC performance:** Achieving wide bandwidth from DC to 34 GHz is the challenge for the industry today. ADGM1001 delivers leading performance from DC to 34 GHz in the areas of critical parameters such as insertion loss, linearity, RF power handling, and R_{ON}.
- **Reduction in OPEX:**
  - **Hardware reduction:** A single insertion test requires single test hardware; hence, users don't need to invest in two sets of hardware and test equipment, enabling a huge reduction in OPEX.
  - **Tester uptime:** The ADGM1001 offers 100 million cycles providing superior reliability as compared to relays and improves tester uptime, which ultimately reduces OPEX.
- **Improved test throughput:** The ADGM1001 enables the use of a single insertion test, reducing the indexing time to half, which improves the test time significantly and provides improved test throughput and better asset utilization.
- **Dense solution and future-proof:** The ADGM1001 offers improved densification and enhanced functionality. MEMS switch technology has robust roadmap serving switches that are operational from DC to high frequencies and it's fully aligned to evolving technologies.
- **Reduction in logistic costs:** The single insertion method requires fewer component moves, which reduces logistic costs and eases off planning overload.
- **Fewer component moves:** In the single insertion test method, the DUT is tested in single insertion only which reduces the component moves and ultimately reduces the risk of human error.

Conclusion

The ADGM1001 is advancing switch technology from DC to 34 GHz, enabling the combination of high speed digital and DC parametric solutions for SoC testing. Its capabilities enable test time reduction, improvements in board real estate (leading to higher DUT counts and throughput), and increased uptime (improved reliability).

The ADGM1001 is the latest addition to the ADI's MEMS switch family that continues to advance the needs of high speed SoC testing. ADI's MEMS switch technology has a robust roadmap serving switching functions from DC to high frequencies to cater to future technology needs. So, stay tuned for future updates on ADI's MEMS switch technology.

About the Author

Richard Houlihan has 25 years in the electronic industry, spanning roles from design, product line management, marketing and business unit directorship. He now spearheads marketing and business development for Analog Devices' leading switch and multiplexer product lines. Richard oversees strategic innovation and product development by leveraging his background in analog front-end architectures and broad market channel experience. He holds a bachelor's degree in electrical engineering from Trinity College Dublin and an M.B.A. from Northeastern University, Boston.

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Naveen Dhull received his B.Eng. degree in electronics from the Waterford Institute of Technology, Ireland in 2011. He joined Analog Devices in 2011 as an IC layout engineer and later moved to the Applications Group for switches and multiplexers in 2016. Since 2016, he has been a product application engineer focusing on RF switches using CMOS and MEMS switch technology.

About the Author

Padraig Fitzgerald graduated from University of Limerick in 2002 with a bachelor's degree in electronic engineering. He started at Analog Devices, Limerick, Ireland, as an evaluation engineer working on solid-state switches in 2002 and moved to switch design in 2007. Padraig completed a research master's at Cork Institute of Technology on the reliability of MEMS switches. He also has a master's degree in finance and economics from the University of London. He is currently a principal design engineer in the Precision Switch Group and is a product and device designer for the MEMS switch.

High IF Sampling Puts Wideband Software-Defined Radio Within Reach

Benjamin Annino, Applications Director

Introduction

Multiband radar and electronic warfare (EW) applications put a high value on wideband, high dynamic range, agile spectral monitoring. Increasingly higher sample rate data converters are allowing architecture changes to the radio front end that shrink size, weight, power, and cost (SWaP-C), maintain performance, and evolve toward software programmable common hardware. We'll explain the technology advancements enabling this age of wideband software-defined radio expected to transform EW and multiband radar architectures.

The discussion follows a series of frequency planning figures that show the progression of improved wideband spectral scanning methods enabled by advancing data converter technology. The example carried through is a 500 MHz to 18+ GHz EW digital receiver. The annotated figures show for a given approach why the frequency planning is necessary and what allows successive improvements to SWaP-C and flexibility while maintaining dynamic range. In the progression of improving schemes, you'll see the receiver RF image gets easier to address, which allows software-defined flexibility. The need for tunable preselection to kill multitone IMD2 doesn't change with the approach and will remain a critical need into the future even as direct sampling grows ever wider.

Spectral Sensing in Days of Yore

Not too long ago, industry-leading digital receivers employed digital data converters like AD9467 and covered up to a few hundred MHz instantaneous bandwidth (iBW) at a high dynamic range. They sampled at much less than 1 GSPS, and the bandwidth centered around DC (zero IF, also known as ZIF) or centered around an IF offset (RF direct sampling). ZIF requires IQ modulators and demodulators as well as quadrature error correction (QEC) to achieve image rejection.[1,2] Radar and EW applications often require wide iBW and high image rejection. It is difficult to implement QEC that achieves acceptable image rejection as iBW exceeds several hundred MHz, a modest iBW requirement by today's EW and radar standards. This is why high performance, bandwidth-hungry multiband radar and EW prefer the latter RF direct sampling of wide iBW in the first and second Nyquist zones.

To cover spectrum outside the Nyquist zones, an RF tuner uses a swept local oscillator (LO) mixer to frequency translate a sliding block of iBW into the fixed IF that matches up with the data converter direct sample zone. Figure 1 is a block diagram of a typical dual-frequency translation low IF receiver feeding a low sample rate data converter. These receivers are capable of a high dynamic range.

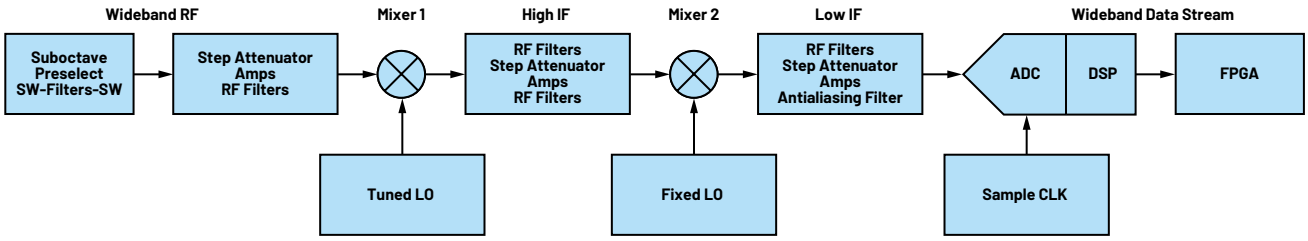

Figure 1. Dual-mixer frequency conversion used in low IF digital receivers.

Figure 2 is the frequency plan employed using the low IF scheme in Figure 1. Just like the digital data converter, the RF tuner requires high RF image rejection to avoid signal ambiguation, spurs, and noise. The single-RF mixer tuner method (red x) does not meet image rejection requirements because the IF frequency is too low to allow enough spacing between the desired band (green) and image band (red). The inadequate separation makes the required RF input filter impossible (or impractical—that is, too large and/or expensive). Thus, a dual-mixer two-stage frequency translation is employed, often called the superheterodyne receiver. The input RF is frequency translated to an intermediate high IF that is several GHz higher than the final direct sample IF. The high IF is RF filtered and frequency translated again to the final IF where it is direct sampled. This method allows realistic high performance RF filters to meet the image rejection requirement. These RF filters are high in the system SWaP-C Pareto.

The RF preselector filtering (Figure 2, yellow) is required to mitigate multiblocker induced IMD2 spurs (that is, F2 – F1 and F2 + F1). The requirement for IMD2 mitigation is independent from the image problem, but the front-end filtering often works to address both.

Spectral Sensing Today (MxFE)

Today's wideband spectral sensing approach improves on days of yore. Thanks to Analog Devices' mixed-signal front end (MxFE®), the ADC sample rate is high enough that you can direct sample the intermediate high IF following that first mixer mentioned previously. Thus, in today's wideband receivers employing MxFE, the RF tuner often doesn't require dual-mixer stages. The second Nyquist IF direct sampling is high enough in frequency to allow adequate frequency spacing of the desired input RF band and image band so that an attainable RF filter can do the job. Figure 3 shows today's single-mixer approach, and the frequency plan is shown in Figure 4.

Today's biggest SWaP-C savings come from eliminating an entire frequency translation stage with mixer, RF amps, filters, and other components. Another SWaP-C benefit of today's higher IF capability is that the direct sample now covers most of LF to 5.5 GHz. So, you don't always need an RF tuner covering all the way down to 2 GHz. In a lot of cases, you could get away with a 5 GHz to 18 GHz RF tuner. Shifting the low limit of the tuner from 2 GHz to 5.5 GHz seems

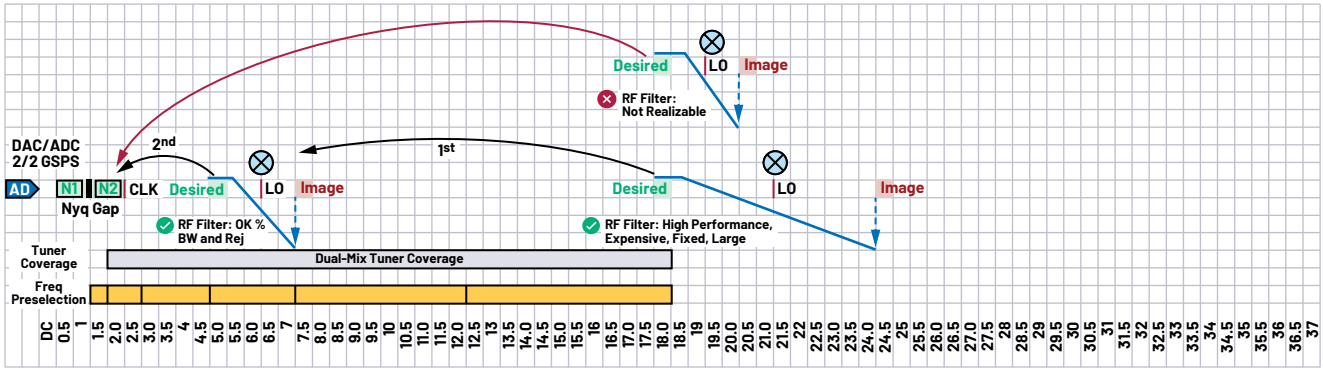

Figure 2. Old spectral scanning with narrow-band superheterodyne tuning.

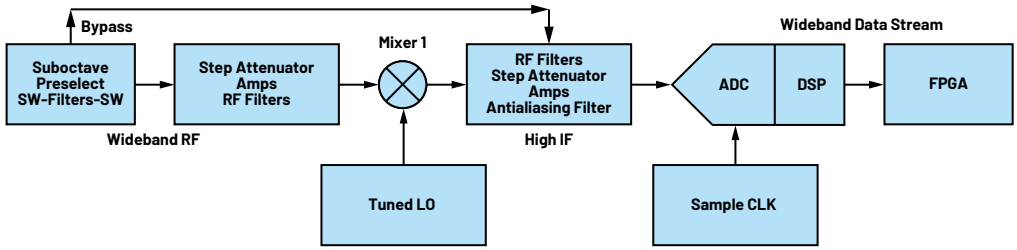

Figure 3. Single-mixer frequency conversion used in high IF digital receivers.

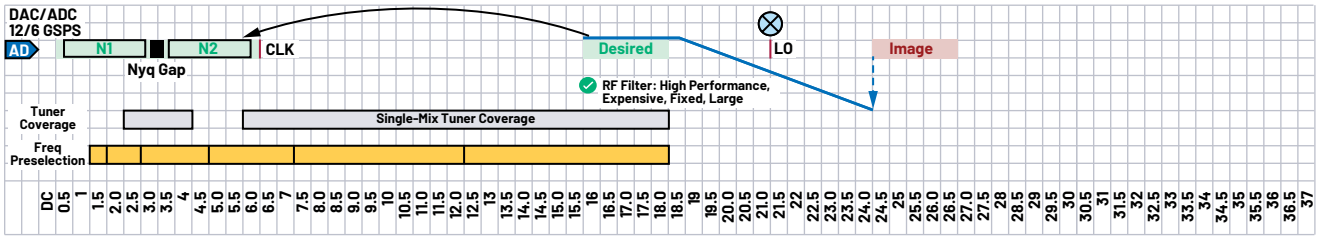

Figure 4. Today's spectral scanning approach, with wideband single-mixer tuning into MxFE sampling at 6 GSPS ADC. Mixer low sideband flips into the direct sample band and sweeps with LO.

minor but is quite significant as it eases filtering, frequency planning, and required LO range. The caveats are you still need to figure out how to cover the gap between the first and second Nyquist, which in the 6 GSPS ADC is roughly 2.7 GHz to 3.3 GHz. Another consideration is the need for switched or tunable ADC antialiasing RF filters that let you toggle between the first and second Nyquist operations.

The RF filters remain high in the system SWaP-C Pareto because they're:

- High performance, requiring low IL, flat pass band, and steep rejection skirts
- Large, using distributed planar geometries on high Q ceramics like alumina
- Lots of them are still required

The suboctave RF preselector is still required, but the requirements may ease allowing less aggressive filtering. The benefit comes from the direct signal chain not using an RF mixer, which should improve IP2.

To summarize today's scheme, wideband Nyquist sampling at high IF improves SWaP-C and iBW by eliminating an entire RF mixer stage. However, it still requires a high part count of discrete MMICs arranged in application-specific line ups and lots of high Q planar filters and structures. Thus, expensive, complex tuners that drive painful SWaP-C trades are still required (see Figure 8). SWaP-C is still looking for a transformative leap forward and it's coming.

Spectral Sensing in the Near Future

Looking ahead, even higher sample rate digital data converters get us over the tipping point to fully software-defined wideband radio at smallest SWaP-C. Today, plenty of companies already market high speed data converters at many 10s of GHz, but buyer beware: pay close attention to the multiblocker dynamic range. In order for high RF direct sample data converters to transform radar and EW, the excellent dynamic range of their narrow-band predecessors must be maintained. As sample rates and iBW push higher, maintaining excellent noise and linearity (that is, the dynamic range) is difficult and relies on countless architectural considerations. This is where ADI differentiates from the competition.

Next-generation higher sample rate data converters will allow many architecture improvements over today's MxFE scheme that is mentioned previously. We see the following three factors as the most significant:

- Direct RF sample higher IF, separating the desired and image band far enough that lower Q tunable MMIC filters are adequate. The MxFE ability to direct sample in the second Nyquist maxes out around 6 GHz. ADI's next-generation high speed digital data converters will significantly extend this coverage, and the resulting benefits are enormous.[3]
  - Now, you've finally eliminated planar high Q ceramic filters, which is a big SWaP-C savings.
  - The RF filters go from fixed (every use case has a custom set of filters) to tunable. This means a single-wideband hardware configuration can be software programmed to optimize the right performance trade for many customer frequency schemes across many use cases.
- Direct RF sample from low frequency up toward millimeter wave (mmW), except the Nyquist gap. Across this direct sample zone, you're digitally tuning while steering an RF tunable filter to knock down IMD2 inducing blockers. Noncontinuous multiband systems, common in radar, can likely eliminate the RF mixer and avoid the gap between Nyquist zones. In this case, the block diagram simplifies further to what is shown in Figure 5, and direct RF sample radar and digital beamforming take off. Systems that require continuous spectral coverage, common in EW, will still need an RF mixer stage to cover the gap between the first and second Nyquist zones and thus the block diagram looks more like Figure 3. Still, SWaP-C reduction is realized for the reasons previously mentioned.
- Extensive on-chip programmable digital signal processing (DSP) features to process the high speed wideband data stream.[4,5] The downstream FPGA responsible for processing the digital converter data payload is the worst size, power, and cost bottleneck in the system. Implementing diverse, flexible DSP on the data converter chip is more power efficient and frees up external FPGA resources for higher level mission-specific algorithms or allows a smaller, cheaper, cooler class of FPGA.

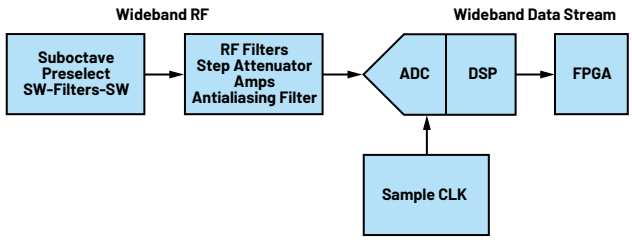

Figure 5. Direct RF sample digital receiver.

To illustrate the frequency planning advantage, Figure 6 and Figure 7 show an EW scheme providing continuous spectral coverage up to 44 GHz with the ADC clocked at 18 GSPS. First Nyquist RF direct sampling covers low frequency—8 GHz. The Nyquist gap is at 8 GHz to 10 GHz, and second Nyquist RF direct sampling covers 10 GHz to 16 GHz. The RF tuner covers the Nyquist gap plus band overlap by flipping 7 GHz to 11 GHz to an IF at 2 GHz to 6 GHz. A tunable band-pass is required at the input to the frequency mixer. The LPF rejects the image, and the HPF rejects IF feedthrough.

The RF tuner also covers higher frequencies outside the ADC RF direct sample range, shown in Figure 7. In this example, the high IF sampling at 10 GHz to 14 GHz pushes the image band far enough away so that lower Q MMIC tunable filtering is capable of achieving the required image rejection. High SWaP-C fixed filtering is eliminated from the signal chain.

Another advantage in using the RF tuner is added flexibility. It is possible that the ADC has degraded noise and linearity the higher you try to direct sample, or

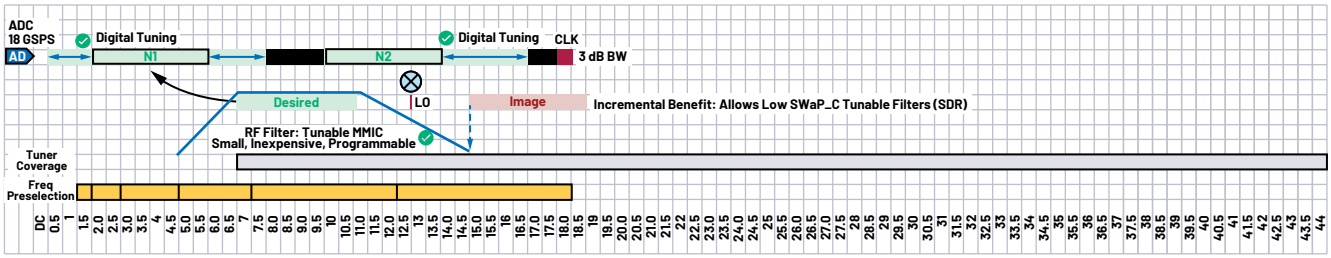

Figure 6. Tomorrow's spectral scanning covering the gap between Nyquist 1 and Nyquist 2.

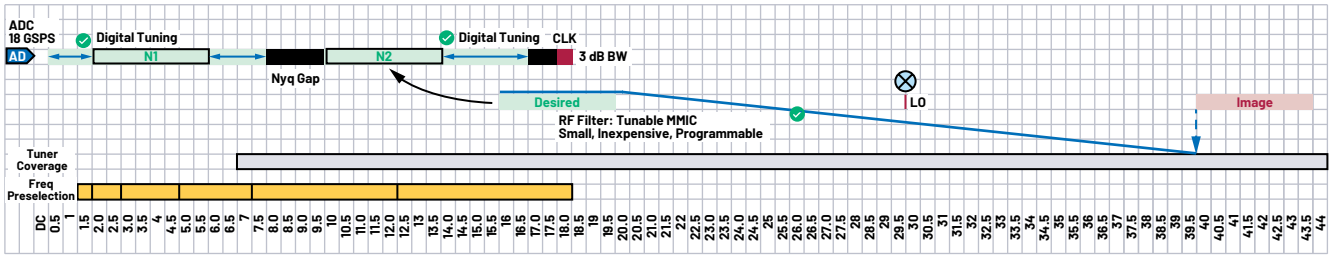

Figure 7. Tomorrow's spectral scanning using a tuner to cover mmW.

you may prefer certain ADC frequency zones that are free of HD2 and/or HD3. If better performance can be attained using the RF tuner vs. direct RF sampling, a run-time software decision can toggle modes on-the-fly.

Despite the simplifications to the frequency planning and filtering, the need for preselect suboctave filtering carries through unchanged into the future and is only helped by IP2 improvements to the data converter and RF conditioning path. For example, wideband RF amplifiers continue to improve IP2 performance and will approach OIP2 = 50 dBm from several hundred MHz to 20 GHz.

Size Comparison

What size advantage can we expect to realize going to tomorrow's receiver front end? We estimate the typical receiver RF chain goes from the size of a business card today to a postage stamp tomorrow. This is a 90% reduction in size.

To get to this size assertion, we sum the component area needed for a typical receiver and add a 50% to 65% component fill factor to account for passive components, traces, walls, and keep outs. We do the same for the next-generation receiver front end that integrates all functional blocks on chip into an integrated downconverter. The tunable LO feeding the mixer is the same for each. The assumptions are shown in Table 1, Table 2, and Table 3.

Table 1. Today's Receiver Front-End Component and Total Area

RF Chain	L (mm)	W (mm)	Area (mm^2)
Preselector, Suboctave	40	25	1000
Digital Step Attenuator	4	4	16
RF Amp	4	4	16
BPF	5	10	50
Mixer	4	4	16
BPF	5	10	50
RF Amp	4	4	16
RF Amp	4	4	16
BPF	5	10	50
Mixer	4	4	16
BPF	5	10	50
RF Amp	4	4	16
Digital Step Attenuation	4	4	16
RF Amp	4	4	16
Antialiasing BPF	5	10	50
LO1			91
LO2			91
Total Components			**1576**
Fill Factor			0.35
Total RF Front End			**4503**

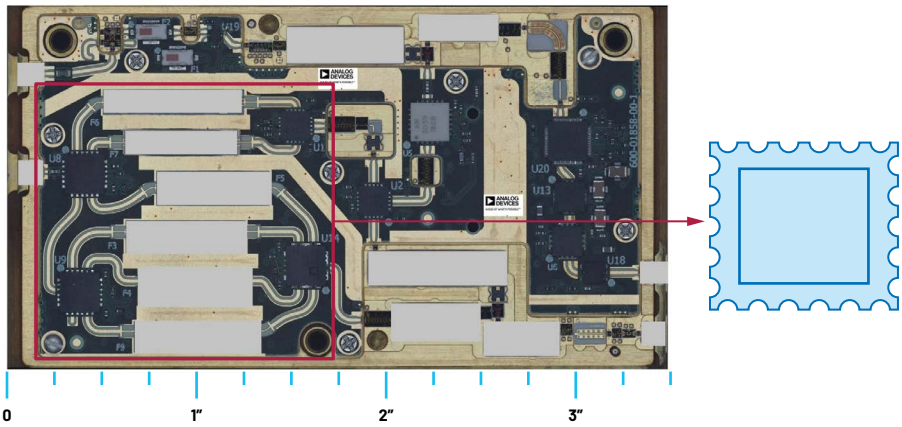

Figure 8. An example of a 2 GHz to 18 GHz receive tuner at high IF meant for an AD9082 MxFE. The need for many high Q planar RF filters (gray) drives up complexity, size, and cost. Suboctave preselection is shown in the red box. The future SDR chipset size is expected to be no larger than a stamp, as shown on the right.

Table 2. Tuned LO Component Area

RF Chain	L (mm)	W (mm)	Area (mm²)
PLL-VCO	7	7	49
TBPF	5	5	25
RF Amp	4	4	16
LPF	1	1	1
Total LO Chain			**91**

Table 3. Tomorrow's Receiver Front-End Component and Total Area

RF Chain	L (mm)	W (mm)	Area (mm²)
Preselector, Suboctave	14	10	140
Integrated Downconverter	10	10	100
Antialiasing TBPF	6	3	18
LO			91
Total Components			**258**
Fill Factor			0.5
Total RF Front End			**516**

Conclusion

As ADI's high speed data converter Nyquist sample rate and iBW push higher while maintaining leading dynamic range, frequency planning benefits allow converged, simplified RF front-end architectures. In the past, high performance integrated frequency translation ICs employing suboctave RF filtering and gain control were hard to nail down because everybody's use case, frequency plan, and resulting RF/IF filtering were different. Things are about to change drastically.

New monolithic radio tuners will be natively wideband with on-chip adaptive RF filtering capability and AGC. The vast, fragmented application realm of wideband tuning will converge to common hardware blocks within application-specific adaptive software loops. The system developer realizes time to market and cost benefits as application-specific advantage shifts away from unique hardware toward differentiated software algorithms on common flexible hardware platforms. All this at shrinking SWaP-C.

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About the Author

Benjamin Annino is the applications director for the Aerospace and Defense Business Unit at Analog Devices. He joined Hittite Microwave in 2011 before transitioning to Analog Devices in 2014. Prior to that, he worked at Raytheon on various radar technologies. He has a B.S.E.E. from Dartmouth College, an M.S.E.E. from University of Massachusetts-Lowell, and an M.B.A. from University of Massachusetts-Amherst.

What Are the Best Applications for IoT in the New World of IC Power Management?

Diarmuid Carey, Central Applications Engineer

Abstract

This article explores Internet of Things (IoT) battery technology. It describes some of the problems that designers face with power sourcing and provides solutions from Analog Devices. These solutions are highly efficient and can help curb other problems in your IoT devices, including size, weight, and temperature.

With the growing use of IoT devices in industrial equipment, home automation, and medical applications, there is increasing pressure to optimize the power management portion of these devices—either through smaller form factor, better efficiency, improved current consumption, or faster charging times (for portable IoT devices). All of this must be achieved in a small form factor that does not negatively impact thermals nor interfere with the wireless communication implemented by these devices.

What Is IoT?

This particular IoT application area comes under many different guises. It generally refers to a smart, network connected electronic device that is likely battery-powered and sends precomputed data to the cloud-based infrastructure. It utilizes a mixture of embedded systems such as processors, communication ICs, and sensors to collect, respond to, and send data back to a central point or other node in the network. This can be anything from a simple temperature sensor reporting room temperature back to a central monitoring area, all the way up to a machine health monitor that tracks the long-term health of very expensive factory equipment.

Ultimately, these devices are being developed to solve a particular challenge, whether that be to automate tasks that would typically require human intervention, like home or building automation, or perhaps to improve the useability and longevity of equipment in the case of industrial IoT applications, or even to improve safety if you consider condition-based monitoring applications implemented in structure-based applications such as bridges.

Example Applications

The application areas for IoT devices are almost endless with new devices and use cases being thought of every day. Smart transmitter-based applications gather data about the environment in which they sit to make decisions about controlling heat, setting off alarms, or automating particular tasks. In addition, portable instruments like gas meters and air quality measurement systems provide an accurate measurement through the cloud to a control center. GPS tracking systems are another application. They allow the tracking of shipping containers as well as livestock such as cows through smart ear tags. These comprise just a small area of cloud connected devices. Other areas include wearable healthcare and infrastructure sensing applications.

A significant growth area is industrial IoT applications, which are part of the fourth industrial revolution where smart factories take center stage. There's a broad range of IoT applications that are ultimately trying to automate as much of the factory as possible, whether that be through the use of automated guided vehicles (AGVs), smart sensors such as RF tags or pressure meters, or other environmental sensors positioned around the factory.

From an ADI perspective, the high level IoT focus has been on five main areas:

- Smart health—supporting vital signs monitoring applications both at a clinical level as well as consumer applications.
- Smart factories—focusing on building Industry 4.0 by making factories more responsive, flexible, and leaner.
- Smart buildings/smart cities—using intelligent sensing for building security, parking space occupancy detection, as well as thermal and electrical control.
- Smart agriculture—using the technology available to enable automated farming and resource usage efficiencies.
- Smart infrastructure—building on our condition-based monitoring technology to monitor movement and structural health.

More information on these focus areas and the technologies available to support them can be found at analog.com/IoT.

IoT Design Challenges

What are the key challenges facing a designer in the ever-growing IoT application space? The majority of these devices, or nodes, are being installed after the fact or in hard-to-reach areas, so running power to them is not a possibility. This of course means that they are totally reliant on batteries and/or energy harvesting as a power source.

Moving power around large facilities can be quite expensive. For example, consider powering a remote IoT node in a factory. The idea of running a new power cable to power this device is costly as well as time consuming, which essentially leaves battery power or energy harvesting as the remaining options to power these remote nodes.

The reliance on battery power introduces a need to follow a stringent power budget to ensure that the lifetime of the battery is maximized, which of course has an impact on the total cost of ownership of the device. Another downside to battery usage is the need to replace the battery after its life has expired. This includes not only the cost of the battery itself, but also the high cost of human labor to replace and possibly dispose of the old battery.

An additional consideration on the battery cost and size—it is very easy to just overdesign the battery to ensure that there is sufficient capacity to achieve the lifetime requirement, which is very often greater than 10 years. However, overdesign results in additional cost and size, so it is extremely important to not only optimize the power budget but also to minimize the energy usage where possible in order to install the smallest possible battery that will still meet your design requirements.

Power in IoT

For the purposes of this power discussion, the power sources for IoT applications can be seen as three scenarios:

- Devices that rely on nonrechargeable battery power (primary battery)
- Devices that require rechargeable batteries
- Devices that utilize energy harvesting to provide system power

These sources can be used individually, or alternatively combined if the application requires it.

Primary Battery Applications

You are all aware of different primary battery applications, which are also known as nonrechargeable battery applications. These are geared toward applications where only occasional power is used—that is, the device is powered up occasionally before going back into a deep sleep mode where it draws minimal power. The main advantage of using this as a power source is it provides a high energy density and a simpler design—since you don't need to accommodate battery charging/management circuitry—as well as a lower cost, as batteries are cheaper and fewer electronics are required. They fit well into low cost, low power drain applications, but because these batteries have a finite lifetime, they are not well suited to applications where power consumption is a little higher, so this incurs a cost for both a replacement battery as well as the cost of the service technician required to replace the batteries.

Consider a large IoT installation with many nodes. As you have a technician on-site replacing the battery for one device, very often all the batteries will end up being replaced at one time to save the labor cost. Of course, this is wasteful and just adds to our overall global waste problem. On top of that, nonrechargeable batteries provide only about 2% of the power used to manufacture them in the first place. The ~98% of wasted energy makes them a very uneconomical power source.

Obviously, these do have a place in IoT-based applications. Their relatively low initial cost makes them ideal for lower power applications. There are loads of different types and sizes available, and as they don't need much additional electronics for charging or management, they are a simple solution.

From a design perspective, the key challenge is making the most use out of the energy available from these little power sources. To that end, much time needs to be spent creating a power budget plan to ensure that the lifetime of the battery is maximized, with 10 years being a common lifetime target.

For primary battery applications, two parts from our nanopower family of products are worth considering—the LTC3337 nanopower coulomb counter and the LTC3336 nanopower buck regulator, shown in Figure 1.

The LTC3336 is a low power DC-to-DC converter running from up to a 15 V input with programmable peak output current level. The input can go as low as 2.5 V, making it ideal for battery-powered applications.

The quiescent current is exceptionally low at 65 nA while regulating with no load. As DC-to-DC converters go, this is pretty easy to set up and use in a new design. The output voltage is programmed based on how the OUT0 to OUT3 pins are strapped.

The companion device to the LTC3336 is the LTC3337, a nanopower primary battery state of health monitor and coulomb counter. This is another easy device to use in a new design—simply strap the IPK pins according to the peak current required, which is in the 5 mA to 100 mA region. Run a few calculations based on your selected battery, then populate the recommended output cap based on the selected peak current, which is noted in the data sheet.

Ultimately, this is a fantastic pairing of devices for IoT applications with a limited power budget. These parts can both accurately monitor the energy usage from the primary battery and efficiently convert the output to a usable system voltage.

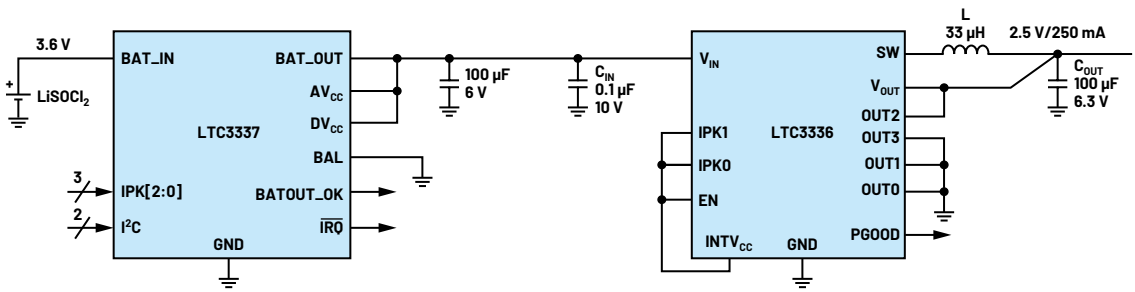

Figure 1. LTC3337 and LTC3336 application circuit.

Rechargeable Battery Applications

Let's move on to rechargeable applications. These are a nice choice for higher power or higher drain IoT applications where primary battery replacement frequency is not an option. A rechargeable battery application is a higher cost implementation because of the initial cost of the batteries and the charging circuitry, but in higher drain applications where the batteries are drained and charged frequently, the cost is justified and soon paid back.

Depending on the chemistry used, a rechargeable battery application can have a lower initial energy than a primary cell, but on a longer term it is the more efficient option, and, overall, is less wasteful. Depending on the power needs, another option is capacitor or supercapacitor storage, but these are more for shorter-term backup storage.

Battery charging involves several different modes and specialist profiles depending on the chemistry used. For example, a lithium-ion battery charge profile is shown in Figure 2. Across the bottom is the battery voltage, and charge current is on the vertical axis.

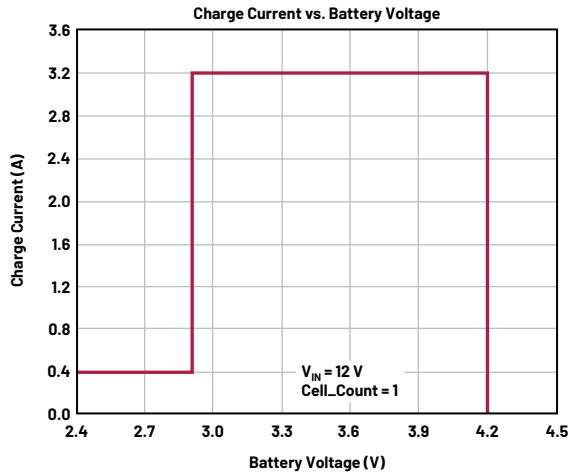

Figure 2. Charge current vs. battery voltage.

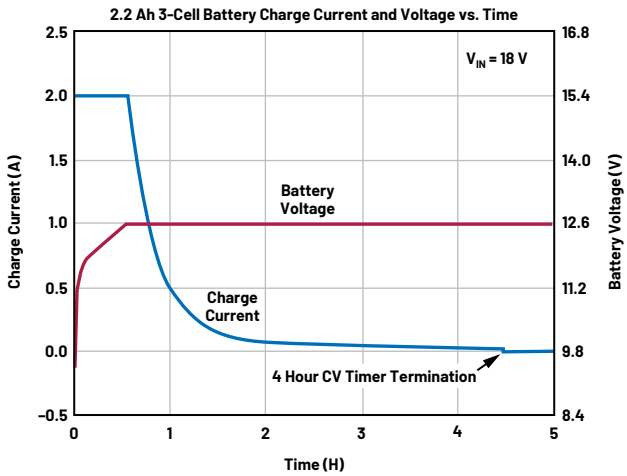

Figure 3. Charge voltage/current vs. time.

When the battery is severely discharged, as on the left of Figure 2, the charger needs to be clever enough to put it in precharge mode to slowly increase the battery voltage to a safe level before entering constant current mode.

In constant current mode, the charger pushes the programmed current into the battery until the battery voltage rises to the programmed float voltage.

Both the programmed current and voltage are defined by the battery type used—the charge current is limited by the C-rate and the required charge time, and the float voltage is based on what is safe for the battery. System designers can reduce the float voltage a little to help with lifetime of the battery if required by the system—like everything with power, it's all about trade-offs.

When the float voltage is reached, it can be seen that the charge current drops to zero and this voltage is maintained for a time based on the termination algorithm.

Figure 3 provides a different graph for a 3-cell application showing the behavior over time. The battery voltage is shown in red and charge current is in blue. It starts off in constant current mode, topping out at 2 A until the battery voltage reaches the 12.6 V constant voltage threshold. The charger maintains this voltage for the length of time defined by the termination timer—in this case, a 4-hour window. This time is programmable on many charger parts.

For more information on battery charging, as well as some interesting products, I'd recommend the *Analog Dialogue* article "Simple Battery Charger ICs for Any Chemistry."

Figure 4 shows a nice example of a versatile buck battery charger, the LTC4162, which can provide a charge current up to 3.2 A and is suitable for a range of applications including portable instruments and applications requiring larger batteries or multicell batteries. It can also be used to charge from solar sources.

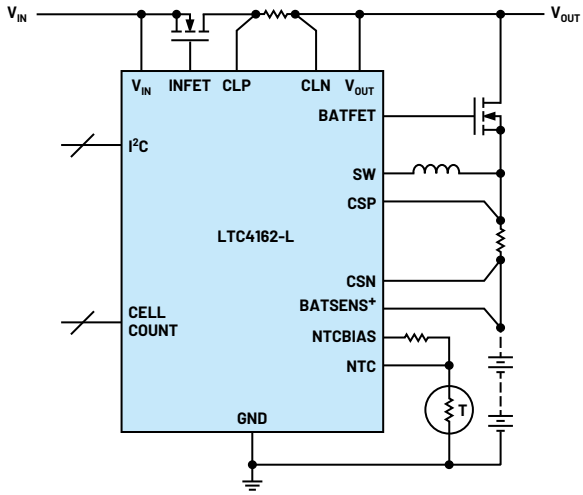

Figure 4. The LTC4162, a 3.2 A buck battery charger.

Energy Harvesting Applications

When working with IoT applications and their power sources, another option to consider is energy harvesting. Of course, there are several considerations for the system designer, but the appeal of free energy cannot be understated, especially for applications where the power requirements aren't too critical and where the installation needs to be hands off—that is, no service technician can get to it.

There are many different energy sources to choose from, and they don't need to be an outdoor application to take advantage of them. Solar as well as piezoelectric or vibrational energy, thermoelectric energy, and even RF energy can be harvested (although this has a very low power level).

Figure 5 provides an approximate energy level when using different harvesting methods.

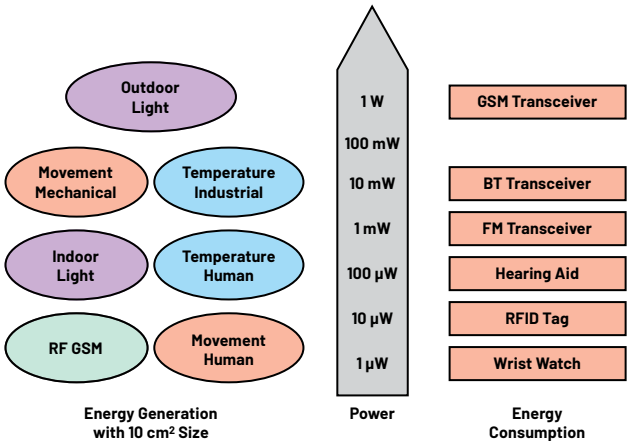

Figure 5. Energy sources and approximate levels available for various applications.

As for disadvantages, the initial cost is higher compared to the other power sources discussed before, since you need a harvesting element such as a solar panel, piezoelectric receiver, or a Peltier element, as well as the energy conversion IC and associated enabling components.

Another disadvantage is the overall solution size, particularly when compared to a power source like a coin cell battery. It's difficult to achieve a small solution size with an energy harvester and conversion IC.

Efficiency wise, this can be a tricky one to manage low energy levels. This is because many of the power sources are AC, so they need rectification. Diodes are used to do this. The designer must deal with the energy loss resulting from their inherent properties. The impact of this is lessened as you increase the input voltage, but that's not always a possibility.

The devices that pop up in most energy harvesting discussions are from the ADP509x family of products, and the LTC3108, which can accommodate a wide range of energy harvesting sources with multiple power paths and programmable charge management options that offer the highest design flexibility. A multitude of energy sources can be used to power the ADP509x but also to extract energy from that power source to charge a battery or power a system load. Anything from solar (both indoor and outdoor) to thermoelectric generators to extract thermal energy from body heat in wearable applications or engine heat can be used to power the IoT node. Another option is to harvest energy from a piezoelectric source, which adds another layer of flexibility—this is a nice option to extract power from an operational motor, for example.

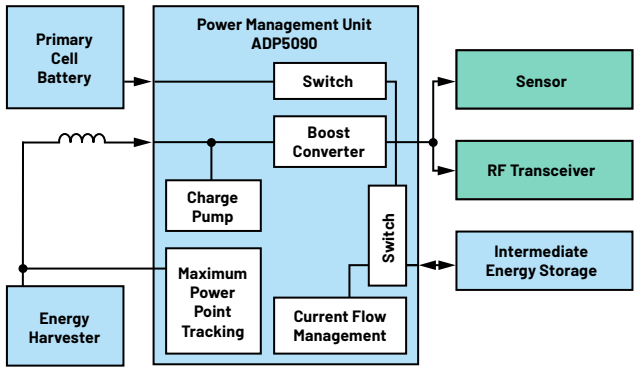

Figure 6. Block diagram of the ADP5090 in a harvesting application.

Another device that is capable of being powered from a piezoelectric source is the ADP5304, which operates with a very low quiescent current (260 nA typical with no load), making it ideal for low power energy harvesting applications. The data sheet shares a typical energy harvesting application circuit (see Figure 7), powered from a piezoelectric source and being used to provide power to an ADC or an RF IC.

Energy Management

Another area that should be part of any discussion relating to applications with a limited power budget is energy management. This starts with developing a power budget calculation for the application prior to looking at different power management solutions. This essential step helps system designers understand the key components used in the system and how much energy they require. This impacts their decision to select a primary battery, rechargeable battery, energy harvesting, or a combination of these as the power supply methodology.

The frequency of the IoT device gathering a signal and sending it back to the central system or cloud is another important detail when looking at energy management, which has a large impact on overall power consumption. A common technique is to duty cycle the power usage or stretch the time between waking the device up to gather and/or send data.

Making use of standby modes on each of the electronic devices (if available) is also a useful tool when trying to manage the system energy usage.

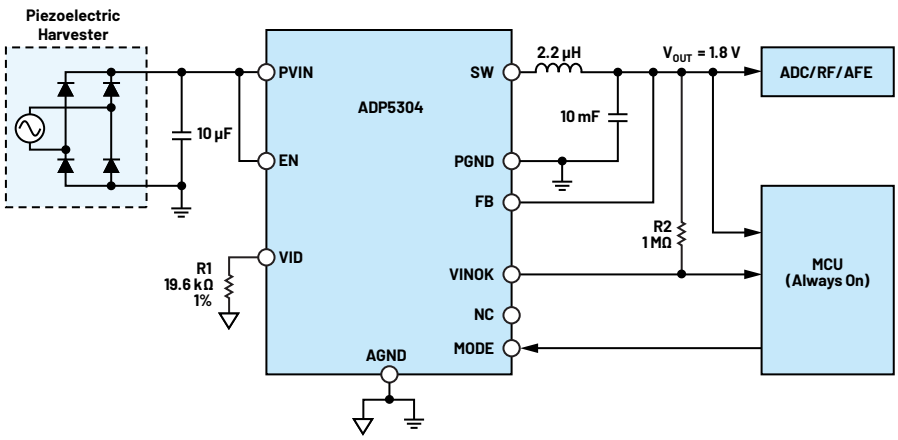

Figure 7. ADP5304 piezoelectric source application circuit.

Conclusion

As with all electronic applications, it is important to consider the power management portion of the circuit as early as possible. This is even more important in power-constrained applications such as IoT. Developing a power budget early in the process can help the system designer identify the most efficient path and suitable devices that meet the challenges posed by these applications while still achieving high energy efficiency in a small solution size.

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About the Author

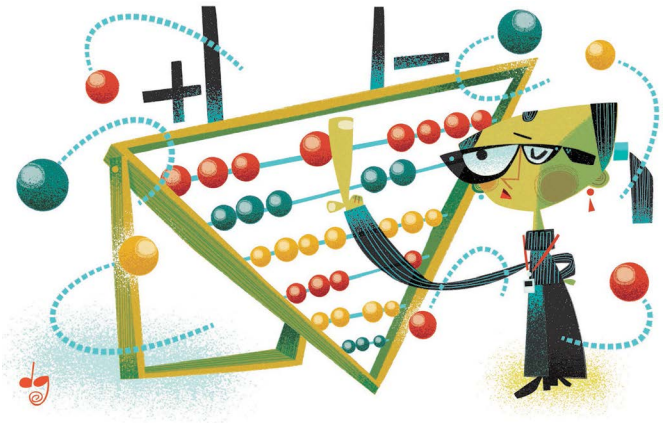
Diarmuid Carey is an applications engineer with the European Centralized Applications Center based in Limerick, Ireland. He has worked as an applications engineer since 2008 and joined Analog Devices in 2017, providing design support for the Power by Linear portfolio for European broad market customers. He holds a Bachelor of Engineering in computer engineering from University of Limerick.

RAQ Issue 201: How to Measure Op Amp Input Capacitance to Minimize Noise

Thomas Brand, Field Applications Engineer

Question:

While measuring op amp input capacitance, what should I focus on?



Answer:

You must ensure that the measurement accuracy is not degraded by the stray capacitance and inductance of the PCB or test setup. You can minimize these issues by using probes with low capacitance, using short lines on the PCB, and avoiding huge ground planes below the signal traces.

Operational amplifiers are used in a wide variety of electronic circuits. Their task is to amplify small electrical voltages for further signal processing. Applications such as smoke detectors, photodiode transimpedance amplifiers, medical instruments, and even industrial control systems require the lowest possible op amp input capacitance because, among other things, this affects the noise component, which in turn affects system stability, especially for systems with high frequencies and gains.

To maximize the accuracy of a corresponding circuit, it is necessary to know the input capacitance of the op amp. Data sheets, however, often do not provide this information, so it must be independently determined. This can be difficult because the input capacitance in many cases is only a few pF.

Table 1 lists a few different examples of operational amplifiers and their respective input capacitance values.

Table 1. Different Operational Amplifiers and Their Input Capacitance Values

Op Amp	Op Amp Type	Input Capacitance
LT1792	JFET input op amp	14 pF
LT1813	Low noise op amp	2 pF
AD826	High speed dual op amp	1.5 pF
ADA4097-1	Low input bias current/precision op amp	3 pF
AD8009	Current feedback op amp	2.6 pF

How to Determine Input Capacitance

An easy way to determine the input capacitance of an op amp is to add a resistor in series (R_{SERIES}) with the op amp input as shown in Figure 1. This yields a first-order low-pass filter with a frequency response that can be recorded by a network analyzer. The input capacitance can be calculated from the frequency response. The resistance R_{SERIES} is typically in the range of 10 kΩ to 100 kΩ.

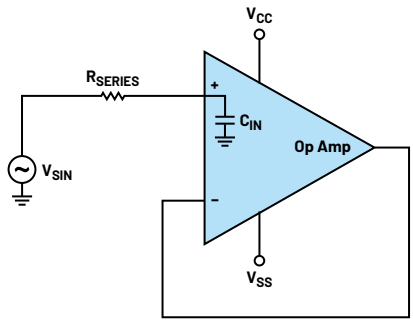


Figure 1. With a series resistor at the op amp input, the input capacitance of the op amp can be measured.

When recording the frequency response, you must ensure that the measurement accuracy is not degraded by the stray capacitance and inductance of the PCB or test setup.

A high measurement resolution should be selected for minimal stray capacitance. The use of FET probes of low capacitance (<1 pF) is advisable.

The PCB capacitance with respect to ground should also be kept as low as possible. This can be achieved by ensuring that there is no ground plane below the signal traces and the series resistor.

In addition, the shortest possible lines and (resistor) leads should be used to avoid additional sources of error such as series and parasitic inductance.

Figure 2 shows a possible test setup, using a network analyzer and a power splitter.

The power splitter has the task of dividing the signal. The signal 1:1 is fed unchanged to the input of the network analyzer and is also passed through the inserted low-pass filter to the op amp input. The network analyzer then generates the frequency response from the difference between these two signals.

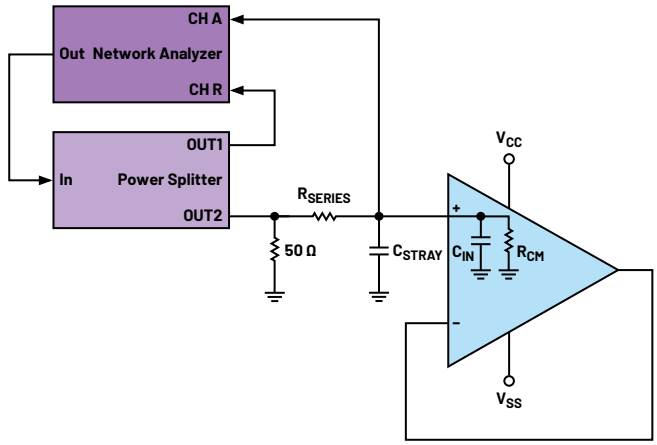


Figure 2. Test setup for determining the op amp input capacitance.

For the measurement itself, the stray capacitance C_{STRAY} needs to be determined. For this, the signal is applied without the op amp on the board. From the resulting Bode plot, C_{STRAY} is calculated as shown in Equation 1:

$$C_{STRAY} = \frac{1}{2 \times \pi \times R_{TH1} \times f_1 (-3\ \text{dB})} \quad (1)$$

f_1(–3 dB) is the –3 dB corner frequency measured with the network analyzer without an operational amplifier, and R_{TH1} is a function of the inserted series resistance (R_{SERIES}), the input termination resistance (50 Ω), and the 50 Ω source impedance at the power splitter (Thévenin equivalent):

$$R_{TH1} = R_{SERIES} + (50||50) \quad (2)$$

Next, the op amp is placed on the PCB.

Because the stray capacitance of the PCB is in parallel with the input capacitance of the op amp, Equation 1 is supplemented with C_{IN} as shown in Equation 3:

$$C_{IN} + C_{STRAY} = \frac{1}{2 \times \pi \times R_{TH2} \times f_2 (-3\ \text{dB})} \quad (3)$$

This time, f_2(–3 dB) is the –3 dB corner frequency measured by the network analyzer with an op amp and R_{TH2} is a function of the inserted series resistance, the input termination resistance (50 Ω), the output impedance of the power splitter (50 Ω), and the common-mode input impedance of the op amp (R_{CM}):

$$R_{TH2} = (R_{SERIES} + (50||50))|R_{CM} \quad (4)$$

In general, for op amps with CMOS inputs, $R_{SERIES} << R_{CM}$. Therefore, $R_{TH2} \approx R_{TH1}$ and Equation 3 can be rewritten as shown in Equation 5:

$$C_{IN} + C_{STRAY} = \frac{1}{2 \times \pi \times R_{TH1} \times f_2 (-3\ \text{dB})} \quad (5)$$

The input capacitance of the operational amplifier can then be determined using equations 1 and 5.

Conclusion

The input capacitance of an operational amplifier can be difficult to measure. It often lies in the pF range and parasitic effects in the test setup distort the result. With a small test setup and the appropriate measuring equipment consisting of a network analyzer and a power splitter, it is easy to determine the input capacitance by first determining the stray capacitance (error capacitors in the test setup) and then determining the combined capacitance (error capacitors and input capacitance) of the op amp circuit via the frequency response. With the equations shown earlier, the actual input capacitance of the operational amplifier can be calculated.

About the Author

Thomas Brand began his career at Analog Devices in Munich in 2015 as part of his master's thesis. After graduating, he was part of a trainee program at ADI. In 2017, he became a field applications engineer. Thomas supports large industrial customers in Central Europe and also specializes in the field of Industrial Ethernet. He studied electrical engineering at the University of Cooperative Education in Mosbach before completing his postgraduate studies in international sales with a master's degree at the University of Applied Sciences in Constance.

How Monolithic Driver + MOSFET (DrMOS) Technology Improves Power System Design

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Joseph Rommel Viernes, Power Applications Staff Engineer
Kareem Atout, Senior Systems Engineer
Gary Sapia, Team Leader, and
Marvin Neil Cabuenas, Senior Firmware Engineer

Abstract

This article describes the latest driver plus MOSFET (DrMOS) technology and its advantages in voltage regulator module (VRM) applications. Monolithic DrMOS devices enable power systems to improve greatly in terms of power density, efficiency, and thermal performance, which in turn can enhance the overall performance of end applications.

Introduction

Through the advancement of technology, microprocessors have become denser and faster on a horizontal scale thanks to the multicore architecture. Thus, the corresponding power required by these devices has increased drastically. Such power for microprocessors is provided by a voltage regulator module (VRM).

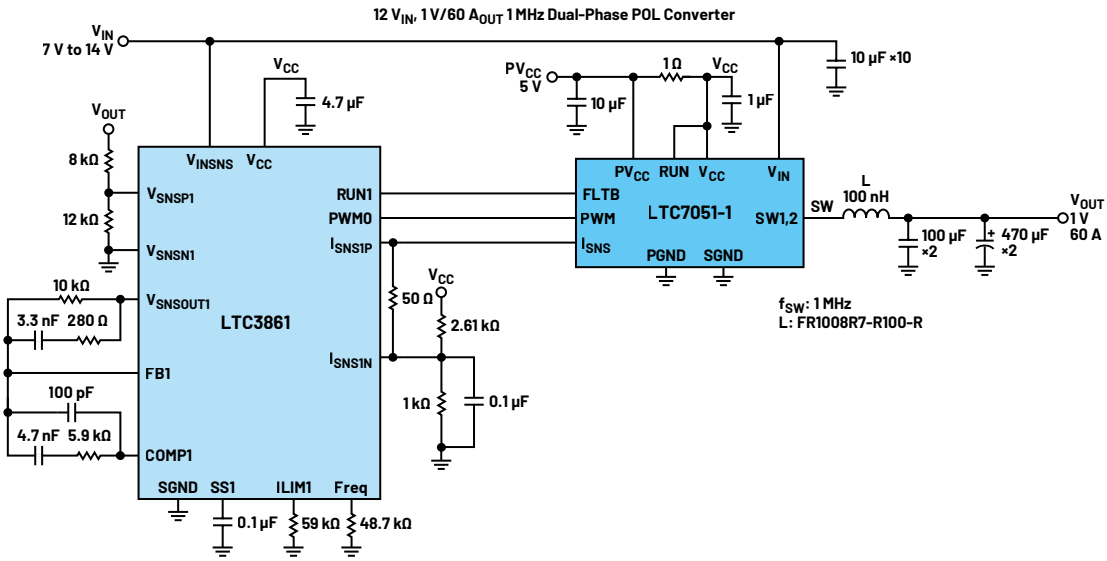

Figure 1. Dual-phase POL converter.

There are two main parameters driving the development of voltage regulators in this field. First is the power density (power over unit volume) of the voltage regulator, which must be increased sharply to meet the high power requirement of the system in a limited volume of space. The other parameter is power conversion efficiency for reduced power losses and better thermal management.

As developmental challenges continue to evolve, the power industry will find ways of satisfying the consequential requirements. One solution incorporates an advanced switching MOSFET, which is a major building block of voltage regulators, and its corresponding driver in a single, monolithic die along with advanced packaging, enabling compact and efficient power conversion. These DrMOS power stages have optimized high speed power conversion.

As the demand for these power stages, known as smart power stages, increased steadily and power-switching technologies continued to advance, Analog Devices came up with its version of DrMOS smart power modules. The LTC705x DrMOS series makes use of ADI's patented Silent Switcher® 2 architecture, along with an integrated bootstrap circuitry, which allow the DrMOS module to switch at an ultrafast speed with reduced power losses and switch-node voltage overshoot for improved performance. LTC705x DrMOS devices also offer safety features such as overtemperature protection (OTP), input overvoltage protection (V_{IN} OVP), and undervoltage lockout (UVLO) protection.

LTC7051 SilentMOS Smart Power Stage

The LTC7051, a member of the LTC705x DrMOS family, is a 140 A monolithic smart power module that successfully combines high speed drivers with high figure of merit (FOM) top and bottom power MOSFETs and a comprehensive monitoring and protection circuitry in one electrically and thermally optimized package. Together with a suitable PWM controller, this smart power stage provides the industry's highest efficiency, lowest noise, and highest density power conversion available to the market. This combination equips a high current voltage regulator module with the latest techniques on efficiency and transient response. The typical application of LTC7051 is illustrated in Figure 1. It functions as the main switching circuitry of a buck (step-down) converter in conjunction with the LTC3861 dual, multiphase step-down voltage mode DC-to-DC controller with accurate current sharing.

To demonstrate the key features of LTC7051, ADI created an evaluation board to showcase the performance of the LTC7051 vs. a product available from the competition. Such a demonstration platform facilitates an unbiased, accurate way of comparing essential parameters such as efficiency, power loss, telemetry accuracy, thermal, and electrical performance of LTC7051 DrMOS with those of a competitive product. The objective of the comparison was to remove any doubt on the validity of the outcome. The said demonstration platform was used to highlight best-in-class DrMOS performance metrics regardless of the manufacturer.

DrMOS Analysis Evaluation Hardware

The analysis demonstration hardware has the following key features:

- A PWM controller that can operate on a wide range of input and output voltages and switching frequencies. In this application, the controller is LTC7883, a quad output polyphase step-down DC-to-DC voltage-mode controller, shown in Figure 2.
- Identical power stage design for both the LTC7051 and competitor devices.
- LTpowerPlay® power system management environment for comprehensive telemetry of system performance provided by the LTC7883.
- Can withstand extended ambient temperature in accordance with the specified operating temperature range of both ADI and competitor devices.
- Board is designed for easy thermal capture and measurement.

The DrMOS analysis demonstration board is shown in Figure 3. The board was carefully designed to include the key features previously mentioned. Components are symmetrically and systematically placed across each power rail and have the same PCB size and area to limit discrepancies between the power rails. Layout routing and layer stack-up are done symmetrically as well.

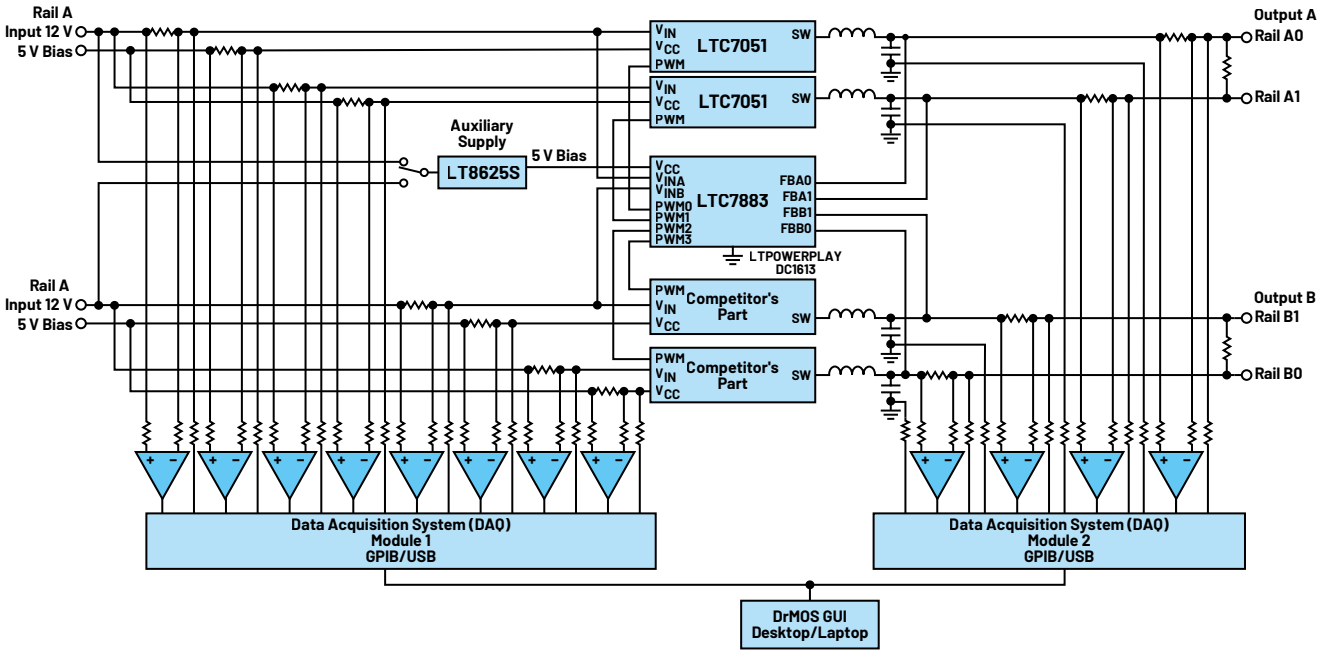

Figure 2. Analysis demonstration board block diagram.

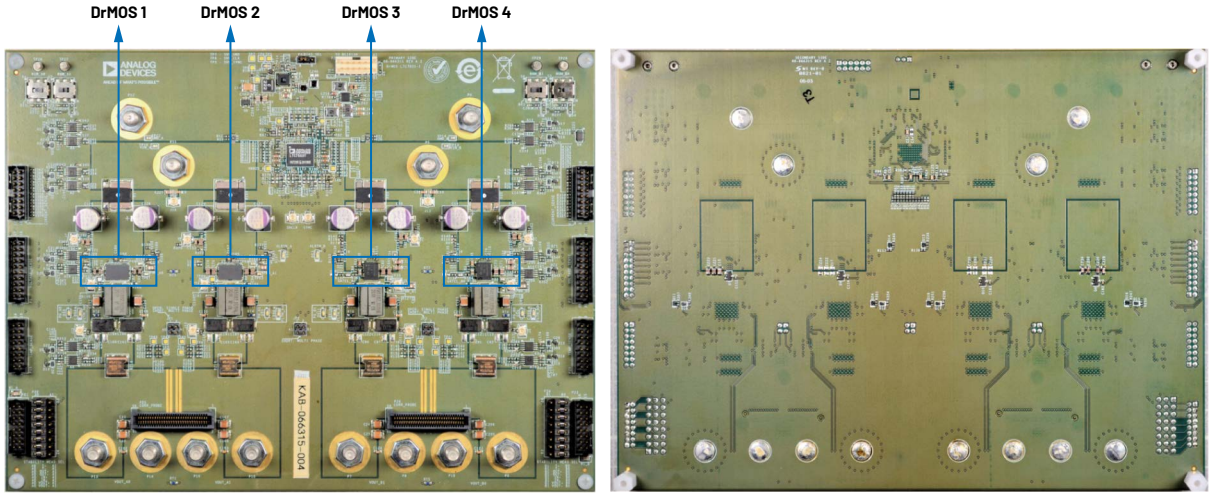

Figure 3. DrMOS evaluation board, top and bottom. PCB dimensions: 203 mm × 152 mm × 1.67 mm (L × H × W) with 2 ounces of copper thickness.

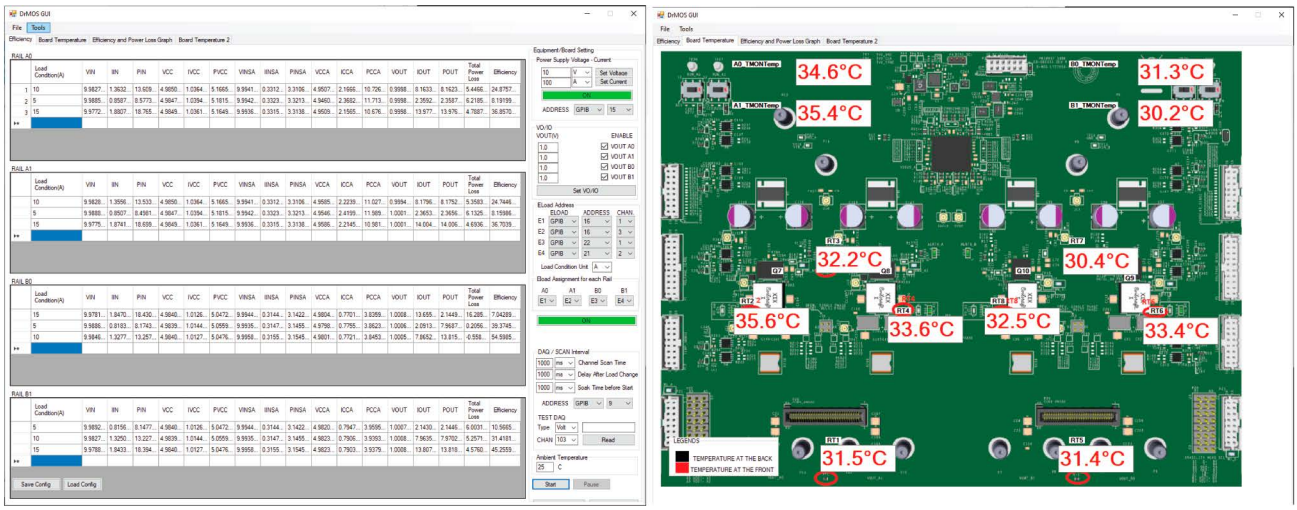

Figure 4. DrMOS evaluation software, showing the configuration and thermal analysis tab.

DrMOS Analysis Testing Methodology and Software

Aside from the demonstration board itself, test setup and testing methodology are equally important for unbiased data and results. For this purpose, the team also created a complementary evaluation software with a graphical user interface (GUI) shown in Figure 4 for a more user-friendly approach of testing and data gathering. The user just needs to specify input and output parameters and the software will take care of the automated testing. The software automatically controls the corresponding test and measurement equipment such as the DC supply, electronic load, and multiplexed data acquisition device (DAQ) to measure temperature, current, and voltage figures directly from the demo board, and then plot those measurements on the GUI. Important telemetry data from on-board devices are also gathered by the software through PMBus/I²C protocol. All this information is important in comparing system efficiency and power losses.

Data and Results

The following test results cover the steady-state performance measurements, functional performance waveforms, thermal measurement, and output noise measurement. The demonstration board was tested with the following configurations:

- Input voltage: 12 V
- Output voltage: 1 V
- Output load: 0 A to 60 A
- Switching frequency: 500 kHz and 1 MHz

Performance Data

Efficiency and Power Loss

The test result in Figure 5 shows that, at a switching frequency of 500 kHz, the LTC7051 managed to have higher efficiency (0.70% better) compared to its competitor. With a further increase in switching frequency from 500 kHz to 1 MHz, the LTC7051 also provided better efficiency (0.95% greater).

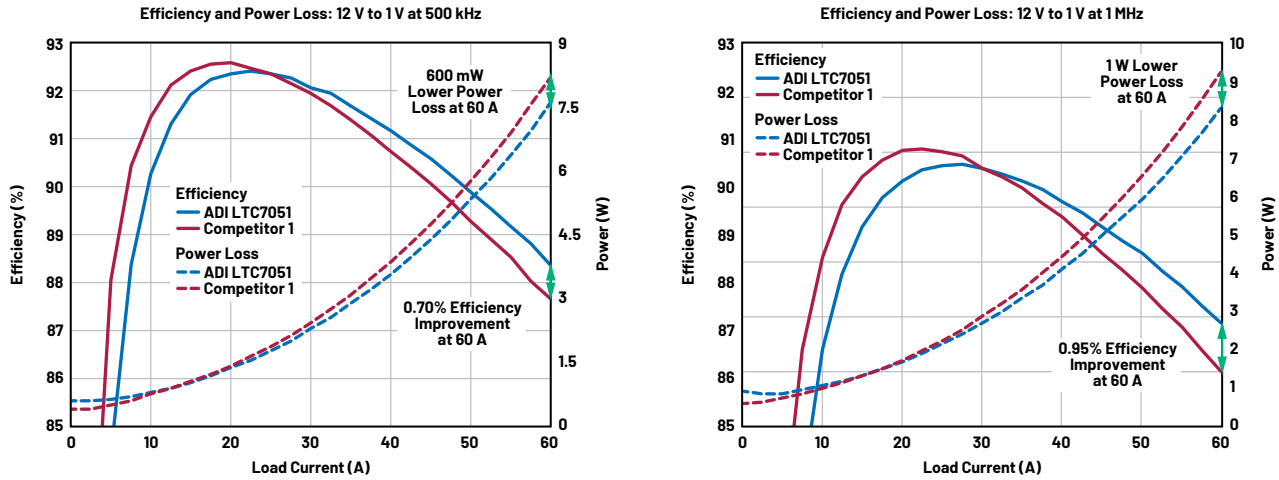

Figure 5. Efficiency and power loss at 1 V from 0 A to 60 A load with 500 kHz and 1 MHz switching frequency, respectively.

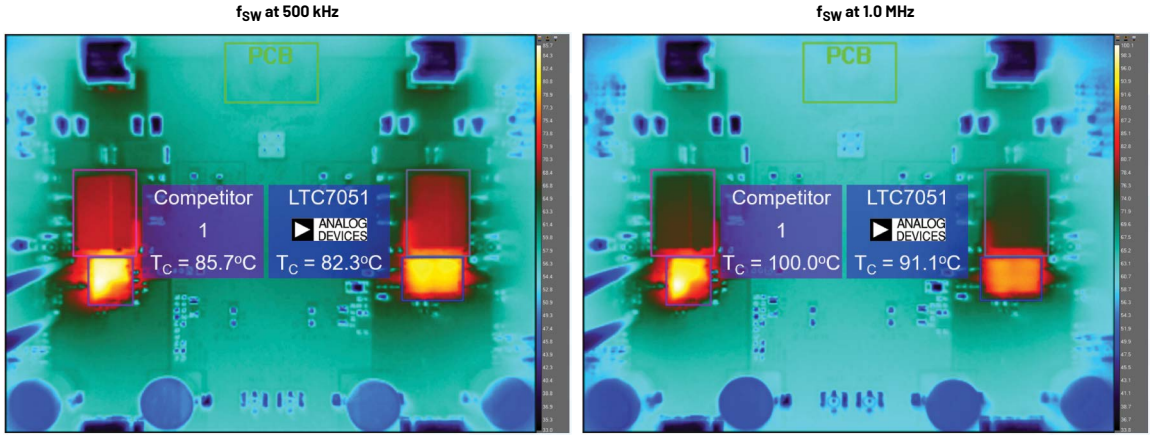

Figure 6. Thermal performance at 1 V output, 60 A load with 500 kHz and 1.0 MHz switching frequency, respectively.

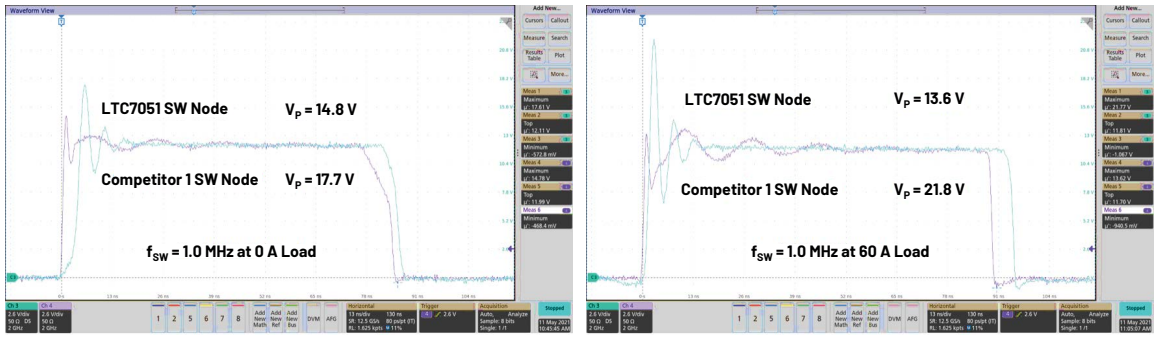

Figure 7. Switch node waveforms at 1 V evaluated at 0 A and 60 A load, respectively.

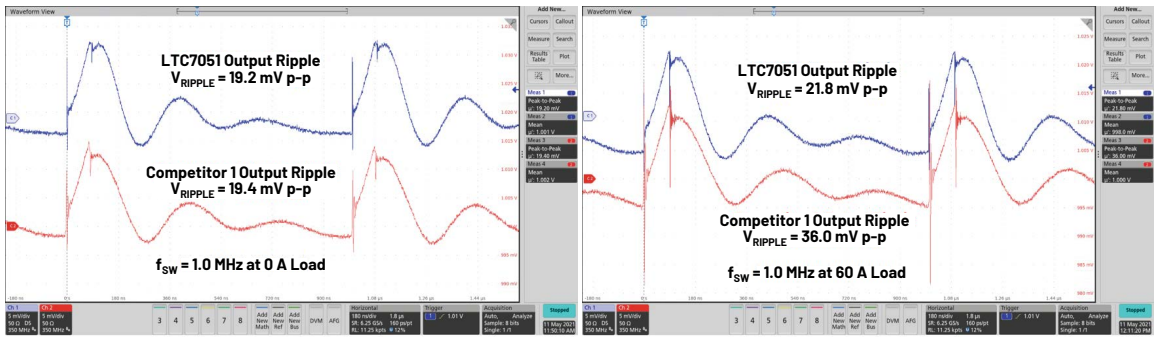

Figure 8. Output ripple waveforms at 1 V evaluated at 0 A and 60 A load, respectively.

Efficiency Performance

Noteworthy here is the higher efficiency performance of the LTC7051 over the competitor at high output load current and at elevated switching frequency. This is the benefit of ADI's patented Silent Switcher technology where improvements in both switching edge rate and shorter dead-times reduce total power losses. This enables higher switching frequency operation for a smaller solution size without a significant impact in overall efficiency. With lower total power loss comes lower temperature operation for higher current outputs, thereby significantly increasing power density.

Thermal Performance

Advantages in efficiency and power losses brought about by LTC7051 also translate to its better thermal performance. A temperature difference of approximately 3°C to 10°C was observed between the LTC7051 and the competitor offering, with the former being cooler as shown in Figure 6. That better performance of LTC7051 is due to its well-designed, thermally enhanced package.

With increased ambient temperature from 25°C to 80°C, the temperature difference observed between LTC7051 and its competitor widened to approximately 15°C, with the former again being cooler.

Device Switch Node Performance

It can be observed from Figure 7 that the LTC7051 drain-to-source voltage (V_{DS}) peak is less than that of the competitor's device. Also, with the load increased to 60 A, V_{DS} measured on the competitor's part is at its peak while prolonged oscillation can be seen. The LTC7051, on the other hand, managed to have a smaller spike and reduced oscillation, again due to the Silent Switcher 2 architecture and integrated bootstrap capacitor inside of LTC705x DrMOS family. This will translate to lower overshoot on the switch node, meaning reduced EMI, as well as radiated and conducted noise, and higher reliability as switch-node overvoltage stresses are reduced.

Device Output Ripple Performance

Another parameter is the output voltage ripple shown in Figure 8. It can be seen that the noise exhibited by LTC7051 is less compared to that of the competitor's part. Reduced noise is due to the lower V_{DS} spike and minimal oscillation on the switching node, which are the result of Silent Switcher technology. If switch-node spikes are not generated, then there is no conducted noise to the output.

Likewise, the LTC7051 and the competitor device were also subjected to output noise spread spectrum measurements as shown in Figure 9. LTC7051 outperformed the other DrMOS device, and showed that the noise generated at the switching frequency is lower compared to that of the competitor's part. The noise difference was approximately 1 mV rms.

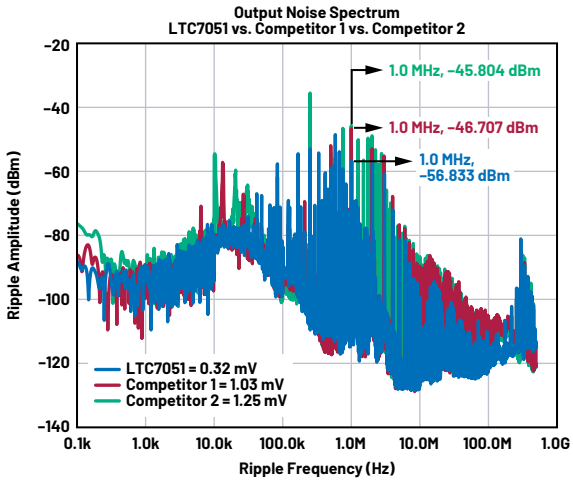

Figure 9. Output noise spectrum response at 1 V having 60 A load running at 1 MHz switching frequency.

Conclusion

The LTC7051 DrMOS demonstration platform can be used to provide an unbiased comparison between competitive product offerings. Operating in high switching frequency, the LTC7051 significantly boosts power conversion efficiency and thermal performance by integrating SilentMOS™ architecture and bootstrap capacitor into a single, thermally enhanced package. Also, the LTC7051 can reduce ringing and spike energy, which shows not only on the switch node but also propagates to the output. In actual applications, output load requires tight tolerance, and part of this is nominal DC. However, the noise contributed by high spike energy and ripple, which also shows at the output, consumes the overall budget. Power-hungry data centers will save substantial energy and cost, not to mention the added benefits of less thermal management and EMI that would be reduced significantly or eventually be eliminated, while still properly observing filter design and component placement. With all that being said, LTC7051 should be your go-to power stage and the must-have DrMOS device for your VRM design and application needs.

About the Author

Gary Sapia began working for Linear Technology (now part of Analog Devices) nearly 23 years ago. Before that he was an analog design engineer for Ashtech, which later became Magellan/Orbital Sciences. Back in the early days of GPS, Gary designed GPS RF analog front-end solutions. He also designed and troubleshot analog circuits for power supplies, as well as LNAs, complete analog front ends, op amp and comparator solutions, miscellaneous data converter solutions, and the resulting product test systems. His job also included writing the software to run these test systems. After joining Linear Technology, Gary came aboard as an FAE assigned to Bay Area companies and had the pleasure of working with multiple engineers on several different analog system designs. After four decades of experience working with people and hardware, Gary is now the team leader for ADI's New Technologies and Market Expansion Team and is eager to help continue ADI's path toward profitable future growth.

About the Author

Long before Kareem Atout decided to pursue a career in the tech world, he tinkered with electronics, built his own stereo equipment, and generally kept his parents constantly worried about the next Kareem-induced power outage! Kareem parlayed his love for creative electronic discovery into his successful 25-year career in electrical engineering. As a senior systems engineer for communications infrastructure, he is learned in the areas of both analog and digital design. He continues to break barriers that invigorate the semiconductor industry by applying his upbeat brand of professionalism and inspired designs to wired communications and power systems.

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Marvin Neil Solis Cabueñas graduated with a bachelor's degree in electronics engineering from De La Salle University in Manila, Philippines. Before joining ADI in 2021, Marvin worked as a systems engineer for Azeus Systems Philippines, Inc., then worked as a network engineer for Technistock, Philippines, Inc. from 2014 to 2017 and as a research and development engineer for Nokia Technology Center Philippines from 2017 to 2020. He has more than nine years of work experience in different fields such as embedded systems programming, digital signal processing, simulation modeling, and others. He currently works as a senior firmware engineer working on various projects for the Power Business Unit of ADI. He is currently working toward his master's degree in electrical engineering at the University of the Philippines.

How Digitally Tunable Filters Enable Wideband Receiver Applications

Brad Hall, Systems Applications Engineering Manager, and
David Mailloux, Product Applications Engineer

Abstract

In today's multichannel, wideband multioctave tuning RF receivers, it is often necessary to eliminate unwanted blockers to preserve the fidelity of signals of interest. Filters have played an essential role in reducing these unwanted signals, particularly in the receiver RF front end and local oscillator (LO) portions of these systems. This article will explore filters within RF signal chains, discuss the concept of blocker signals, review traditional filtering technologies, and conclude with the latest product solutions for optimizing signal chain performance.

Introduction

With the goal to continuously reduce size, weight, power, and cost, while increasing or maintaining performance, it has become necessary for RF system designers to evaluate each component in the signal chain and look for opportunities to innovate. As filters have traditionally consumed large amounts of area, they are an obvious area to explore size reduction.

At the same time, receiver architectures are evolving with the ability for analog-to-digital converters (ADCs) to sample at higher input frequencies. With a higher ADC input frequency, the constraints placed on filters in the signal chain have changed. In general, this trend means a relaxation of rejection requirements for filters, which opens them up to further size and tunability optimization.

To start this exploration, a general overview of RF signal chains and definitions can assist in explaining where and why filters are needed. Further, a review of traditional technologies can give insight into the status quo. Then, by comparing these traditional technologies vs. the latest product solutions, it becomes clear how system designers can easily achieve their goals.

RF Signal Chain Overview

A typical wideband signal chain covering 2 GHz to 18 GHz is shown in Figure 1. The basic theory of operation of this signal chain is the following. The antenna receives a broad spectrum of frequencies. There is a series of amplification, filtering, and attenuation control (the RF front end) before the frequencies are converted to an IF signal that the ADC can digitize. The filtering functions in this block diagram can be divided into four main categories:

- Preselector suboctave filtering
- Image/IF signal rejection
- LO harmonics
- Antialiasing

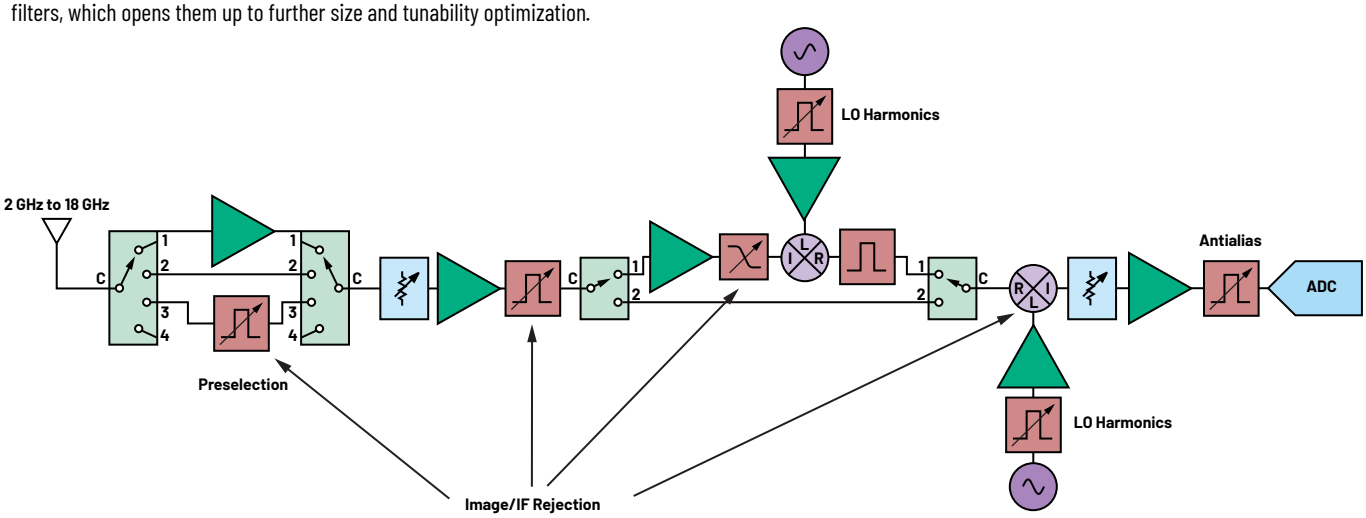


Figure 1. 2 GHz to 18 GHz receiver block diagram.

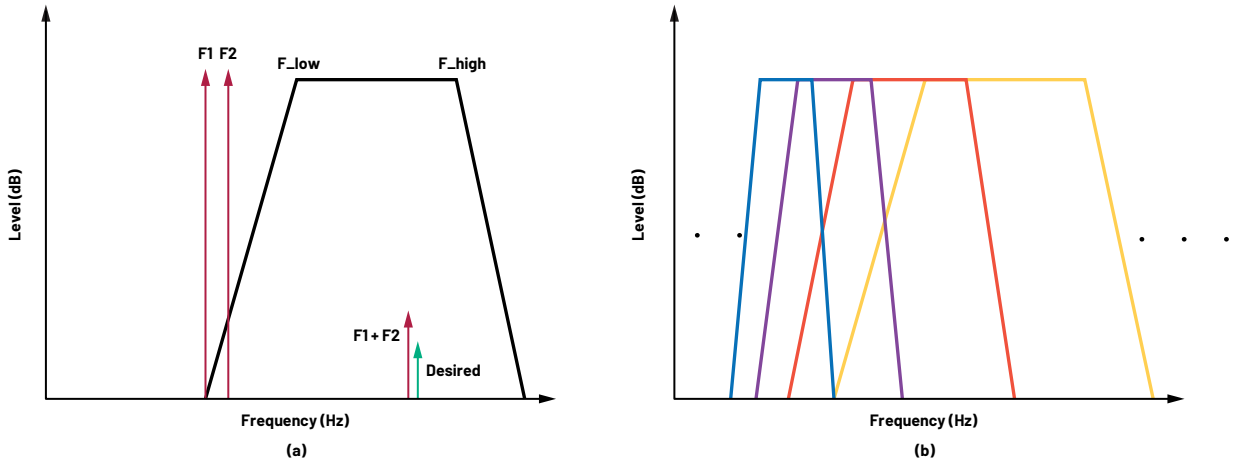


Figure 2. (a) Suboctave preselection mitigates IMD2 issues; (b) filter bands become wider as frequency increases.

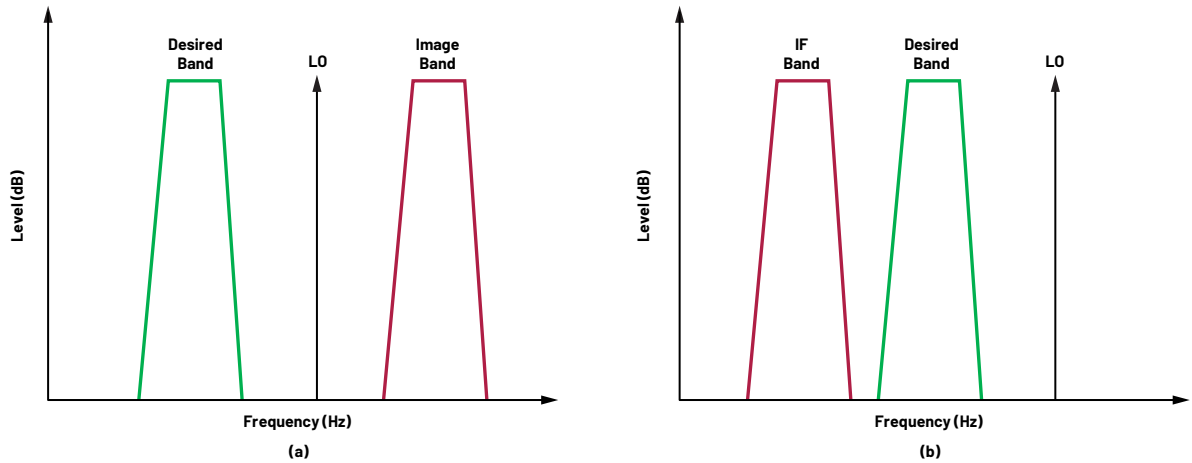


Figure 3. (a) An image band and (b) an IF band must be rejected before the mixer.

The preselector suboctave filtering needs to be near the beginning of the signal chain and is used to address second-order intermodulation distortion (IMD2) spurs that can show up in the presence of interferer signals (also known as blockers). This occurs when two out-of-band (OOB) spurs add or subtract and create a spur that falls in band, potentially masking a desired signal. A suboctave filter removes these interfering signals before they can hit a nonlinear component in the signal chain (such as an amplifier or mixer). Often, the absolute bandwidth requirement for the suboctave filter becomes narrower as the center frequency reduces. For example, the first band in a 2 GHz to 18 GHz signal chain may only cover 2 GHz to 3 GHz and would need good rejection at 1.5 GHz on the low-side (F_high/2) and at 4 GHz on the high-side (F_low × 2), whereas the highest band in the signal chain may cover 12 GHz to 18 GHz, with good rejection at 9 GHz on the low-side and at 24 GHz on the high-side. These differences mean many more filters are needed to cover lower frequencies bands than high frequency bands. A frequency spectrum example of the preselector filtering is shown in Figure 2.

The image/IF rejection filtering is typically further down the signal chain, between the LNA and the mixer. It is used to reject the image frequencies and unwanted IF frequencies. The image is a frequency band that, when present at the mixer input, will generate signals equal in amplitude to the desired signals at the mixer output. Image mitigation can be achieved from several components in the signal chain, such as preselector filters, dedicated image reject filters, and image rejection from single-sideband (SSB) mixers. IF signal rejection is required to knock down spectrum at IF frequencies before the mixer to avoid them from leaking directly across the mixer and showing up as unwanted spurs. A frequency spectrum example of the unwanted image and IF bands is shown in Figure 3.

Depending on the circuitry used to generate the LO, filtering requirements may vary at this point in the signal chain. The desired signal feeding the LO port of the mixer is a clean sine wave or a square wave. Often, the LO circuitry creates subharmonics and harmonics of the desired LO signal. These unwanted signals (see Figure 4) need to be rejected before they reach the mixer to avoid generating unwanted MxN spur products. If the LO signal is at a single frequency, then a fixed band-pass filter is sufficient and can be optimized to pass only the desired signal. In wideband signal chains, a tunable LO signal is usually implemented and therefore requires either a set of switched filters or a tunable filter.

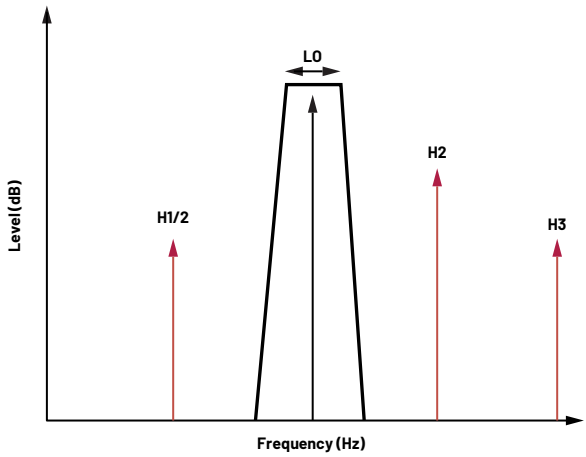


Figure 4. LO harmonic filtering.

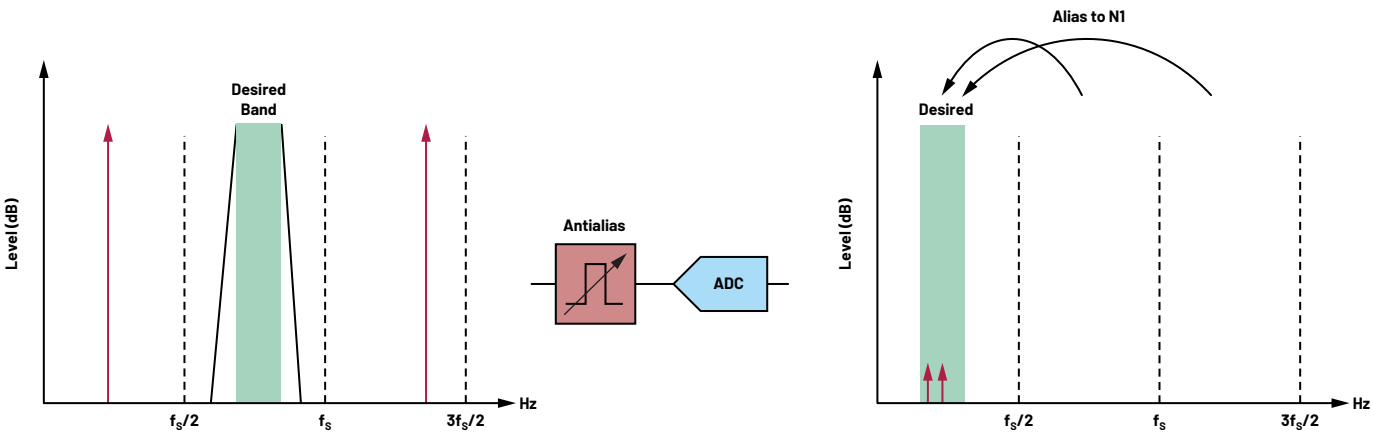


Figure 5. Aliasing in the ADC can cause interfering signals to show up in a band if there is insufficient rejection.

When sampling with an ADC, the system designer needs to select which Nyquist zone to digitize. The first Nyquist zone ranges from DC to $f_S/2$ (where f_S is the sample rate of the ADC). The second Nyquist zone is from $f_S/2$ to f_S and so forth. Antialiasing filters are used to reject interferer signals in Nyquist zones adjacent to the desired Nyquist zone. Interferers at this location in the signal chain can come from various sources, such as the MxN spurs generated in the mixer, the downconverted signals adjacent to the desired signals, or from harmonics generated in the IF signal chain. Any unwanted signals that are input to the ADC will alias into the first Nyquist zone when performing digitization. A frequency spectrum example of the unwanted aliasing signals is shown in Figure 5.

Blocker Signals

In RF communications systems, a blocker is a received and unwanted input signal that degrades the gain and signal-to-noise-and-distortion (SINAD) ratio of the desired signals of interest. A blocker can be a signal that masks the desired signal directly or creates spurious products that mask the desired signal. These unwanted signals could be the result of unintentional or intentional interference. In the former case, it comes from another RF communications system operating in the adjacent frequency spectrum. In the latter case, it comes from nefarious electronic warfare (EW) systems designed to intentionally disrupt RF communication or radar systems. A frequency spectrum example of a blocker signal and a desired signal is shown in Figure 6.

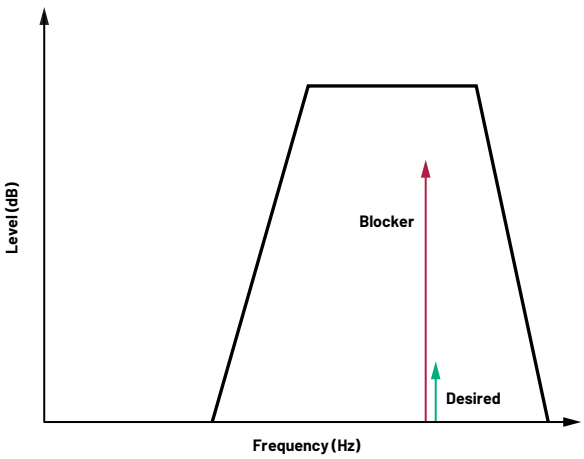


Figure 6. Desired and blocker signals.

Many RF components exhibit weakly nonlinear memoryless behavior. This means they can be approximated by a low order polynomial. For example, a wideband frequency amplifier could be modeled by the odd-order polynomial that includes only the first-order and third-order terms:

$$y(t) \approx \alpha_1 x(t) + \alpha_3 x^3(t) \quad (1)$$

When there are two incident signals present at the input of the amplifier, within the operating frequency range, as might be the case with a desired signal, ω_1, and a blocker signal, ω_2, the input signal can be described as:

$$x(t) = A\cos(\omega_1 t) + B\cos(\omega_2 t) \quad (2)$$

Substituting the input equation into the odd-order polynomial results in an output of:

$$y(t) \approx \left(\alpha_1 + \frac{3}{4}\alpha_3 A^2 + \frac{3}{2}\alpha_3 B^2\right) A\cos(\omega_1 t) + \ldots \quad (3)$$

When the amplitude of the desired signal is much less than the blocker signal, A << B, then the polynomial in Equation 3 further reduces to:

$$y(t) \approx \left(\alpha_1 + \frac{3}{2}\alpha_3 B^2\right) A\cos(\omega_1 t) + \ldots \quad (4)$$

Given the simplification in Equation 4, the desired signal amplitude is now a strong function of the blocker signal amplitude, B. Since most RF components of interest are compressive, the alpha coefficients must be of opposite sign,[1] such that $\alpha_1\alpha_3 < 0$. The result of the two statements mentioned previously is consequential, in that the gain of the desired signal goes to zero for large blocker signal amplitudes.

Filter Definitions

To solve the problem of unwanted signals in RF communications systems, engineers have relied upon filters to reduce these signals and preserve the desired signals of interest. In simple terms, a filter is a component that allows the transmission of frequencies within a pass band and rejection of frequencies in a band-stop.[2]

Usually, the insertion loss (dB) of a filter can be described as either low-pass, high-pass, band-pass, or band-stop (notch). This nomenclature refers to the allowable pass-band frequency response plotted vs. increasing frequency. Filters can further be categorized by their frequency response shape, such as pass-band ripple, stop-band ripple, and how fast they roll-off vs. frequency. For illustrative purposes, Figure 7 shows the four primary filter types.

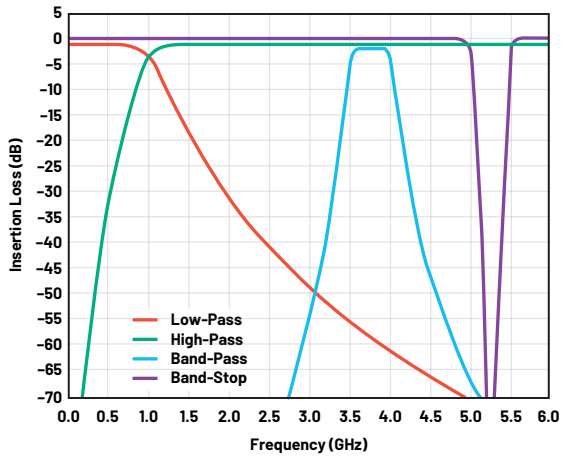


Figure 7. Filter shapes by type.

Besides insertion loss, another important characteristic of filters is group delay, which is defined as the rate of change of transmission phase with respect to frequency. The units of group delay are time (seconds), and therefore this metric can be thought of as the transit time for a particular signal through the filter. The transit time by itself for a single frequency is typically of little consequence, but when a wideband modulated signal passes through a filter, the flatness of the group delay becomes important because it can distort the signal by introducing different time delays in the received signal. The equation for the group delay is given in Equation 5 where θ is the phase and f is the frequency:

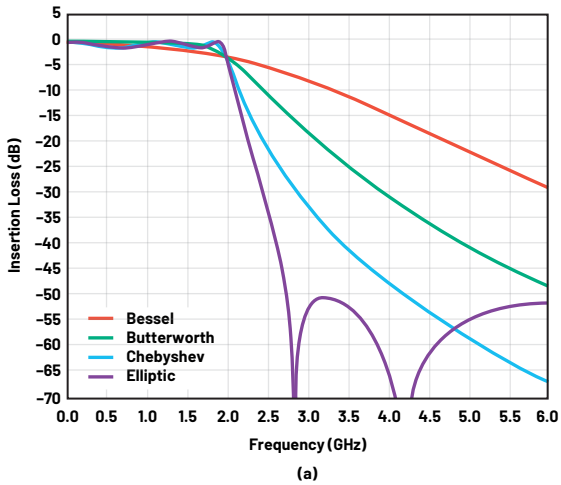
$$Group\ Delay\ (s) = gd = -\frac{d\theta}{df} \times \frac{1}{360} \quad (5)$$

Classical filter types with distinct insertion loss and group delay characteristics are Butterworth, Chebyshev, elliptic, and Bessel. Each one is usually defined by an order number that describes how many reactive elements are in the filter. The higher the order number, the faster the frequency roll-off.

When considering similarly ordered filters, the Butterworth style offers a maximally flat pass-band response at the expense of frequency roll-off, whereas a Chebyshev filter has good frequency roll-off with some pass-band ripple. An elliptic filter (sometimes called the Cauer-Chebyshev) has more frequency roll-off than a Chebyshev filter, but consequently ripple in both the pass band and the stop band. The Bessel filter has maximally flat frequency and group delay responses, although with the worst frequency roll-off performance. For illustrative purposes, Figure 8 shows the ideal insertion loss and group delay for a fifth-order low-pass filter with a 3 dB frequency ($f_{3\ dB}$) of 2 GHz, allowable pass-band ripple of 1 dB, and stop-band ripple of 50 dB.

For systems where maintaining constant phase across frequency is important, such as radar systems, the group delay flatness across the band of interest is critical to avoid unexpected phase deviations on the pulse being received. Given that received signals can span 1 GHz or more, the group delay flatness across a wide bandwidth should be minimized. A rule of thumb is to keep the group delay flatness to <1 ns but this will depend on the system's tolerance for the phase deviation. The plots in Figure 9 show an example of a filter with a group delay flatness of 2.24 ns and 0.8 ns, respectively. Observation of the plots shows a much more consistent phase change across frequency for a flatter group delay.

Lastly, the quality factor (Q factor) of reactive elements used to design filters is an important attribute that can impact performance. The quality factor is defined as the ratio of reactive impedance to the series loss resistance for a particular circuit element. It is a function of the technology process and the physical area used for implementation. Higher quality factors allow for sharper frequency responses and less insertion loss.



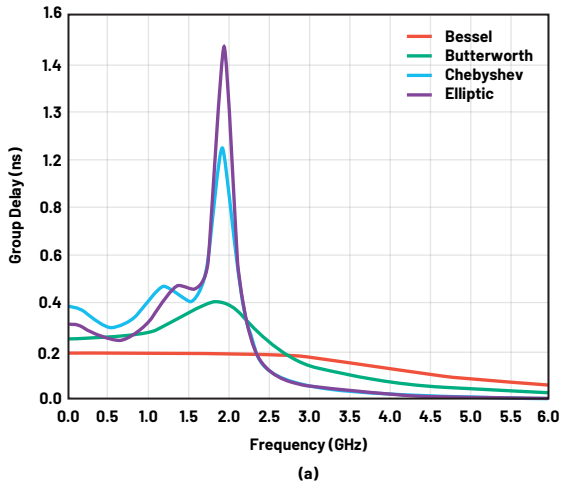


Figure 8. Insertion loss and group delay for fifth-order low-pass filters.

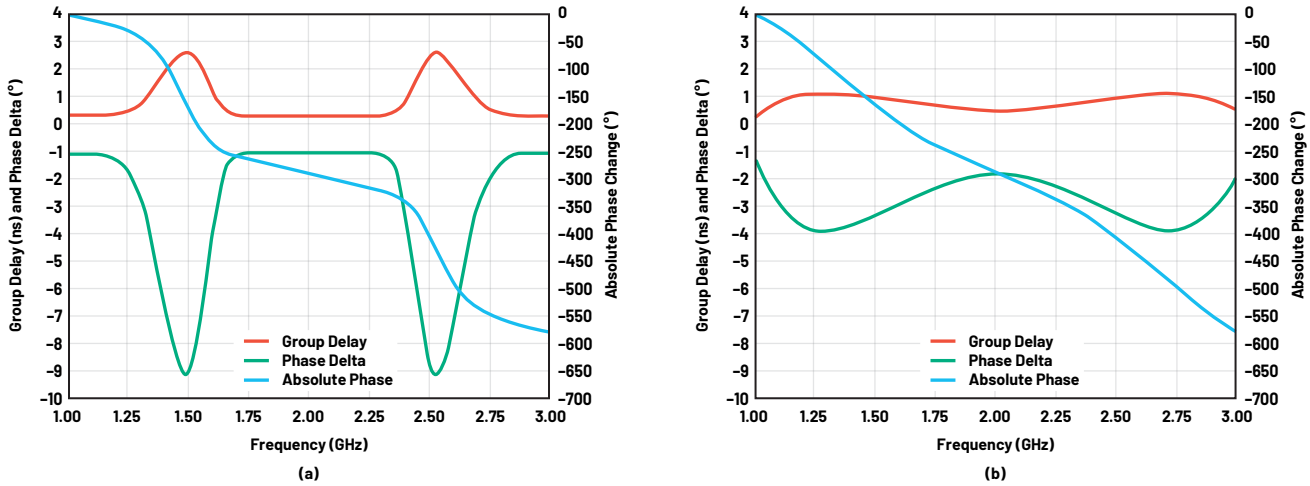


Figure 9. The group delay flatness affects the deviation from the linear phase: (a) showing 2.24 ns group delay flatness vs. (b) showing 0.8 ns flatness resulting in more consistent phase change vs. frequency.

Traditional Filter Technologies for RF Communications

When designing a filter for RF communications systems, there are a variety of technologies available to implement the classical filter types. Traditionally, RF engineers relied upon discrete lumped element implementations with surface-mount components or distributed element filters containing transmission lines printed on PCB materials. However, in recent years, filters have been designed on semiconductor processes that allow for precise temperature stable reactive components with improved quality factors. Additionally, the semiconductor processes allow for switched and tunable reactive elements that can be more challenging to implement in the discrete lumped element implementations. There are other technologies as well, such as the bulk acoustic wave (BAW), surface acoustic wave (SAW), low temperature cofired ceramic (LTCC), cavity filters, or ceramic resonators.

Trade-offs exist with each approach and technology:

Lumped LC filters are implemented with surface-mount inductors and capacitors on a PCB. The benefit is the ease of assembling and then changing the performance of the filter by swapping out values.

Distributed filters are designed as resonant pieces of a transmission line implemented on a dielectric (either integrated into the PCB or standalone on a separate dielectric) and are oriented to behave as quasi-inductors or quasi-capacitors in some frequency range. They exhibit periodic characteristics. In some cases, lumped components are added to improve/miniaturize the distributed filter.

Ceramic resonator filters use multiple ceramic resonators (which are a distributed element) that are coupled via lumped elements. The coupling element is typically a capacitor but sometimes inductors are also used. This type of filter is a hybrid of distributed and lumped elements.

Cavity filters are implemented with distributed elements (rods) enclosed within a conducting box. They are known for being able to handle high amounts of power with little loss but at the expense of size and cost.

BAW and SAW technologies can provide excellent performance but they tend to be frequency selective and not suitable for wideband applications.

LTCC filters are implemented by combining many layers of distributed transmission lines within a ceramic package, which is similar to a distributed filter and can serve a number of applications but are fixed. Since they are 3D stacked, they end up taking little space on the PCB.

Lastly, filters integrated into semiconductors support a wide frequency range with recent advances in semiconductor performance. The ability to easily integrate digital control elements into these components aids in the adoption into software-defined transceivers. In general, the trade-off between performance and integration provides a compelling value to designers of wideband systems.

Table 1. Filter Type Comparison

	Frequency Range	Tunability	Size	Cost	Q-factor
Lumped LC	<6 GHz	Difficult to implement	Medium	$	Medium
Distributed	<50 GHz	Fixed	Medium	$$	Medium/high
Ceramic Resonator	<6 GHz	Fixed	Large	$$	High
Cavity	<40 GHz	Fixed	Large	$$$	High
SAW/BAW	<6 GHz	Fixed	Small	$	High
LTCC	<40 GHz	Fixed	Small	$	Medium
Semiconductor	<50 GHz	Digital tuning integrated	Small	$$	Medium

Latest Filter Solutions

Analog Devices has developed a new family of digitally tunable filter products that utilize an enhanced semiconductor process along with industry friendly packaging techniques. This technology results in small, high rejection filters that alleviate the blocker issues that arise in a receiver. These filters are designed to be highly configurable by standard serial to parallel interface (SPI) communication, with fast RF switching speeds. Additionally, ADI has incorporated a 128-state lookup table within each chip to allow for quickly changing filter states for fast frequency hopping applications. The combination of fast tuning with high rejection and wide frequency coverage enables the next generation of receiver applications operating in adverse spectral environments.

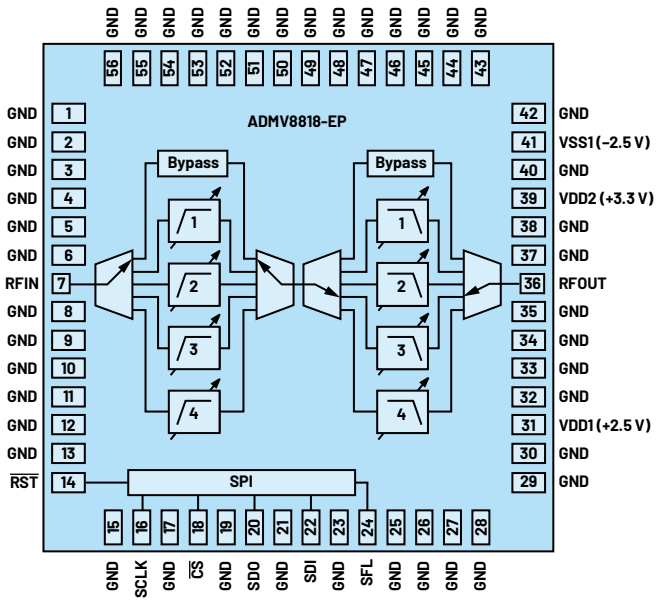


Figure 10. ADMV8818 functional block diagram.

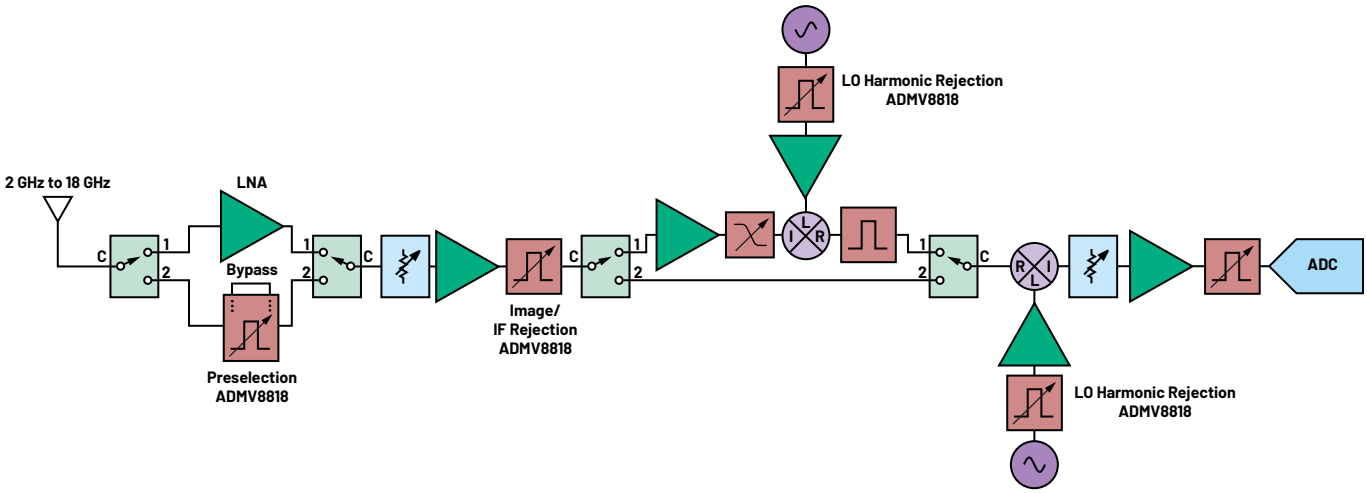


Figure 11. A block diagram of a 2 GHz to 18 GHz receiver using ADMV8818 as a preselector and image filter.

The latest products to be introduced using this technology are the ADMV8818, which has four high-pass and four low-pass filters operating from 2 GHz to 18 GHz, and the ADMV8913, which has a high-pass filter and low-pass filter operating in the 8 GHz to 12 GHz frequency range.

The ADMV8818 is a highly flexible filter in a 9 mm × 9 mm package that can achieve tunable band-pass, high-pass, low-pass, or bypass response between 2 GHz and 18 GHz. The chip consists of two sections: the input section and the output section. The input section has four high-pass filters and an optional bypass that is selectable by the two RF_{IN} switches. Similarly, the output section has four low-pass filters and an optional bypass that is selectable by the two RF_{OUT} switches. Each of the high-pass and low-pass filters are tunable with 16 states (4 bits of control) to adjust the 3 dB frequency ($f_{3\,dB}$). Figure 10 shows a functional block diagram of the ADMV8818.

Thanks to its rapidly reconfigurable flexible architecture and small form factor, the ADMV8818 provides full coverage over the 2 GHz to 18 GHz band without any dead zones. The ADMV8818 can be configured as a suboctave preselector filter, image, or IF filter. When configured in a signal chain as shown in Figure 11, the receiver can maintain high sensitivity with the ability to switch to the ADMV8818 as a preselector in the presence of a larger OOB signal.

For example, if a signal of interest is being received near 9 GHz but a strong OOB blocker is present at 4.5 GHz, then that blocker signal can cause harmonics to show up near the desired 9 GHz signal, preventing operation. Configuring the ADMV8818 as a 6 GHz to 9 GHz band-pass filter would allow for a wideband signal to pass through while properly knocking down the level of the blocker before it can cause harmonic issues to crop up in the nonlinear elements of the signal chain. An S-parameter sweep of the ADMV8818 configured for this case is overlaid with blockers and shown in Figure 12.

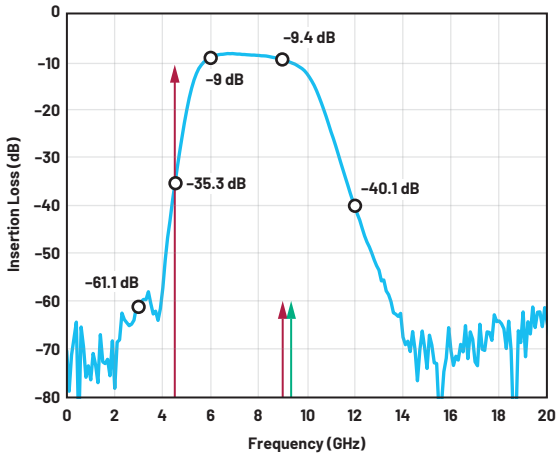


Figure 12. ADMV8818 configured as a 6 GHz to 9 GHz band-pass filter. The filter rejects F2 – F1, F1 + F2, F/2, and F × 2 spur products.

A size comparison of a typical 2 GHz to 18 GHz preselector block is shown in Figure 13. In this comparison, the switched fixed filter preselector bank is implemented with distributed filter technology on a ceramic substrate. The size is estimated based on commercially available filter technology. Eight-throw switches are included in the estimate to compare equivalent functionality. The tunable BPF shown is the ADMV8818 that covers the same frequency range and offers full tuning flexibility over the switched filter bank. The area savings of the ADMV8818 vs. a switched filter bank is greater than 75%. The preselector functionality in a receiver signal chain typically takes up a sizeable portion of the overall size of the system, so this area savings are critical in size limited EW systems that have the flexibility to trade off size with performance.

The ADMV8913 is a combination of high-pass and low-pass filters in a 6 mm × 3 mm package, and it is specifically designed for operation in the 8 GHz to 12 GHz frequency range (X band) with low insertion loss of 5 dB. The high-pass and low-pass filters are tunable with 16 states (4 bits of control) to adjust the 3 dB frequency ($f_{3\,dB}$). Additionally, the ADMV8913 incorporates a parallel logic interface that allows for setting the filter states without the need for SPI communication. This parallel logic interface can be quite useful for systems that require fast filter response times because it eliminates time needed for the SPI transaction. A functional block diagram of the ADMV8913 is shown in Figure 14.

Modern X band radar systems, whether they employ mechanically steered antennas or high channel count phase array beams, often rely upon filtering solutions that are compact in size, have low insertion loss, and are easily configurable. The ADMV8913 is ideally suited for this application thanks to its low insertion loss, small form factor, and flexible digital interface options (either SPI or parallel control). These features allow it to be placed close to the front of these systems to ensure optimum performance, while reducing integration complexity.

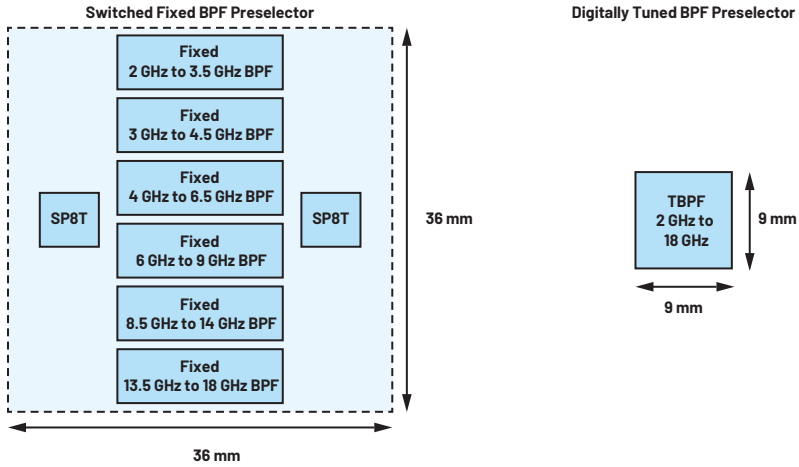


Figure 13. Fixed switched 2 GHz to 18 GHz BPF (left) vs. digitally tunable 2 GHz to 18 GHz BPF (right). The area savings are greater than 75%.

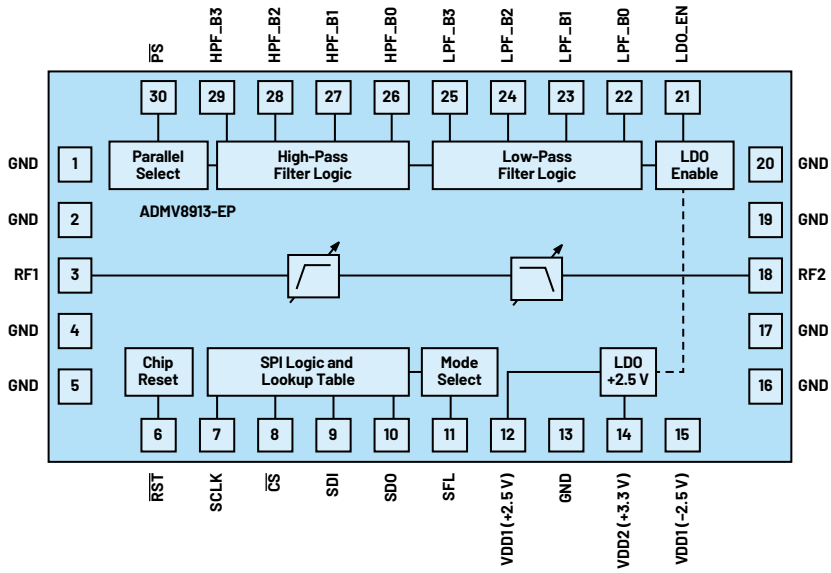


Figure 14. ADMV8913 functional block diagram.

Conclusion

The design considerations for an RF front end for a wideband receiver are numerous. The front end must be designed to handle difficult blocker scenarios, which are unpredictable, while also detecting low level signals. Being able to dynamically adjust the front-end filtering performance to handle these blocker signals is a critical feature for RF front ends. The new digitally controlled tunable filter IC product offerings from ADI provide industry-leading performance with enhanced digital functionalities addressing many front-end applications. These two new products are just the first of many exciting new developments in the digitally tunable filter portfolio. For customers interested in learning more about these product offerings, please visit the Digital Tunable Filters product page to see the latest data sheets or reach out your local representative to discuss a particular end application.

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From 2010 to 2015, his experience includes working for Hittite Microwave and Symmetricom (now Microchip Technology). He has experience designing oscillators both at the semiconductor and the module level, and his theoretical background is complimented by adept laboratory practices.

In 2015, he joined ADI as a product applications engineer supporting highly integrated up/downconverters and tunable filter products. Additionally, his technical support areas have included voltage controlled oscillators, phase-locked loops, frequency dividers, and frequency multipliers.

Automotive LED Driver Power Conversion Topology Guide

Joshua Caldwell, Design Director

Introduction

In many systems—including the myriad of regulators deployed in automotive power delivery systems—the design of power conversion regulators is often a difficult and complex task. This article aims to simplify the selection process by explaining the benefits, trade-offs, and applications for different switching topologies used for LED drivers.

LEDs are unlike traditional electrical light producing filament or gas components. Utilizing specific semiconductor junctions, LED manufacturers can produce specific colors of light spanning the entire visible range—as well as IR and UV. In automotive applications, LEDs can increase the safety in both daylight and nighttime driving scenarios. Increased efficiency can extend battery life in electric vehicles, and multiple LEDs in a single system can eliminate single-component failures.

Due to their versatility, LEDs offer the capability of being driven in many different ways. Since the output from LEDs is well-controlled light, LED loads are unlike traditional loads to a power system. LEDs only rely upon accurately regulated current, through the semiconductor junction, to produce light, where the relative voltages at the terminals to the system ground (or chassis in an automotive system) are unrelated. As a result, LED systems can take advantage of the different topologies offered by switching technologies.

How to Select the Correct Switching Topology for Automotive LED Systems

The choice of a particular switching topology in an automotive system is related to the complete system design; considerations should be taken into account for minimum input voltage, maximum string voltage, chassis return capability, shorted output capability, maximum input current, output/LED current, and PWM dimming.

Step-Down (Buck) Converters

Step-down (or buck) LED drivers regulate the current in an LED string from a voltage that is higher than the total LED string voltage. Buck LED drivers can be safely shorted to the system ground, making them both intrinsically safe. They can have the capability of chassis return (one wire for power), and they can easily be adapted to matrix or animation applications. Figure 1 and an example schematic in Figure 2 show basic system diagrams with the controller modulating the high-side switch for current control.

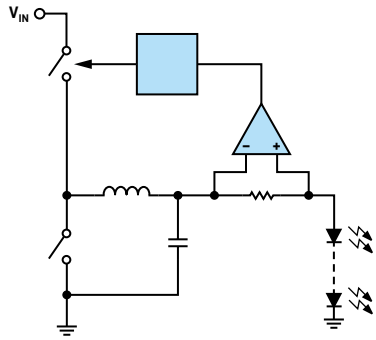

Figure 1. Buck converter.

Several critical features to look for in step-down LED drivers are fixed frequency operation, high efficiency through excellent switching control and low resistance switches, high accuracy throughout the analog dimming range, and, for excellent EMI, a properly designed spread spectrum frequency modulation.

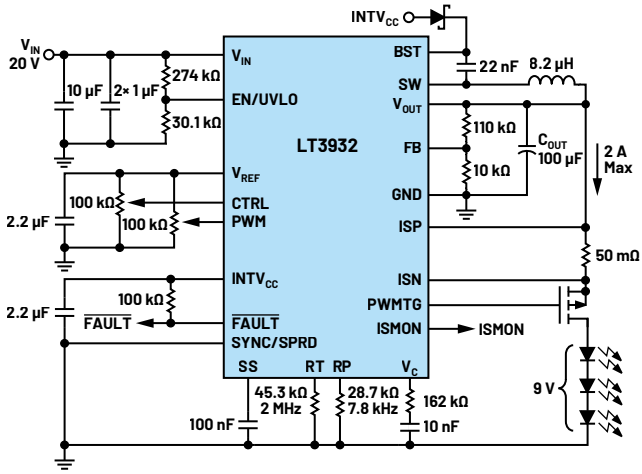

Figure 2. Buck converter example: LT3932.

Table 1. Advantages and Trade-Offs of Using Buck Converters as LED Drivers

Benefits to Buck LED Drivers	Trade-Offs to Step-Down LED Drivers	Applications
Grounded string—chassis return	Input voltage must be higher than LED voltage	High beam/low beam
Matrix switches can shunt entire string	Preboost regulator required in most automotive systems	Turn signals/animation
Higher bandwidth (>1/5 of f_{SW})		Matrix headlamps
Best EMI performance		Short-safe systems
Smallest inductor sizing		

Step-Up (Boost) Converters

Step-up (or boost) LED drivers regulate the current in an LED string from a voltage that is lower than the total LED string voltage. This is useful in many automotive systems, where many LEDs need to conduct in a single string. Typical 12 V automotive systems have operational ranges from 6 V to 18 V—requiring that the LED driver runs down to 6 V, providing large step-up ratios for the LEDs to remain illuminated. Figure 3 and an example schematic in Figure 4 show basic system diagrams with the controller modulating the low-side switch for current control.

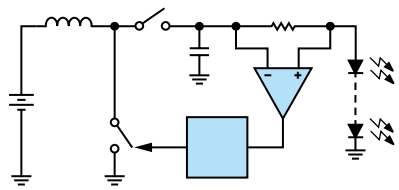

Figure 3. Boost converter.

Table 2. Advantages and Trade-Offs of Using Boost Converters as LED Drivers

Benefits to Boost LED Drivers	Trade-Offs to Step-Up LED Drivers	Applications
Grounded—chassis return	Input voltage must be higher than LED voltage	High beam/low beam
Typically, smallest total solution size	Lower bandwidth (<1/20 of f_{SW})	Heads-up displays
Good EMI performance	Higher inductor current rating	Backlighting
Direct battery to LED conversion	Cannot short output to GND	

Boost-Buck Using a Boost Converter

Some step-up (or boost) LED drivers may be configured to return the LED cathode to the supply. This configuration is referred to as buck-boost. The total output voltage is V_{IN} ($V_{BATTERY}$), which is added to the total LED string voltage. The benefit of this topology is being able to drive an LED string that is higher, lower, or equal to the supply voltage. The limitations of this topology are only bounded by the converter—on the low end by the minimum supply voltage of the controller IC and on the high end by the controller IC's maximum output voltage.

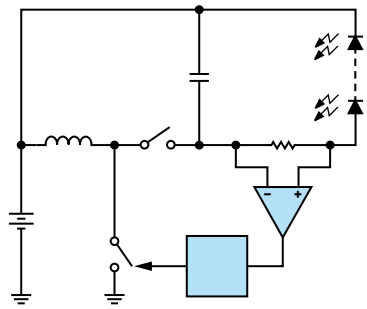

Figure 5. Boost-buck converter.

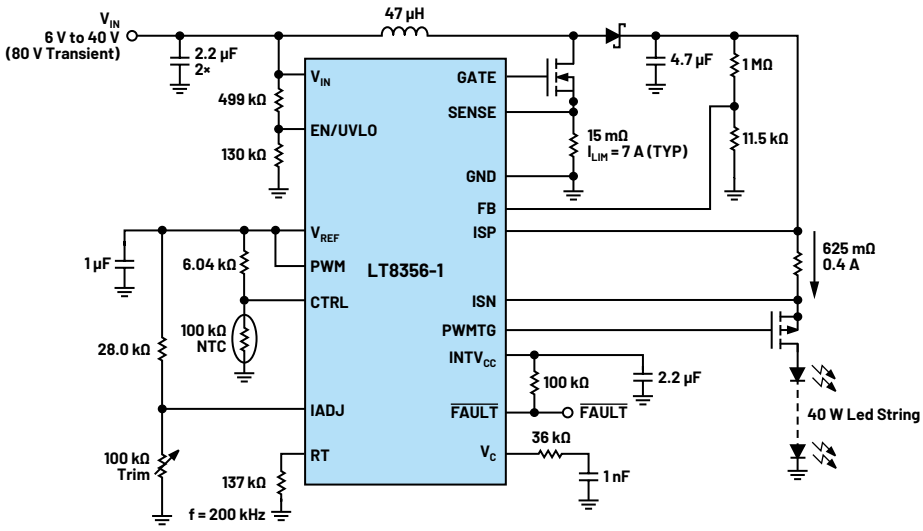

Figure 4. Boost converter example: LT8356-1.

Table 3. Advantages and Trade-Offs of Using Boost-Buck Converters as LED Drivers

Benefits to Boost-Buck LED Drivers	Trade-Offs to Boost-Buck LED Drivers	Applications
Direct battery to LED conversion	Lower efficiency	High beam/low beam
LED voltage may be higher or lower than supply	Lower bandwidth (<1/20 of f_{SW})	Turn signal
Good EMI performance	Higher inductor current rating	Daytime running lights
May use matrix to short entire string	Cannot short output to GND	Multiple strings on the same output

Buck Mode Using a Boost Converter

Some step-up (or boost) LED drivers may be configured to step-down from the supply (rather than ground referenced, as in a standard buck)—creating a buck-mode configuration. This configuration has the same limitations as a buck, where the total LED string voltage must be less than the input supply.

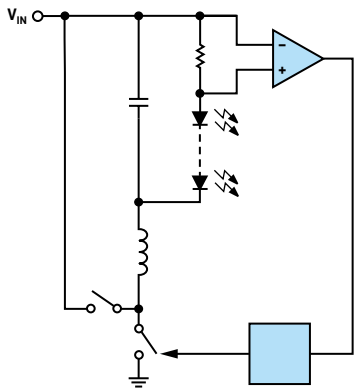

Figure 7. Buck-mode converter.

Table 4. Advantages and Trade-Offs of Using Buck-Mode Converters as LED Drivers

Benefits to Buck-Mode LED Drivers	Trade-Offs to Buck-Mode LED Drivers	Applications
Good EMI performance	Input voltage must be higher than LED voltage	High beam/low beams
May use matrix to short entire string	Preboost regulator required in most automotive systems	Turn signal
May use the same driver for multiple applications	Cannot short output (LED cathode) to GND	Daytime running lights

Buck-Boost Converter

Buck-boost LED drivers regulate LED current from a supply that is higher or lower than the total LED string voltage. The converter modulates the high-side switch connected to the input voltage in the step-down mode and the low-side on the output-side in step-up mode. This topology is the most complex but also the most flexible. V_{IN} and V_{OUT} ranges are only limited by the controller IC. This is a good choice for matrix applications.

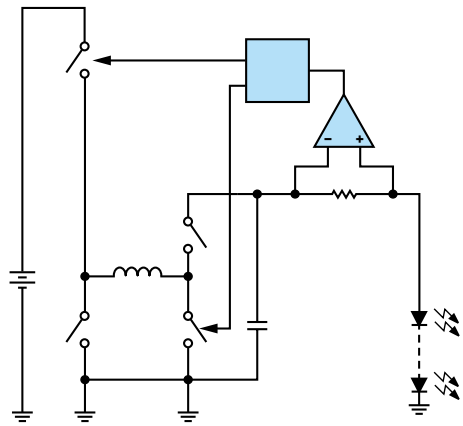

Figure 9. Buck-boost converter.

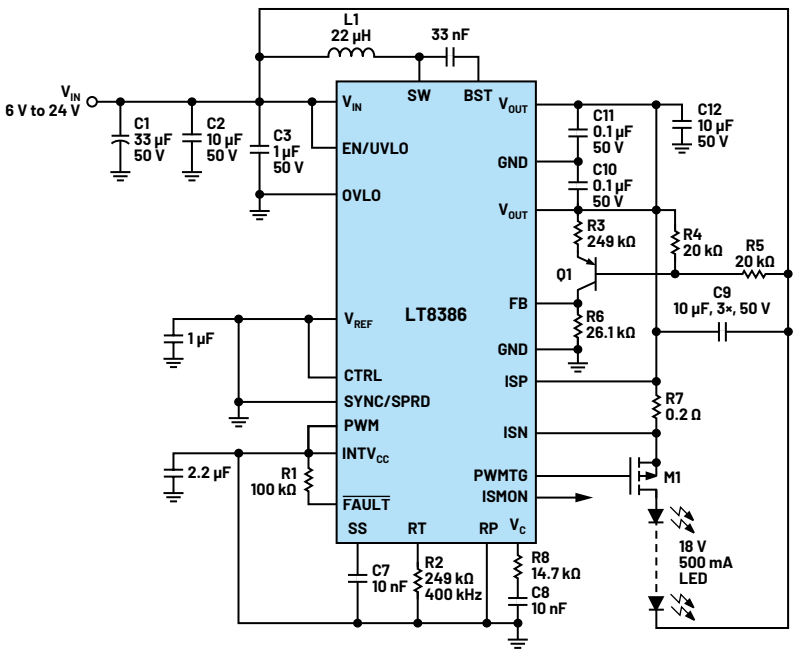

Figure 6. Boost-buck converter: LT8386.

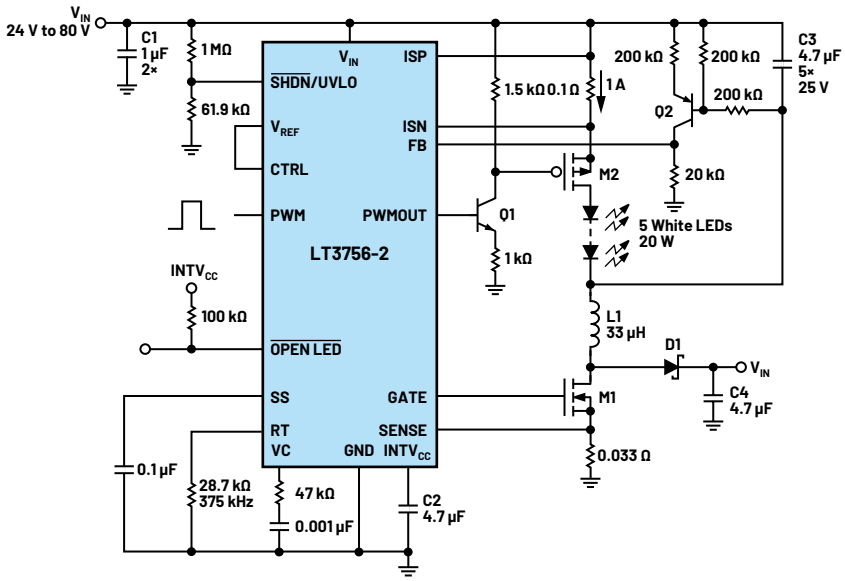

Figure 8. Buck-mode example: LT3756-2.

Table 5. Advantages and Trade-Offs of Using Buck-Boost Converters as LED Drivers

Benefits to Buck-Boost LED Drivers	Trade-Offs to Buck-Boost LED Drivers	Applications
Most versatile topology	A minimum of two switches and two freewheeling diodes is required	High beam/low beams
May use matrix to short entire string	Typically, the lowest conversion efficiency	Turn signal
May use the same driver for multiple applications	Typically, the lowest (worst) EMI performance	Daytime running lights
		Short safe systems

Conclusion

Automotive LED lighting systems can be driven with switching regulators in many different ways. Depending on the application, the selection of switching topology and configuration allows the lighting designer to create complete subsystems for the different lighting requirements throughout an automobile. Selecting the correct power conversion switching topology and configuration for the system optimizes requirements such as complexity, efficiency, EMI, and safety.

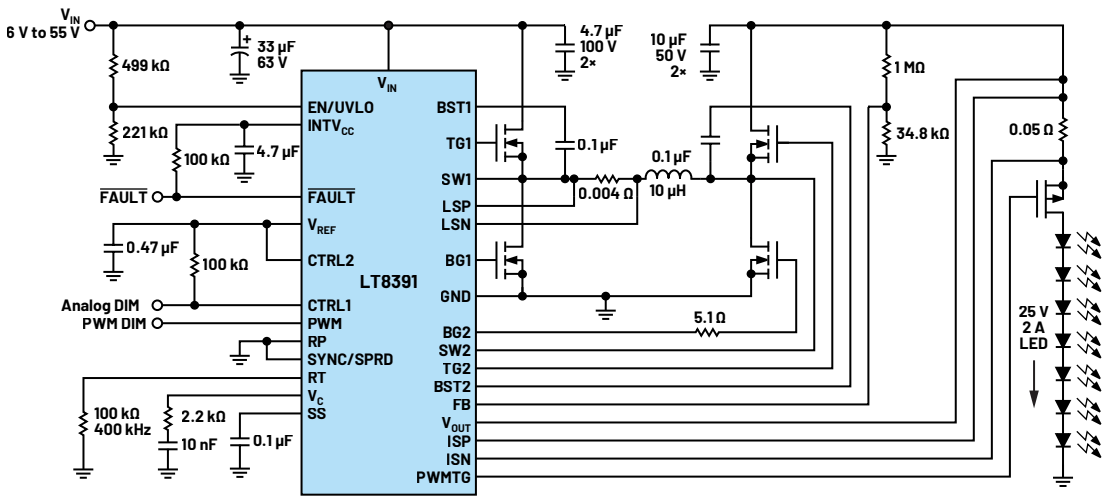

Figure 10. Buck-boost example: LT8391.

About the Author

Josh Caldwell was with Linear Technology (now part of Analog Devices) for 10 years as a design engineering section leader responsible for the definition, design, and development of monolithic buck, boost, and controller LED drivers. He holds a bachelor's degree in electrical engineering from the University of Colorado. In his spare time, he enjoys bicycling and drawing.

RAQ Issue 202: RF Demystified: Scattering Parameters and Their Types

Anton Patyuchenko, Field Applications Engineer

Question:

What are S-parameters and their main types?

Answer:

S-parameters describe the fundamental characteristics of RF networks, and their main types include small signal, large signal, pulsed, cold, and mixed-mode S-parameters.

Introduction

This article continues a series of short discourses written to solve much of the RF mystery for non-RF engineers. Some of these RF articles are: "RF Demystified—Understanding Wave Reflections," which discusses wave reflections, and "How to Easily Select the Right Frequency Generation Component," which reviews the main types of frequency generation components that fulfill functions in the RF signal chain.

This time we will talk about the most basic term one needs to know to describe any RF component—the scattering parameters (or S-parameters). However, unlike many other articles on this topic, this one will not only focus on the basic definitions of S-parameters but will also give a concise overview of their key types commonly used in RF engineering.

Fundamental Definitions

S-parameters quantify how RF energy propagates through a system and thus contain information about its fundamental characteristics. Using S-parameters, we can represent even the most complex RF device as a simple N-port network. Figure 1 shows an example of a two-port unbalanced network, which can be used to represent many standard RF components such as RF amplifiers, filters, or attenuators, just to name a few.

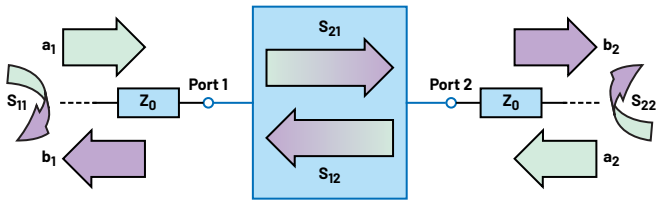

Figure 1. Two-port unbalanced RF network.

The wave quantities a, schematically shown in Figure 1, are complex amplitudes of the voltage waves incident on Port 1 and Port 2 of the device. If we stimulate one port at a time with the corresponding wave quantity a_1 or a_2 when the other port is terminated into the matched load, we can define the forward and reverse responses of the device in terms of the wave quantities b. These quantities represent voltage waves reflected from and transmitted through the ports of the network. If we take the ratio of the resulting complex responses and the initial stimulus quantities, we can define the S-parameters of a two-port component as shown in Equation 1:

$$S_{11} = \frac{b_1}{a_1};\ S_{12} = \frac{b_1}{a_2};\ S_{21} = \frac{b_2}{a_1};\ S_{22} = \frac{b_2}{a_2} \quad (1)$$

The intrinsic response of the network can then be expressed by grouping S-parameters together into a scattering matrix (S-matrix), which relates the complex wave quantities at all its ports. For the two-port unbalanced network, the stimulus-response relation will obtain the form in Equation 2:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (2)$$

The S-matrix can be defined in a similar manner for an arbitrary N-port RF component.[1,2]

Types of S-Parameters

If not explicitly stated otherwise, the term "S-parameters" usually refers to the small signal S-parameters. They represent an RF network response to a small signal stimulus quantifying its reflection and transmission characteristics over frequency in a linear operational mode. Using small signal S-parameters, we can determine basic RF characteristics including voltage standing wave ratio (VSWR), return loss, insertion loss, or gain at given frequencies.

However, if we continuously increase the power level of a signal that is passing through an RF device, it will often result in more pronounced nonlinear effects. These effects can be quantified using another type of scattering parameters called large signal S-parameters. They vary not only across different frequencies but also across different power levels of a stimulus

signal. This type of scattering parameter can be used to determine nonlinear characteristics of a device such as its compression parameters.

Both small and larger signal S-parameters are usually measured using continuous-wave (CW) stimulus signals and applying a narrow-band response detection. However, many RF components are designed to be operated with pulsed signals, which have a broad frequency-domain response. This makes it challenging to accurately characterize an RF component using the standard narrow-band detection method. Therefore, for the characterization of devices in a pulsed mode, the so-called pulsed S-parameters are typically utilized. These scattering parameters are obtained using special pulse-response-measurement techniques.[3]

Another particular type of S-parameters, which is rarely talked about, but which might sometimes become important to consider, is cold S-parameters. The term "cold" means that the scattering parameters are obtained for an active device in a nonactive mode (that is, when all its active elements are inactive, for example, transistor junctions are reverse or zero biased and no transfer currents flow). This type of S-parameters can be used for instance to improve matching of the signal chain segments with off-state components that cause high reflections in the signal path.

Up until now, we have defined S-parameters for a typical example of a single-ended component when the stimulus and response signals are referenced to ground. However, for balanced components that have differential ports, this definition is not sufficient. Balanced networks require a broader characterization approach, which must be able to fully describe their differential-mode and common-mode responses. This can be achieved by using mixed-mode S-parameters. Figure 2 shows an example of the mixed-mode scattering parameters grouped together into an extended S-matrix representing a typical two-port balanced component.

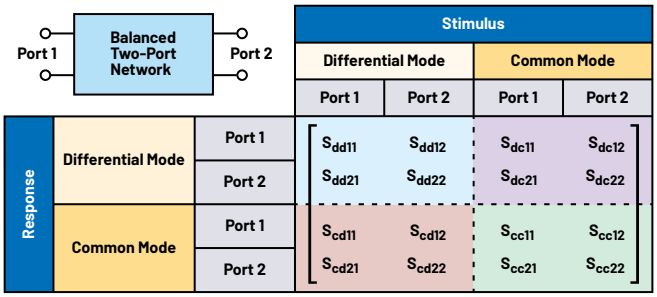

Figure 2. Two-port balanced RF network and its mixed-mode scattering matrix.

Subscripts of the mixed-mode S-parameters in this matrix use the naming convention b-mode, a-mode, b-port, and a-port, where the former two describe the modes of the response port (b-mode) and stimulus port (a-mode), and the latter two specify index numbers of these ports, where b-port corresponds to the response and a-port to the stimulus port. In our example, the port modes are defined either by the subscript d—differential—or c—common mode. However, in a more general case of a component that has both balanced and unbalanced ports, a mixed-mode S-matrix will also have additional elements with subscript s describing the quantities obtained for the single-ended ports. The mixed-mode scattering parameters allow us to determine not only the basic parameters of an RF component such as return loss or gain but also the key figures of merit used to characterize performance of the differential circuits such as common-mode rejection ratio (CMRR), magnitude imbalance, and phase imbalance.

Conclusion

This article has presented basic definitions and briefly discussed the key types of scattering parameters. The S-parameters can be used to describe fundamental characteristics of RF components at different frequencies and for different power levels of a signal. The development of RF applications highly relies on the use of S-parameter data describing integral structures and constituent components of RF designs. RF engineers measure or rely on already existing S-parameter data, which is typically stored in standard text files known as Touchstone or SnP files. These files are often freely provided for the most popular RF components available on the market today.

Analog Devices provides the broadest portfolio of integrated RF components in the industry addressing the most demanding requirements across a wide variety of applications. In order to support RF engineers and ease the development process of the target applications, ADI offers the entire ecosystem around RF technologies including scattering parameters for a wide range of RF products, design tools, simulation models, reference designs, rapid prototyping platforms, and a discussion forum.

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[2]Michael Hiebel. *Fundamentals of Vector Network Analysis*. Rohde & Schwarz, 2007.

[3]"Pulsed Measurements Using Narrowband Detection and a Standard PNA Series Network Analyzer." Keysight Technologies, December 2017.

About the Author

Anton Patyuchenko received his Master of Science in microwave engineering from the Technical University of Munich in 2007. Following his graduation, Anton worked as a scientist at German Aerospace Center (DLR). He joined Analog Devices as a field applications engineer in 2015 and is currently providing field applications support to strategic and key customers of ADI specializing in RF applications.

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