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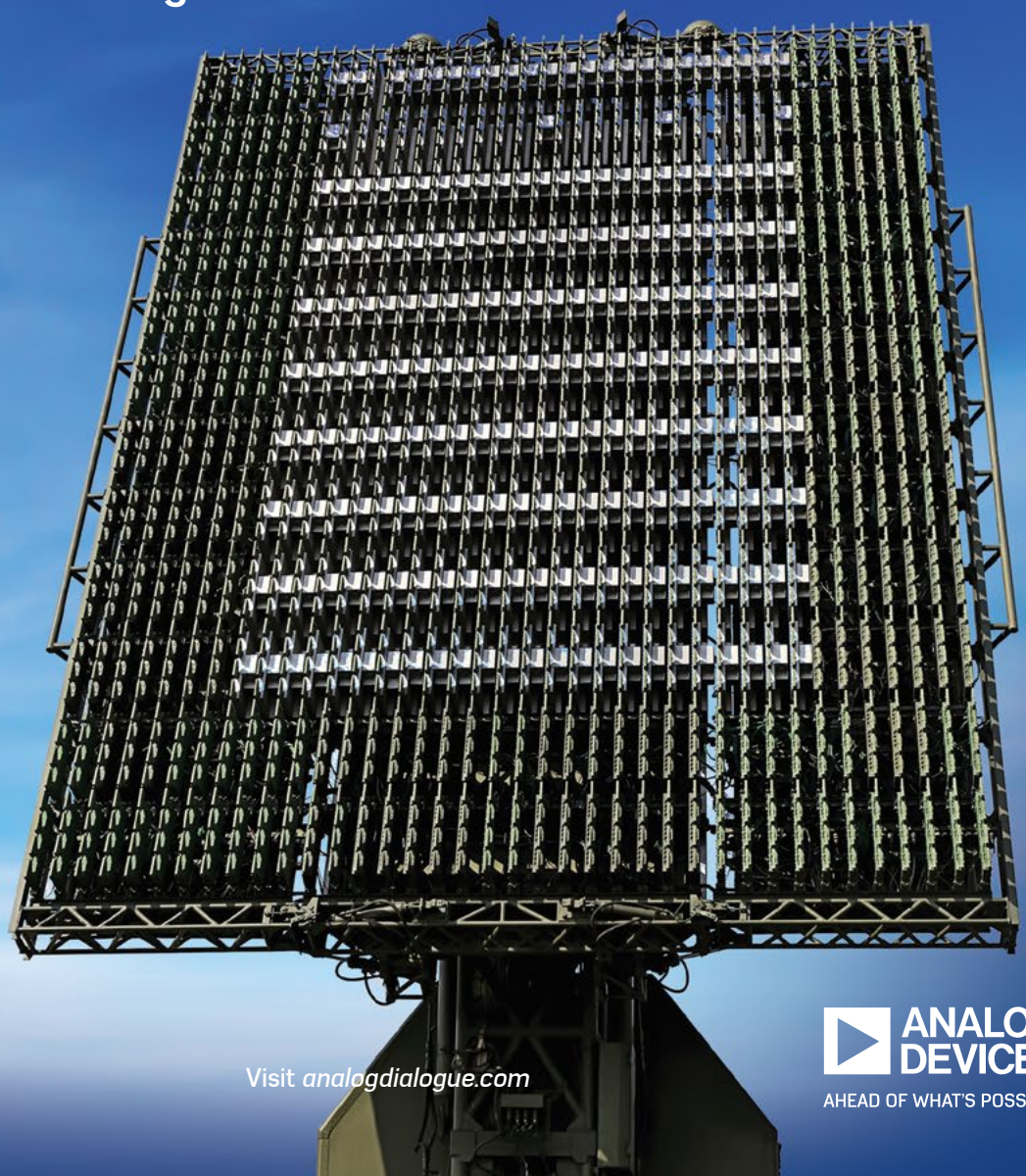
10 Phased Array Beamforming ICs Simplify Antenna Designs



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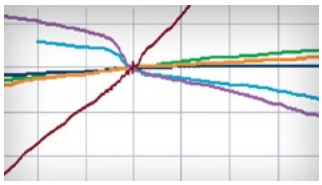

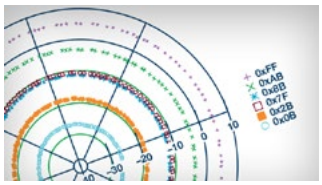

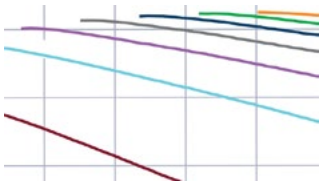

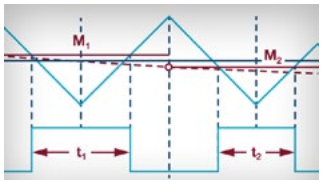

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Bernhard became editor of *Analog Dialogue* in March 2017. He has been with Analog Devices for over 25 years, starting at the ADI Munich office in Germany. In his current role as the chief technical editor, he is responsible for the worldwide technical article program within Analog Devices.

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AnalogDialogue

Analog Dialogue is a technical magazine created and published by Analog Devices. It provides in-depth design related information on products, applications, technology, software, and system solutions for analog, digital, and mixed-signal processing. Published continuously for over 50 years—starting in 1967—it is produced as a monthly online edition and as a printable quarterly journal featuring article collections. For history buffs, the *Analog Dialogue* archive includes all issues, starting with Volume 1, Number 1, and four special anniversary editions. To access articles, the archive, the journal, design resources, and to subscribe, visit the *Analog Dialogue* homepage, *analogdialogue.com*.

Clock Skew in Large Multi-GHz Clock Trees

By **Chris Pearson**

Introduction

It is not uncommon for large clock trees to route clock signals through multiple clock devices, using multiple transmission line types, and across multiple boards and coaxial cables. Even when best practices are followed, any one of these media can introduce greater than 10 ps clock skew. However, in some applications, it is desired for all clock signals to achieve less than 1 ps skew. Some of these applications include phased array, MIMO, radar, electronic warfare (EW), millimeter wave imaging, microwave imaging, instrumentation, and software-defined radio (SDR).

This article identifies several areas of concern in the design process, manufacturing process, and application environment that can cause clock skews of 1 ps or more. With regards to these areas of concern, several recommendations, examples, and rules of thumb will be provided to help the reader gain an intuitive feel for the root cause and magnitude of clock skew errors.

Delay Equations for Transmission Lines

A list of equations is provided that estimate propagation delay (τ_{pd}) for a single clock path and delta propagation delays ($\Delta\tau_{pd}$) for multiple clock paths or a change in environmental conditions. In a large clock tree application, $\Delta\tau_{pd}$ between clock traces is a portion of the total system's clock skew. Equation 1 and Equation 2 provide the two main variables that control a transmission line's τ_{pd}: the transmission line's physical length (ℓ) and effective dielectric constant (ε_{eff}). Referring to Equation 1, v_p represents the transmission lines phase velocity, V_F represent the velocity factor (%), and c represents the speed of light (299,792,458 m/s).

$$\upsilon_p = VF \times c = \frac{c}{\sqrt{\varepsilon_{eff}}} \tag{1}$$

$$\tau_{pd} = \frac{\ell}{\upsilon_P} \tag{2}$$

Equation 3 calculates the delta propagation delay ($\Delta\tau_{pd}$) between two transmission lines.

$$\Delta\tau_{pd} = \frac{\ell_1}{\upsilon_{p1}} - \frac{\ell_2}{\upsilon_{p2}} \tag{3}$$

Transmission line dielectric materials have properties that change with temperature. The dielectric constant's temperature coefficient (TCDk) is often provided in a plot of phase change ($\Delta\phi_{ppm}$) in parts per million (ppm) vs. temperature, where the $\Delta\phi_{ppm}$ value compares the phase at a desired temperature to the phase at a reference temperature, typically 25°C. For a known temperature, $\Delta\phi_{ppm}$, and transmission line length, Equation 4 estimates the change in propagation delay from the reference temperature.

$$\Delta\tau_{pd} = \frac{\ell \times \Delta\Phi_{ppm}}{\upsilon_p \times 10^6} \tag{4}$$

Coaxial cable dielectric materials have properties that change based on the bend in a cable. The radius and angle over which the cable bend occurs determine the change in the effective dielectric constant. Typically, this is provided as a change in phase ($\Delta\phi_{deg}$) by comparing the phase of a specific cable bend to a straight cable. For a known $\Delta\phi_{deg}$, signal frequency (f), and cable bend, Equation 5 estimates the change in propagation delay.

$$\Delta\tau_{pd} = \frac{\Delta\Phi_{deg}}{f \times 360} \tag{5}$$

Delay Variation Considerations

Transmission Line Selection

Recommendation: For best delay matching results between multiple traces, match trace lengths, and transmission line types.

Rules of Thumb:

- A 1 mm difference between two trace lengths equates to a $\Delta\tau_{pd}$ ~6 ps (a 6 mil difference between two trace lengths equates to a $\Delta\tau_{pd}$ ~1 ps).
- Striplines are ~1 ps/mm slower than a microstrip- or conductor-backed coplanar waveguide (CB-CPW).

Different transmission line types produce different ε_{eff} and v_p. Using Equation 2, this means different transmission types of the same physical length have a different τ_{pd}. Table 1 and Figure 1 provide simulation results of three common transmission line types—CB-CPW, microstrip, and stripline that highlight the differences in ε_{eff}, v_p, and τ_{pd}. This simulation estimates τ_{pd} for a 10 cm CB-CPW trace is 100 ps greater than a stripline trace of the same length. Simulations were generated using the Microwave Impedance Calculator from Rogers Corporation.

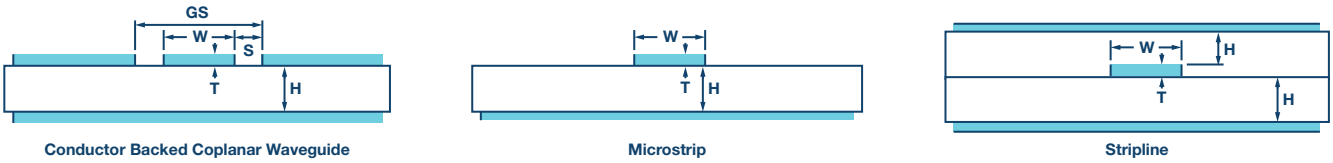


Figure 1. Matching transmission line types.

Figure 2. Adjacent traces vs. isolated traces.

Table 1. Rogers 4003C Simulation Results of Figure 1

	CB-CPW	Microstrip	Stripline
ε_{eff}	2.52	2.76	3.55
v_p (m/s)	1.89×10^8	1.80×10^8	1.59×10^8
τ_{pd}/mm	5.29	5.54	6.28
(ps/mm)	0.508	0.508	0.508
H (mm)	0.863	1.16	0.538
W (mm)	0.228		
S (mm)			

Rogers 4003C has a relative permeability (ε_r), also known as dielectric constant (Dk), of 3.55. In Table 1, note CB-CPW and microstrip have lower ε_{eff} since they are exposed to air, whose $\varepsilon_r = 1$.

It is not always possible to route all delay matched signals on the same layer or with the same transmission line type. Table 2 provides some generalized considerations for selecting a transmission line type for different traces. If it is necessary to match τ_{pd} for different transmission line types, it is best to use a board simulation tool rather than hand calculations and rules of thumb.

Table 2. Generalized Transmission Line Considerations

	CB-CPW	Microstrip	Stripline
Routing Density		Okay	Best
Signal Isolation	Okay		Best
Least Signal Attenuaton	Best		
Manufacturing Process Variation	Best		
Overall Best Performance at High Frequencies	Typically, lower ε_{eff} are best		

Transmission Line VIAs

Recommendation: If a signal path has a via, remember to include the via length between the two signal layers of interest when calculating propagation delays.

For a rough propagation delay calculation, assume the via length connecting the two signal layers has the same phase velocity as the transmission line. For instance, a via connecting the top and bottom signal layers of a 62 mil thick board, would account for an additional τ_{pd} ~10 ps.

Adjacent Traces, Differential and Single-Ended Signals

Recommendation: Keep a minimum of one line width between traces to avoid a significant change in ε_{eff}.

Rules of Thumb:

- 100 Ω differential signals (odd mode) are faster than a 50 Ω single-ended signal.
- Closely spaced in-phase 50 Ω single-ended signals (even mode) are slower than a single 50 Ω single-ended signal.

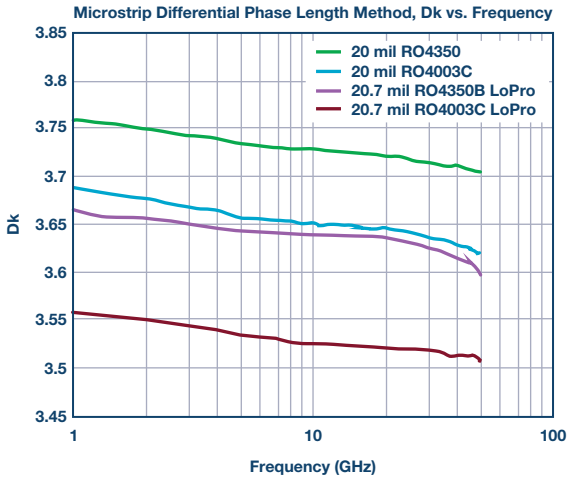
The signal direction of closely spaced adjacent traces changes the ε_{eff} and, as a result, the delay match between equal length traces. A simulation for two edge-coupled microstrip traces vs. a single microstrip trace are provided in Figure 2 and Table 3. This simulation estimates that the τ_{pd} for two 10 cm edge-coupled even mode traces is 16 ps greater than a standalone single trace of the same length.

When trying to match single-ended τ_{pd} to differential τ_{pd}, it is important to simulate the phase velocity of both paths. In clocking applications, this situation may occur when trying to send a CMOS sync or SYSREF request signal that is time aligned to a differential reference or clock signal. Increasing the spacing between the differential signal paths creates a closer phase velocity match between the differential and single-ended signals. However, this is at the expense of the differential signal's common-mode noise rejection, which keeps clock jitter to a minimum.

It is also important to point out that closely spaced in-phase signals (even mode) increase the ε_{eff}, resulting in a longer τ_{pd}. This occurs when multiple copies of single-ended signals are route closely together.

Table 3. Adjacent Traces vs. Isolated Trace

	Even Mode (In-Phase)	Odd Mode (Differential)	Single Trace
ε_{eff}	2.92	2.64	2.76
v_p (m/s)	1.75×10^8	1.84×10^8	1.80×10^8
τ_{pd}/mm (ps/mm)	5.70	5.42	5.54
H (mm)	0.538	0.538	0.538
W (mm)	1.18	1.18	1.18
S (mm)	1.18	1.18	



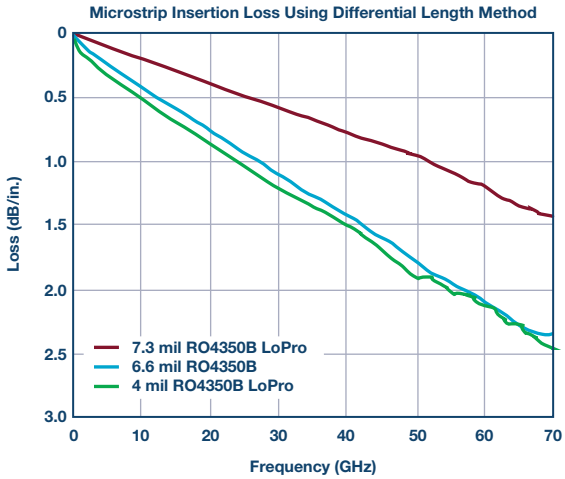


Figure 3. Dk and DF vs. frequency.[1]

Delay Match vs. Frequency

Recommendation: To minimize frequency related delay matching errors, choose a low Dk, low dissipation factor (DF) material (Dk <3.7, DF <0.005). DF is also known as loss tangent (tan δ) (see Equation 6). For multi-GHz traces, avoid plating technologies that include nickel.

Matching signal delays to the picosecond level of different frequency signals is challenging due to counteracting variables. Figure 3 shows that with increasing frequencies, dielectric constants typically decrease. Based on Equation 1 and Equation 2, this behavior produces a smaller τ_{pd} as frequencies increase. Based on Equation 3 and the Roger's material in Figure 3,[1] the $\Delta\tau_{pd}$ between a 1 GHz and 20 GHz sine wave on a 10 cm trace is roughly 4 ps.

Figure 3 also shows signal attenuation increases as frequency increases, resulting in larger attenuation of a square wave's higher order harmonic when compared to the fundamental tone. The degree to which this filtering occurs will result in varying levels of rise (τ_R) and fall (τ_F) times. A change in τ_R or τ_F presents the waveform to the receiving device's clock input as a change in total delay, which is composed of the trace's τ_{pd} and the signal's $\tau_R/2$ or $\tau_F/2$. In addition, different frequency square waves may also have a different group delay. For these reasons, square waves are more challenging than sine waves when estimating delay matching between different frequencies.

For a better understanding of attenuation (α in dB/ft) vs. frequency refer to Equation 7 and Equation 8 and the references supplied in this article,[2,3,4,5] which introduce loss tangents (δ) and skin effect. One key point from these references is that skin effect reduces the area (A) in Equation 8, which increases line resistances (R).[3] To avoid excessive attenuation due to skin effect at high frequencies, avoid plating technologies that use nickel, such as solder mask over gold (SMOG) and electroless nickel immersion gold (ENIG) plating.[4,5] One example of a plating technology that avoids nickel is solder mask over bare copper (SMOBC). To summarize, choose a low Dk/DF material, avoid plating technologies that use nickel, and run board-level delay simulations on key traces to improve delay matching of different frequencies.

$$DF = \tan\delta \quad (6)$$

$$\alpha = 2.3 \times f \times \tan\delta \times \sqrt{\varepsilon_{eff}} \quad (7)$$

$$R = \rho \times \frac{\ell}{A} \quad (8)$$

Delay Match vs. Temperature

Recommendation: Choose a temperature stable dielectric material for PCB and cables. Temperature stable dielectrics typically have $\Delta\phi_{ppm}$ <50 ppm.

Dielectric constants vary over temperature, which causes changes in a transmission line's τ_{pd}. Equation 4 calculates $\Delta\tau_{pd}$ with respect to changes in the dielectric constant over temperature.

In general, PCB materials are lumped into two categories: woven glass (WG) or nonwoven glass. Woven glass materials are typically cheaper and exhibit a higher Dk, due to glass having a Dk = 6. Figure 4 compares Dk changes for a variety of different materials. Figure 4 highlights that some PTFE/WG-based materials have a steep TCDk between 10°C and 25°C.

Using Equation 3 and Figure 4, Table 4 calculates the $\Delta\tau_{pd}$ due to 25°C to 0°C temperature change of 10 cm stripline traces on different PCB materials. In a system that requires matching τ_{pd} across multiple traces at different temperatures, PCB material selection can cause τ_{pd} mismatches of a few picoseconds between 10 cm traces.

Coaxial cable dielectrics also have similar TCDk concerns. Coaxial cable lengths are usually much greater than PCB trace lengths, which will result in a much greater $\Delta\tau_{pd}$ over temperature. Using two 1 m cables with the same properties shown in column 2 of Table 4 can create τ_{pd} mismatches of 25 ps when the temperature changes from 25°C to 0°C.

Table 4 assumes constant temperatures for the length of the 10 cm trace. In a real-world situation, the temperature may not be constant over the length of trace or coaxial cable, making analysis more complex than the scenario discussed above.

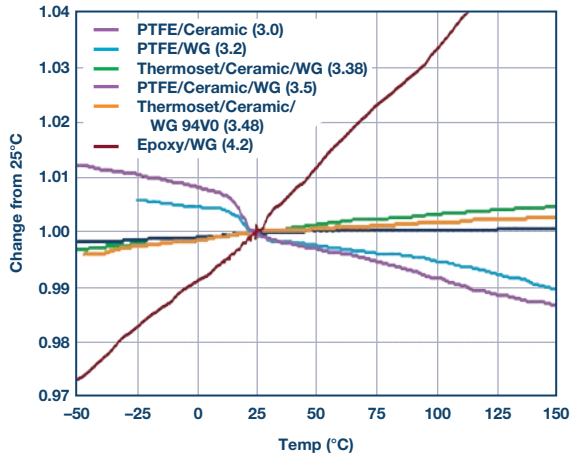


Figure 4. Dk change vs. temperature.[1]

Table 4. $\Delta\tau_{pd}$ of 10 cm Stripline, 25°C to 0°C

	Epoxy/WG (FR-4)	PTFE Ceramic/WG	PTFE Ceramic
Dk at 25°C	4.2	3.5	3.0
Dk Change, 25°C to 0°C	0.992	0.1008	0.999
Dk at 0°C (calculated)	4.1664	3.528	2.997
$\Delta\tau_{pd}$ (ps), 25°C to 0°C	2.74	–2.49	0.29

Delay Matched Cables

Recommendation: Understand cost trade-offs between purchasing delay matched cables and the development cost of a calibration routine to adjust for delay mismatch electronically.

Based on the author's experience, comparing coaxial cables of the same length and material from the same vendor results in delay mismatches in the 5 ps to 30 ps range. From discussions with cable vendors, this range is the result of variations that occur during cable cutting, SMA installation, and lot-to-lot variation of the Dk.

Many coaxial cable manufacturers offer phase matched cables within predetermined matched delay windows of 1 ps, 2 ps, or 3 ps. The price of the cable typically increases as the delay match accuracy increases. To manufacture <3 ps delay matched cables, manufacturers often add several delay measurement and cable cutting steps to their cable manufacturing process. For the cable manufacturer, these added steps result in increased manufacturing cost and yield loss.

Delay Match vs. Cable Bend

Recommendation: When selecting cable materials, understand trade-offs between delay shifts due to temperature vs. delay shift due to cable bends.

Bending coaxial cables results in different signal delays. Cable vendor data sheets often specify the phase error for 90° bend at a specific bend radius and frequency. For instance, an 8° phase change may be specified with a 90° bend at 18 GHz. Using Equation 5, this calculates roughly to 1.2 ps delay.

Delay Match vs. SMA Installation and Selection

Variations in installation of PCB edge mount SMAs can add delay mismatch between clock paths, as shown in Figure 5. Errors of this nature are not measured typically and, as a result, are hard to quantify. However, it is reasonable to assume this could add 1 ps to 3 ps delay mismatch between clock paths.

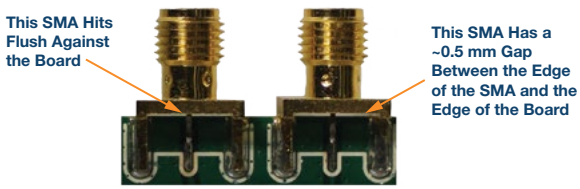


Figure 5. SMA installation delay mismatch.

One way to control delay mismatch due to SMA installation is to select SMAs with alignment features, as shown in Figure 6. There is a trade-off since SMAs with alignment features are typically specified for higher frequencies than those without alignment features and, as a result, cost more. The SMA vendor often provides a recommended PCB to SMA launch board layout for the higher frequency SMAs. This recommended layout alone may be worth the additional price as it could save a board revision, especially if the clock frequency is >5 GHz.

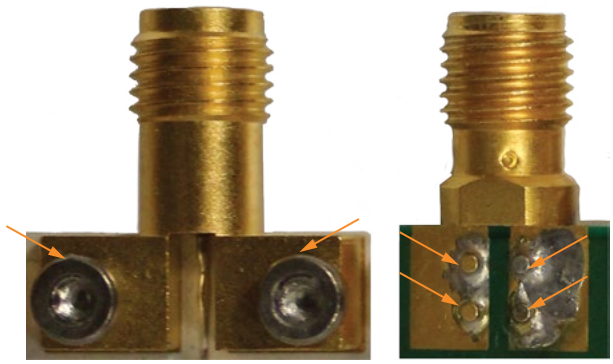


Figure 6. SMA with alignment features.

Delay Match Across Multiple PCBs

Recommendation: Understand the cost trade-off between purchasing PCB materials with well-controlled lot-to-lot ε_r and the development cost of a calibration routine to electronically adjust for delay mismatch.

Trying to match τ_{pd} between traces on multiple PCBs adds several sources of error. Four of the sources of error were discussed above: delay match vs. temperature; delay matched cables; delay match vs. cable bend; and delay match vs. SMA installation and selection. The fifth source of error is process variation of ε_r across multiple PCBs. Contact the PCB manufacturer to understand the process variation of ε_r.

As an example, FR-4's ε_r can vary between 4.35 to 4.8.[6] The extremes of this range produce a possible 35 ps $\Delta\tau_p$d for 10 cm stripline traces on different PCBs. Other PCB material data sheets supply a smaller typical range for ε_r. For instance, Rogers 4003C's data sheet states an ε_r range of 3.38 ± 0.05. The extremes of this range reduce the possible $\Delta\tau_{pd}$ to 9 ps for 10 cm stripline traces on different PCBs.

Clock Skew Due to Clock ICs

Recommendation: Consider newer PLL/VCO ICs that include <1 ps skew adjustments.

In the past, data converter clocks were generated from multiple output clock devices. The data sheets of these clock devices specified the device's clock skew, typically ranging from 5 ps to 50 ps depending on the IC selected. To the author's knowledge, none the multioutput GHz clock ICs available at the time of this article provided the ability to adjust the clock delay on a per output basis.

As data converter clock frequencies >6 GHz become more common, single or dual output PLLs/VCOs will become the clock of choice. The advantage of the single output PLL/VCO clock IC architecture is that methods are being developed to adjust the reference input to clock output delays in <1 ps steps. The ability to adjust reference input to

output delays on a per clock basis allows the end user to perform a system-level calibration to minimize clock skew to <1 ps. This sort of system level clock skew calibration has the potential to relax all PCB, cable, and connector delay matching concerns discussed in this article, and, as a result, will lower the overall BOM cost of system.

Conclusion

Several sources of possible delay variation and delay mismatch have been discussed. It has been shown that ε_{eff} may vary with temperature, frequency, process, transmission line types, and line spacing. It has also been shown that a multi-PCB setup connected via coaxial cables creates additional sources of delay variation. When selecting material to minimize clock skew in a large clock tree, it is very important to understand how different PCB and cable ε_r varies with temperature, process, and frequency. With all these variables, it would be difficult to design a large clock with <10 ps skew without some sort of skew calibration. In addition, purchasing PCB materials, coaxial cables, and SMA connectors to minimize clock skew would add significant material cost. To help ease calibration methods and lower system cost, many of the newer PLL/VCO and clock devices from IC manufacturers allow for sub-1 ps delay adjustment capability.

Table 5 provides a summary of the recommendations discussed in this document to minimize clock skew.

References

[1] Data supplied compliments of Rogers Corporation, used with permission.

[2] Rick Hartley. "Base Materials for High Speed, High Frequency PC Boards." *PCB & A*, March 2002.

[3] Howard Johnson. "Skin Effect Calculation." *High Speed Digital Design,* Signal Consulting, Inc., 1997.

[4] Howard Johnson. "Nickel-Plated Traces." *High Speed Digital Design Online Newsletter*, Vol. 5, Issue 6, 2002.

[5] Howard Johnson. "Nickel Matters." *EDN*, October 23, 2012.

[6] "FR-4." Microwaves101, 2018.

Table 5. Summary Recommendations to Minimize Clock Skew by Topic

	Recommendations
Transmission Line Selection	Match trace lengths and transmission line types
Transmission Line VIAs	Remember to include the via propagation delay in calculations
Adjacent Traces	Keep a minimum of one line width between adjacent traces; be aware of propagation delays difference between even mode, odd mode, and single-ended signals
Delay Match vs. Frequency	Choose PCB material with Dk <3.7 and DF <0.005; avoid nickel-based plating technologies
Delay Match vs. Temperature	Choose temperature stable dielectrics ($\Delta\phi$ppm <50 ppm)
Delay Matched Cables	Understand cost and system clock skew trade-offs when purchasing delay match cables vs. development cost of system level clock skew calibration
Delay Match vs. Cable Bends	Be aware of impact cable bends can have on delay match; this could impact harness design or cable material selection
Delay Match vs. SMA Installation/Selection	Minimize skew variation due to edge launch SMA installation by using SMAs with alignment features
Delay Match Across Multiple PCBs	Understand cost and system clock skew trade-offs when purchasing PCB material with well-controlled lot-to-lot ε_r vs. development cost of system-level clock skew calibration
Clock Skew Due to Clock ICs	Consider PLL/VCO devices that include <1 ps clock skew adjustments

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Chris Pearson

Phased Array Beamforming ICs Simplify Antenna Design

By **Keith Benson**

Abstract

Wireless communications and radar systems are facing increasing demands on antenna architectures to improve performance. Many new applications will only be possible with antennas that consume less power in a lower profile than traditional mechanically steered dish antennas. These requirements are in addition to the desire to reposition quickly to a new threat or user, transmit multiple data streams, and operate over longer lifetimes at aggressive cost targets. In some applications, there is a need to null an incoming blocking signal and have a low probability of intercept. These challenges are met with phased array-based antenna designs that are sweeping the industry. Past disadvantages of phased array antennas are being addressed with advanced semiconductor technology to ultimately reduce the size, weight, and power of these solutions. This article will briefly describe existing antenna solutions and where electrically steered antennas have advantages. It will then go into how semiconductor advancements are helping to achieve the goals of improving SWaP-C for electrically steered antennas, followed by examples of ADI technology that make this possible.

Introduction

Wireless electronic systems relying on antennas to send and receive signals have been operating for over 100 years. They continue to be improved as the need for accuracy, efficiency, and more advanced metrics become increasingly important. In past years, a dish antenna has been widely used to transmit (Tx) and receive (Rx) signals where directivity is important and many of those systems work well at a relatively low cost after years of optimization. These dish antennas having a mechanical arm to rotate the direction of radiation does have some drawbacks, which include being slow to steer, physically large, having poorer long-term reliability, and having only one desired radiation pattern or data stream. As a result, engineers have pushed toward advanced phased array antenna technology to improve these features and add new functionality. Phased array antennas are electrically steered and offer numerous benefits compared to traditional mechanically steered antennas such as low profile/less volume, improved long-term reliability, fast steering, and multiple beams. With these benefits, the industry is seeing adoption in military applications, satellite communications (satcom), and 5G telecommunications including connected automobiles.

Phased Array Technology

A phased array antenna is a collection of antenna elements assembled together such that the radiation pattern of each individual element constructively combines with neighboring antennas to form an effective radiation pattern called the main lobe. The main lobe transmits radiated energy in the desired location while the antenna is designed to destructively interfere with signals in undesired directions, forming nulls and side lobes. The antenna array is designed to maximize the energy radiated in the main lobe while reducing the energy radiated in the side lobes to an acceptable level. The direction of radiation can be manipulated by changing the phase of the signal fed into each antenna element. Figure 1 shows how adjusting the phase of the signal in each antenna can steer the effective beam in the desired direction for a linear array. The result is that each antenna in the array has an independent phase and amplitude setting to form the desired radiation pattern. The attribute of fast steering of the beam in phased array is easily understood with no mechanically moving parts. Semiconductor IC-based phase adjustments can be made in nanoseconds such that we can change the direction of the radiation pattern to respond to new threats or users quickly. Similarly, it is possible to change from a radiated beam to an effective null to absorb an interferer, making the object appear invisible, such as in stealth aircraft. These changes in repositioning the radiation patterns or changing to effective nulls can be done almost instantaneously because we can change the phase settings electrically with IC-based devices rather than mechanical parts. An additional benefit of a phased array antenna over a mechanical antenna is the ability to radiate multiple beams simultaneously, which could track multiple targets or manage multiple data streams of user data. This is accomplished by digital signal processing of the multiple data streams at baseband frequencies.

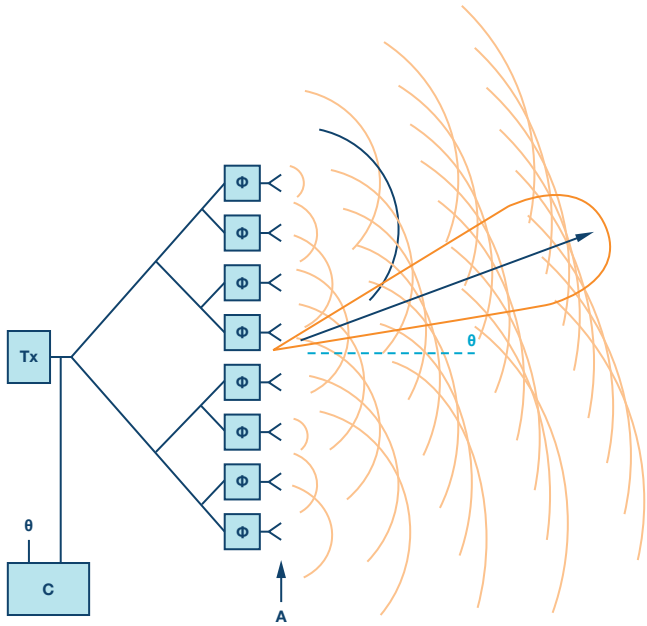

Figure 1. Diagram of phased array elements basic theory.

The typical implementation of this array uses patch antenna elements configured in equally spaced rows and columns with a 4 × 4 design implying 16 total elements. A small 4 × 4 array is shown in Figure 2 below with patch antennas as the radiators. This antenna array can grow quite large in ground-based radar systems, with over 100,000 elements being possible.

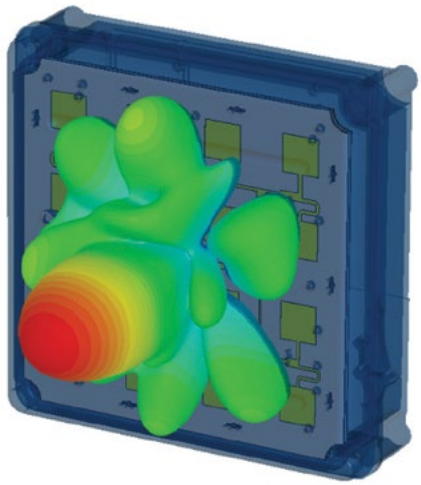

Figure 2. Illustration of radiation pattern for a 4 × 4 element array.

There are design trade-offs to consider with the size of the array vs. the power of each radiating element that impacts the directivity of the beam and effective radiated power. The antenna performance can be predicted by looking at some common figures of merit. Often, antenna designers look at the antenna gain and effective isotropic radiated power (EIRP), as well as a Gt/Tn. There are some basic equations that can be used to describe these parameters shown in the following equations. We can see that the antenna gain and EIRP are directly proportional to the number of elements in the array. This can lead to the large arrays seen in ground-based radar applications.

$$\text{Antenna Gain (Gt)} = \frac{\text{Radiation Intensity in Desired Direction}}{\text{Radiation Intensity of Isotropic Antenna (All Angles)}} = 10\,Log\,N + Ge$$

$$EIRP = Pt \times Gt$$

$$\frac{Gt}{Tn} = \frac{\text{Antenna Gain}}{\text{Noise Temperature}}$$

$$Tn = [Noise\ Factor - 1] \times Temp$$

$$Pt = 10LogN + Pe$$

where

N = number of elements

Ge = element gain

Gt = antenna gain

Pt = total transmitter power

Pe = power per element

Tn = noise temperature

Another key aspect of phased array antenna design is the spacing of the antenna elements. Once we have determined the system goals by setting the number of elements, the physical array diameter is largely driven by limits to each unit cell being less than approximately one-half wavelength, which prevents grating lobes. Grating lobes amount to energy radiated in undesired directions. This puts strict requirements on the electronics that go into the array to be small, low power, and low weight. The half-wavelength spacing creates particularly challenging designs at higher frequencies where the length of each unit cell becomes smaller. This drives the ICs at higher frequencies to be increasingly integrated, packaging solutions to become more advanced, and thermal management techniques to be simplified in spite of becoming increasingly challenging.

As we construct the entire antenna, there are many challenges of the array design, including the routing of control lines, power supply management, pulsed circuitry, thermal management, environmental considerations, etc. There is a major push in the industry toward low profile arrays that consume less volume and weight. The traditional plank architecture uses small PCB planks with electronics on them perpendicularly fed into the backside of the antenna PCB. This approach has been improved over the past 20 years to continually reduce the size of the plank thereby reducing the depth of the antenna. Next-generation designs move from this plank architecture to a flat panel approach where there is enough integration in each IC to fit them simply on the backside of the antenna board, significantly reducing the depth of the antenna and making them easier to fit into portable or airborne applications. In Figure 3, the image on the left shows the gold patch antenna elements on the topside of the PCB and the image on the right shows the analog front end of the antenna on the bottom side of the PCB. This is only a subset of the antenna where there could be a frequency conversion stage occurring in one end of the antenna, for example, and a distribution network to route from a single RF input to the entire array. It can easily be seen that more integrated ICs significantly reduce the challenges in the antenna design and, as the antennas become smaller with more electronics packed into a reduced footprint, the antenna design demands new semiconductor technology to help make the solutions viable.

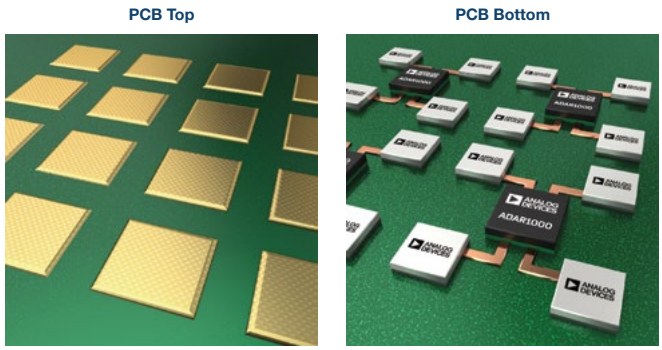

Figure 3. A flat panel array showing antenna patches on the topside of a PCB, while ICs are on the backside of an antenna PCB.

Digital Beamforming vs. Analog Beamforming

Most phased array antennas that have been designed in past years have used analog beamforming where the phase adjustment is done at RF or IF frequencies and there is one set of data converters for the entire antenna. There is increased interest in digital beamforming where there is one set of data converters per antenna element and the phase adjustment is done digitally in the FPGA or some data converters. There are many benefits to digital beamforming starting with the ability to transmit many beams easily or even change the number of beams almost instantly. This remarkable flexibility is attractive in many applications and is driving its adoption. Continuous improvements in the data converters are lowering power dissipation and expanding to higher frequencies where RF sampling at the L-band and S-band are making this technology a reality in radar systems. There are multiple considerations to make when considering analog vs. digital beamforming, but the analysis is usually driven by the number of beams required, power dissipation, and cost targets. The digital beamforming approach typically has higher power dissipation with a data converter per element but offers a lot of flexibility in the ease of

creating multiple beams. The data converters also require higher dynamic range since the beamforming that rejects blockers is only done after the digitization. Analog beamforming can support multiple beams but requires an additional phase adjustment channel per beam. For example, to create a 100 beam system would multiply the number of RF phase shifters for a 1 beam system by 100, so the cost consideration of data converters vs. phase adjustment ICs can change depending on the number of beams. Similarly, the power dissipation is usually lower for an analog beamforming approach that can utilize passive phase shifters but as the number of beams increases, the power dissipation will increase as well if additional gain stages are needed to drive the distribution network. A common compromise is a hybrid beamforming approach where there are subarrays of analog beamforming followed by some digital combination of the subarray signals. This is an area of growing interest in the industry and will continue to evolve in the years to come.

Semiconductor Technology

A standard pulsed radar system transmits a signal that can reflect off an object while the radar waits for the return pulse to map the field of view of the antenna. In past years, this antenna front-end solution would have discrete components, likely based in gallium arsenide technology. The IC components used as the building blocks for these phased array antennas are shown in Figure 4. They consist of a phase shifter to adjust the phase of each antenna element (which ultimately steers the antenna), an attenuator that can taper the beam, a power amplifier used for transmitting a signal, and a low noise amplifier used to receive a signal, as well as a switch to toggle between transmit and receive. In past implementations, each of these ICs could be housed in a 5 mm × 5 mm package, or more advanced solutions could have an integrated monolithic single-channel GaAs IC to achieve this functionality.

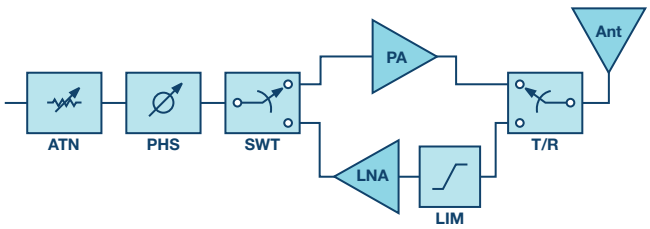

Figure 4. An example of a typical RF front end of a phased array antenna.

The recent proliferation of phased array antennas has been aided by semiconductor technology. The advanced nodes in SiGe BiCMOS, SOI (silicon-on-insulator), and bulk CMOS have combined digital circuitry to control the steering in the array, as well as the RF signal path to achieve the phase, and amplitude adjustment into a single IC. It's possible today to achieve multichannel beamforming ICs that adjust gain and phase in a 4-channel configuration with up to 32 channels aimed at millimeter wave designs. In some lower power examples, a silicon-based IC could be a monolithic solution for all functions above. In high power applications, gallium nitride-based power amplifiers have significantly increased the power density to fit into the unit cell of phased array antennas that would have been traditionally served by traveling wave tube (TWT)-based PAs or relatively low power GaAs-based PAs. In airborne applications, we are seeing a trend to flat panel architectures with the power added efficiency (PAE) benefits of GaN technology. GaN has also enabled large ground-based radars to move to phased array-based antenna technology from a dish antenna driven by a TWT. We are now able to have monolithic GaN ICs capable of delivering over 100 W of power with over 50% PAE. Combining this level of PAE with the low duty cycle of radar applications size, weight, and cost of the antenna array. The additional benefit beyond the pure power capability of GaN is the size reduction compared to existing GaAs IC solutions. Comparing a 6 W to 8 W GaAs power amplifier at X-band to a GaN-based solution reduces the footprint by 50% or more. This footprint reduction is significant when trying to fit these electronics into the unit cell of a phased array antenna.

Analog Devices Analog Phased Array ICs

Analog Devices has developed integrated analog beamforming ICs aimed at supporting a range of applications including radar, satellite communications, and 5G telecommunication. The ADAR1000 X-/Ku-band beamforming IC is a 4-channel device covering 8 GHz to 16 GHz operating in time division duplex (TDD) mode with the transmitter and receiver integrated into one IC. This is ideal for X-band radar applications as well as Ku-band satcom, where the IC can be configured to operate in transceiver-only or receiver-only mode. The 4-channel IC is housed in a 7 mm × 7 mm QFN surface-mount package for easy integration into flat panel arrays dissipating only 240 mW/channel in transmit mode and 160 mW/channel in receive mode. The transceiver and receiver channels are brought directly, externally designed to mate with a front-end module (FEM) that Analog Devices offers. Figure 5 shows the gain and phase control with full 360 phase coverage where phase steps less than 2.8° are possible, as well as better than 31 dB of gain control. The ADAR1000 contains on-chip memory to store up to 121 beam states where one state contains all phase and gain settings for the entire IC. The transmitter delivers an approximately 19 dB gain with 15 dBm of saturated power where the receive gain is approximately 14 dB. Another key metric is the phase change over gain control, which is approximately 3° over 20 dB of range. Similarly, the gain change with phase control is about 0.25 dB over the entire 360° phase coverage, easing the calibration challenges.

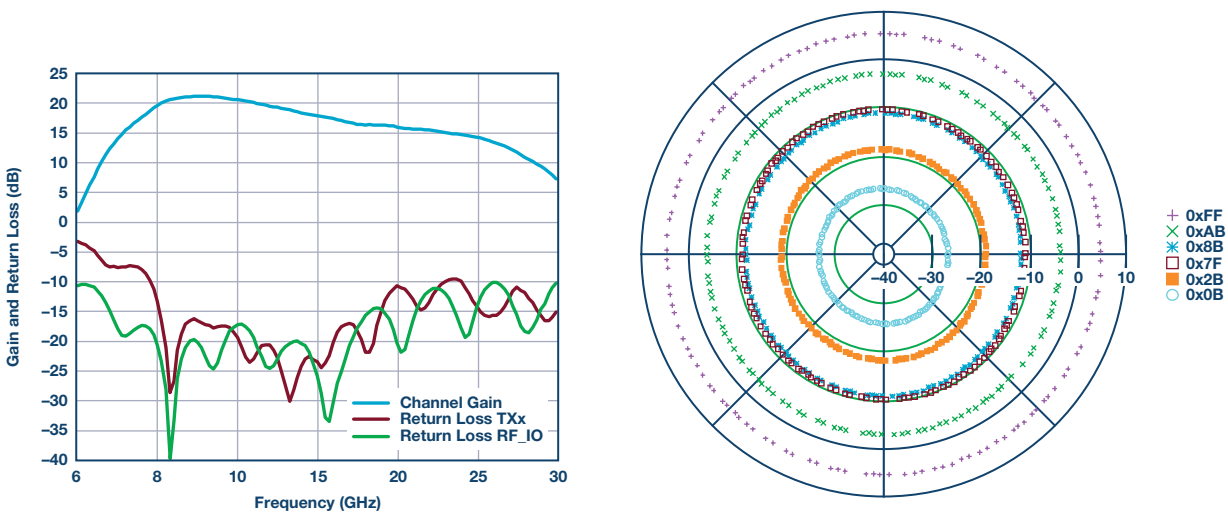

Figure 5. ADAR1000 Tx gain/return loss and phase/gain control, with frequency = 11.5 GHz.

This beamforming IC is developed for analog phased array applications or hybrid array architectures that combine some digital beamforming with analog beamforming. Analog Devices offers a complete solution from antenna to bits, including the data converters, frequency conversion, and analog beamforming IC, as well as the front-end module. The combined chipset allows Analog Devices to combine functionality and optimize the ICs appropriately to more easily implement an antenna design for our customers.

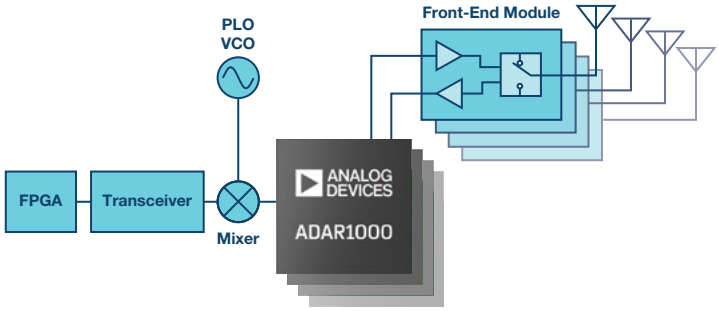

Figure 6. Learn more about ADI's phased array capabilities at analog.com/phasedarray.

Keith Benson [keith.benson@analog.com] graduated from the University of Massachusetts, Amherst with a B.S.E.E. in 2002 and from the University of California, Santa Barbara with an M.S.E.E. in 2004. He spent much of his early career at Hittite Microwave designing ICs used in RF wireless electronics. He then moved to manage a team of IC design engineers focusing on wireless communication links. In 2014, Hittite Microwave was acquired by Analog Devices where Keith became a product line director for RF/microwave amplifiers and phased array ICs. Keith currently holds three U.S. patents related to novel amplifier techniques.

Keith Benson

Also by this Author

GaN Breaks Barriers—RF Power Amplifiers Go Wide and High:

Volume 51, Number 3

Simple Battery Charger ICs for Any Chemistry

By **Steve Knoth**

Background

It is common for many battery-powered devices to require a wide variety of charging sources, battery chemistries, voltages, and currents. For example, industrial, high end, feature-rich consumer, medical, and automotive battery charger circuits demand higher voltages and currents as newer large-battery packs are emerging for all types of battery chemistries. Furthermore, solar panels with wide-ranging power levels are being used to power a variety of innovative systems containing rechargeable sealed lead acid (SLA) and lithium-based batteries. Examples include crosswalk marker lights, portable speaker systems, trash compactors, and even marine buoy lights. Moreover, some lead acid (LA) batteries found in solar applications are deep cycle batteries capable of surviving prolonged, repeated charge cycles, in addition to deep discharges. A good example of this is in deep sea marine buoys, where a 10-year deployment life is a prerequisite. Another example is off-grid (that is, disconnected from the electric utility company) renewable energy systems such as solar or wind power generation, where system uptime is paramount due to proximity access difficulties.

Even in nonsolar applications, recent market trends imply a renewed interest in high capacity SLA battery cells. Automotive, or starting, SLA cells are inexpensive from a cost/power output perspective and can deliver high pulse currents for short durations, making them an excellent choice for automotive and other vehicle starter applications. Embedded automotive applications have input voltages >30 V, with some even higher. Consider a GPS location system used as an antitheft deterrent; a linear charger with the typical 12 V input stepping down to 2-in-series Li-Ion battery (7.4 V typical) and needing protection to much higher voltages could be valuable for this application. Deep cycle LA batteries are another technology popular in industrial applications. They have thicker plates than automotive batteries and are designed to be discharged to as low as 20% of their total capacity. They are normally used where power is required over a longer time constant such as fork lifts and golf carts. Nevertheless, like their Li-Ion counterpart, LA batteries are sensitive to overcharging, so careful treatment during the charging cycle is very important.

Current integrated circuit (IC)-based solutions cover just a fraction of the many possible combinations of input voltage, charge voltage, and charge current. A cumbersome combination of ICs and discrete components has routinely been used to cover most of the remaining, more difficult combinations and topologies. That wasn't until, in 2011, when Analog Devices addressed and simplified this market application space with its popular 2-chip charging solution consisting of the LTC4000 battery charging controller IC mated with a compatible, externally compensated dc-to-dc converter.

Switching vs. Linear Chargers

Traditional linear topology battery charger ICs were often valued for their compact footprints, simplicity, and low cost. However, drawbacks of these linear chargers include a limited input and battery voltage range, higher relative current consumption, excessive power dissipation, limited charge termination algorithms, and lower relative efficiency (efficiency ~ [VOUT/VIN] × 100%). On the other hand, switch-mode battery chargers are also popular choices due to their flexible topology, multichemistry charging, high charging efficiencies (which minimize heat to enable fast charge times), and wide operating voltage ranges. Nevertheless, some of the drawbacks of switching chargers include relatively high cost, more complicated inductor-based designs, potential noise generation, and larger footprint solutions. Modern LA, wireless power, energy harvesting, solar charging, remote sensor, and embedded automotive applications have been routinely powered by high voltage linear battery chargers for the reasons stated above. However, an opportunity exists for a more modern switch-mode charger that negates the associated drawbacks.

An Uncomplicated Buck Battery Charger

Some of the tougher challenges a designer faces at the outset of a charging solution are the wide range of input sources combined with a wide range of possible batteries, the high capacity of the batteries needing to be charged, and a high input voltage.

Input sources are as wide as they are variable, but some of the more complicated ones that deal with battery charging systems are: high powered wall adapters with voltages spanning from 5 V to 19 V and beyond, rectified 24 V ac systems, high impedance solar panels, and car and heavy truck/Humvee batteries. Therefore, it follows that the combination of battery chemistries possible in these systems—lithium-based (Li-Ion, Li-Polymer, lithium-iron phosphate (LiFePO4)) and LA-based—increases the permutations even more, thus making the design even more daunting.

Due to IC design complexity, existing battery charging ICs are primarily limited to step-down (or buck) or the more complex SEPIC topologies. Add solar charging capability to this mix and you open a variety of other complexities. Finally, some existing solutions charge multiple battery chemistries, some with onboard termination. However, up until now, no single IC charger has provided all of the necessary performance features to solve these issues.

New, Feature-Rich Compact Chargers

A buck IC charging solution that solves the problems discussed above would need to possess most of the following attributes:

- Wide input voltage range
- Wide output voltage range to address multiple battery stacks
- Flexibility—ability to charge multiple battery chemistries
- Simple and autonomous operation with onboard charge termination algorithms (no microprocessor needed)
- High charge current for fast charging, large, high capacity cells
- Solar charging capability
- Advanced packaging for improved thermal performance and space efficiency

When ADI developed the popular LTC4000 battery charging controller IC (which works in conjunction with an externally compensated dc-to-dc converter to form a powerful and flexible 2-chip battery charging solution) a few years ago, it greatly simplified the existing solution, which was quite convoluted and cumbersome. To enable PowerPath control, step-up/down functionality, and input current limiting, solutions consisted of a buck-boost dc-to-dc switching regulator or a buck-switching regulator charger controller paired with a front-end boost controller, and a microprocessor, plus several ICs and discrete components. Key drawbacks included limited operating voltage range, no solar panel input capability, an inability to charge all battery chemistries, and no onboard charge termination. Fast forward to the present and now some simpler, and much more compact, monolithic solutions are available to solve these problems. The LTC4162 and LTC4015 buck battery chargers from Analog Devices both provide single-chip step-down charging solutions, with varying charge current levels and a full feature set.

The LTC4162 Battery Charger

The LTC4162 is a highly integrated, high voltage multichemistry synchronous monolithic step-down battery charger and PowerPath manager with onboard telemetry functions and optional maximum power point tracking (MPPT). It efficiently transfers power from a variety of input sources, such as wall adapters, backplanes, and solar panels, to charge a Li-Ion/polymer, LiFePO4, or LA battery stack while still providing power to the system load up to 35 V. The device provides advanced system monitoring and PowerPath management, plus battery health monitoring. While a host microcontroller is required to access the most advanced features of the LTC4162, the use of the I²C port is optional. The main charging features of the product can be adjusted using pin-strap configurations and programming resistors. The device offers precision ±5% charge current regulation up to 3.2 A, ±0.75% charge voltage regulation, and operates over a 4.5 V to 35 V input voltage range. Applications include portable medical instruments, USB power delivery (USB-C) devices, military equipment, industrial handhelds, and ruggedized notebooks/tablet computers.

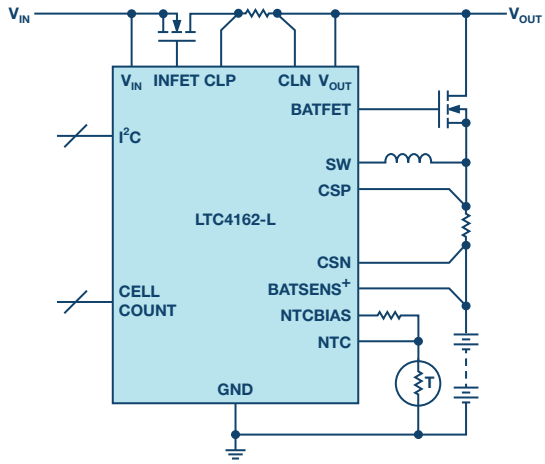

Figure 1. Typical application circuit for the LTC4162-L.

The LTC4162 (see Figure 1) contains an accurate 16-bit analog-to-digital converter (ADC) that continuously monitors numerous system parameters on command, including input voltage, input current, battery voltage, battery current, output voltage, battery temperature, die temperature, and battery series resistance (BSR). All system parameters can be monitored via a two-wire I²C interface, while programmable and maskable alerts ensure that only the information of interest causes an interrupt. The device's active maximum power point tracking algorithm globally sweeps an input undervoltage control loop and selects an operating point to maximize power extraction from solar panels and other resistive sources. Further, its built-in PowerPath topology decouples the output voltage from the battery, thereby allowing a portable product to start up instantly when a charging source is applied under very low battery voltage conditions. The LTC4162's onboard charging profiles are optimized for a variety of battery chemistries including Li-Ion/polymer, LiFePO4, and LA. Both charge voltage and charge current can be automatically adjusted based on battery temperature to comply with JEITA guidelines or be customized. For LA batteries, a continuous temperature curve automatically adjusts the battery voltage based on the ambient temperature. For all chemistries, an optional die junction temperature regulation system can be engaged, preventing excess heating in space constrained or thermally challenged applications. See Figure 2 for Li-Ion charging efficiency performance.

Finally, the LTC4162 is housed in a 28-lead, 4 mm × 5 mm QFN package with an exposed metal pad for excellent thermal performance. E- and I-grade devices are guaranteed for operation from –40°C to +125°C.

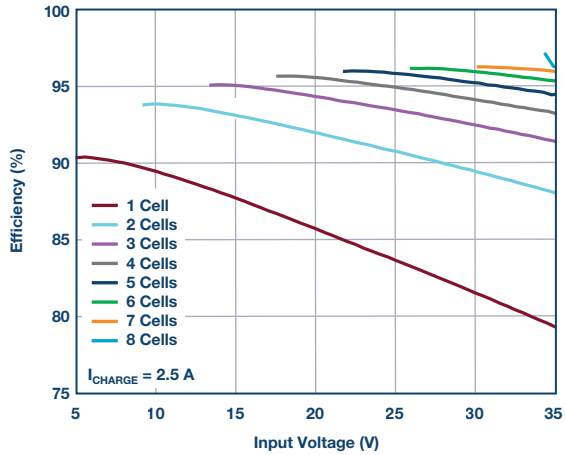

Figure 2. Li-Ion charging efficiency vs. input voltage by cell count.

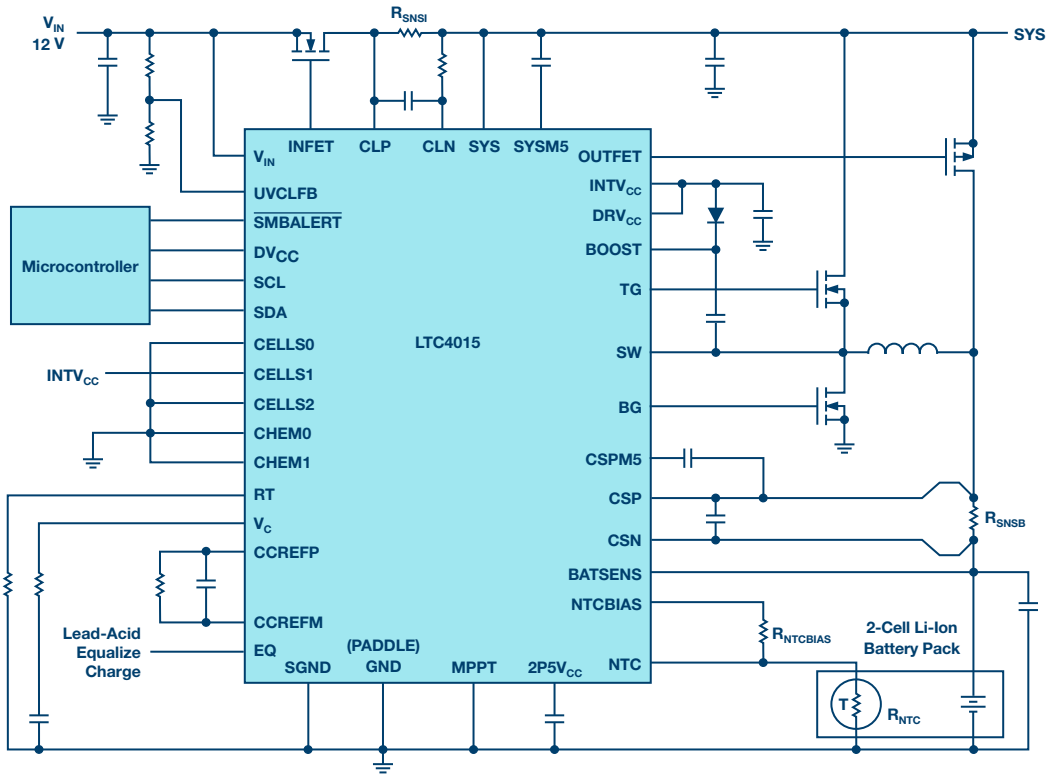

Figure 3. 12 V_{IN} to 2-cell Li-Ion 8 A buck battery charger circuit.

What if Higher Current Is Needed?

The LTC4015 is also a highly integrated, high voltage, multichemistry, synchronous step-down battery charger with onboard telemetry functions. However, it features a controller architecture with offboard power FETs for higher charge current capability (up to 20 A or more depending on external components chosen). The device efficiently supplies power from an input source (wall adapter, solar panel, etc.), to a Li-Ion/polymer, LiFePO4, or LA battery. It provides advanced system monitoring and management functionality, including battery coulomb counting and health monitoring. While a host microcontroller is required to access the most advanced features of the LTC4015, the use of its I²C port is optional. The main charging features of the product can be adjusted using pin-strap configurations and programming resistors.

The LTC4015 offers precision ±2% charge current regulation up to 20 A, ±1.25% charge voltage regulation and operation over a 4.5 V to 35 V input voltage range. Applications include portable medical instruments, military equipment, battery backup applications, industrial handhelds, industrial lighting, ruggedized notebooks/tablet computers, and remote powered communication and telemetry systems.

The LTC4015 also contains an accurate 14-bit ADC, as well as a high precision coulomb counter. The ADC continuously monitors numerous system parameters, including input voltage, input current, battery voltage, battery current, and reports battery temperature and BSR on command. By monitoring these parameters, the LTC4015 can report on the state of health of the battery, as well as its state of charge. All system parameters can be monitored via a two-wire I²C interface, while programmable and maskable alerts ensure that only the information of interest causes an interruption. The LTC4015's onboard charging profiles are optimized for each of a variety of battery chemistries including Li-Ion/polymer, LiFePO4, and LA. Configuration pins allow the user to select between several predefined charge algorithms for each battery chemistry, as well as several algorithms whose parameters can be adjusted via I²C. Both charge voltage and charge current can be automatically adjusted based on battery temperature to comply with JEITA guidelines, or even custom settings. See Figure 4 for LA charging efficiency performance. The LTC4015 is housed in a 5 mm × 7 mm QFN package with an exposed metal pad for excellent thermal performance.

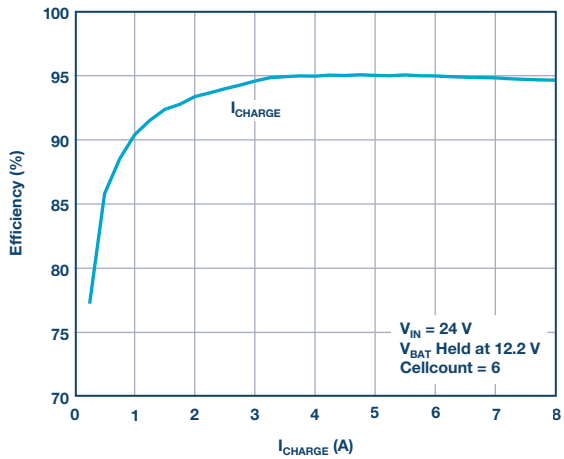

Figure 4. Lead acid charging efficiency with the LTC4015.

Space Savings, Flexibility, and Higher Power Levels

At equal power levels (for example, 3 A), because it is a monolithic device with integrated power MOSFETs, the LTC4162 can save up to 50% of the PCB area compared to the LTC4015. Since their feature sets are similar, the LTC4015 should be used when output currents are >3.2 A up to 20 A or more. None of the industry competing IC battery charger solutions offer the same high level of integration, nor can they generate the same power levels. Those that approach the charge current (2 A to 3 A) are limited to only a single battery chemistry (Li-Ion) or are limited in battery charge voltage (13 V maximum), and therefore do not offer the power levels nor the flexibility of the LTC4162 or LTC4015. Furthermore, when you consider

the number of external components required for the nearest competing monolithic battery charger solution, the LTC4162 offers up to 40% savings in PCB area footprint, making it an even more enticing choice for designs.

Solar Charging

There are many ways to operate a solar panel at its maximum power point (MPP). One of the simplest methods is to connect a battery to the solar panel through a diode. This technique relies on matching the maximum output voltage of the panel to the relatively narrow voltage range of the battery. When available power levels are very low (approximately less than a few tens of milliwatts), this may be the best approach. However, power levels are not always low. Therefore, the LTC4162 and LTC4015 utilize MPPT, a technique that finds the maximum power voltage (MPV) of a solar panel as the amount of incident light changes. This voltage can change drastically from 12 V to 18 V as the panel current changes over 2 or more decades of dynamic range. The MPPT circuit algorithm finds and tracks the panel voltage value that delivers the maximum charge current to the battery. The MPPT function not only continuously tracks the maximum power point, but it is also able to select the correct maximum on the power curve to increase power harvested from the panel during partial shade conditions when multiple peaks occur on the power curve. During periods of low light, a low power mode allows the charger to deliver a small charge current even if there is not enough light for the MPPT function to operate.

Conclusion

Analog Devices' newest powerful and full-featured battery charging and PowerPath manager ICs, the LTC4162 and LTC4015, simplify a very difficult high voltage and high current charging system. These devices efficiently manage power distribution between input sources, such as wall adapters, backplanes, solar panels, etc., and the charging of various battery chemistries, including Li-Ion/polymer, LiFePO4, and SLA. Their simple solution and compact footprints enable them to achieve high performance in leading-edge applications where only more complicated, older technology switching regulator-based topologies such as SEPIC were once the only option. This greatly simplifies the designer's task when it comes to medium-to-high power battery charger circuits.

Steve Knoth [steve.knoth@analog.com] is a senior product marketing engineer in Analog Devices' Power by Linear™ Group. He is responsible for all power management integrated circuit (PMIC) products, low dropout (LDO) regulators, battery chargers, charge pumps, charge pump-based LED drivers, supercapacitor chargers, low voltage monolithic switching regulators, and ideal diode devices. Prior to joining Analog Devices (formerly Linear Technology) in 2004, Steve held various marketing and product engineering positions since 1990 at Micro Power Systems, Analog Devices, and Micrel Semiconductor. He earned his bachelor's degree in electrical engineering in 1988 and a master's degree in physics in 1995, both from San Jose State University. Steve also received an M.B.A. in technology management from the University of Phoenix in 2000. In addition to enjoying time with his kids, Steve can be found tinkering with pinball and arcade games or muscle cars, and buying, selling, and collecting vintage toys, movie, sports, and automotive memorabilia.

Steve Knoth

Also by this Author:

Vehicle Tracking Systems: Anytime, Anywhere, Anyhow

Volume 52, Number 1

Rarely Asked Questions—Issue 161 A New Spin on a Classic Architecture: Achieving a Fully Differential Output Using Single-Ended Instrumentation Amplifiers

By **Rusty Juszkiewicz**

Question:

Can we generate a differential output signal using instrumentation amplifiers?

Answer:

As the drive for precision moves forward, fully differential signal chain components are desired for their performance with one of the major advantages being noise rejection that can be picked up by signal routing. Since outputs pickup this noise, error will be common and therefore attenuated further in the signal chain. Also, a differential signal can achieve twice the signal range as a single-ended signal on the same supply. Therefore, the signal-to-noise ratio (SNR) is higher with a fully differential signal. The classic three op amp instrumentation amplifier (in-amp) has many advantages, including common-mode signal rejection, high input impedance, and precise (adjustable) gain; however, it falls short when a fully differential output signal is required. A few methods have been used to achieve a fully differential in-amp using standard components. However, they come with their own disadvantages.

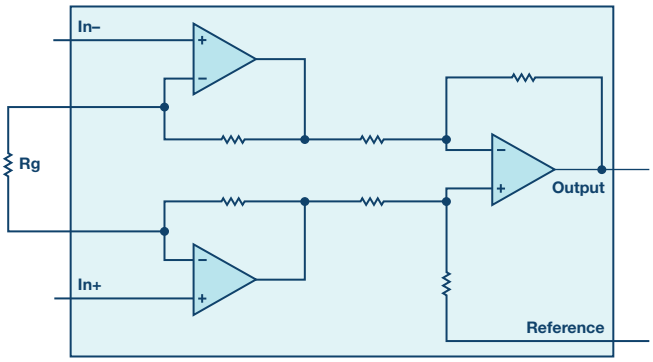

Figure 1. Classical instrumentation amplifier.

One technique is to drive the reference pin with an op amp with the positive input at common mode and the negative input at the center of two matched resistors that connect the outputs together. This configuration uses the in-amp output as the positive output and the op amp output as the negative output. Since the two outputs are different amplifiers, mismatches in dynamic performance between these amplifiers can drastically affect the overall circuit performance. Also, the matching of the two resistors causes the output common mode to move with the output signal, which can result in distortion. When designing this circuit, stability must be considered when choosing amplifiers and a feedback capacitor on the op amp may be required, which limits the overall bandwidth of the circuit. Lastly, the gain range of this circuit is based on the in-amp. Therefore, a gain of less than one is not achievable.

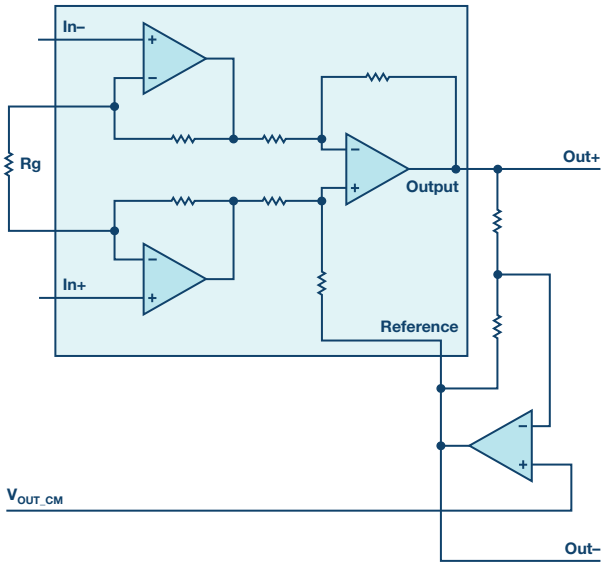

Figure 2. Using an external op amp to generate the inverting output.

Another technique is to connect two in-amps in parallel with the inputs switched. This configuration has better matched driving circuits and frequency response than the previous circuit. However, it is not capable of gains less than two. This circuit also requires precision matching gain resistors to achieve a purely differential signal. Mismatches in these resistors result in shifts in the output common-mode level with the same implications as the previous architecture.

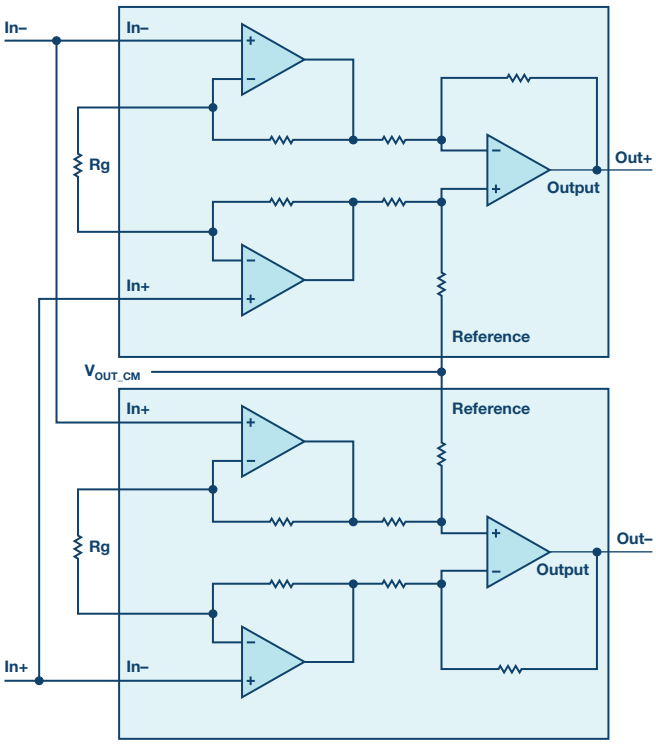

Figure 3. Using a second instrumentation amplifier to generate the inverting output.

These two approaches have limitations on the achievable gain, as well as the requirement for matched components.

The New Cross-Connection Technique

By cross connecting two in-amps as seen in Figure 4, this new circuit provides a fully differential output with precise gain or attenuation using a single gain resistor. By connecting the two reference pins together, the user is able to adjust the output common mode as needed.

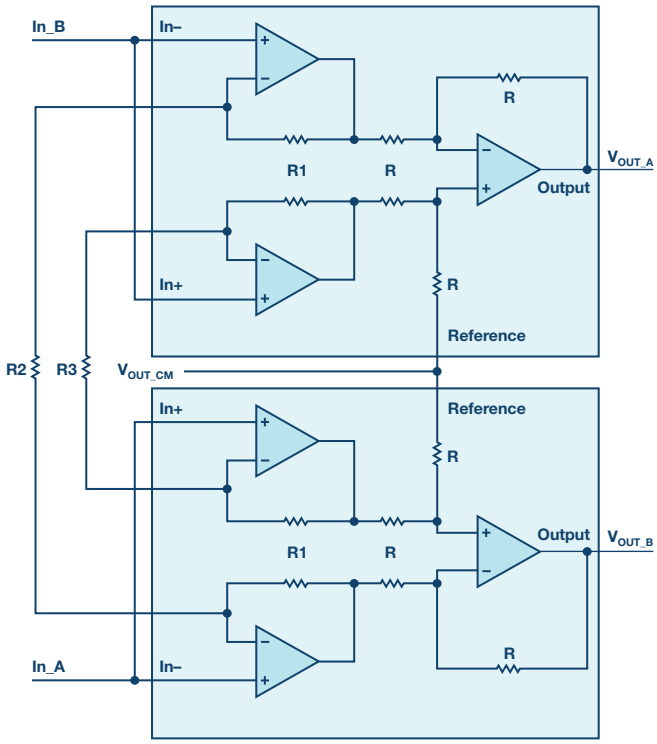

Figure 4. Cross-connection technique—the solution to generate a differential instrumentation amplifier output.

The gain for In_A is derived in the following equations. Since the input voltage appears at the positive terminals of the input buffers of in-amp 2, and the other side of the resistors R2 and R3 are at 0 V, the gain for those buffers follows the formula for a noninverting op amp configuration. Similarly, for the input buffers of in-amp 1, the gain follows the inverting op amp configuration. Since all resistors in the difference amplifier are matched, the gain from the output of the buffers is in unity.

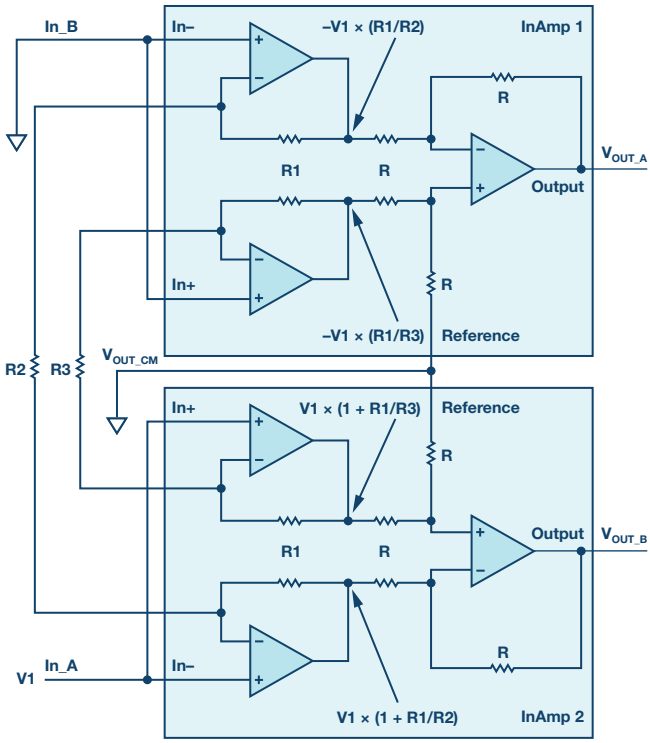

Figure 5. Matched resistors inside the in-amps are the key for the cross-connection technique.

$$V_{OUT\_A} = -V1 \times (R1/R3 - R1/R2)$$
$$V_{OUT\_B} = V1 \times (R1/R3 - R1/R2)$$

By symmetry, if a voltage V2 is applied at In_B with In_A at ground, the result would be the following:

$$V_{OUT\_A} = V2 \times (R1/R3 - R1/R2)$$
$$V_{OUT\_B} = -V2 \times (R1/R3 - R1/R2)$$

Combining the two results yields the gain of the circuit.

$$V_{IN} = In\_A - In\_B = V1 - V2$$
$$V_{OUT} = V_{OUT\_A} - V_{OUT\_B}$$
$$Gain = 2 \times (R1/R2 - R1/R3)$$

The gain resistors R3 and R2 set the gain of the circuit and only one is needed to achieve a fully differential signal. The positive/negative output is determined depending on which resistor is installed. Not installing R3 would result in the second term in the gain equation going to zero. Therefore, the resulting gain is 2 × R1/R2. Not installing R2 would result in the first term in the gain equation going to zero. Therefore, the resulting gain is –2 × R1/R3. Another thing to note is that the gain is purely a ratio and therefore a gain less than one is achievable. Keep in mind that since R2 and R3 have opposite effects on the gain, including both gain resistors would put the first stage into a higher gain than output. This can exacerbate the offset at the output due to the first stage op amps if care is not taken when selecting the resistor values.

In order to demonstrate this circuit in use, two AD8221 in-amps were connected together. The data sheet lists R1 as 24.7 kΩ, so therefore a gain of one is achievable when R2 is 49.4 kΩ.

CH1 is the input signal at In_A, CH2 is $V_{OUT_}$A, and CH3 is $V_{OUT_}$B. The outputs A and B are matched and out of phase, and the difference is equal in magnitude to the input signal.

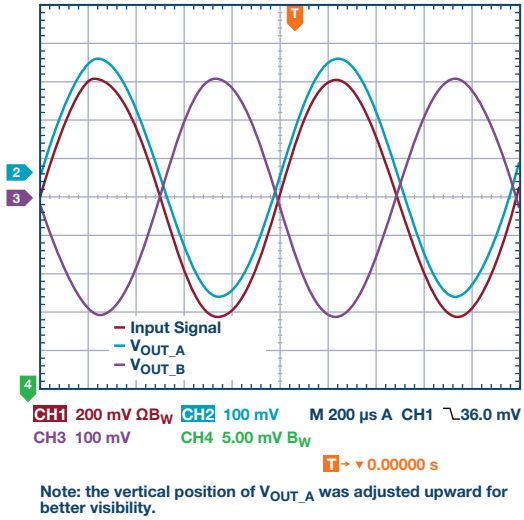

Figure 6. Measurement results with gain = 1 using the cross-connection technique to generate a differential in-amp output signal.

Next, by moving the 49.4 kΩ gain resistor from R2 to R3, the new gain for the circuit is –1. Now Out_A is out of phase with the input and the difference between outputs equals the input signal in magnitude.

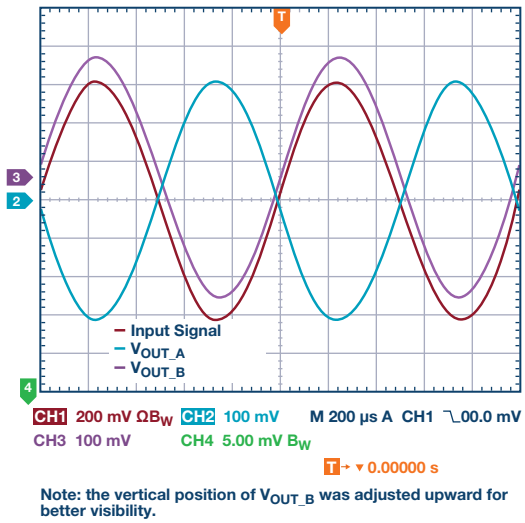

Figure 7. Measurement results with gain = –1 using the cross-connection technique to generate a differential in-amplifier output signal.

As mentioned earlier, one limitation of the other techniques is the inability to achieve attenuation. Following the gain equation, using R2 = 98.8 kΩ, the circuit attenuates the input signal by a factor of two.

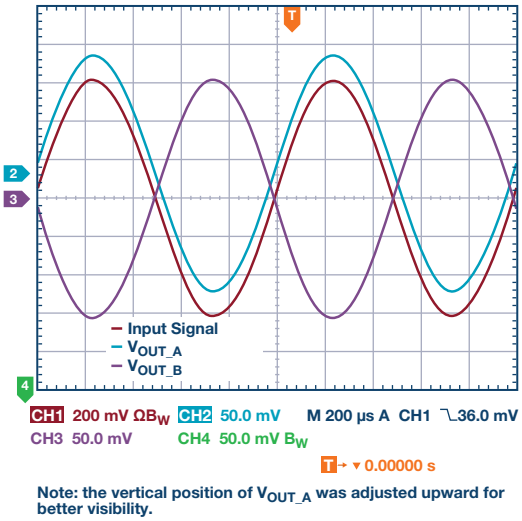

Figure 8. Measurement results with gain = 1/2 using the cross-connection technique to generate a differential in-amp output signal.

Lastly, to demonstrate a high gain, R2 = 494 Ω was chosen to achieve G = 100.

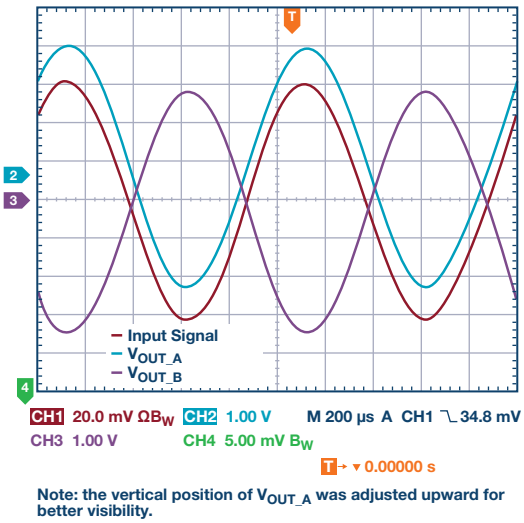

Figure 9. Measurement results with gain = 100 using the cross-connection technique to generate a differential instrumentation amplifier output signal.

The circuit performed as described by the gain equation. To achieve optimal performance, some precautions should be taken when using this circuit. The precision and drift of the gain resistor(s) will add to the gain error of the in-amp, therefore chose appropriate tolerances based on the error requirements. Since capacitance at the Rg pins of an in-amp can cause poor frequency performance, care should be taken at these nodes if high frequency performance is required. Also, mismatches in temperature between the two in-amps can cause offsets in the system due to offset drift, so care should be taken here with respect to layout and loading. Using a dual-channel in-amp like the AD8222 would facilitate overcoming these potential issues.

Conclusion

The cross-connection technique maintains the desired characteristics of an instrumentation amplifier while providing additional features. Although all examples discussed achieved a differential output, in the cross-connection circuit, the common mode of the outputs is not affected by mismatches in resistor pairs like the other architectures. Therefore, a truly differential output is always achieved. Also, as shown in the gain equation, differential signal attenuation is possible, which eliminates the need for a funnel amplifier where one would previously have been required. Lastly, the polarity of the output is determined by the location of the gain resistor (using R2 or R3), which adds more flexibility for the user.

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Rusty Juszkiewcz

Synchronization of Multiaxis Motion Control over Real-Time Networks

By **Jens Sorensen**, **Dara O'Sullivan**, and **Christian Aaen**

Abstract

Real-time deterministic Ethernet protocols, such as EtherCAT, have enabled synchronized operation of multiaxis motion control systems.[1] There are two aspects to this synchronization. First, the delivery of command and references between the various control nodes must be synchronized to a common clock and, second, the execution of the control algorithms and feedback functions must be synchronized to the same clock. The first kind of synchronization is well understood and an inherent part of the network controller. However, the second kind of synchronization has up to this point been neglected and is now a bottleneck when it comes to motion control performance.

This article presents novel concepts to synchronize motor drives all the way from a network controller and down the motor terminals and sensors. The presented technologies enable much improved synchronization that leads to significantly increased control performance.

Problem Statement and State of the Art

To define the limitations of state-of-the-art solutions, consider a 2-axis networked motion control system, as shown in Figure 1. A motion control master is sending commands and references across a real-time network to two servo controllers, with each servo controller constituting a slave node on the network. The servo controller itself consists of a network controller, a motor controller, a power inverter, and a motor/encoder.

The real-time network protocols employ different methods to synchronize slave nodes to the master, but an often used approach is to have a local synchronized clock at each node. This common understanding of time ensures references and commands for all servo axes are tightly synchronized. In other words, all network controllers on the real-time network are synchronized.

Typically, there are two interrupt lines between the network controller and the motor controller. The first notifies the motor controller when it is time to gather inputs and put them on the network. The second notifies the motor controller when to read data from the network. Following this approach, the data exchange between the motion controller and the motor controller happens in a synchronized manner and very high timing accuracy is possible. However, it is not enough to get synchronized data across to the motor controllers; the motor controllers must also be able to respond to the data in a synchronized way. Without this capability, the motor controllers cannot take advantage of the timing accuracy of the network. When it comes to responding to references and commands, the motor controller's I/Os pose a problem.

Each of the I/Os in a motor controller, such as pulse-width modulation (PWM) timers and ADCs, have an inherent delay and time quantization. As an example, consider the PWM timer generating gate drive signals for the power inverter, as shown in Figure 2. The timer generates gate signals by comparing reference Mx to an up-down counter. When Mx is changed by the control algorithm, the new duty cycle does not take effect until the

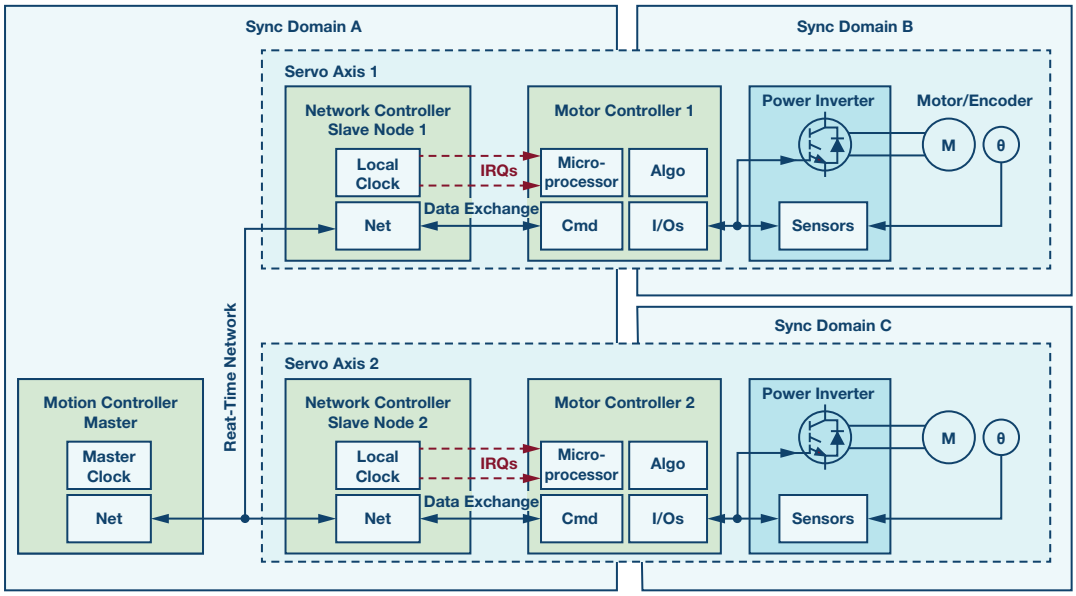

Figure 1. A typical 2-axis network motion control system.

next PWM period. This is equivalent to a zero-order hold effect meaning the duty cycle is only updated once per PWM period, T, or twice if double update mode is used.

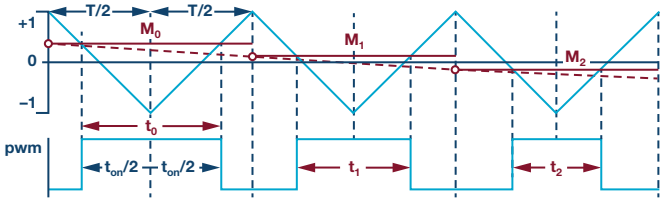

Figure 2. Update of duty cycle for PWM timer.

No matter how tightly the data exchange is synchronized on the real-time network, the time quantization of the PWM timer ends up being the determining factor in axis synchronization. When a new reference is received, it is not possible to respond to it until a new duty cycle takes effect. This introduces a time uncertainty of up to one PWM period, which is typically in the range of 50 µs to 100 µs. In effect, there will be an undefined and varying phase relationship between the network synchronization period and the PWM period. Compare this to a time uncertainty of sub-1 µs on the real-time network and it is clear that the I/Os of the motor controller play a crucial role when it comes to synchronizing motion control over a network. In fact, it is not the real-time network that determines the synchronization accuracy—rather it is the I/Os of the system.

Again referring to Figure 1, the system has three synchronization domains, A, B, and C, that are not tied together. They are effectively out of synchronization with a variable uncertainty of up to one PWM period.

Synchronization Uncertainty and Application Impact

The impact of timing uncertainty can be clearly seen in high performance multiaxis servo systems for applications like robotics and machining. The varying time offset between motor control axes at the I/O level has a direct and measurable impact on the final three-dimensional positioning accuracy of the robot or machine tool.

Consider a simple motion profile, as shown in Figure 3. In this example, the motor speed reference (red curve) is ramped up and then back down again. If the ramp rate is within the capability of the electromechanical system, the actual speed is expected to follow the reference. However, if there is a delay anywhere in the system, the actual speed (blue curve) will lag reference, which results is a position error, Δθ.

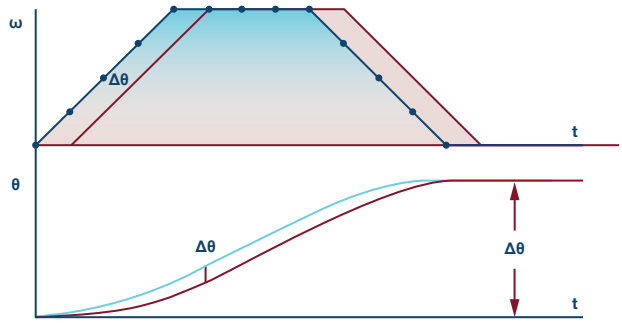

Figure 3. Effect of timing delay on position accuracy.

In multiaxis machines, a target position (x, y, z) is translated into angular axis profiles (θ1, ..., θn) according to the mechanical construction of the machine. The angular axis profiles define a sequence of equally time spaced position/velocity commands for each axis. Any difference in timing between the axes results in reduced accuracy of the machine. Consider the 2-axis example shown in Figure 4. A target path for the machine is described by a set of (x, y) coordinates. A delay causes a timing error on the command for the y-axis and the actual path ends up being irregular.

The impact of a constant delay may, in some cases, be minimized by proper compensation. More critical is a varying and unknown delay for which compensation is impossible. Furthermore, a varying delay results in varying control loop gain, which makes it difficult to tune the loop for optimal performance.

It should be noted that a delay anywhere in the system will cause inaccuracy in the precision of the machine. As a consequence, minimizing or eliminating delays enables increased productivity and end-product quality.

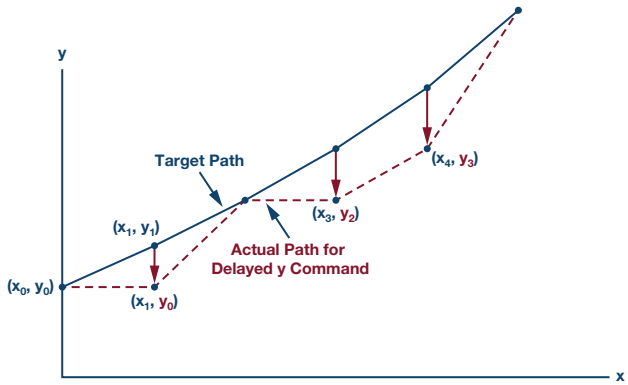

Figure 4. Effect of timing delay on position accuracy.

Synchronization and New Control Topologies

The traditional approach to motion control is shown in the top part of Figure 5. A motion controller, typically a PLC, sends position references (θ*) to a motor controller over a real-time network. The motor controller consists of three cascaded feedback loops with the inner loop controlling torque/current (T/i), the middle loop controlling speed (ω), and the other loop controlling position (θ). The torque loop has the highest bandwidth and the position loop has the lowest. Feedback from the plant is kept local to the motor controller and is tightly synchronized with the control algorithm and pulse-width modulator.

With this system topology, axes are synchronized through the exchange of position references between the motion and motor controllers, but the correlation to synchronization of the motor controller's I/O (feedback and PWM) only becomes an issue for very high precision applications such as CNC machining. The position loop often has fairly low bandwidth and is therefore less sensitive to synchronization of I/O. That means synchronization of nodes at a reference level typically gives acceptable performance even though the network and I/O are in different synchronization domains.

While the control topology shown at the top of Figure 5 is common, other control partitioning approaches in which position and/or speed loops are implemented at the motion controller side and speed/torque references are passed across the network are also used. Recent trends in the industry are indicating a move toward a new partitioning method, in which all of the control loops are moved away from the motor controllers to a powerful motion controller on the master side of the network (see the bottom of Figure 5). The data exchange on the real-time network is a voltage reference (v*) for the motor controller and plant feedback (i, ω, θ) for the motion controller. This control topology, which is enabled by powerful multicore PLCs and real-time networks, has several benefits. Firstly, the architecture is very scalable. Axes can also be easily added/removed without having to worry about the processing power of the motor controller. Secondly, increased precision is possible since both trajectory planning and motion control are done in one central place.

The new control topology has drawbacks, too. By removing the control algorithms from the motor controller, tight synchronization of code execution and I/O is lost. The higher the bandwidth of a control loop, the more of a problem the loss of I/O synchronization is. The torque/current loop is especially sensitive to synchronization.

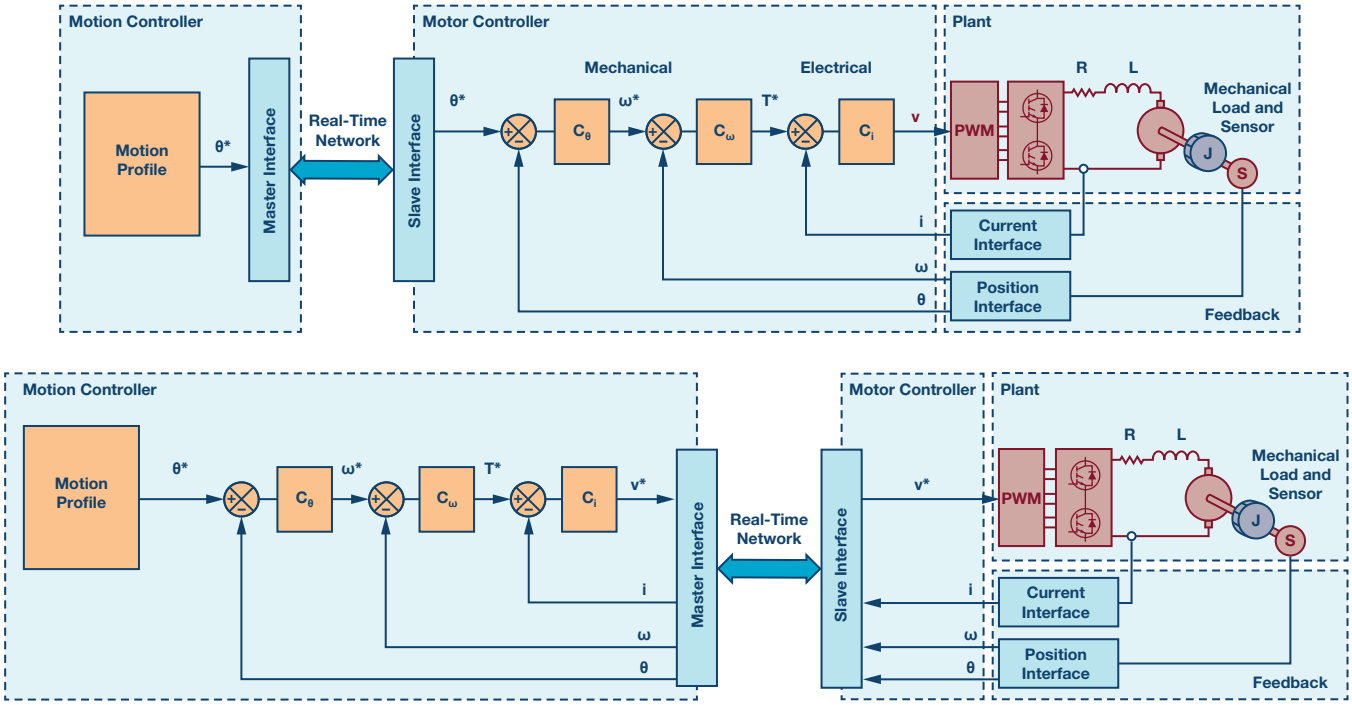

Figure 5. Traditional (top) and emerging (bottom) motion control topologies.

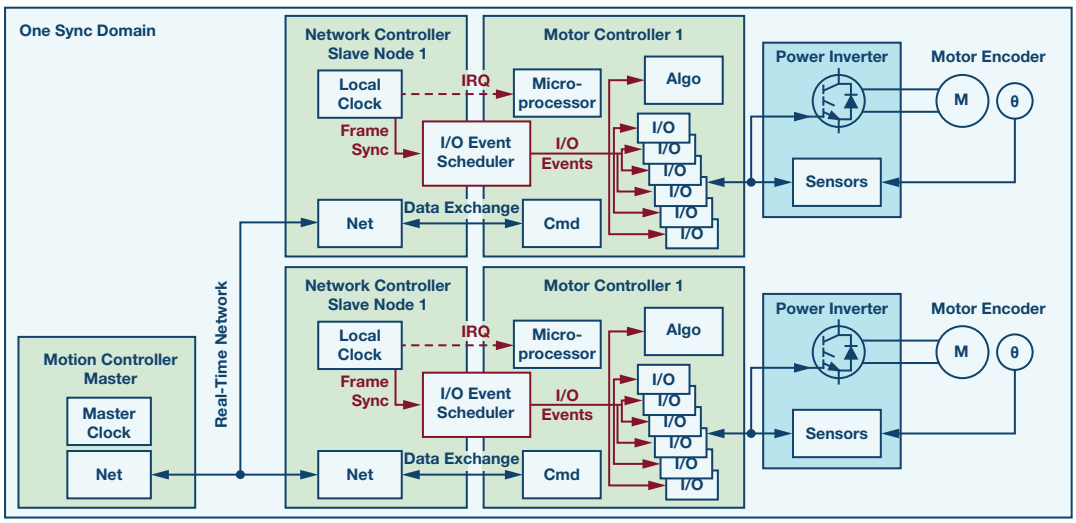

Figure 6. An I/O scheduler ties the sync domains together.

Proposed Solution

Moving the faster control loops to the motion controller creates a demand for synchronization all the way from the network master and down to the motor terminals.

The overall idea is to bring the I/Os of all axes into synchronization with the network so that everything runs in one sync domain. Figure 6 shows an I/O event scheduler, which sits between the network controller and the motor controller. The main function of the I/O event scheduler is to generate sync/reset pulses to all the peripherals so that they are kept in synchronism with the network traffic. The I/O event scheduler takes the frame sync signal, which is derived from the local clock of the network controller, and outputs appropriate hardware triggers for all I/Os that must be kept synchronized to the network.

Each I/O has its own set of timing/reset requirements, which means the I/O event scheduler must provide tailored triggers for each I/O. While trigger requirements differ, a general principle applies to all of them. Firstly, all triggers must be referenced to the frame sync. Secondly, there is a delay/offset associated with each trigger. This delay is related to the I/O's inherent delay—for example, the conversion time of an ADC or the group delay of a sinc filter. Thirdly, there is the response time of the I/O—for example, the transfer of data from an ADC. The I/O event scheduler knows the timing requirements of each I/O and adjusts the trigger/reset pulses to the local clock continuously. The principle behind generating each output pulse of the I/O event scheduler is summarized in Figure 7.

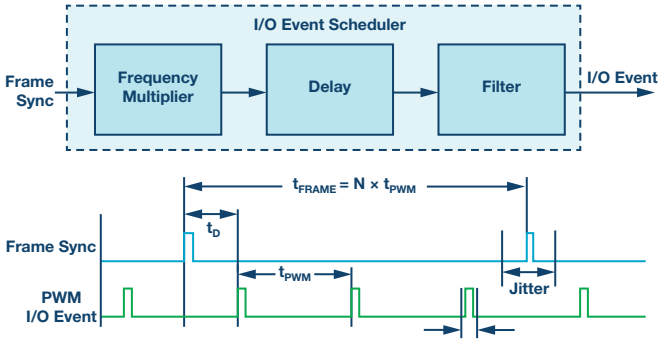

Figure 7. The I/O scheduler generates trigger pulses.

In most networked motion control systems, the frame rate, and hence the frame sync rate, is equal to or lower than the PWM update rate of the motor controller. This means that the I/O event scheduler must provide at least one and possibly several trigger pulses per frame period. For example, if the frame rate is 10 kHz and the PWM rate is 10 kHz, the I/O event scheduler must provide 1 trigger pulse per network frame and, similarly, if the frame rate is 1 kHz and the PWM rate is 10 kHz, the I/O event scheduler must provide 10 trigger pulses per network frame. This is equivalent to the frequency multiplier in Figure 7. A delay, t_D, is applied to each synchronization pulse to compensate for the inherent delay of each I/O. The final element of the I/O event scheduler is an intelligent filtering function. On every network there is some jitter on the traffic. The filter reduces the jitter on trigger pulses and also ensures the rate of change of frame sync frequency is limited.

The bottom half of Figure 7 shows an example timing diagram for PWM synchronization. Note in this example how the frame sync frequency is a multiple of the PWM frequency and how the jitter on the I/O trigger signal is reduced.

Implementation

Figure 8 shows an example of the proposed synchronization scheme that has been implemented and tested in a networked motion control system. The network master is a Beckhoff CX2020 PLC that is connected to a PC for development and deployment of the PLC program. The protocol of the real-time network (red arrows) is EtherCAT.

The main elements of the motor controller are the fido5200 and ADSP-CM408, both from Analog Devices. Together the two provide a highly integrated chipset for a network connected motor drive.

fido5200 is a real-time Ethernet multiprotocol (REM) switch with two Ethernet ports. It provides a flexible interface between a host processor and the industrial Ethernet physical layer. fido5200 includes a configurable timer control unit (TCU) that makes it possible to implement advanced synchronization schemes for the various industrial Ethernet protocols. Additional functions like input capture and the output of square wave signals can also be realized via dedicated timer pins. Timer input/output are kept in phase with the synchronized local time and therefore with the network traffic. This makes it possible to synchronize not only the I/O of a single slave node, but the slave nodes across the whole network.

The REM switch has two Ethernet ports and hence connects to two Phys (PHY1 and PHY2). This topology supports both ring and line networks. However, in the experimental setup, only one slave node is used for illustration and only one Ethernet port is active.

The REM switch communicates with a host processor though a parallel memory bus, which ensures high throughput and low latency.

The host processor used to realize the motor controller is the ADSP-CM408. It is an application specific processor based on an ARM® Cortex®-M4F core to implement control and application functions. The processor includes peripherals to support industrial control applications such as timers for PWM inverter control, ADC sampling, and position encoder interfaces. To keep all peripherals in sync with the network, a flexible trigger routing unit (TRU) is utilized. The TRU redirects the triggers generated by the fido5200's TCU to all timing critical peripherals on the ADSP-CM408. These are the pulse-width modulator, sinc filter for phase current measurement, ADC, and absolute encoder interface. The principles behind synchronizing I/Os are illustrated in Figure 9.

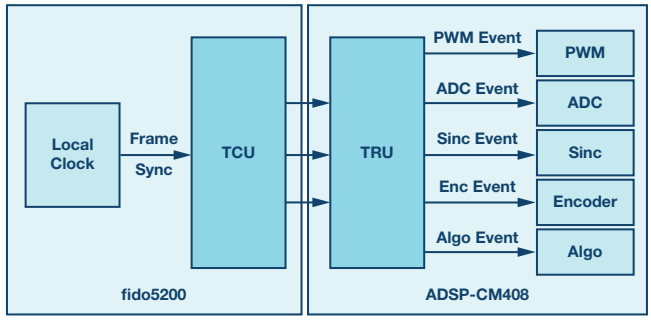

Figure 9. Generating synchronization events for I/Os.

In Figure 9, notice how the I/O event scheduler is realized using the TCU on the REM switch and the TRU on the motor control processor. In other words, the function is implemented across two integrated circuits.

The feedback for the motor controller is phase current and the rotor position from a 3-phase servo motor. Phase current is measured using isolated Σ-Δ ADCs and the rotor position is measured with an EnDat absolute encoder. Both the Σ-Δ ADCs and the encoder interface directly to ADSP-CM408 without the need for any external FPGA or CPLD.

The PWM switching frequency is 10 kHz and the control algorithm is executed once per PWM period. As discussed in this article, the TCU provides synchronization pulses to ADSP-CM408 once per PWM period.

Experimental Results

A photo of the experimental setup is shown in Figure 10. To illustrate the synchronization of the system, the PLC was setup to run a program with a task time of 200 µs. The task time also determines the frame rate on the EtherCAT network. The motor controller runs with a PWM and control update period of 100 µs (10 kHz) and therefore needs synchronization pulses to happen at this rate. The result is shown in Figure 11.

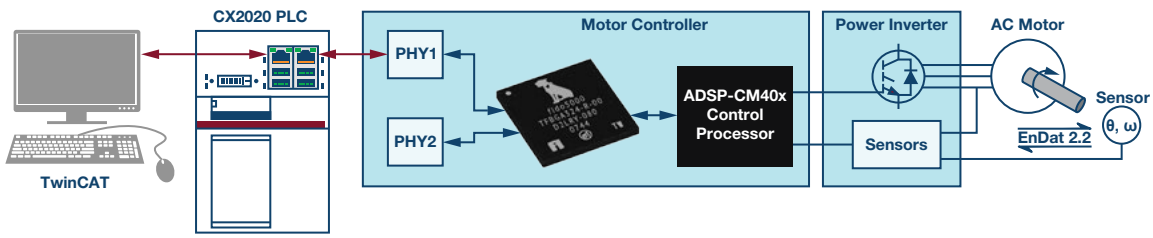

Figure 8. Implementation of a synchronization scheme.

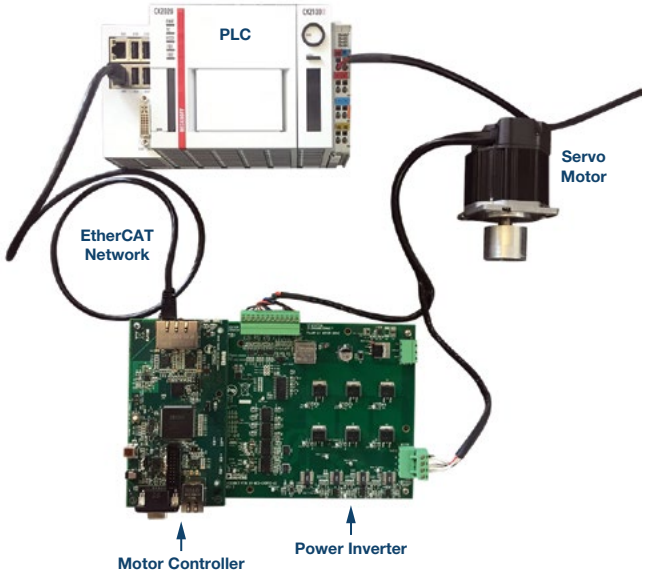

Figure 10. Implementation of a synchronization scheme.

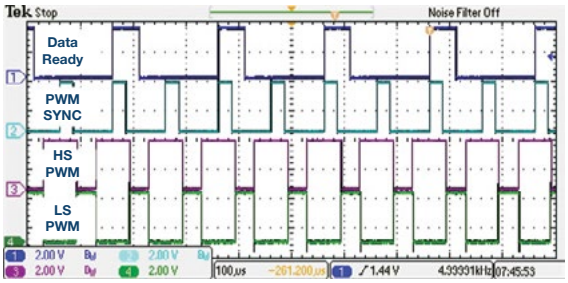

Figure 11. Generating synchronization events for I/Os.

The signal **Data Ready** indicates when the REM switch has made network data available to the motor control application. The signal is asserted every 200 µs, which corresponds to the EtherCAT frame rate. The PWM sync signal is also generated by the REM switch and used to keep the I/O of the motor controller in synchronism with the network traffic. Since the PWM period is 100 µs, the REM switch schedules two PWM sync pulses per EtherCAT frame. The lower two signals on Figure 11, HS PWM and LS PWM, are high-side and low-side PWM for one of the motor phases. Notice how the PWM signals are synchronized to the network traffic.

Summary

Real-time Ethernet is widely used in motion control systems and some protocols achieve time synchronization with an accuracy of sub-1 µs. However, the synchronization only involves data traffic between the network master and slaves. Existing network solutions do not include synchronization of motion control I/O, which limits the achievable control performance.

The synchronization scheme proposed in this article enables synchronization all the way from the network master right down to the motor terminals. Because of much improved synchronization, the proposed scheme offers significant improvement in control performance. The proposed scheme also offers seamless synchronization across multiple axes. Axes can easily be added and the synchronization tailored to the individual motor controller.

The synchronization is based on an I/O event scheduler, which resides between the network controller and the motor controller. The I/O event scheduler is programmable on the fly and can be conditioned to minimize the effect of jitter/frequency changes.

The article's proposed scheme has been verified in an experimental setup and results were presented. EtherCAT was used as the communication protocol in the experiment. However, the ideas presented apply to any real-time Ethernet protocol.

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[1] Jie Ma. "Multi-DOF Motion Control System Design and Realization Based on EtherCAT." 2016 Sixth International Conference on Instrumentation and Measurement, Computer, Communication, and Control, July 2016.

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Christian Aaen

High Performance Data Converters for Medical Imaging Systems

By **Anton Patyuchenko**

The discovery of X-radiation by Wilhelm Conrad Röntgen in 1895 earned him the first Nobel Prize in Physics and laid the historical foundations for the field of medical imaging. Since then it has developed into an extensive scientific discipline that, in its widest sense, designates diverse techniques for noninvasive visualization of the internal aspects of the body.

This article considers the main types of modern medical imaging systems that utilize fundamentally different physical principles and processing techniques but have one thing in common—an analog data acquisition front end for signal conditioning and conversion of raw imaging data into a digital domain.

This tiny, functional front-end block is hidden deep inside a complex machine. However, it is its performance that has a crucial impact on the resulting image quality of the complete system. Its signal chain comprises a sensing element, a low noise amplifier (LNA), a filter, and an analog-to-digital converter (ADC), of which the latter is the main subject of this article.

The data converter constitutes the most demanding challenges imposed by medical imaging on the electronics design in terms of required dynamic range, resolution, accuracy, linearity, and noise. This article discusses these design challenges in the context of different imaging modalities and gives an overview of advanced data converters and integrated solutions needed to make them work at optimum levels.

Digital Radiography

Digital radiography (DR) is based on physical principles common to all conventional absorption-based radiography systems. The X-rays passing through the body are attenuated by tissues of different radiographic opacity and projected on a flat panel detector system, as shown schematically in Figure 1. The detector converts the X-ray photons into electrical charges that are proportional to the energy of the incident particles. The resulting electrical signal is amplified and converted into a digital domain to produce an accurate digital representation of the X-ray image. The quality of this image depends on the signal sampling in the spatial and intensity dimensions.

In the spatial dimension, the minimum sampling rate is defined by the pixel matrix size of the detector and the update rate for real-time fluoroscopy imaging. Flat panel detectors with millions of pixels and typical update rates as high as 25 fps to 30 fps employ channel multiplexing and multiple ADCs with sampling rates up to several dozens of MSPS to meet the minimum conversion time without sacrificing accuracy.

In the intensity dimension, the digital output signal of an ADC represents the integrated amount of X-ray photons absorbed in a given pixel over a specific exposure time. This value is binned into a finite number of discrete levels defined by the bit-depth of an ADC. The signal-to-noise ratio (SNR) is another important parameter that defines the intrinsic ability of the system to faithfully represent the anatomic features of the imaged body. Digital X-ray systems use 14-bit to 18-bit ADCs with SNR levels ranging from 70 dB up to 100 dB depending on the type of the imaging system and its requirements. There are a wide range of discrete ADCs and integrated analog front ends to enable various types of DR imaging systems with increased dynamic range, finer resolution, higher detection efficiency, and lower noise.

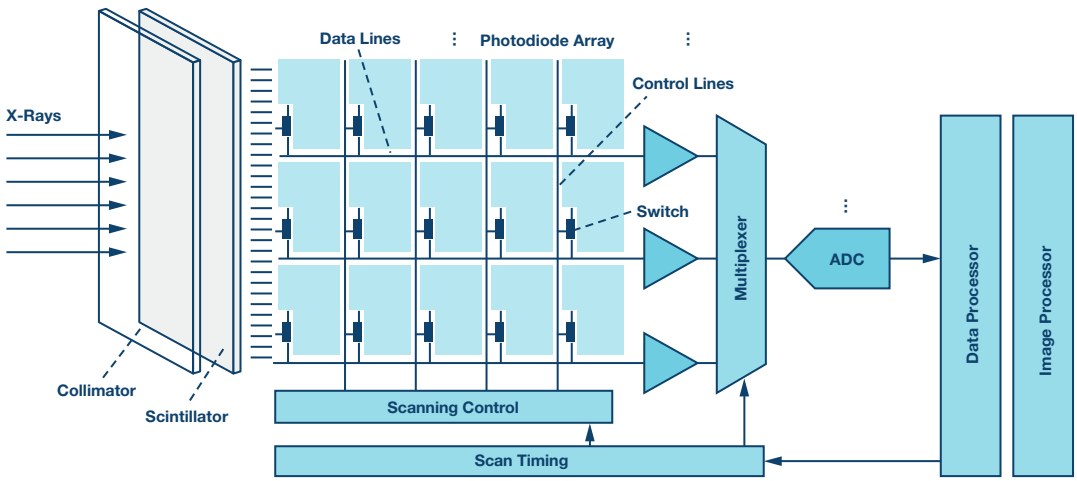

Figure 1. Digital X-ray detector signal chain.

Computed Tomography

Computed tomography (CT) also uses ionizing radiation but, unlike digital X-ray technology, it is based on an arc-shaped detector system synchronously rotating with an X-ray source and utilizes more sophisticated processing techniques to produce high resolution 3D images of blood vessels, soft tissue, and more.

The CT detector is the central component of the entire system architecture and, indeed, is the heart of the CT system. It is comprised of multiple modules, which are depicted in Figure 2. Each module transforms the incident X-rays into electrical signals routed into the multichannel analog data acquisition system (ADAS). Each module contains a scintillating crystal array, a photodiode array, and the ADAS, which contains multiple integrator channels that are multiplexed into the ADCs. The ADAS must have very low noise performance to maintain good spatial resolution with reduced X-ray dosage and to achieve high dynamic range performance with extremely low current outputs. To avoid image artifacts and ensure good contrast, the converter front end must have highly linear performance and offer low power operation to relax cooling requirements for the temperature sensitive detector.

The ADC must have high resolution of at least 24 bits to achieve better and sharper images, and a fast sampling rate to digitize detector readings that can be as short as 100 µs. The ADC sampling rate must also enable multiplexing, which would allow the use of fewer converters as well as the reduction of the size and power of the entire system.

Positron Emission Tomography

Positron emission tomography (PET) involves ionizing radiation resulting from a radionuclide introduced into a human body. It emits positrons that collide with electrons in tissue, generating pairs of gamma rays radiated roughly in opposite directions. These pairs of high energy photons simultaneously strike opposing PET detectors aligned in a ring around a gantry bore.

The PET detector, schematically shown in Figure 3, consists of an array of scintillators and photomultiplier tubes (PMTs) converting gamma rays into electrical currents that are translated into voltages, and then amplified and compensated for amplitude variations by using variable gain amplifiers (VGAs). The resulting signal is split between ADC and comparator paths to provide energy and timing information used by the PET

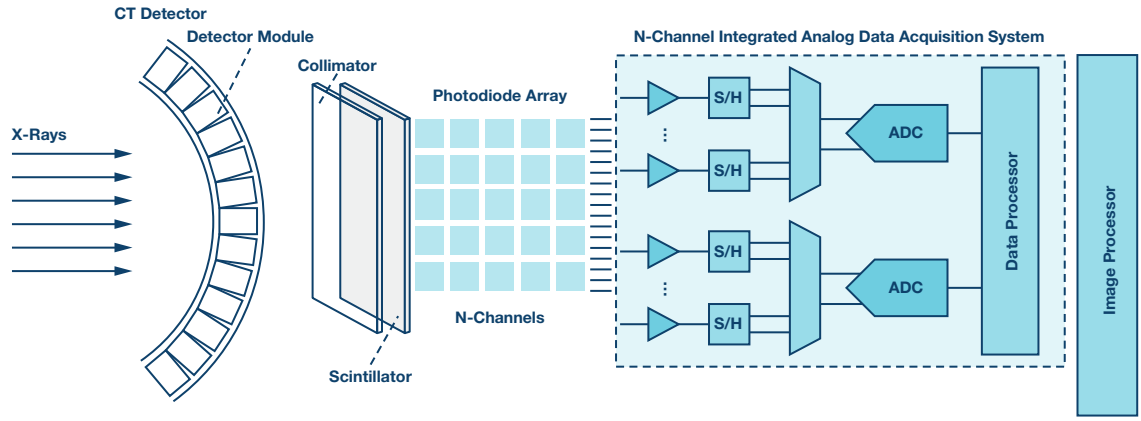

Figure 2. CT detector module signal chain.

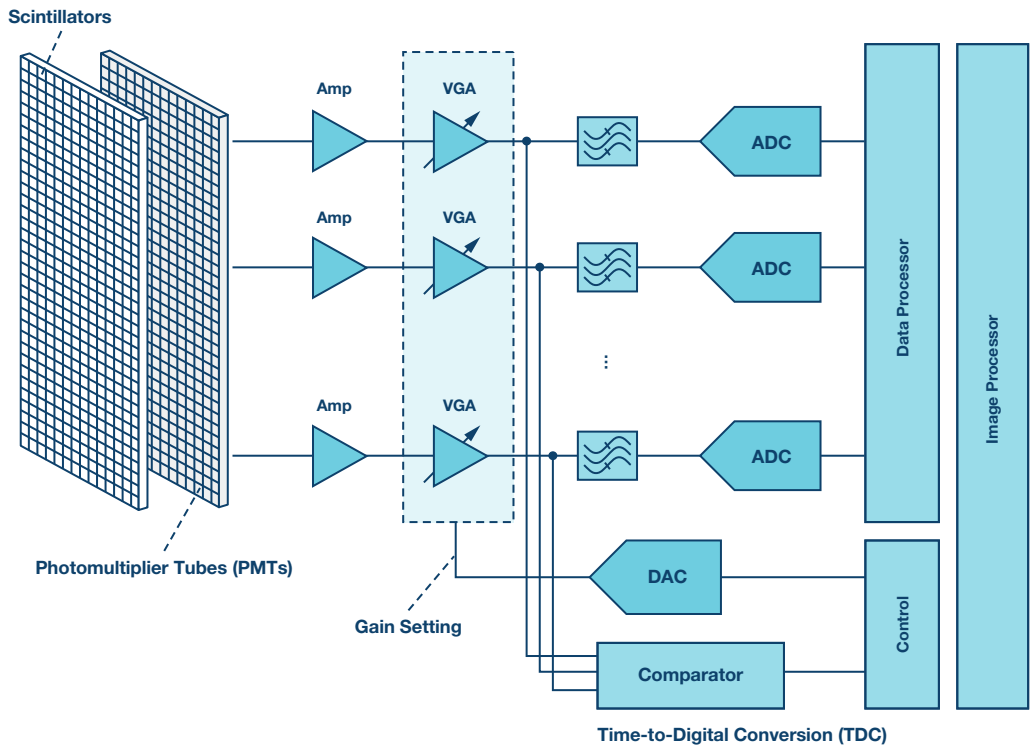

Figure 3. PET electronic front-end signal chain.

coincidence processor to reconstruct a 3D image of a radioactive tracer concentration within the body.

Two photons can be classified as relevant if their energies are around 511 keV and if their detection times differ by less than one ten-billionth of a second. The photons' energy and the detection time difference impose strict requirements on the ADC, which must have good resolution of 10 bits to 12 bits and fast sampling rates typically better than 40 MSPS. Low noise performance to maximize the dynamic range and low power operation to reduce heat dissipation are also important for PET imaging.

Magnetic Resonance Imaging

Magnetic resonance imaging (MRI) is a noninvasive medical imaging technique that relies on the phenomenon of nuclear magnetic resonance and does not use ionizing radiation, which distinguishes it from DR, CT, and PET systems.

The carrier frequencies of the MR signals scale directly with the main magnetic field strength, with the frequencies ranging in commercial scanners from 12.8 MHz to 298.2 MHz. Signal bandwidth is defined by the field-of-view in the frequency-encoding direction and can vary from a few to several dozens of kHz.

This imposes specific requirements on the receiver front end, which is typically based on a superheterodyne architecture (see Figure 4) with lower speed SAR ADCs. However, recent advancements in analog-to-digital conversion enabled fast and low power multichannel pipeline ADCs for direct digital conversion of the MR signals in the most common frequency ranges at conversion rates exceeding 100 MSPS at a 16-bit depth. The requirement for dynamic range is very demanding—it typically exceeds 100 dB. Enhanced image quality is achieved by oversampling the MR signal, which improves resolution, increases SNR, and eliminates aliasing artifacts in the frequency-encode direction. For fast scan acquisition times, the compressed sensing technique based on undersampling is applied.

Ultrasonography

Ultrasonography, or medical ultrasound, is based on a physical principle different from all other imaging modalities discussed in this article. It utilizes pulses of acoustic waves in the frequency range from 1 MHz to 18 MHz. These waves screen the internal body tissue and reflect them back as echoes of varying intensity. These echoes are acquired and displayed in real-time as a sonogram that may contain different types of information, including the acoustic impedance, blood flow, motion of tissue over time, or its stiffness.

The key functional block of the medical ultrasound front end shown in Figure 5 is represented by an integrated multichannel analog front end (AFE) that includes a low noise amplifier, a variable-gain amplifier, an antialiasing filter (AAF), an ADC, and demodulators. One of the most important requirements imposed on the AFE is the dynamic range. Depending on the imaging mode, this requirement can demand 70 dB to 160 dB to distinguish between blood signals and background noise resulting from probe and body tissue movements. Therefore an ADC must provide high resolution, a high sampling rate, and low total harmonic distortion (THD) to maintain dynamic fidelity of the ultrasound signal. Low power dissipation is another important requirement dictated by the high channel density of the ultrasound front end. There is a range of integrated AFEs for medical ultrasound equipment to enable the best image quality, reduced power consumption, and smaller system size and cost.

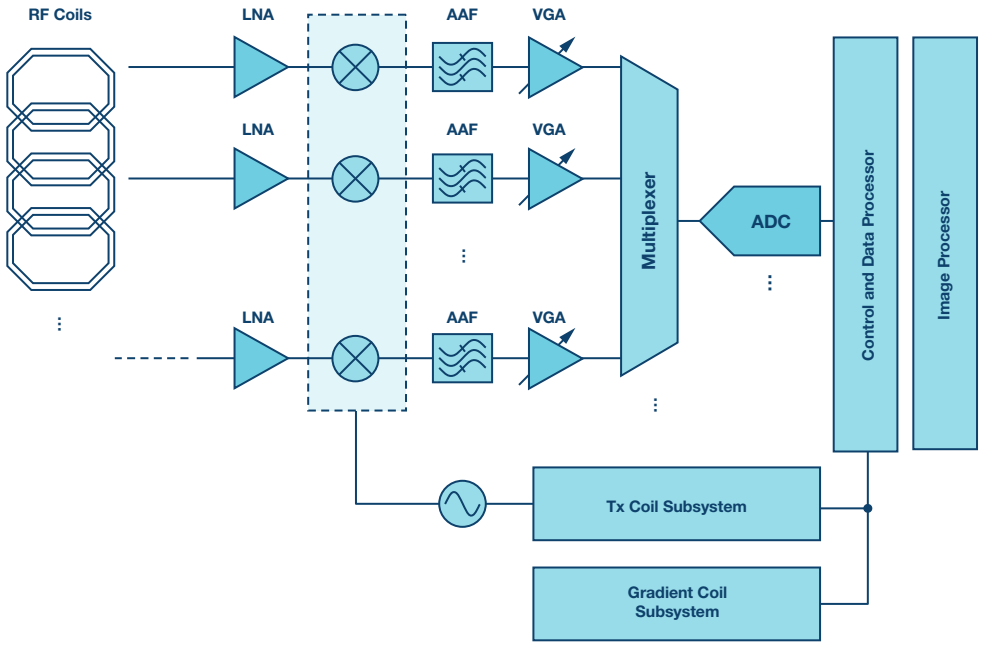

Figure 4. MRI superheterodyne receiver signal chain.

Conclusion

Medical imaging imposes most demanding requirements on the electronic design. Low power, low noise, high dynamic range, and high resolution performance at low cost and in a compact package are common trends dictated by the requirements of the modern medical imaging systems discussed in this article. Analog Devices addresses these requirements and offers highly integrated solutions for the key signal chain functional blocks to enable best-in-class clinical imaging equipment that is increasingly becoming an integral part of international healthcare systems today. Here is a list of products ideal for the various medical imaging modalities mentioned in this article.

- ADAS1256: This highly integrated analog front end incorporates 256 channels with low noise integrators, low-pass filters, and correlated double samplers that are multiplexed into a high speed, 16-bit ADC. It is a complete charge-to-digital conversion solution designed for DR applications that can be directly mounted on a digital X-ray panel.
- For discrete DR systems, the 18-bit PulSAR® ADC AD7960 offers 99 dB of SNR and a 5 MSPS sampling rate to deliver unmatched performance to meet requirements for the highest dynamic range both in noise and in linearity. The 16-bit, dual-channel AD9269 and 14-bit, 16-channel AD9249 pipeline ADCs offer sampling rates of up to 80 MSPS and 65 MSPS, respectively, to enable high speed fluoroscopy systems.
- ADAS1135 and ADAS1134: These highly integrated 256- and 128-channel data acquisition systems are comprised of low noise, low power, low input current integrators, simultaneous sample-and-hold devices, and two high speed ADCs with a configurable sampling rate and resolution of up to 24 bits with excellent linearity performance to maximize image quality for CT applications.
- AD9228, AD9637, AD9219, and AD9212: These 12- and 10-bit multichannel ADCs with sampling rates from 40 MSPS to 80 MSPS are optimized for outstanding dynamic performance and low power to meet PET requirements.
- AD9656: This 16-bit quad pipeline ADC offers a conversion rate up to 125 MSPS and is optimized for outstanding dynamic and low power performance for conventional and direct digital conversion MRI system architectures.
- AD9671: This 8-channel integrated receiver front end is designed for low cost and low power medical ultrasound applications featuring a 14-bit ADC with up to 125 MSPS. Each channel is optimized for a high dynamic performance of 160 dBFS/$\sqrt{\text{Hz}}$ and low power of 62.5 mW in continuous wave mode for applications where a small package size is critical.

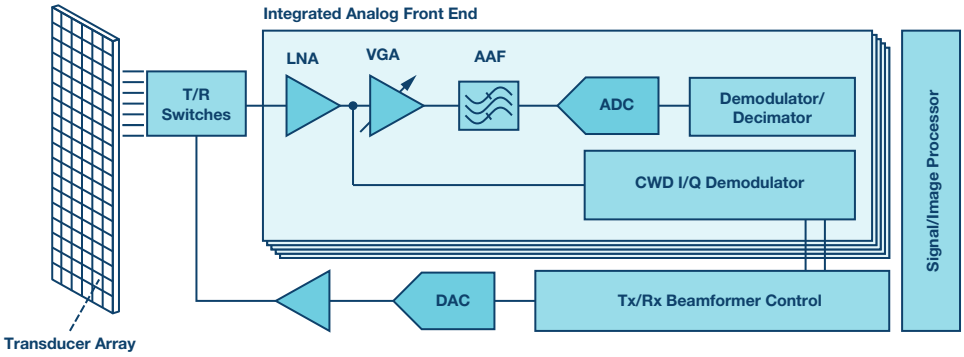

Figure 5. Medical ultrasound front-end signal chain.

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Anton Patyuchenko

Synchronous Boost Converter Powers High Current LEDs Even at Low Input Voltages

By **Kyle Lawrence**

High power LEDs continue to proliferate in modern lighting systems, spanning automotive headlights, industrial/commercial signage, architectural lighting, and a variety of consumer electronics applications. The industry's transition toward LED technology is driven by the distinct advantages that solid-state lighting offers over conventional light sources: the high efficiency conversion of electrical power to light output, as well as long operational life spans.

As LED lighting is incorporated into an expanding array of applications, the demand for higher LED currents for increased light output also grows. One of the biggest challenges for powering strings of high current LEDs is maintaining high efficiency in the power converter stage that is responsible for providing a well-regulated LED current. Inefficiency in the power converter presents itself in the form of unwanted heat, which originates from the switching elements of the current regulator circuitry.

The LT3762 is a synchronous boost LED controller designed to curtail the sources of efficiency loss common in high power step-up LED driver systems. This device's synchronous operation minimizes the losses normally incurred from the forward voltage drop of a catch diode in an asynchronous dc-to-dc converter. This increased efficiency allows the LT3762 to deliver much higher output current than similar asynchronous step-up LED drivers, especially at low input voltages. In order to improve low input voltage operation, an on-board dc-to-dc regulator provides 7.5 V to the gate drive circuitry, even when the input drops below 7.5 V. The result of having a strong gate drive voltage source at low input voltages is that the MOSFETs generate less heat as the input voltage decreases, which extends the low end of the operational input range to 3 V.

Figure 1. The LT3762 demonstration circuit (DC2342A) powers up to 32 V of LEDs at 2 A over a wide input voltage range. This demo circuit can easily be modified with additional MOSFETs and capacitors to increase the output power.

This step-up LED controller can be configured to operate between 100 kHz and 1 MHz fixed switching frequency, with optional −30% × f_{SW} spread spectrum frequency modulation to reduce switching-related EMI energy peaks. The LT3762 can be run in a step-up, step-down, or step-up/step-down topology for powering LEDs. A high-side PMOS disconnect switch facilitates PWM dimming and protects the device from potential damage when the LEDs are placed in an open-/short-circuit condition.

The LT3762 features an internal PWM generator, which uses a single capacitor and a dc voltage to set the frequency and pulse width for up to a 250:1 PWM dimming ratio, and can alternatively use an external PWM signal to achieve ratios as high as 3000:1. The schematic in Figure 2 shows the demonstration circuit application (DC2342A) using the LT3762, which is configured to power up to 32 V of LEDs at 2 A from an input voltage range of 4 V to 28 V. The LT3762 synchronous boost LED controller is offered in a 4 mm × 5 mm QFN package, as well as a 28-lead TSSOP package.

Synchronous Switching

In asynchronous dc-to-dc converter topologies, Schottky catch diodes are used as passive switches to simplify the control scheme of the converter to pulse-width modulate a single MOSFET. While this does simplify things from a control perspective, it limits the amount of current that can be delivered to the output. Schottky diodes, like PN junction devices, experience a forward voltage drop before any current can pass through the device. As the power dissipated in the Schottky diode is the product of its forward voltage drop and current, conduction-related power dissipation can result in several watts of loss at excessive output current levels, resulting in the Schottky diode heating up, which causes inefficiencies in the converter.

The LT3762 synchronous switching converter does not encounter the same output current limitations that asynchronous converters do. This is because synchronous converters replace the Schottky diode with a second MOSFET. Unlike Schottky diodes, MOSFETs do not have a forward voltage drop. Instead, MOSFETs feature a small resistance that is formed from drain to source when the device is fully enhanced. The conduction losses incurred from a MOSFET are much lower than with Schottky diodes at high current, as the power lost is proportional to the product of the square of the current through the device and drain-source resistance. Even at the lowest full power input voltage of 7 V, the MOSFETs only experience a temperature increase of roughly 30°C, as shown in Figure 3.

Low Input Voltage Operation

Another challenging region for high power boost LED controllers occurs during low input voltage operation. The majority of boost dc-to-dc regulator ICs use an internal LDO voltage regulator powered from the input of the device to provide lower voltage power to the analog and digital control circuitry within the IC. Of the circuitry that draws power from the internal LDO regulator, the gate driver consumes the most power, and its performance is affected by fluctuations in the output of the LDO regulator. As the input voltage drops below the LDO output voltage, the LDO output begins to collapse, which limits the gate driver's ability to properly enhance the

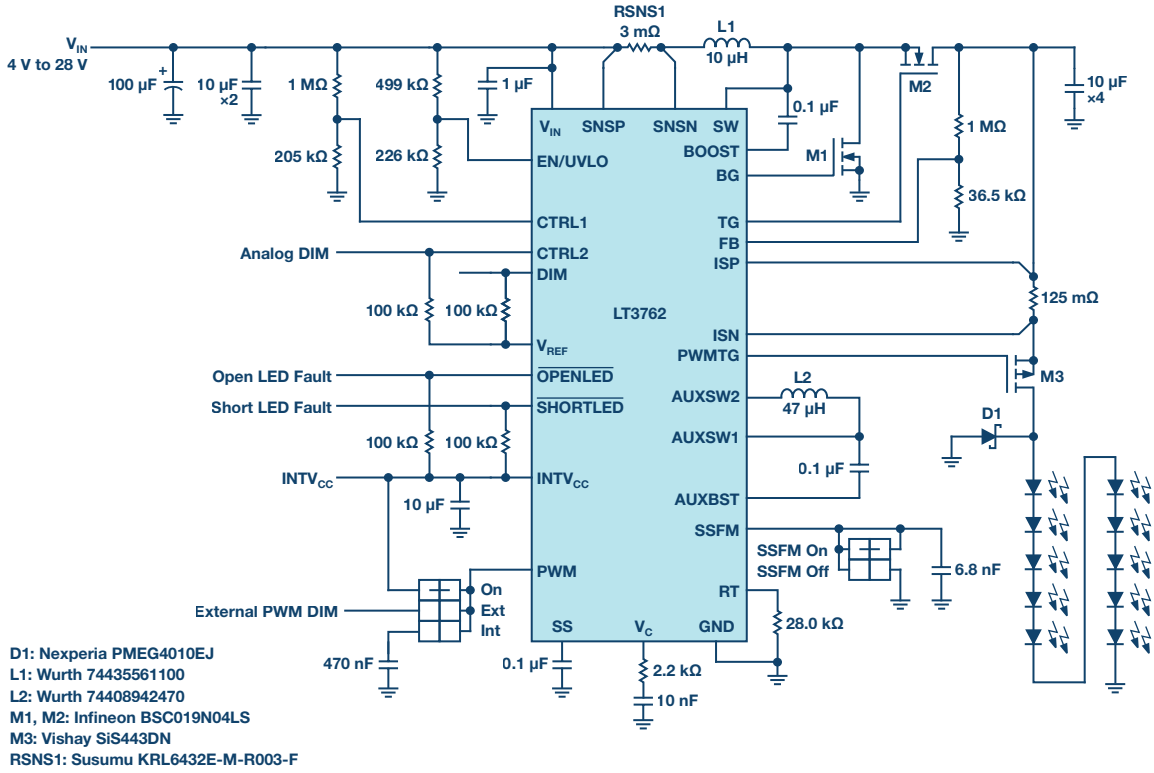

Figure 2. A 32 V, 2 A LT3762 boost LED driver.

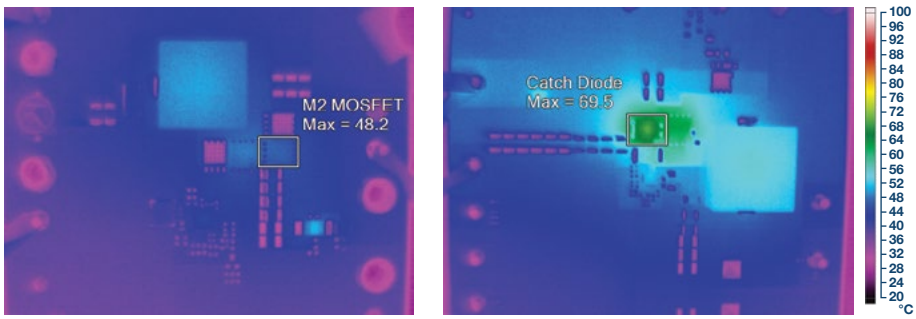

Figure 3. Under identical test conditions and using similar component selection, the synchronous LT3762 (left) powers a 32 V string of LEDs at 2 A with far less temperature rise than observed in an asynchronous LT3755-2 circuit (right). This increase in thermal performance is attributed to replacing the Schottky catch diode with a synchronous MOSFET, which eliminates the loss caused by the forward voltage drop of the diode.

MOSFETs. When MOSFETs are not fully enhanced, they operate in a higher resistance state, causing them to dissipate power in the form of heat as current is passed through the device.

Low input voltage operation in step-up converter topologies results in higher input current, which, when having to pass through a more resistive MOSFET device, exacerbates conduction losses. Depending on the gate drive voltage of the regulator IC, this can severely limit the low input voltage range that the device can successfully achieve without overheating.

The LT3762 features an integrated buck-boost dc-to-dc regulator, instead of an LDO regulator, which provides 7.5 V to power the internal circuitry even when the input voltage is low. This buck-boost regulator only consumes three pins of the LT3762 IC, and requires only two additional components. Compared to internal LDO controller devices, which have minimum input voltages of 4.5 V and 6 V, the LT3762 is able to extend its input operating range down to 3 V. The 7.5 V output of the buck-boost converter supplies power to the gate driver, and allows for 6 V/7 V gate drive MOSFETs to be used. Higher gate drive voltage MOSFETs tend to have lower drain-source resistances, and (barring switching losses) operate more efficiently than their lower gate drive voltage counterparts.

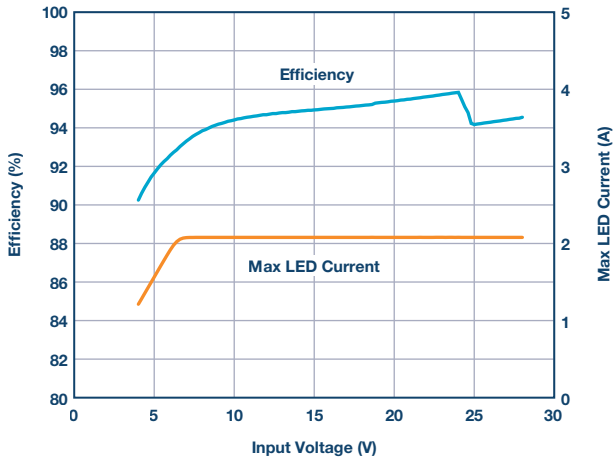

Figure 4. A 32 V, 2 A LT3762 LED driver maintains high efficiency over a wide input range. Low V_{IN} foldback helps avoid excessive switch/inductor currents. Asynchronous switching starts at 24 V input.

Flexible Topologies

Like most other boost LED drivers from ADI, the LT3762 can be reconfigured to power LEDs in a step-up configuration, and also as a step-down (buck mode), and step-up/step-down (buck-boost mode and boost-buck mode). Of these boost converter topology variants, the ADI-patented boost-buck mode configuration offers the ability to operate as a step-up/step-down converter with the added benefit of low EMI operation. This topology utilizes two inductors, one input facing and the other output facing, to aid in filtering noise generated by switching. These inductors help suppress EMI from coupling to the input supply and the other devices that may be connected, as well as the LED load.

Additional circuitry can be added on to the boost-buck mode topology to offer short-circuit protection of the LED⁻ node to GND. The schematic in Figure 5 shows the LT3762 in a boost-buck mode configuration with this protection circuitry added. In the event that LED⁻ is shorted to GND, M4 is forced to turn off, blocking the conduction path to the input through the inductors and preventing excessive current draw. When M4 is forced to turn off, D3 pulls the EN/UVLO pin low to stop the converter from switching until the short circuit has been removed. The addition of this protective circuitry used in conjunction with the LT3762's built-in open-/short-circuit detection results in a robust solution capable of surviving a variety of fault conditions in harsh environments.

Conclusion

Asynchronous boost converters often struggle to provide high output current without experiencing substantial power losses and heating of the catch diode under normal operation. In addition to loss generated by the Schottky diode, such converters struggle to maintain maximum power output capabilities as the input voltage decreases, which limits the power delivery across the input range. Asynchronous dc-to-dc converters are simply not suited for higher power levels, and a synchronous switching scheme must be implemented to meet application specifications. The LT3762 boost LED controller addresses the issues of delivering high output current with its synchronous switching, is capable of operating at much lower input voltages thanks to its onboard dc-to-dc converter, and has the flexibility to be used in a variety of circuit topologies.

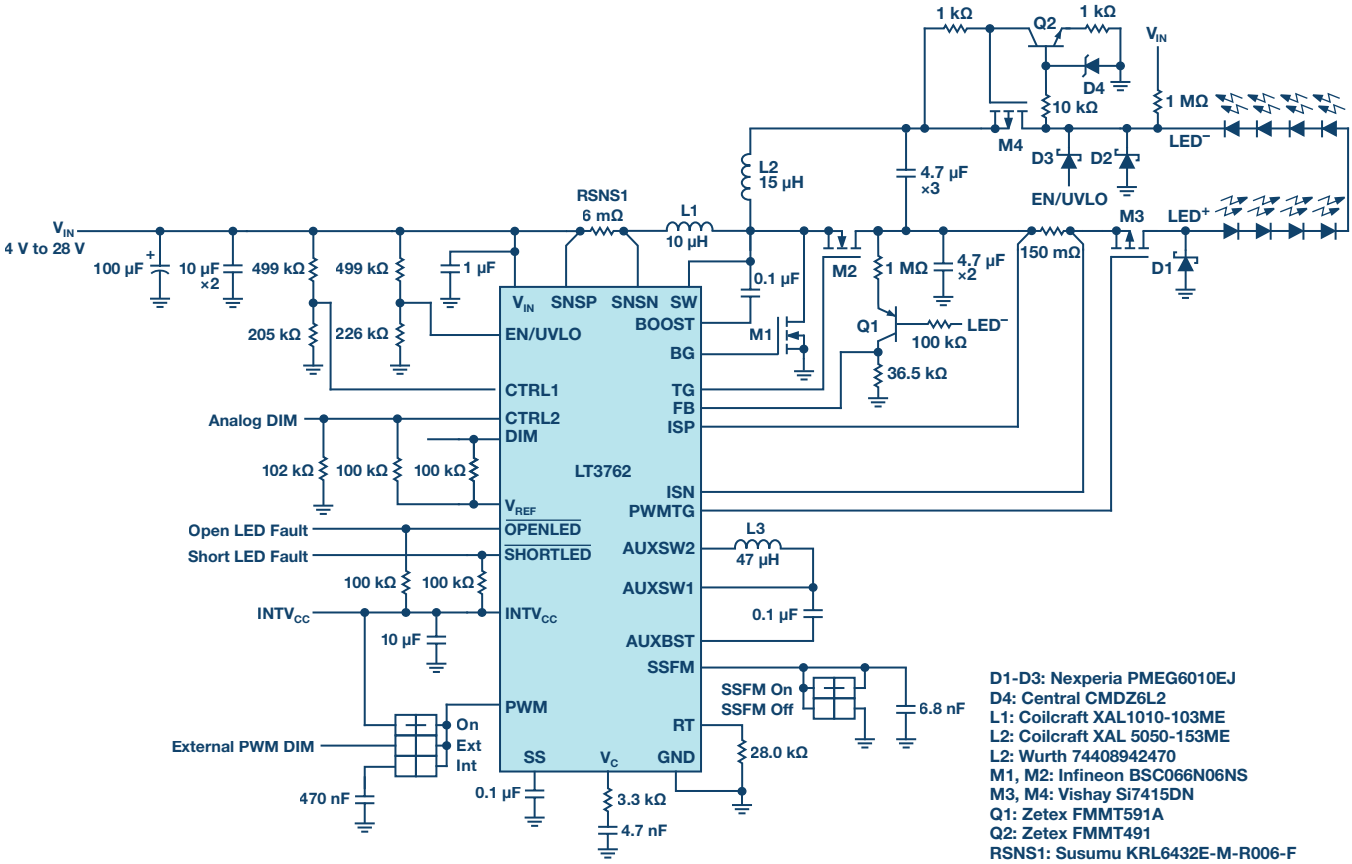

Figure 5. A 25 V, 1.5 A boost-buck configuration of LT3762 with additional LED⁻ to GND short-circuit protection.

Kyle Lawrence [kyle.lawrence@analog.com] is an applications engineer at Analog Devices. He is responsible for the design and testing of a variety of dc-to-dc converters, including 4-switch buck-boost voltage regulators and LED drivers targeting low EMI automotive applications. Kyle received his B.S. degree in electrical engineering from the University of California, Santa Cruz in 2014.

Kyle Lawrence

Also by this Author:

LED Driver for High Power Machine Vision Flash

Volume 52, Number 2

Rarely Asked Questions—Issue 162 Enablement of Batteryless Applications with Wireless Power

By **Mark Vitunic**

Question:

My application doesn't have a battery. Is it possible to power it wirelessly?

Answer:

Yes, sure—a simple integrated nanopower solution originally designed for energy harvesting is available.

A wireless power transfer (WPT) system is composed of two parts separated by an air gap: transmitter (Tx) circuitry with a transmit coil and receiver (Rx) circuitry with a receive coil (see Figure 1). Much like in a typical transformer system, ac generated in the transmit coil induces ac in the receive coil via a magnetic field. However, unlike in a typical transformer system, the coupling between the primary (transmitter) and secondary (receiver) is typically very low. This is due to the nonmagnetic material (air) gap.

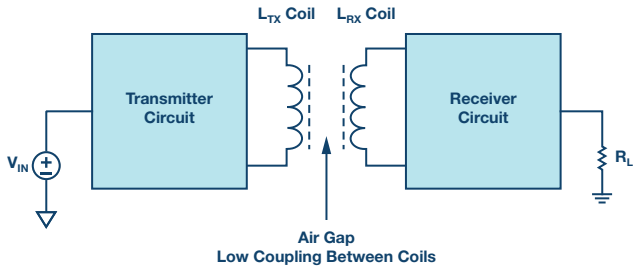

Figure 1. Wireless power transfer system.

Most wireless power transfer applications in use today are configured as wireless battery chargers. A rechargeable battery resides on the receiver side and is charged wirelessly whenever in the presence of a transmitter. After charging is complete, and when the battery is subsequently taken off of the charger, the rechargeable battery then powers the end application. Downstream loads can connect either directly to the battery, indirectly to the battery through a PowerPath ideal diode, or to the output of a battery-powered regulator integrated into the charger IC. In all three scenarios (see Figure 2), the end application can run either on or off the charger.

But what if a particular application does not have a battery at all, and instead what is desired is just providing a regulated voltage rail when wireless power is available? Examples of such applications abound in remote sensors, metering, automotive diagnostics, and medical diagnostics. For example, if a remote sensor does not need to be continuously powered, then it doesn't have to have a battery, which would either need to be replaced periodically (if it is a primary cell) or charged (if it is rechargeable). If that remote sensor only needs to give a reading when the user is in the vicinity of it, then it can be wirelessly powered on demand.

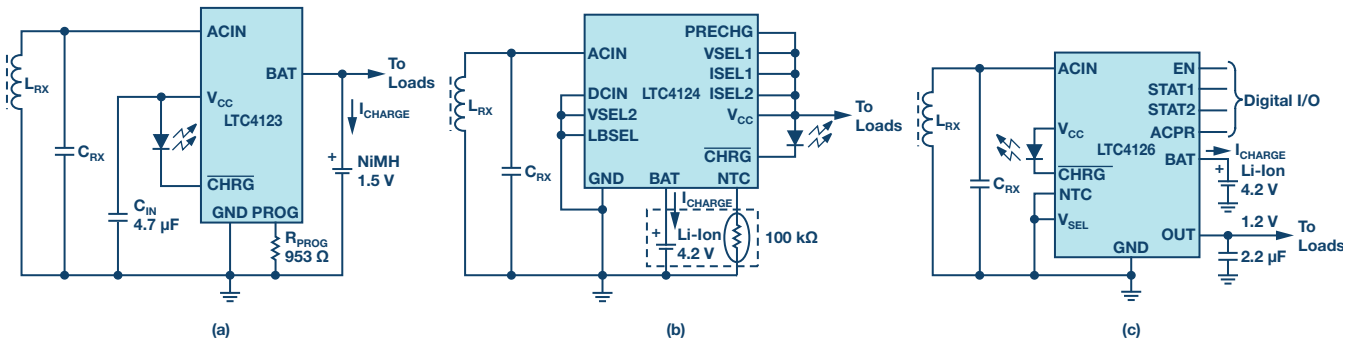

Figure 2. Wireless Rx battery chargers with downstream loads connected to a) a battery, b) a PowerPath ideal diode, and c) a regulator output.

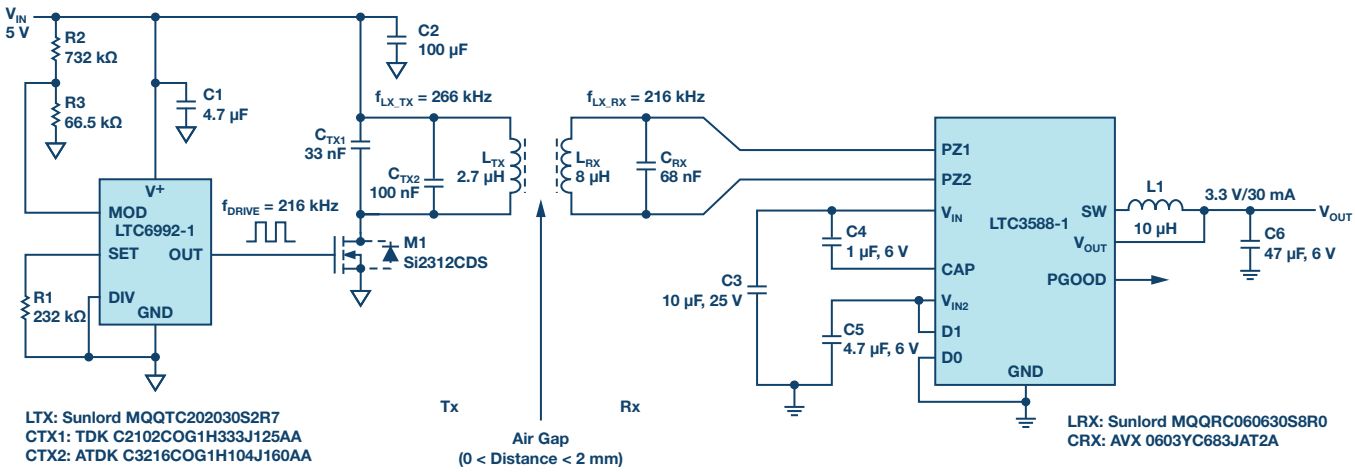

Figure 3. WPT employing the LTC3588-1 to supply a regulated 3.3 V rail.

Enter the LTC3588-1 nanopower energy harvesting power supply. Although originally designed for energy harvesting (EH) applications powered from a transducer (for example, piezoelectric, solar, etc.), the LTC3588-1 can also be used for wireless power. In Figure 3, a complete transmitter plus receiver WPT solution using the LTC3588-1 is shown. On the transmitter side, a simple open-loop wireless transmitter based on the LTC6992 TimerBlox® silicon oscillator is used. For this design, the drive frequency is set at 216 kHz, which is below the LC tank resonant frequency of 266 kHz. The exact ratio of f_{LC_TX} to f_{DRIVE} is best determined empirically with the goal of minimizing switching losses in M1 due to zero voltage switching (ZVS). Design considerations on the transmitter side with respect to coil selection and frequency of operation are no different than those for other WPT solutions: that is, there is nothing unique to having an LTC3588-1 on the receiver side.

On the receiver side, the LC tank resonant frequency is set equal to the drive frequency of 216 kHz. Because many EH applications require ac-to-dc rectification (just like WPT), the LTC3588-1 already has this built-in, allowing the LC tank to connect directly to the LTC3588-1's PZ1 and PZ2 pins. Rectification is wideband: dc to >10 MHz. Similar to the V_{CC} pin on the LTC4123/LTC4124/LTC4126, the V_{IN} pin on the LTC3588-1 is regulated to a level appropriate for providing power to its downstream output. In the case of the LTC3588-1, the output is that of a hysteretic buck dc-to-dc regulator instead of a battery charger. Four pin-selectable output voltages: 1.8 V, 2.5 V, 3.3 V, and 3.6 V are available with up to 100 mA of continuous output current. The output capacitor can be sized to provide higher short-term current bursts provided that the average output current does not exceed 100 mA. Of course, realizing the full 100 mA output current capability depends on having an appropriately sized transmitter, coil pair, and sufficient coupling.

If the load demand is less than the available wireless input power can support, the V_{IN} voltage will increase. Although the LTC3588-1 integrates an input protective shunt that can sink up to 25 mA if the V_{IN} voltage rises to 20 V, this function may be unnecessary. As the V_{IN} voltage rises, the peak ac voltage on the receiver coil does as well, and this corresponds to a drop in the amount of ac deliverable to the LTC3588-1 as opposed to simply circulating in the receiver tank. If the open circuit voltage (VOC) of the receiver coil is reached before V_{IN} rises to 20 V, the downstream circuit is protected with no wasted heat in the receiver IC.

Test results: For the application shown in Figure 3 with a 2 mm air gap, the measured max deliverable output current at 3.3 V was 30 mA and the measured no load V_{IN} voltage was 9.1 V. For a near-zero air gap, the max deliverable output current increased to approximately 90 mA, while the no load V_{IN} voltage increased to only 16.2 V—well below the input protective shunt voltage (see Figure 4).

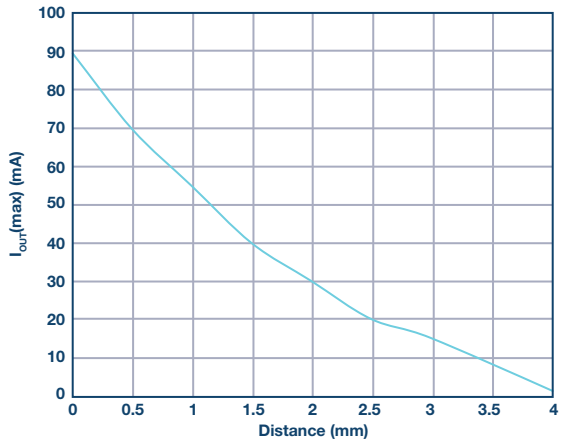

Figure 4. Max deliverable output current at 3.3 V for various distances.

For battery-free applications where a wireless power source is available, the LTC3588-1 provides a simple integrated solution for providing a low current regulated voltage rail with full input protection.

Mark Vitunic [mark.vitunic@analog.com] is a design manager in the Power by Linear™ Group of Analog Devices. He officially joined ADI in 2017 as part of the acquisition of Linear Technology, where he had worked for the previous 19 years. Mark manages numerous project developments in North Chelmsford, MA and in Munich, Germany, with a focus on wireless power transfer, ultra low power ICs, energy harvesting, active battery balancing, and multichannel dc-to-dc regulators. Mark holds B.S. and M.S. degrees in electrical engineering from Carnegie-Mellon University and the University of California at Berkeley, respectively.

Mark Vitunic

Looking Inside Real-Time Ethernet

By **Volker Goller**

Industrial Ethernet—real-time Ethernet—has experienced a huge upswing over the last few years. Although classic fieldbuses are still running in large numbers, they have passed their prime. The popular real-time Ethernet protocols extended the Ethernet standard to meet the requirements for real-time capabilities. TSN now provides a new route to real-time Ethernet.

Real Time and Communications

In the context of factory automation and drive technology, real time means safely and reliably reaching cycle times in the range of less than ten milliseconds down to microseconds. For these real-time requirements to be satisfied, Ethernet also had to gain real-time capabilities.

Ethernet Is a Lot Faster Than a Fieldbus—So What?

For the real-time requirements of automation to be satisfied, both transmission bandwidth and transmission latency need to be guaranteed. Even if these bandwidths are usually decidedly small (a few dozen bytes per device), this transmission channel must be available in every I/O cycle with the required latency.

However, the guarantee of latency and bandwidth is not provided with classic Ethernet. On the contrary, an Ethernet network may discard frames at any time if this is necessary for operation. What does this mean?

Ethernet is a so-called bridged network. The frames (Ethernet frames) are sent from one point to another: from the endpoint to the switch (bridge), from there possibly to other bridges, and finally to the other endpoint. This architecture is largely self-configuring. The bridges first completely receive frames before forwarding them. And this is where multiple problems arise:

- If at peak times there are more frames to store than the buffer memory in the bridge can hold, then the newly incoming frames are discarded.
- Because the frames differ in length, they are delayed as a function of their lengths. This leads to fluctuating latencies (jitter).
- Because the port through which the switch is supposed to send a frame may already be occupied by other frames up to the full frame size, additional delays come into play. The sending of a large Ethernet frame (1522 bytes) takes about 124 µs at 100 Mbps.

We can argue that Ethernet normally works well and is somehow fair. However, by doing so, we use two words that make no sense in connection with hard real time. It is not enough if a real-time condition is only normally met. It always has to be met.

Anyone who lives next to a chemical plant or a refinery can appreciate this. And industrial communications aren't fair either: The most important thing, the control/closed-loop control application, always has priority.

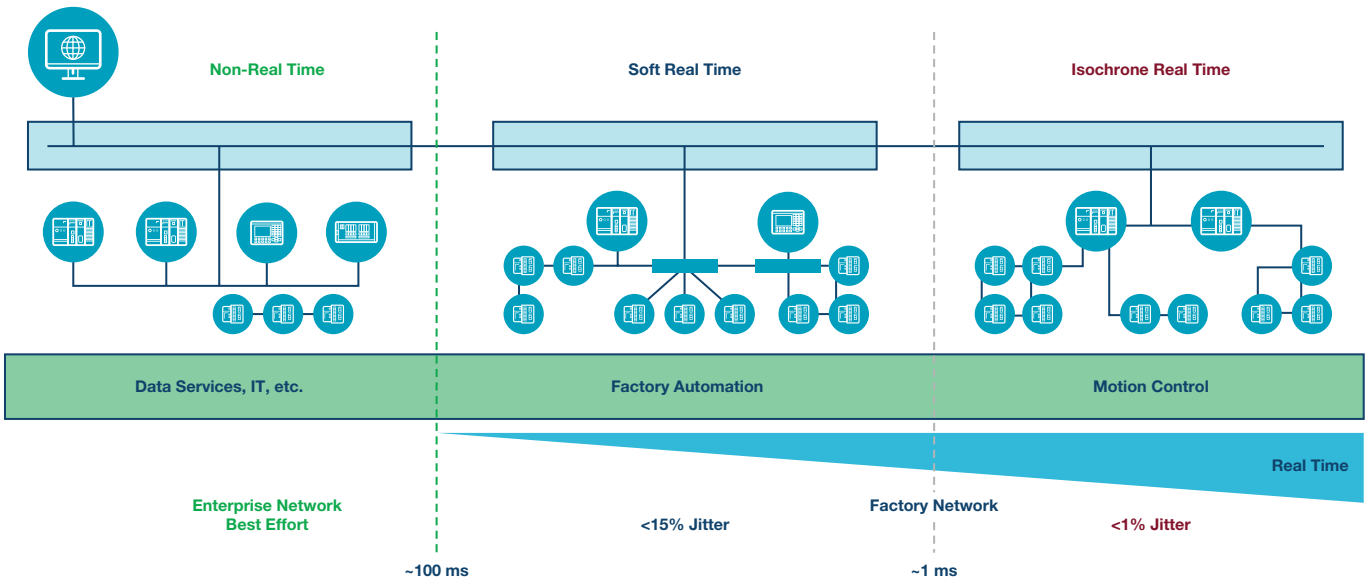

Figure 1. Real-time communications in automation.

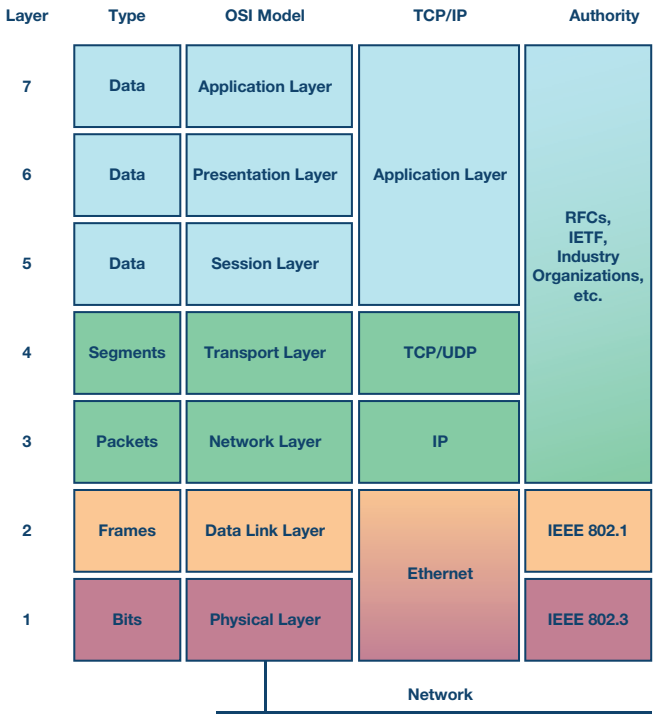

Figure 2. ISO seven-layer model.

Real-Time Extensions Illustrated Using PROFINET and EtherCAT as Examples

Because no solution to the problem was available in the IEEE, which is responsible for Ethernet standardization, the industry developed its own solutions—once again demonstrating its innovativeness. The solutions all have their strengths and weaknesses and ultimately address different markets.

PROFINET: Universally Applicable

With PROFINET®, two complementary solutions are offered. PROFINET RT is a factory automation solution with a cycle time of up to 1 ms. RT is directly based on standard Ethernet. The possibilities of Ethernet (for example, quality of service (QoS, prioritization)) are utilized to give real-time traffic priority. That helps, but QoS does not completely solve the resource and latency problem. That's the reason for restriction to soft real time. The good compatibility with other protocols (such as HTTP, SNMP, and TCP/IP) used in the network is a clear strength of the technology.

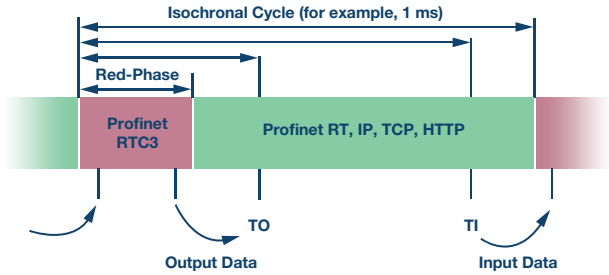

Figure 4. PROFINET IRT.

For hard real time, PROFINET offers the isochronous real-time (IRT) extension. Here, part of the Ethernet bandwidth is reserved exclusively for IRT traffic through an extension to standard Ethernet hardware. This is made possible by precise synchronization of the clocks in the IRT nodes. As a result, a channel (the red phase), can be blocked for normal traffic in every cycle. Only IRT frames in the red phase reach the network. In addition, the network participants send the IRT frames exactly at precalculated times, enabling maximization of efficiency within the red phase. The IRT frames move almost without slip through the network. One advantage of this is that it limits the length of the red phase, in which all other traffic must wait, to the bare minimum. The red phase can occupy up to 50% of the bandwidth of the Ethernet channel.

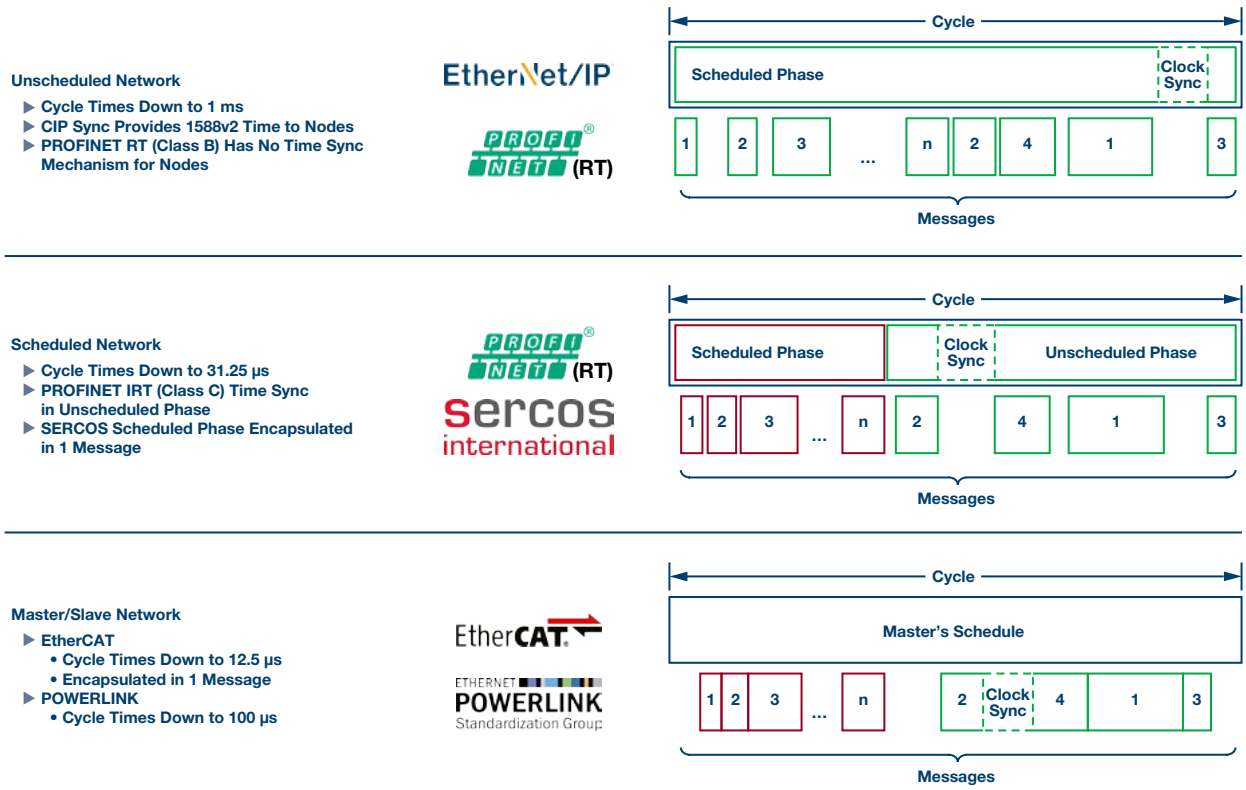

Figure 3. Overview of protocols.

As already mentioned, a full length (1552 byte) Ethernet frame needs about 124 µs on the wire. If PROFINET IRT occupies max. 50% of the bandwidth, the fastest cycle time is 2 × 124 µs = 248 µs, or 250 µs when rounded up. Only in this way can other protocols (like HTTP) coexist in unchanged form with it.

Even faster cycle times of down to 31.25 µs are possible due to PROFINET 2.3 for IRT's optimizations, including fast forwarding, dynamic frame packaging, and fragmentation.

EtherCAT: The Ethernet Fieldbus

In the development of EtherCAT, there were other requirements in the beginning. EtherCAT is a fieldbus based on the physical Ethernet—that is, layer 1. Even layer 2 is optimized for fieldbus applications and high throughput. EtherCAT doesn't have the classic Ethernet bridge. It uses a summation frame telegram, which makes data transmission especially efficient. Instead of normal Ethernet, in which a separate frame is sent by each device involved in communication between devices, EtherCAT sends one frame per cycle. However, this frame contains all data for the addressed devices. While the EtherCAT frame is being forwarded by a device, the data for that particular device are inserted into and taken out of the frame live. Through this, very short cycle times of even less than 31.25 µs, in the extreme case, can be achieved.

EtherCAT also has time synchronization. A lot of effort was put into enabling the not always ideal Ethernet interfaces on a PC to be used as masters for EtherCAT.

Ethernet traffic such as web or TCP/IP traffic can only be transported in small portions in piggyback style over EtherCAT; direct coexistence on the wire is not possible.

What About the Others?

POWERLINK takes the same basic approach that EtherCAT does; it assumes complete control over the Ethernet and transports IP applications by piggyback to the nodes. But that's the only thing they have in common. POWERLINK does not employ a summation frame protocol. Nevertheless, it performs similarly well in practical applications.

Like IRT, SERCOS has a reserved bandwidth, but uses a summation frame protocol within it. SERCOS allows other protocols to coexist.

It's Time for TSN

IEEE approached the topic of real time within the scope of the audio/video bridging (AVB) protocol. In the improvement of the protocol, the more challenging real-time communications of industry were also considered. The original name for the set of standards, AVB2, was hereupon changed to TSN (for time-sensitive networking). With these standards, it is now possible to use a unified, deterministic version of Ethernet.

This actually makes many things easier. For example, the well-known industrial networks are nearly all defined for 100 Mbps. Today, however, gigabit Ethernet and 10 Mbps Ethernet have become the focus of attention in special applications. The TSN standards cover all speeds. With TSN, the wheel does not have to be reinvented: if it weren't for TSN, all of the existing standards would have to be redefined for gigabit—which would result in costs for hardware development and in market fragmentation.

How Does TSN Help? Real Time with TSN

TSN extends layer 2 of Ethernet to include a series of mechanisms needed for real-time operation:

- 802.1AS/802.1AS-Rev provides for extremely precise synchronization of the clocks in the network.
- The time-aware shaper (TAS) option enables Ethernet to be operated with hard scheduling. With it, one or more queues of the QoS model can be blocked/released at specific times.
- The preemption (interspersing express traffic) option enables long frames to be broken up into smaller parts so that delays are minimized for higher priority frames. It can be used to optimize the guard band for TAS or replace TAS at speeds of above 100 Mbps.
- The frame replication and elimination for reliability option can be used for the definition of redundant paths through the network; for example, in rings.
- Use of software-defined networking means that frames are no longer forwarded to the destination by means of the hardware MAC address of the destination node, but are rather forwarded through a combination of special MAC addresses (locally administered multicast MAC) and VLAN IDs. How these frames are routed through the network is no longer automatically determined, but rather configured by software. This combination of multicast MAC and VLAN ID is called the stream ID and all TSN frames with the same stream ID are called the TSN stream. A TSN stream always has just one sender, but it can have several recipients.

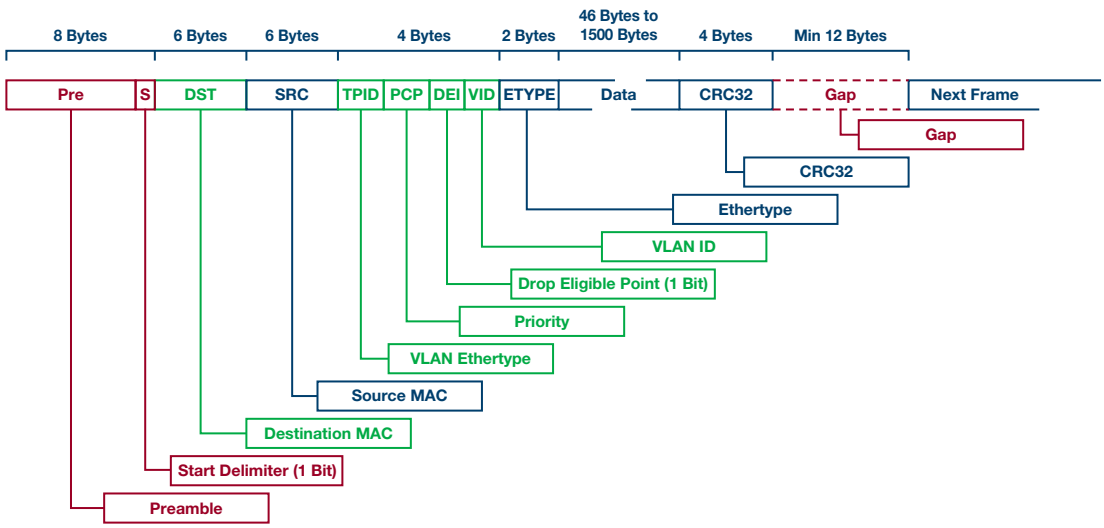

Figure 5. An Ethernet frame, with parts relevant to TSN data stream identification shown in green.

The TSN streams can now be set up in consideration of the existing resources in such a way that no frame has to be discarded anymore. The bridges now use their resources for loss-free forwarding of the TSN streams.

The best effort traffic (standard Ethernet, IP, web) takes place completely normally with the remaining resources (memory/bandwidth).

And What Happens Above Layer 2?

Behind every internet Ethernet protocol lies an organization that advances the standardization and popularization of the respective protocol. Each of these organizations has formulated a TSN strategy. Consequently, we will see nearly all existing protocols again with TSN—in one form or another. Staying with our examples:

For PROFINET, the path to TSN is a relatively short one because there is already a wealth of experience with time-aware shaping available (it is already done very similarly to IRT) and the coexistence of industry and IT protocols has always been supported. Much remains the same for the user, so a familiar environment can yield new performance.

EtherCAT and, similarly, SERCOS will make TSN accessible above the field level. For example, the EtherCAT automation protocol (EAP) is very suitable for networking classic EtherCAT segments via TSN at a low overhead.

However, there are also new players in the field.

There is a group that is defining a completely new industrial Ethernet protocol. OPC UA is being used as the application layer. TSN is seen as a means for making this protocol real-time capable. However, work still has to be done here. A new transport layer for OPC UA, the so-called OPC UA PUB/SUB protocol, is needed for the transport.

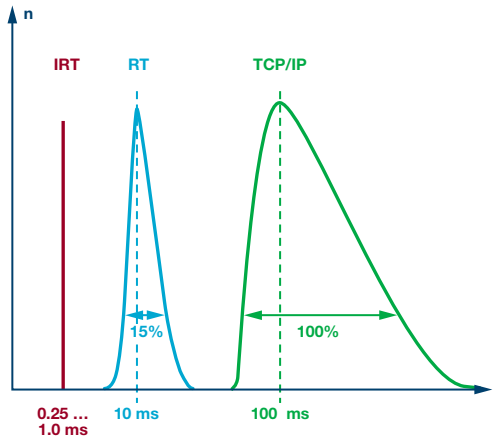

Figure 6. Magnitude of latency/jitter for hard real time (IRT), soft real time (RT), and IT protocols (TCP/IP).

Does a Lot Help a Lot? Not in Real Time

Today we are using 100 Mbps Ethernet in industrial automation and soon gigabit Ethernet will be available. However, higher speed does not automatically mean guaranteed latency and guaranteed transmission. Hence, for hard real time, special mechanisms are always necessary. With TSN, they are now standardized.

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Volker Goller

Strapdown Inertial Navigation System Based on an IMU and a Geomagnetic Sensor

By **Joel Li** and **Van Yang**

Abstract

This article introduces a strapdown inertial navigation system (SINS) we built using Analog Device's inertial measurement unit (IMU) sensor ADIS16470 and PNI's geomagnetic sensor RM3100. Some basic processes for SINS based on magnetics, angular rates, and gravity (MARG) are implemented, including electromagnetic compass calibration, an attitude and heading reference system (AHRS) that uses an extended Kalman filter (EKF), and trace tracking. Loosely coupling sensor fusion by using the minimum squared error (MSE) method is also implemented. Both algorithm and experiment setup in each process step are shown. The result analysis and the method used to improve accuracy are discussed at the end of the article.

Introduction

With the market and technique growth of service robots, navigation has become a hot research and application point. Compared to vehicles, ships, or aircraft, service robots are small and low cost, so their navigation systems should be strapdown and low cost. Traditional, stable-platform navigation systems commonly involve separate accelerators and fibers or laser-based gyroscopes, with all the components mechanically and rigidly mounted on a stable platform that is isolated from the moving vehicle. This leads to the drawbacks of large size, poor reliability, and high cost. In contrast, in strapdown navigation systems, the inertial sensors are fastened directly to the vehicle's body, which means the sensors rotate together with the vehicle. This strapped down method eliminates the drawbacks of stable platform navigation. However, the accuracy of platform navigation is often higher than SINS. Platform navigation can often reach the strategic grade (0.0001°/hr gyroscope bias, 1 µ*g* accelerator bias) or military grade (0.005°/hr gyroscope bias, 30 µ*g* accelerator bias), while most SINS can only reach the navigation grade (0.01°/hr gyroscope bias, 50 µ*g* accelerator bias) or tactical grade (10°/hr gyroscope bias, 1 m*g* accelerator bias). For most service robot or AGV navigation applications, this is enough.

There are multiple navigation methods, including machine vision, GPS, UWB, lidar with SLAM, etc., while inertial navigation is always an important component in navigation where an IMU is used. However, due to the limitation of this kind of sensor—such as bias error, cross-axis error, noise, and especially bias instability—inertial navigation often needs a partner sensor to give it a reference or calibration periodically, which is called sensor fusion here. There are many sensors to fuse with an IMU, such as cameras and odometers, but among these sensors, a geomagnetic sensor is a low cost way to get attitude together with an IMU.

In this article, we use ADI's IMU, ADIS16470, and a geomagnetic sensor to develop a platform and an algorithm to implement a strapdown inertial navigation system. However, the sensor can only provide the attitude information. For the dead reckoning or distance measurement, we can only use the acceleration sensors in the IMU.

ADIS16470 IMU Introduction

ADI's ADIS16470 is a miniature MEMS IMU that integrates a 3-axial gyroscope and a 3-axial accelerometer. It supplies 8°/hr bias stability for the gyroscope and 13 µ*g* bias stability for the accelerometer, while its key parameters are factory calibrated. Also, ADIS16470's low cost price is attractive in the same level parts and is widely used by many customers. In this article, we use a microcontroller to communicate with ADIS16470 with SPI interface.

Geomagnetic Sensor Introduction

A geomagnetic sensor is a sensor used to measure the geomagnetic field in the compass' body coordinates (that is, frame), which provides an absolute reference for the heading. Its x, y, and z component values are projected from the local geomagnetic field. There are two key drawbacks to this kind of sensor—one is that its accuracy and resolution cannot be high—for example, the commonly used compass sensor HMC5883L from Honeywell only has a 12-bit resolution. The other drawback is that the sensor is easily interfered with by its surrounding environment, since the geomagnetic field is very weak, from milligauss to 8 gauss.

Despite these drawbacks, it can still be used in many circumstances, such as open field, low EMI environments, etc. By loosely coupling the geomagnetic sensor to the IMU, we can use it in most environments.

In this article, we use a high performance compass sensor, RM3100 from PNI Sensor Corporation, that supplies a 24-bit resolution. PNI uses the active excitation method to improve the immunity from noise.

Calibration of Compass Sensor

Before using a compass sensor, it needs to be calibrated to eliminate two main errors. One is offset error, which is originally caused by the sensor's and the circuit's offset error. The other is scale error. Both errors are easily interfered with by the surrounding magnetic environment. For example, if there is an x-axis direction external magnetic field applied to the sensor, it will give out an external x-axis offset error. Simultaneously, the x-axis scale will also be different to the y- and z-axis.

The method commonly used to calibrate a magnetic sensor is to rotate the sensor as a circle in an x-y plane and then draw out the data. The geomagnetic field strength at a place is a constant value, so the data drawn should be a circle; however, we will, in fact, see an oval, which means we need to move and rescale the oval to a circle centered at zero.

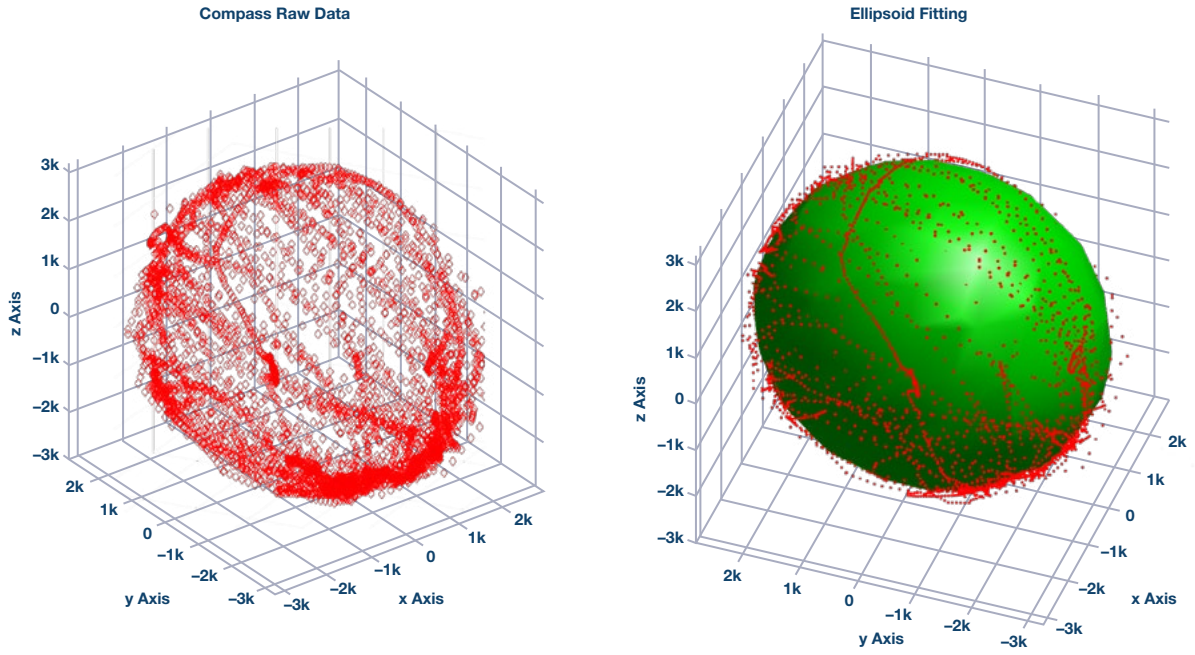

Figure 1. The raw compass data distribution (left) and compass data after the usage of the ellipsoid fitting (right).

The method of 2D calibration mentioned above has some drawbacks and requires an accelerator to measure its inclination. We use a 3D spherical fitting method to calibrate the compass sensor. First, we need to rotate the sensor to every direction in x-y-z space and draw its values in a 3D coordinate. Then we need to fit the data as an ellipsoid using the minimum squared error (MSE) method.

An ellipsoid equation can be expressed as

$$aX^2 + bY^2 + cZ^2 + 2fXY + 2gXZ + 2hYZ + 2pX + 2qY + 2rZ + d = 0 \quad (1)$$

where X, Y, and Z are the geomagnetic components of the compass output in its three directions. Fitting these values to an ellipsoid means we need to get a best value set of the coefficients. We define the coefficients as:

$$\sigma = [a\ b\ c\ f\ g\ h\ p\ q\ r\ d]^T$$

when fitting, we define vector as:

$$\beta = [X^2\ Y^2\ Z^2\ 2XY\ 2XZ\ 2YZ\ 2X\ \ 2Y\ 2Z]^T$$

so we need to calculate a best σ, and use Equation 2 to find the minimum value:

$$min\ (\sigma^T \beta^T \beta\sigma) \quad (2)$$

This way we can get the fitting result shown in Figure 1.

To calibrate the sensor, we need to stretch and move the fitted ellipsoid to a sphere centered at zero. We use a matrix singular value decomposition (SVD) method to do this calibration. The postcalibration sphere is shown in Figure 2.[1,2]

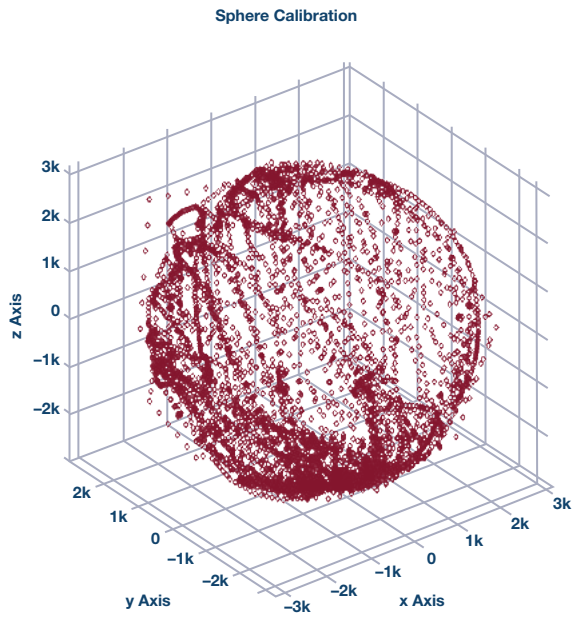

Figure 2. The compass data after sphere calibration with the SVD method.

After calibration, we can see the measured magnetic field strength (sphere radius) will keep to a nearly constant value, as shown in Figure 3.

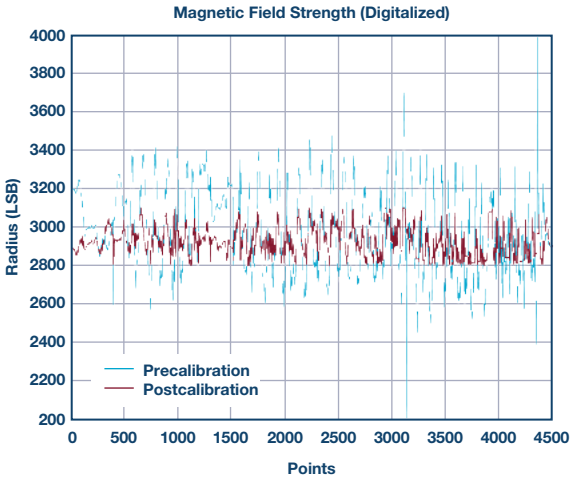

Figure 3. Magnetic field comparison between precalibration and postcalibration.

Attitude and Heading Reference System Using ADIS16470 and a Compass

An AHRS consists of sensors on three axes that provide attitude information, including roll, pitch, and yaw. AHRS is a concept from aircraft navigation. We use it to describe the orientation; that is, attitude.

Before introducing our method, it is necessary to explain the reason for fusion to find the attitude first. In fact, there are three kinds of sensors in our system now: gyroscope, accelerator, and compass.

The gyroscope gives out the angular rate of rotation around each axis. By integrating the angular rate, we can find the rotation angle. If we know the initial heading, we will always get the heading attitude. Because of integration, the gyroscope's unstable bias will be accumulated, which will lead to an angle error. Besides, the Gaussian distributed noise from the gyroscope will be integrated to a Brownian moving process and lead to random walking error. Thus, it is difficult for us to use a gyroscope for an extended period of time, and gyroscopes need to be calibrated periodically.

The accelerator provides the acceleration rate of movement in each axis direction. In static status, we can get the angle between each axis and gravity acceleration rate. Because the gravity acceleration is constant in direction and value, we can get the heading attitude relative to the direction of gravity. However, this method uses gravity acceleration as a reference, so the angle rotating around gravity acceleration cannot be solved.

The compass provides the value in each axis projected from the geomagnetic field. We can derive the angular value from the relation between each axis and the geomagnetic field direction, which is also a constant vector. As mentioned in the previous section, because of poor immunity to the external magnetic field, the compass needs a low interference environment.

From this explanation, we can see it is difficult to rely on only one sensor to find the attitude, and that we need to use two or three sensors in combination and fuse the information. This article involves accelerators, gyroscopes, and geomagnetic compasses to find the attitude. This kind of fusion is called the magnetic, angular rate, and gravity (MARG) system.

Extended Kalman Filter Design and Sensor Fusion

There are multiple methods to fuse IMU and compass data together, such as complementary filters, statistics ARMA filters, Kalman filters, and more. We use an extended Kalman filter in this article.

First, we need to introduce some definitions used in this article.

Coordinate Definition

The heading, or orientation, is the relation between two coordinates (that is, frames). One coordinate is always changing, the other remains constant. For a coordinate definition method, we use navigation coordinates and body coordinates. As opposed to north-east-down (NED) or geographic methods, we define the initial body coordinate value measured as the navigation coordinate, which is a constant coordinate afterward. The mapping (projecting) matrix from the body coordinate to the navigation coordinate is defined as

$$C_b^n$$

Attitude Definition

Different from the Euler angles or direction cosine matrix (DCM), we use quaternions here, defined as

$$q$$

which is commonly used in navigation to avoid argument.[3]

Attitude Updating Using a Kalman Filter

The kinematics equation, that is, the state transition equation, we use in this article is a deviation format, which is not linear, so we need to use an EKF with first-order linear approximation to the deviation equation. For EKF designs, we define

$$x = [\omega \;\; q]^T$$

a 1 × 7 vector as a state variable, where

$$\omega = [\omega_x \; \omega_y \; \omega_z]^T$$

is the angular rate, and

$$q = [a \; b \; c \; d]^T$$

is the attitude quaternion.

$$z = [\omega \;\; q]^T$$

a 1 × 7 vector, is the observation variable, which has the same component as the state variable.

$$A = \begin{bmatrix} \frac{1}{T}(\omega_k - \omega_{k-1}) & \frac{1}{2} q_{k-1} \omega_{k-1} \end{bmatrix}$$

a 7 × 7 matrix, is the state transition matrix, where the first part in A is the digitalized differential equation of the angular rate, and the second part is the digitalized quaternion updating equation, which is derived from the kinematics equation.

$$H = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

a 7 × 7 matrix, is the observation matrix.

$$P = E[e^T e]$$

is the error covariance matrix, a 7 × 7 matrix, where

$$e$$

is the error vector estimated, $\hat{x}$, from the real, x. We set the initial error to a relatively small value in testing. It will converge to a small value automatically.

$$R, Q$$

are set as the noise covariance of state transition noise and observation noise. We get their initial value,

$$R_0$$

and

$$Q_0$$

by measuring the square of ac rms value of the gyroscopes and the accelerators. While keeping the IMU and compass in static status, we set

$$R_0 = Q_0$$

With this definition, our Kalman filter will be accomplished with the following five steps:

Step 1: calculate the Kalman gain, *K*, using Equation 3:

$$K_k = P_k^- H^T (HP_k^- H^T + R_k) \quad (3)$$

Step 2: calculate the error covariance matrix, *P*:

$$P_k = (I - K_k H) P_k^- \quad (4)$$

Step 3: output the estimated status, $\hat{x}$:

$$\hat{x}_k = \hat{x}_k^- + K_k(z_k - H_k\hat{x}_k^-) \quad (5)$$

Step 4: project the status, $\hat{x}^-$:

$$\hat{x}_{k+1}^- = A\hat{x}_k \quad (6)$$

Step 5: project the error covariance matrix, P^-:

$$P_{k+1}^- = AP_kA^T + Q_k \quad (7)$$

The process can be simply described as the block diagram in Figure 4.

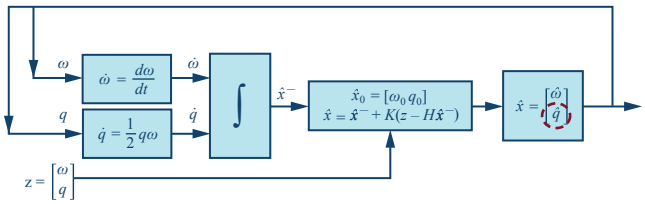

Figure 4. The Kalman filter flow chart for updating attitude.

Sensor Fusion Based on MSE

In the previous section, the observation variable is

$$z = [\omega \;\; q]^T$$

wherein there is no information from the compass. Since ω is the angular rate, we can only use the quaternion to import compass data *q*. We used the MSE method to get *q*, the component in the observation variable.

We define the variables as follows:

m_b and a_b: the compass magnetic value and acceleration value in the body frame.

m_n and a_n: the compass magnetic value and acceleration value in the navigation frame.

m_{n0} and a_{n0}: the initial static compass magnetic value and acceleration value in the navigation frame.

$$C_b^n$$

is the attitude transformation matrix from the body frame to the navigation frame, expressed using quaternion, which can be written as

$$C_b^n(q)$$

which gives us the error, ε, between the initial value in the navigation frame and the value mapped to the navigation frame from the body frame in real time.

Based on the previous definition, the MSE method can be used to get a best

$$C_b^n(q)$$

by minimizing Equation 8:

$$f(q) = \varepsilon^T \varepsilon = \left(\begin{bmatrix}a_{n0}\\ m_{n0}\end{bmatrix} - C_b^n(q)\begin{bmatrix}a_b\\ m_b\end{bmatrix}\right)^T \left(\begin{bmatrix}a_{n0}\\ m_{n0}\end{bmatrix} - C_b^n(q)\begin{bmatrix}a_b\\ m_b\end{bmatrix}\right) \quad (8)$$

By taking the derivation of *f(q)* and making it equal zero,

$$\frac{f(q)}{q} = 0 \quad (9)$$

we will get a best *q* in variance meaning. We used the Gauss-Newton method to solve the nonlinear equation above with first-order gradient convergence.

By combining the angular rate, we will get the observation variable,

$$z = [\omega \;\; q]^T$$

which fused compass data and IMU data in the Kalman filter.

The process can be simply described by the block diagram in Figure 5.

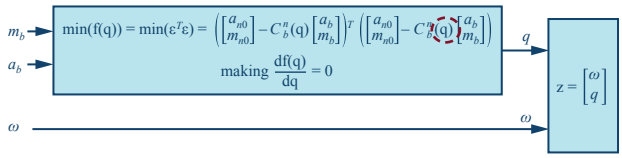

Figure 5. A sensor fusion block diagram using the MSE method.

Loose Coupling

As previously mentioned, we often encounter circumstances where compass sensors cannot be used. If the magnetic data is interfered with, the solved attitude accuracy will be worse than when using an IMU only. Therefore, we use loose coupling, which judges whether the magnetics sensor is available or not. When the magnetics sensor is not available, we will use only the IMU to find the attitude, and when the magnetics sensor is available, we will use the fusion algorithm to find the attitude, as shown in Figure 6.

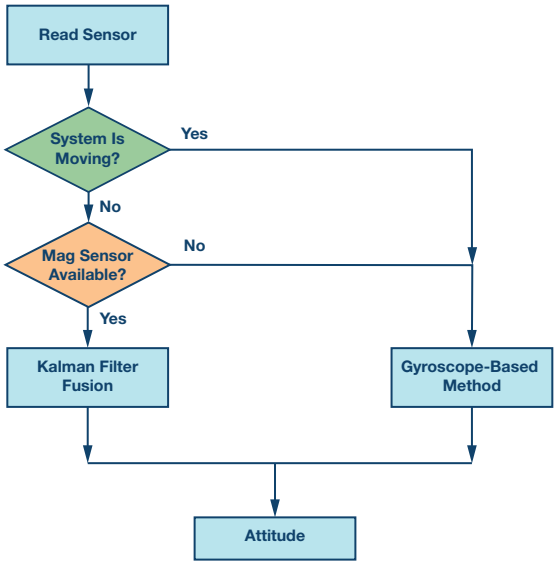

Figure 6. The attitude calculating flow chart.

After getting new data, or in a new attitude solving cycle (in some systems the sampling cycle is different from the attitude resolving cycle, but we are doing single sample cycle resolving here), we calculate the magnitude of acceleration. If it does not equal 1 *g*, we will not use the accelerator's output for the attitude calculation. Then we calculate the magnitude of the compass output and compare this with the initial value. If they do not equal each other, we will not use the geomagnetic sensor's data in this cycle. When both conditions are met, we will use the Kalman filter and perform MSE fusion.

Dead Reckoning (DR) Using ADIS16470

In navigation, dead reckoning is the process of calculating one's current position by using a previously determined position, and advancing that position based on known or estimated speeds or acceleration over a resolving cycle. The ADIS16470 accelerator will be used here. Based on the attitude resolved in the last section, we get the strapdown system's moving orientation, then we need to calculate the distance in the orientation, and the position will finally be determined.

Dead Reckoning Method Introduction

Strapdown dead reckoning needs to track the position of an INS using a specific force equation, which is based on the acceleration measurement. Specific force equations can be simply described as Equation 10, Equation 11, and Equation 12:

$$a_e(t) = C_b^e a_b(t) \tag{10}$$

$$v_e(t + \delta t) = v_e(t) + \delta t \times (a_e(t + \delta t) - g_e) \tag{11}$$

$$s_e(t + \delta t) = s_e(t) + \delta t \times (v_e(t + \delta t)) \tag{12}$$

Where a_e is the acceleration in the Earth frame, a_b is the acceleration in the body frame, v_e is the velocity in the Earth frame, s_e is the distance in the Earth frame, g_e is the gravity acceleration in the Earth frame, which is [0 0 1] in *g* units. We need to emphasize that the Earth frame is different from the navigation frame—the Earth frame is NED oriented. This δt is the resolving cycle.

The first equation finds the acceleration projection from the IMU body frame to the Earth frame as the format

$$C_b^e$$

shows.

The second equation integrates or accumulates the acceleration into velocity; however, since the measured acceleration involves a gravity component, the gravity needs to be subtracted.

Similar to Equation 11, Equation 12 integrates velocity into the distance.

There are several problems in the traditional method.

- Accelerator outputs always have bias, which is combined with gravity, making it difficult to be subtracted in Equation 10, so the more accurate expression should be:

$$\begin{bmatrix} a_n^e \\ a_e^e \\ a_d^e \end{bmatrix} = C_b^e \left(\begin{bmatrix} a_x^b \\ a_y^b \\ a_z^b \end{bmatrix} - \begin{bmatrix} a_x^{bias} \\ a_y^{bias} \\ a_z^{bias} \end{bmatrix} \right) - \begin{bmatrix} 0 \\ 0 \\ g \end{bmatrix} \tag{13}$$

  unless using some professional equipment, such as a dividing header.

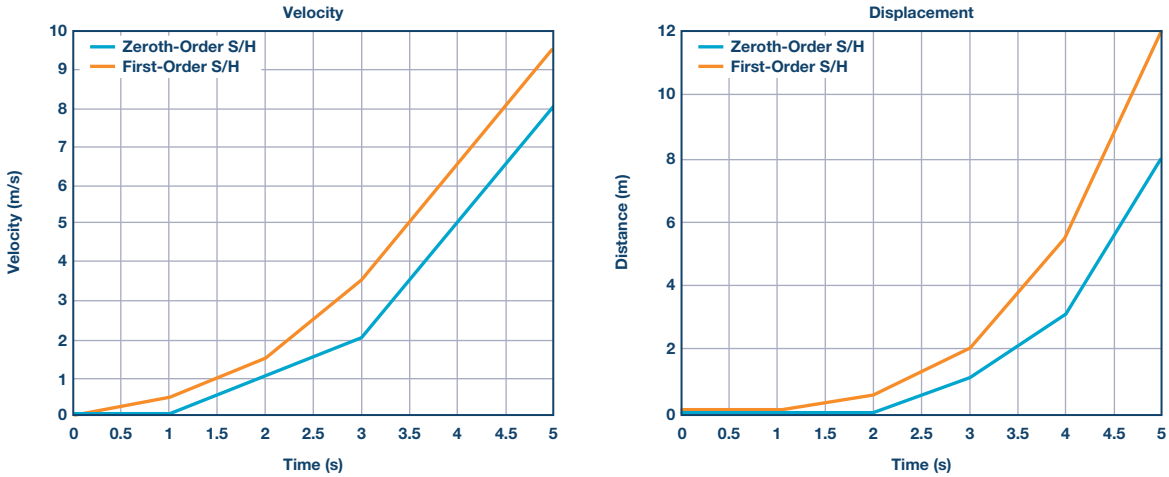

Figure 7. The comparison between zeroth-order and first-order integration methods in velocity calculation.

- The numerical integration method, the traditional method, commonly uses the zeroth-order holder method (the previous value) to do integration. However, for continuous movement, this will introduce significant error. For example, let's compare the following methods:

Method 1:

$$v_i = v_{i-1} + a_{i-1}t$$

(Zeroth-order holder)

Method 2:

$$v_i = v_{i-1} + a_{i-1}t + \frac{a_i - a_{i-1}}{2}$$

(linear interpolation)

With an acceleration of 0.5 m/s² across 5 seconds, the displacement will differ up to 4 m. The simulation result shows in Figure 7.

Based on the previous discussion, we modified two points of the traditional specific force equation for our application:

- We don't use the Earth coordinates as the navigation frame. Instead, as we did in finding the previous attitude, we use the initial attitude

  $$\left[a_{x0}^n \; a_{y0}^n \; a_{z0}^n\right]$$

  as the navigation frame. In this way, both bias and gravity can be cancelled easily as in Equation 14:

  $$\begin{bmatrix} a_x^n \\ a_y^n \\ a_z^n \end{bmatrix} = C_b^n \left(\begin{bmatrix} a_x^b \\ a_y^b \\ a_z^b \end{bmatrix} \right) - \begin{bmatrix} a_{x0}^n \\ a_{y0}^n \\ a_{z0}^n \end{bmatrix} \quad (14)$$

  Though the bias and gravity components are contained in the initial attitude, this way we do not need to separate them to get each component, and we instead can directly subtract them.

- As compared between zeroth-order holder and first-order interpolation, we use the first-order to receive a more accurate integration result.

Kinematics Pattern and Zero Speed Updating Technology (ZUPT)

By using the IMU's initial value as the navigation frame, we can partially cancel the accelerator's initial bias impact. However, even if we can accurately measure the bias using the dividing header before we use a device, it is still difficult to cancel, unless we use another accurate sensor to periodically calibrate it. This is mainly caused by two parts: one is bias instability, which means the bias we measured before is not the actual bias now. The other is velocity random walk, which is integral to the acceleration. The previously mentioned undesired characteristics will make our calculated distance drift significantly. Even when we stop moving and remain static, the speed integrated from the acceleration still exists, and the distance will still increase.

To solve this problem, we need to find a way to reset the speed by using ZUPT technology. ZUPT technology closely relies on the application, so we need to get the kinematics characteristics of our system and application, then give some rules to our algorithm. The more kinematics patterns we find, the more accurate our result will be.

We apply our experiment by moving a swivel chair with the SINS system in place. Since our research is not limited to a specific application, we use the following kinematics assumptions:

- For dead reckoning, there is no z-axis moving in the navigation frame. This limit is only for dead reckoning, it is not used in attitude resolving. Obviously, we are moving the system in 2D space. This helps cancel the z-axis error.
- All turning happens after stopping. If turning happens when moving, attitude resolving will be interfered with since extra acceleration will be involved.
- The acceleration cannot remain unchanged for more than 500 ms if the system is moving. Velocity cannot stay unchanged for longer than 2 s. Since we are pushing or pulling a swivel chair, it is difficult to manually keep the force accurately unchanged for more than 500 ms, and it is difficult for a human to keep pushing a swivel chair with uniform speed for more than 2 s. In fact, we are using this rule to do ZUPT.
- The acceleration cannot be larger than ±1 m/s². This rule is used for some noise filtering, which is based on our pulling or pushing force on the chair, which will not be large.

As we can see in Figure 8, when the system is moving in the X direction (after projected to the navigation frame), the Y direction will also generate acceleration, after integration, the Y direction speed will not be zero, which means even if we are only moving in the X direction, the dead reckoning system will still give us the Y component.

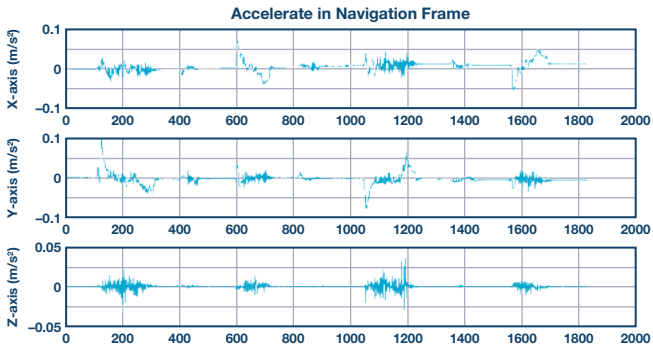

Figure 8. The acceleration in three directions in the navigation frame.

Based on the third kinematic assumption, we can use ZUPT to cancel this error. The integrated velocity after ZUPT is shown in Figure 9.

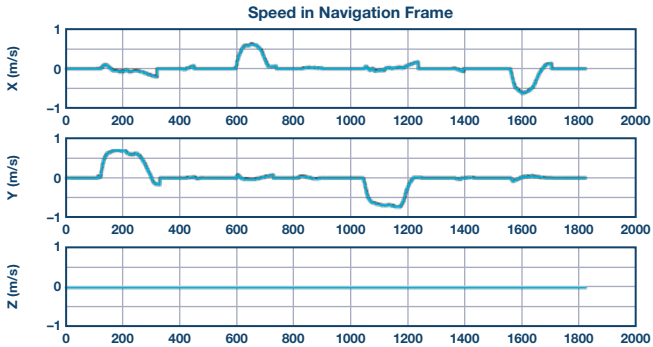

Figure 9. The velocity in three directions in the navigation frame.

Though we used the third assumption, as previously shown, the error still cannot be totally cancelled. The error cancellation depends on the threshold to the set zero acceleration and zero speed. However, most errors have been corrected.

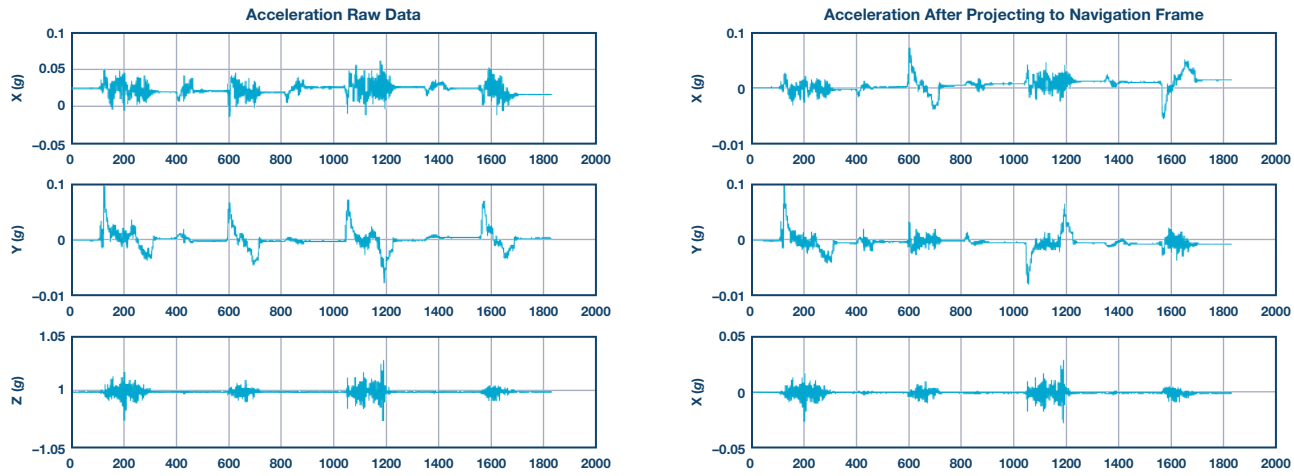

Figure 10. The acceleration in the body frame (left) and in the navigation frame (right).

Baseline Shifting Cancellation

Although ZUPT is used, the zero acceleration may still be unreachable at times. This results in two factors:

- We can't totally cancel the bias instability error and the velocity random walk using ZUPT.
- The attitude we resolved has some error, which will lead to the projected (from body frame to navigation frame) acceleration error.

Take Figure 10 for example. The left picture in Figure 10 is the raw data (body frame) from ADIS16470 and the right picture in Figure 10 is the acceleration projected in the navigation frame. It can be seen that the projected acceleration is not zero when it stops moving. As it always changes, we call this baseline shifting.

In order to cancel the baseline shifting, we need to continuously get the shifted bias in real time and subtract it from the projected acceleration. The result is shown in Figure 11.

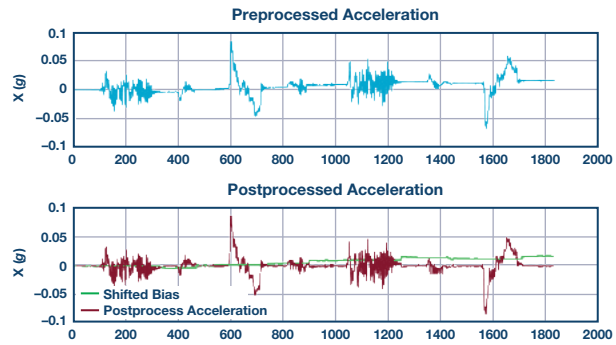

Figure 11. The acceleration before (top) and after (bottom) baseline shift cancellation.

The upper plot is the acceleration before baseline shift cancellation, the green trace in the bottom plot is the baseline shifting we calculated, and the red trace is the acceleration after baseline shift cancellation.

The dead reckoning process can be described briefly using the block diagram in Figure 12. We input the body frame acceleration a_b and the attitude transforming matrix (from AHRS)

$$C_b^n$$

to the DR system. Once this is done, we will get the position in the navigation frame.

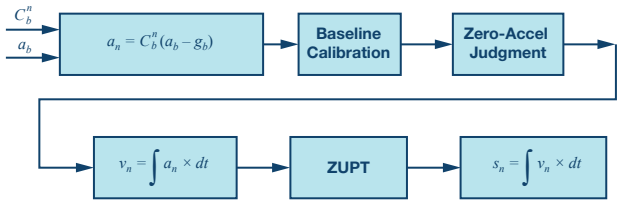

Figure 12. The flow chart for dead reckoning.

Experiment Result and Conclusion

Experiment Result

We build our system, as in Figure 13, by connecting the ADIS16470 evaluation board and the RM3100 compass evaluation board to ADI's ADuCM4050 board using an SPI port. The ADuCM4050 adjusts the data format and does time synchronization (since the data rate of the IMU and the compass are different). Then the captured data is transmitted to the computer using the UART. All the calculations, including calibration, AHRS, and DR, are performed in MATLAB®.

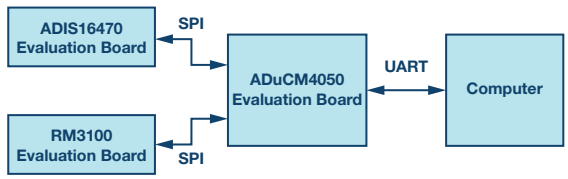

Figure 13. The experiment platform setup.

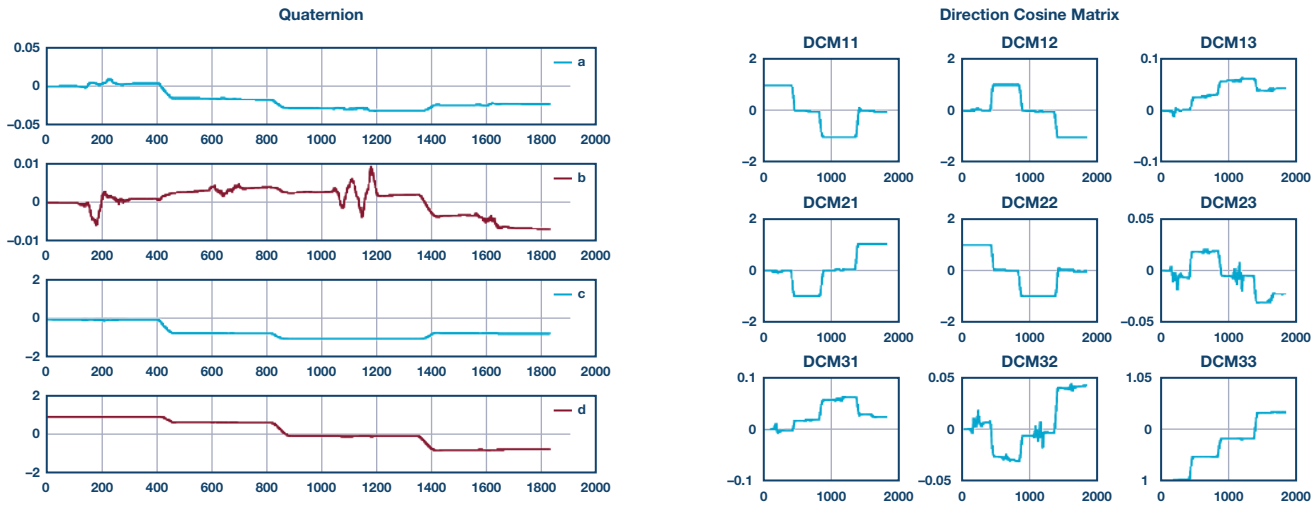

Figure 14. The attitude in quaternion format (left) and DCM format (right).

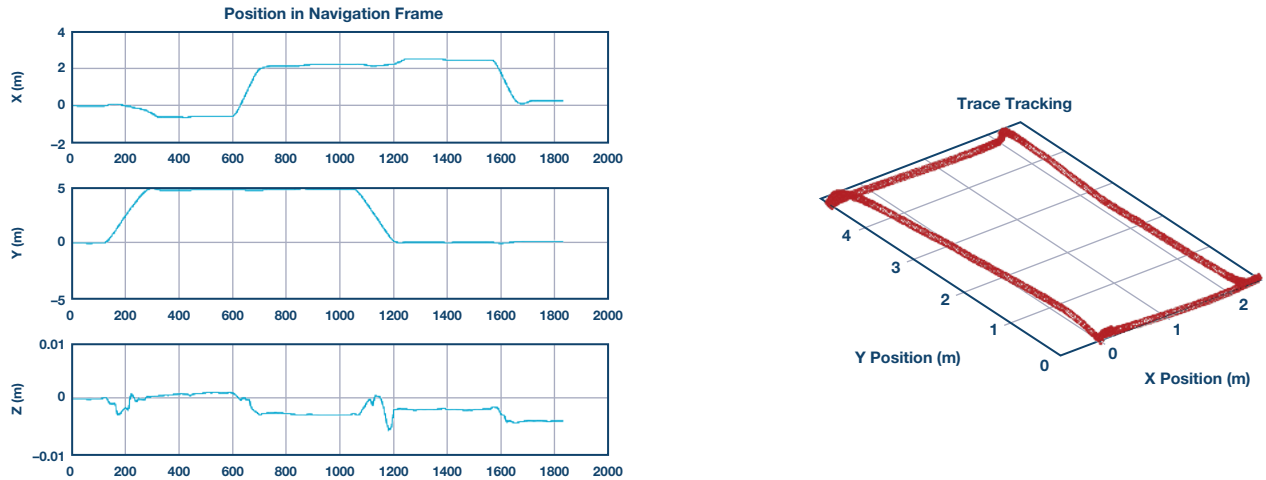

Figure 15. The position calculation result.

The experiment was implemented by placing the boards and computer on a swivel chair and pushing the swivel chair around a circle in our laboratory.

- AHRS output: The attitude is shown in quaternion format and DCM format as shown in Figure 14.
- DR output: The dead reckoning result with X-Y-Z position and 3D plot are shown in Figure 15.

Conclusion

This article shows a basic process used to build a navigation system using ADI's IMU ADIS16470 and geomagnetic sensor RM3100 by introducing the calibration, AHRS, and DR methods we used. With limited conditions, such as the platform and experiment environment, it is difficult for us to further test the platform and algorithm.

There are a lot of methods that can be used to improve the result, for example:

- Using an odometer or UWB distance measurement to fuse the accelerator with the IMU to get better distance in DR.
- Using a more complicated kinematics model that involves more characteristics at the sensor level and system level in AHRS and DR, such as the vibration, acceleration, and deceleration models of the system, the ground surface flatness, etc. This means giving more boundary conditions to our calculation to achieve more accurate results.
- Using more accurate numerical calculation methods, such as using Simpson's rule or cubic splines interpolation to do integration in DR, or by using the Newton method instead of the Gauss-Newton method to solve nonlinear MSE equations, etc.

The last, but most important, point we find in experiments is that INS is extremely closely related to the application, or the kinematics pattern. For example, we performed the experiment in two places: a laboratory without carpeting on the floor and an office with carpeting. The DR result shows a huge difference if we use the same set of parameters. Accordingly, no matter which application, such as patient tracking, AGV navigation, or parking localization, or for different conditions in the same application, we all need to comprehensively understand its kinematics model.

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Van Yang

Finally, a 12 V to 12 V Dual Battery Automotive Bidirectional DC-to-DC Controller for Redundancy

By **Bruce Haug**

Background

The signs are everywhere that the self-driving car revolution is about to shift into full gear. Automotive companies are joining up with tech giants like Google and Uber, as well as prominent start-ups, to develop the next-generation autonomous vehicles that will alter our roads and throughways and lay the framework for future smart cities. They're harnessing technological advances such as machine learning, the Internet of Things (IoT), and the cloud in order to accelerate this development.

More significantly, autonomous vehicles will advance the industry disruption already set in motion by popular ride-sharing services like Uber and Lyft. The pieces are coming together to create a world where intelligent and driverless vehicles become the future of transportation.

Eventually, all self-driving cars will employ a combination of sensors, cameras, radar, high performance GPS, light detection and ranging (lidar), artificial intelligence (AI), and machine learning to achieve a level of autonomy. Connectivity to secure and scalable IoT, data management, and cloud solutions are also important to the mix, as they provide a resilient and high performance foundation on which to collect, manage, and analyze sensor data.

The rise of the connected vehicle has far-reaching societal implications, from environmental benefits to improved safety. Fewer cars on the road also means a reduction in greenhouse gas emissions, leading to lower energy consumption and better air quality.

For both self-driving cars and smart roadway systems, endpoint telemetry, smart software, and the cloud are essential enablers. The onboard cameras and sensors in autonomous vehicles collect vast amounts of data, which must be processed in real time to keep the vehicle in the right lane and operating safely as it heads to its destination.

Cloud-based networking and connectivity is another important part of the mix. Autonomous vehicles will be outfitted with onboard systems that support machine-to-machine communications, allowing them to learn from other vehicles on the road in order to make adjustments that account for weather changes and shifting road conditions such as detours and in-path debris. Advanced algorithms and deep learning systems are central to ensuring that self-driving cars can quickly and automatically adapt to changing scenarios.

Beyond the specific components, such as scalability of cloud computing infrastructure and intelligent data management, there is a need for redundancy of mission critical systems, including power sources. There are previously released redundant battery solutions available, like the LTC3871 which works with two batteries that have different voltage ratings, such as a 48 V Li-Ion and 12 V lead-acid battery. However, most of these existing solutions do not provide redundancy for same battery voltages, like two 12 V, 24 V, or 48 V batteries. Up until now, that is.

Clearly there is a need for a bidirectional, buck-boost dc-to-dc converter that can go between two 12 V batteries. Such a dc-to-dc converter could be used to charge either battery and allow both batteries to supply current to the same load. Furthermore, if one of these batteries should fail, that failure needs to be detected and isolated from the other battery, so that the other battery continues to provide power to the load without any disruption. The recently released LT8708 bidirectional dc-to-dc controller from Analog Devices solves this critical function of allowing two batteries with the same voltage to be hooked up by utilizing the LT8708 controller.

A Single Bidirectional IC Solution

The LT8708 is a 98% efficient bidirectional buck-boost switching regulator controller that can operate between two batteries that have the same voltage, which is ideal for redundancy in self-driving cars. It can operate from an input voltage that can be above, below, or equal to the output voltage, making it well-suited for two 12 V, 24 V, or 48 V batteries commonly found in electric and hybrid vehicles. The LT8708 operates between two batteries and prevents system shutdown should one of the batteries fail. This device can also be used in 48 V/12 V and 48 V/24 V dual battery systems.

The LT8708 uses a single inductor and operates over an input voltage range from 2.8 V to 80 V while producing an output voltage from 1.3 V to 80 V, delivering up to several kilowatts of power depending on the choice of external components and number of phases. It simplifies bidirectional power conversion in battery/capacitor backup systems that need regulation of V_{OUT}, V_{IN}, and/or I_{OUT}, I_{IN}, both in the forward or reverse direction. This device's six independent forms of regulation allow it to be used in numerous applications.

The LT8708-1 is used in parallel with the LT8708 to add power and phases. The LT8708-1 always operates as a slave to the master LT8708, can be clocked out-of-phase, and has the capability to deliver as much power as the master. Up to 12 slaves can be connected to a single master, proportionally increasing the power and current capabilities of the system.

Forward and reverse current can be monitored and limited for the input and output sides of the converter. All four current limits (forward input, reverse input, forward output, and reverse output) can be set independently using four resistors. In combination with the direction (DIR) pin, the chip can be configured to process power from V_{IN} to V_{OUT} or from V_{OUT} to V_{IN}, ideal for automotive, solar, telecom, and battery-powered systems.

The LT8708 is available in a 5 mm × 8 mm, 40-lead QFN package. Three temperature grades are available, with operation from –40°C to +125°C for the extended and industrial grades and a high temperature automotive range of –40°C to +150°C. Figure 1 shows a simplified LT8708 block diagram.

Complete Solution

The block diagram in Figure 2 shows the other parts required to complete the circuit for dual battery redundancy in an automotive application. As shown, the LT8708 works with two LT8708-1 parts to form a 3-phase solution design that can deliver up to 60 A in either direction. Additional LT8708-1 devices can be added for higher power applications up to and exceeding 12 phases. The AD8417 is a bidirectional current sense amplifier that senses the current flowing into and out of the batteries. And when this current exceeds a preset value, the LTC7001 high-side NMOS static switch driver opens the back-to-back MOSFETs to isolate either battery from the circuit.

The LTC6810-2 monitors and controls the Li-Ion battery. It accurately measures the battery cells with a total measurement error of less than 1.8 mV. Connecting multiple LTC6810-2 devices in parallel to the host processor will create additional redundancy for monitoring other voltages within the circuit. The LTC6810-2 has an isoSPI™ interface for high speed, RF immune, long distance communications, and it supports bidirectional operation. The device also includes passive balancing with PWM duty cycle control for each cell and the ability to perform redundant cell measurements.

Control Overview

The LT8708 provides an output voltage that can be above, below, or equal to the input voltage. It also provides bidirectional current monitoring and regulation capabilities at both the input and the output. The ADI proprietary control architecture employs an inductor current-sensing resistor in buck, boost, or buck-boost regions of operation. The inductor current is controlled by the voltage on the V_C pin, which is the combined output of six internal error amplifiers, EA1 to EA6. These amplifiers can be used to limit or regulate their respective voltages or currents as shown in Table 1.

Table 1. Error Amplifiers (EA1 to EA6)

Amplifier Name	Pin Name	Definition
EA1	IMON_INN	Negative I_{IN}
EA2	IMON_ON	Negative I_{OUT}
EA3	FBIN	V_{IN} Voltage
EA4	FBOUT	V_{OUT} Votalge
EA5	IMON_INP	Positive I_{IN}
EA6	IMON_OP	Positive I_{OUT}

The V_C voltage typically has a min-max range of about 1.2 V. The maximum V_C voltage commands the most positive inductor current and, thus, commands the most power flow from V_{IN} to V_{OUT}. The minimum V_C voltage commands the most negative inductor current and, thus, commands the most power flow from V_{OUT} to V_{IN}.

In a simple example of V_{OUT} regulation, the FB_{OUT} pin receives the V_{OUT} voltage feedback signal, which is compared to the internal reference voltage using EA4. Low V_{OUT} voltage raises V_C and, thus, more current flows into

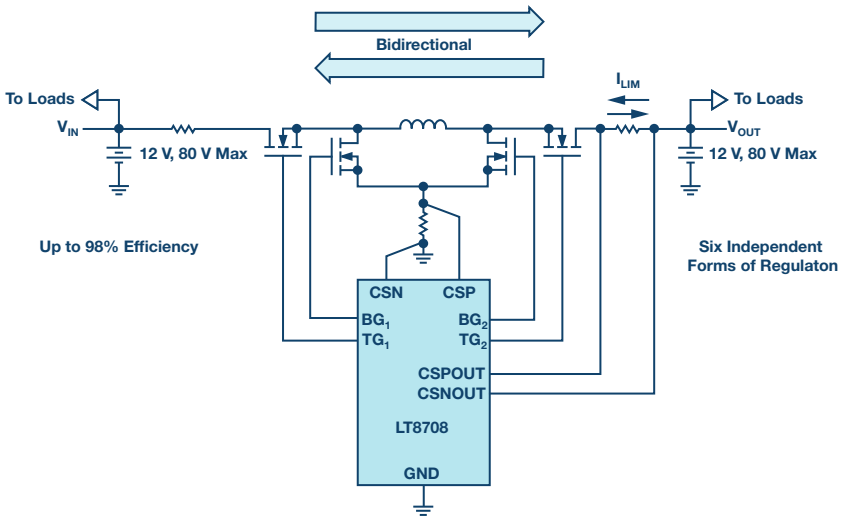

Figure 1. LT8708 simplified bidirectional dual 12 V battery application schematic.

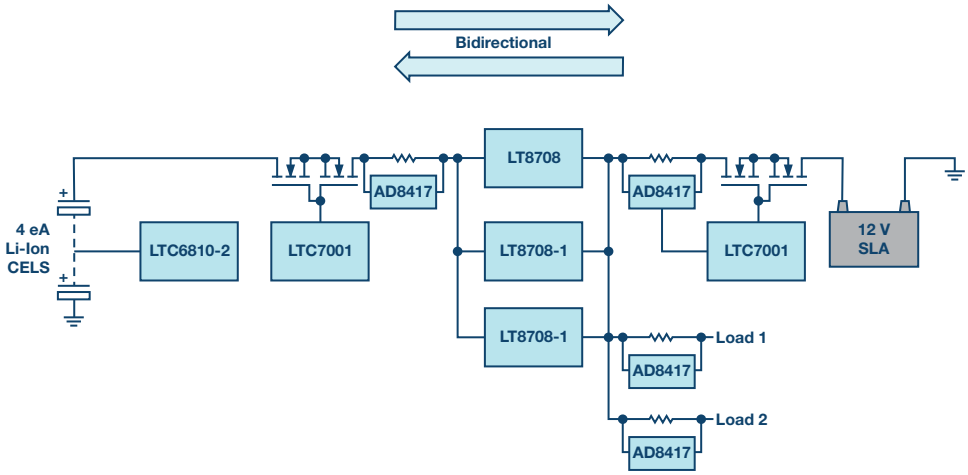

Figure 2. A dual battery redundancy block diagram for a complete solution.

V_{OUT}. Conversely, higher V_{OUT} reduces V_C, thus, reducing the current into V_{OUT} or even drawing current and power from V_{OUT}.

As previously mentioned, the LT8708 also provides bidirectional current regulation capabilities at both the input and the output. The V_{OUT} current can be regulated or limited in the forward and reverse directions (EA6 and EA2, respectively). The V_{IN} current can also be regulated or limited in the forward direction and reverse directions (EA5 and EA1, respectively).

In a common application, V_{OUT} might be regulated using EA4, while the remaining error amplifiers are monitoring for excessive input or output current, or an input undervoltage condition. In other applications, such as a battery backup system, a battery connected to V_{OUT} might be charged with constant current (EA6) to a maximum voltage (EA4) and can also be reversed, at times, to supply power back to V_{IN} using the other error amplifiers to regulate V_{IN} and limit the maximum current. See the LT8708 data sheet for additional information on this subject.

Conclusion

The LT8708-1 brings a new level of performance, control, and simplification to same voltage dual-battery dc-to-dc automotive systems. Whether using it for energy transfer between two power sources for redundancy, or for backup power in mission critical applications, the LT8708 allows users the ability to operate from two batteries or supercapacitors that have the same voltage. This capability allows automotive systems engineers to help pave the way for new advancements in automotive electronics, enabling cars to be safer and more efficient.

Bruce Haug [bruce.haug@analog.com] received his B.S.E.E. from San Jose State University in 1980. He joined Linear Technology (now a part of Analog Devices) as a product marketing engineer in April 2006. Bruce's past experience includes stints at Cherokee International, Digital Power, and Ford Aerospace. He is an avid sports participant.

Bruce Haug

Rarely Asked Questions—Issue 163 SAR Converter with PGA Achieves Dynamic Range of 125 dB

By **Thomas Tzscheetzsch**

Question:

Could a 16-bit SAR converter application reach a dynamic range of 125 dB at 600 kSPS?

Answer:

Yes, 89 dB + 18 dB + 20 dB ≥ 125 dB.

Introduction

For applications requiring a high dynamic range, a Σ-Δ converter is often used. These applications can mainly be found in the fields of chemical analysis, healthcare, and weight management. However, many of these modules are incapable of rapid conversion. The circuit in Figure 1 describes an approach for combining a high dynamic range with a high conversion rate.

The circuit in Figure 1 shows a 16-bit SAR converter with 2.5 MSPS and an upstream programmable instrumentation amplifier, which sets the gain to 1 or 100. By oversampling and digital signal processing in the FPGA, this circuit achieves a dynamic range of greater than 125 dB and is still very quiet. The high dynamic range is achieved through the automatic switching of the AD8253 and through oversampling, in which the signal is sampled at a much higher rate than the Nyquist frequency. As a rule of thumb, a doubling of the sampling frequency improves the signal-to-noise ratio (SNR) by about 3 dB at the original signal bandwidth. In the circuit shown in Figure 1, digital filtering is still applied in the FPGA to remove the noise above the signal bandwidth of interest. The principle is shown in Figure 2.

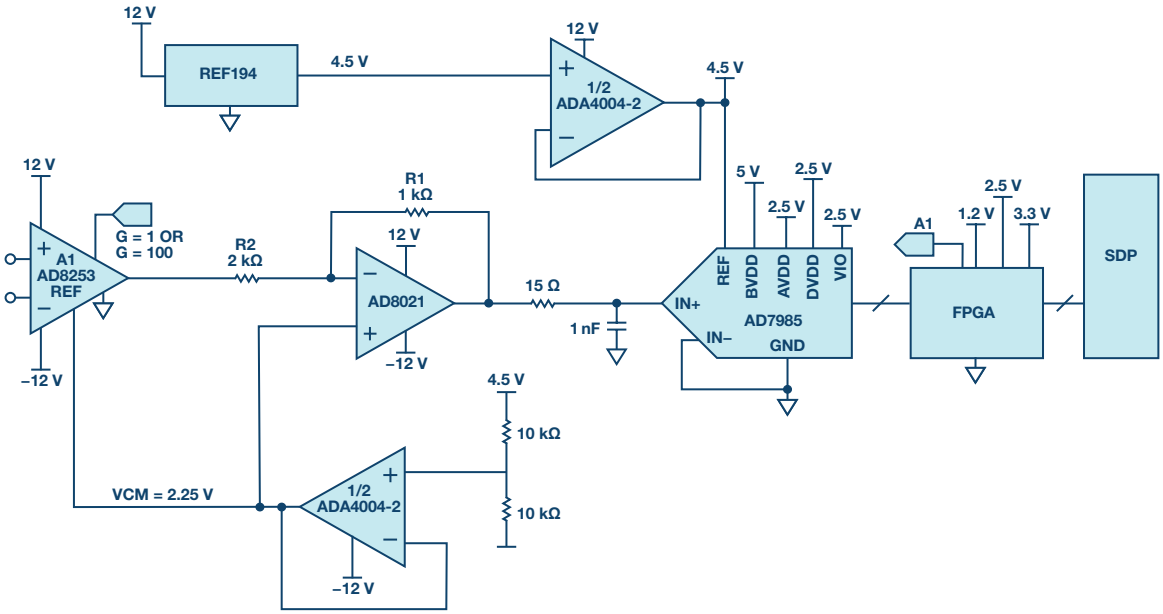

Figure 1. SAR converter with automatic gain adjustment.

To achieve the maximum dynamic range, an instrumentation amplifier is used at the input to amplify the very low signals by a factor of 100. A few considerations regarding noise are made in the following:

For the requirement of a dynamic range of >126 dB, a maximum noise level of 1 µV rms at an input signal of 3 V (6 V p-p) is yielded. The AD7985 is a 16-bit SAR converter with 2.5 MSPS. If it is operated with 600 kSPS (for a low power loss of 11 mW) and oversampling by a factor of 72, it yields a sampling rate of approximately 8 kSPS and thus a bandwidth of 4 kHz. From these conditions, a noise density (ND) of a maximum of 15.8 nV/√Hz is yielded. This value is important for the selection of the correct instrumentation amplifier. The ADC typically has an SNR of 89 dB, while oversampling by a factor of 72 gives an additional 18 dB, and thus about 20 dB are still needed to reach the target of 126 dB, which is the task of the instrumentation amplifier. The AD8253 has a value of 11 nV/√Hz at a gain of 100. The following AD8021, which is used as an ADC driver and for level adjustment, adds another 2.1 nV/√Hz of noise.

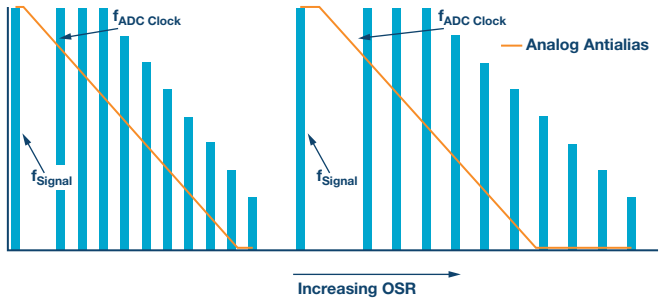

Figure 2. An increase in oversampling removes part of the noise.

The analog signal chain is completed by the voltage reference ADR439 (or REF194) as well as an ADA4004-2 as a reference buffer and driver for generating the offset voltages.

Apart from the components in the analog path, the FPGA (or processor) is important for circuit performance. A key task is to switch the gain of the instrumentation amplifier from 1 to 100. For this purpose, a number of threshold values are programmed to ensure that the ADC is not saturated. Thus, the AD8253 is operated with a gain of 100 at input voltages up to approximately 20 mV, which leads to a maximum of 2.0 V at the ADC input. Then the FPGA reduces the gain of the AD8253 to 1 with no delay to prevent overdrive (see Figure 3).

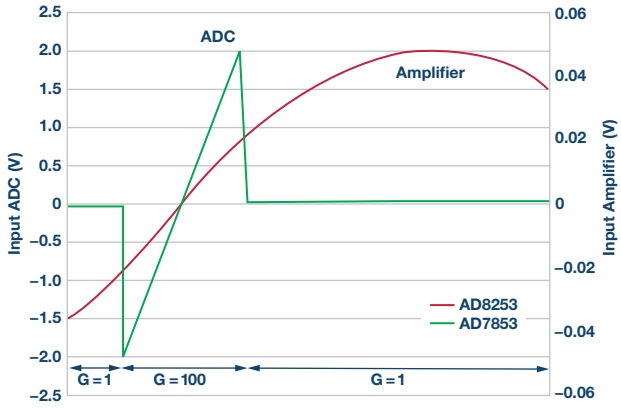

Figure 3. Example of a gain switch.

Variations of the circuit can be operated with other ADCs such as the AD7980 (16-bit, 1 MSPS), the AD7982 (18-bit, 1 MSPS), or the AD7986 (18-bit, 2 MSPS). Likewise, instead of the AD8253 with gains of 1, 10, 100, and 1000, an instrumentation amplifier such as the AD8251 with a lower range can be used (gains of 1, 2, 4, and 8). Variations in the choice of reference voltage are also possible.

A complete development system can be found at *analog.com/CN0260*.

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At the beginning of his career, he worked as an electronics engineer in a machine building company from 1992 to 1998, as head of the department. After his study of electrical engineering at the University of Applied Sciences in Göttingen, he worked at the Max Planck Institute for solar system research as a hardware design engineer. From 2004 to 2010, he worked as an FAE in distribution and worked with Analog Devices' products.

Thomas Tzscheetzsch

Notes

Notes

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