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In This Issue

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Bernhard became editor of *Analog Dialogue* in March 2017. He has been with Analog Devices for over 25 years, starting at the ADI Munich office in Germany. In his current role as the chief technical editor, he is responsible for the worldwide technical article program within Analog Devices.

Bernhard has worked in various engineering roles including sales, field applications, and product engineering, as well as in technical support and marketing roles.

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Automotive Radar Sensors and Congested Radio Spectrum: An Urban Electronic Battlefield?

By **Sefa Tanis**

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As automotive radars become more widespread, the heavily occupied RF spectrum will resemble an electronic battlefield in an urban environment. Radar will face a combination of unintentional or intentional jamming attacks, and designers must implement counter-jamming techniques like ones used in electronic warfare (EW).

An automotive radar could typically experience a denial or deceptive jamming attack. Denial jamming blinds the victim radar. This technique reduces the signal-to-noise ratio and, as a result, the probability of target detection is degraded. On the other hand, deceptive jamming makes victim radar "think" there are false targets. The victim radar loses the ability to track real targets and, hence, the victim's vehicle behavior is severely influenced.

These jamming attacks could originate from mutual interference between automotive radars or happen deliberately by simply pointing a strong continuous wave (CW) signal into victim radar using inexpensive HW.

While current jamming avoidance techniques might be adequate for today, with the proliferation of radar sensors, a resilient type of mitigation techniques will need to be used by itself or in conjunction with the avoidance approaches. Resilient techniques include time frequency domain signal processing or complex radar waveforms.

Radar Waveforms

The radar waveform is one of the critical system parameters that determines the sensor performance in the presence of jammers. Automotive radars in today's 77 GHz band mainly use FMCW type waveforms. In FMCW radar, a CW signal is linearly swept or chirped in frequency across an RF band. Figure 1 shows an example FMCW chirp sequence (CS) waveform.

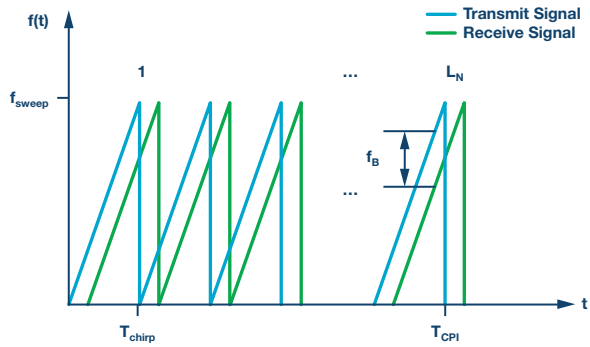

Figure 1. FMCW CS example.

The frequency difference (f_b, beat frequency) is proportional to the distance R to the target and can be determined by the following relation:

$$f_B = \frac{2}{c}\frac{f_{sweep}}{T_{chirp}}R \quad (1)$$

Impacts of Jamming

Jamming occurs in a dense RF environment when FMCW radar sensors are operating in the same portion of the frequency band. See a typical oncoming automobile jamming example in Figure 2.

Denial Jamming

An arbitrary FMCW type strong jamming signal that falls into the receiver bandwidth raises the noise floor of the victim radar. This denial jamming may cause small targets (that is, small radar cross section (RCS)) to disappear due to the poor SNR.

A denial attack could also purposefully be carried out by simply beaming a strong CW signal into the victim FMCW radar. The impact in the victim radar would be similar to an FMCW jamming case (see Figure 4).

Deceptive Jamming

If the jamming signal sweep is synchronized but delayed with the victim radar, then the impact would be deceptive false target generation at a fixed range. Such techniques are common with EW jammers. An oncoming automobile radar of a similar type will act as an unintentional jammer. However, the probability of time alignment, between victim and jamming radar, would be very small. A jammer delay offset that is less than the maximum range delay of the victim radar could look like a real target. For example, a 200 m max range would require sweep alignment of less than 1.3 µs. However, such a deceptive attack could be carried out intentionally using sophisticated EW-like equipment mounted on the oncoming automobile platform.

More generally, deceptive jamming is based on retransmitting the victim radar's signal with a systematic change in delay and frequency. This can be either noncoherent, in which case the jammer is called a transponder, or coherent, when it's a repeater. Repeaters receive, alter, and retransmit one or more jamming signals, whereas transponders transmit a predetermined signal when a desired victim signal is detected by the jammer.

A sophisticated repeater-based attack would typically require a digital RF memory (DRFM). A DRFM is capable of carrying out coordinated range delay and Doppler gate pull off attacks. So, the false target range and Doppler properties are maintained to deceive the victim radar.

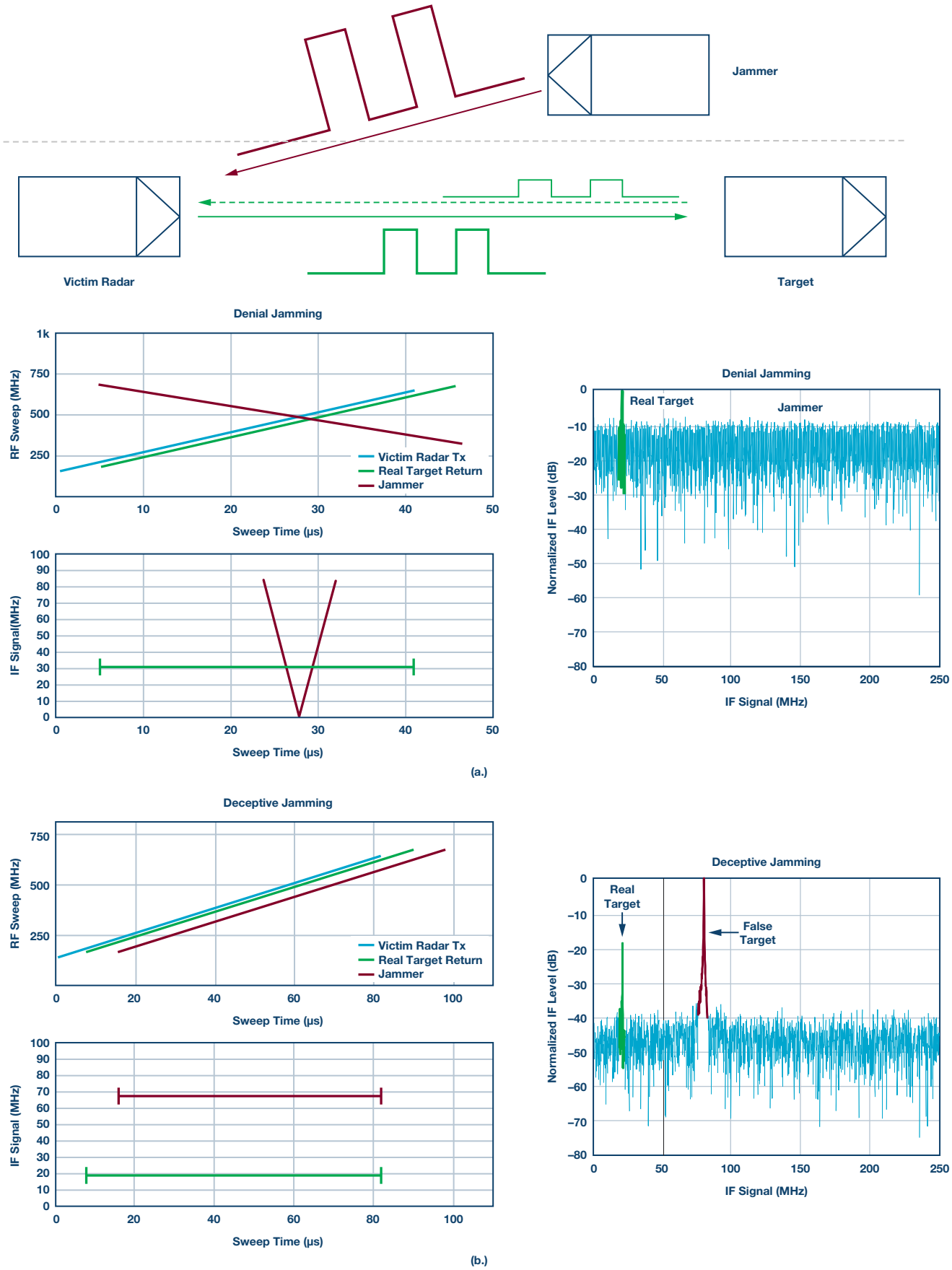

Figure 2. Examples of a) FMCW denial jamming and b) FMCW deceptive jamming.

Jamming Mitigation Techniques

Basic Approach: Avoidance

Basic radar jamming mitigation techniques mostly rely on the avoidance approach. The objective is to reduce the probability of overlap in space, time, and frequency such as:

- Spatial: Use of narrow and electronically scanned beam can reduce jamming risk. A typical field of view for long range automotive cruise control (ACC) radar is ±8°. Nonetheless, a strong jammer could still be effective through the antenna side lobes.
- Temporal: Randomize FMCW chirp slope parameters to avoid periodic jamming.
- Spectral: Randomize FMCW chirp start and stop frequencies to reduce the probability of overlap and jamming.

The basic methods of randomization would avoid accidental synchronization with other radars, but might not be as useful in dense RF environments. The growing number of radar sensors will require more sophisticated resilience techniques to mitigate the jamming.

A Strategic Approach: Detect and Repair

An alternative method of avoidance could be used to repair the received waveform using signal processing algorithms. Time frequency domain techniques could be effective against the denial type of jamming attacks. In the oncoming automobile FMCW jamming scenario, the jammer sweeps all frequency bins for a very short duration of time. This fast time varying signal manifests itself as a raised noise floor in regular FFT domain. Time frequency domain signal processing technique transfers the signal to another domain where it is easier to filter out the jamming in comparison to FFT domain (see Figure 3).

For time varying signals, a short time Fourier transform (STFT) provides more information than a regular FFT. STFT-based techniques could be used for narrow-band jamming excision. The STFT essentially moves a window through the signal and takes the FFT of the windowed region. The signal is filtered in the frequency domain to remove the jammer components before being transformed back to the time domain.

Figure 4 shows a typical FMCW jamming scenario of overlapping RF chirp sequences along with resulting IF beat signal in the STFT domain.

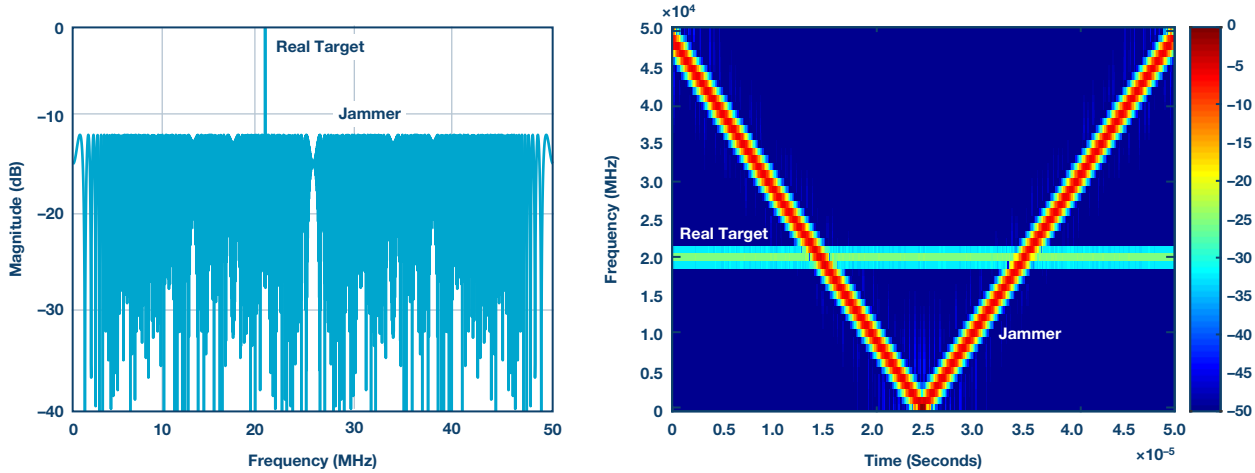

Figure 3. FFT and STFT domain representation of radar echo IF waveform.

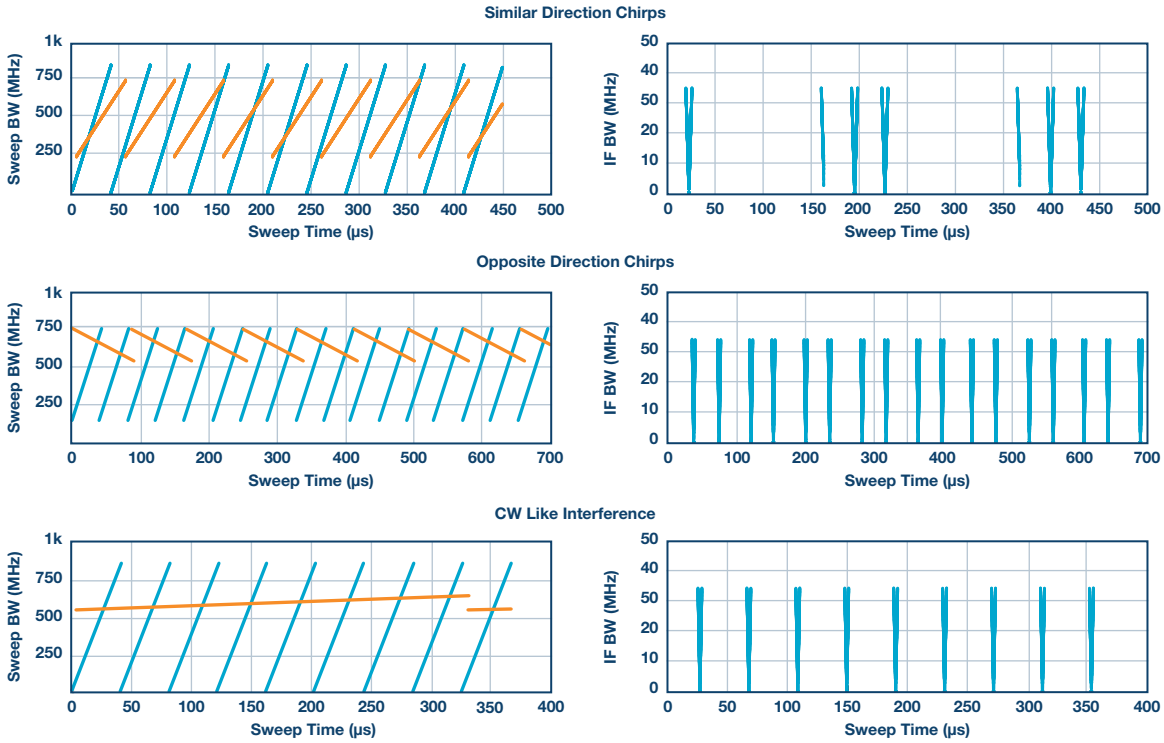

Figure 4. STFT domain, left: FMCW radar and jammer, right: IF domain.

The plots on the right of Figure 4 show the IF domain that is the end result of the mixing of radar (blue) and jamming (orange) signal. A horizontal line would indicate a target, whereas V shaped vertical lines indicate the presence of a jamming signal.

Similar or opposite direction jamming FMCW, or even a CW-like slow chirp, have similar impacts in the IF signal. In all of these jamming scenarios, the fast moving V shaped IF signal raises the noise floor in the regular FFT domain, as shown in Figure 3.

An amplitude-based masking could be used to filter out the jamming signal in the STFT domain. This assumes, of course, that the victim radar front end and quantization have enough dynamic range to process the stronger jammer signal and the small intended target linearly at the same time. See Figure 5.

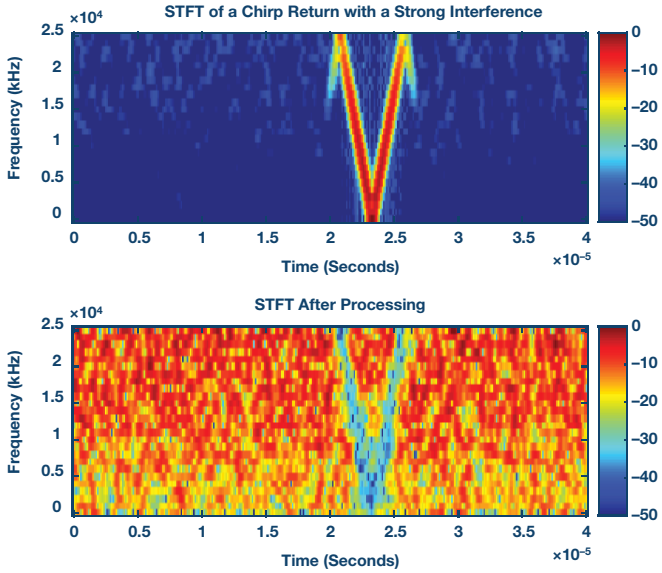

Figure 5. Amplitude-based masking in the STFT domain.

The top image of Figure 5 depicts a strong jammer, while the bottom shows an STFT after processing. Multiple real targets are not visible in the presence of strong jammer, as in the top. The V shaped jammer in the lower plot is excised and the low SNR targets would now be discernable when transferred back to the time domain.

The STFT-based jamming mitigation technique could be used in denial jamming scenarios against strong jammers. For deceptive jamming attacks, an STFT alone cannot authenticate whether the return signal is real or false.

Encrypted RF

The elementary countermeasure to reduce the impact of deceptive jamming from repeater attacks is the use of low probability of intercept (LPI) radar waveforms. The objective of an LPI radar is to escape detection by spreading the radiated energy over a wide spectrum of frequencies, usually via quasi-random sweep, modulation, or hopping sequences. FMCW is a type of LPI waveform. If phase coding, or encryption, is introduced into the frequency chirp, it is possible to further reduce the chances of a DRFM intercepting the automotive radar signal.

An encrypted RF signature unique to each radar sensor could authenticate the return signal. Figure 6 shows a use case where two identical radars (one of which is mounted on a different automobile) with frequency offset and delay between them generates a false target in the victim radar. The jamming radar is time aligned (same chirp slope and a short offset) with the victim radar.

Phase coded FMCW radars could offer high jamming robustness in this use case. The use of orthogonal codes could also make MIMO radar operation possible by enabling multiple simultaneous transmit waveforms.

Requirements of coding:

- Code length: The goal is to achieve minimal range sidelobe levels with short sequences. A PRN sequence length of 1024 results in a peak side lobe level (PSLL) of about 30 dB (10log1024). Transmit codes together with the receive filter weights could be optimized to improve the PSLL at the expense of SNR.
- Good cross-correlation properties: Cross-correlation coefficients of the members of a set should be zero to achieve a good separation between sensors
- Doppler resistance: Phase coded radar performance could suffer from the Doppler shift. Binary codes are Doppler intolerant. Polyphase codes degrade less rapidly than binary codes.
- Available number of different codes: A large family size is better to assign a unique code to each radar sensor.

Figure 7 illustrates the radar echo with no phase coding. Jamming signal shows itself as a false target. When the transmitter FMCW waveform is phase coded with a PRN sequence, the jamming signal could be suppressed, as shown in Figure 8.

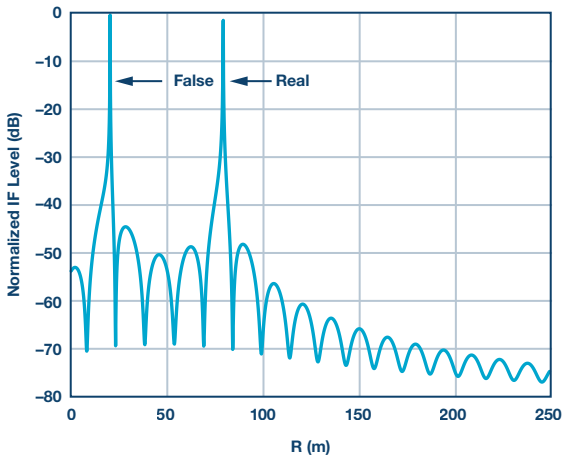

Figure 7. Radar return without phase coding false and real targets.

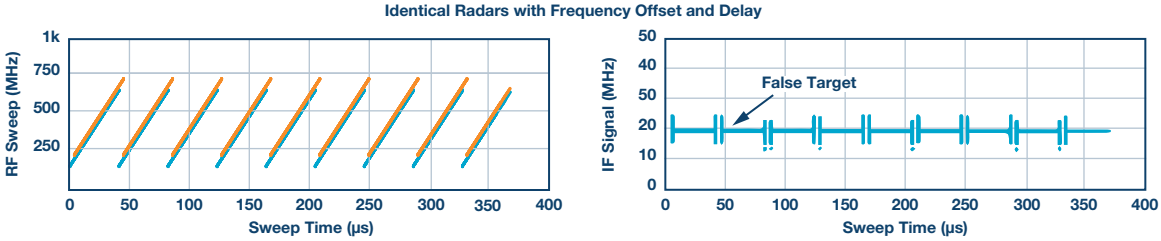

Figure 6. Jamming due to identical radars with frequency offset and delay.

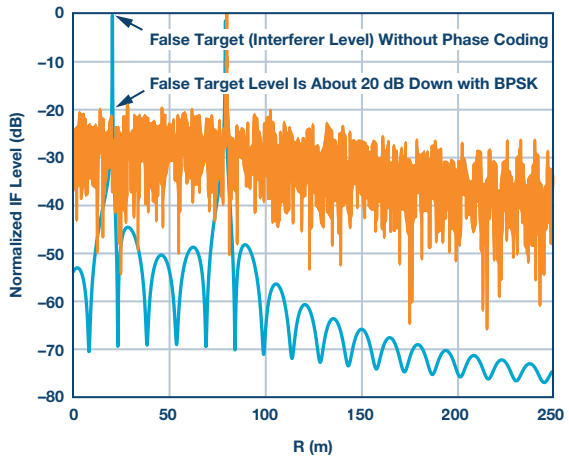

Figure 8. Radar return with and without phase coding.

The dynamic range is compromised with this method. However, the radar signal processor could use phase coded FMCW for a few chirps to flag a false target and then switch back to normal operation.

Conclusion and Future Trends

Jamming in congested automobile radar sensor environments can be mitigated using advance signal processing algorithms and complex waveform generation techniques. STFT-based signal processing techniques could be used against denial type of attacks. Phase coded FMCW provides an additional layer of resistance to both noncoherent and coherent deceptive attacks by means of processing gain and interception avoidance. See Table 1 for the summary of mitigation techniques.

Table 1. Mitigation Techniques for FMCW-Based Automotive Radars

Jamming Type	Denial	Deceptive	
Jamming HW	Another radar sensor or a simple CW generator	DRFM (coherent)	Transponder (noncoherent)
Impact on the victim radar	Poor SNR	False target	False target
Resilient mitigation technique	STFT	Phase coded FMCW	Phase coded FMCW
Mitigation principle	Repair the radar return waveform	Escape detection	Processing gain of the coding sequence
Mitigation effectiveness (expected)	High	Moderate	Good

The previously detailed jamming mitigation principles for automotive radars are also applicable for other radar sensor environments—for example, robotics, road tolling, GPS, and UAV landing or collision avoidance systems.

Currently automotive radar sensors are operating in noncooperative mode without communicating with each other. Although a cooperative mode of operation would require industry-wide harmonization, the arbitration between radar sensors could help resolve the interference issue.

A future radar concept including the sensor cooperation would be the fusion of communication nodes and radar sensors. Future radars with complex waveforms offer the possibility to include information in the radar signal as well. The same HW could be used for radar and communications (RadCom) simultaneously.

RadCom: One Single System for Simultaneous Radar and Communications

- Multi-user capability without interference
- The coding of the radar signal with OFDM or similar communication codes offers the possibility to include information in the radar signal
- Simultaneous due to OFDM-based radar transmit signals

5G millimeter wave transceiver signal solutions from ADI with greater than GHz bandwidth and beam steering capabilities could be a potential candidate for a RadCom system concept.

ADI is in a unique position to develop both state-of-the-art radar sensors and 5G millimeter wave solutions to pave the way for future RadCom systems.

Analog Devices Drive360 28 nm CMOS Radar Technology

ADI's Drive360™ 28 nm CMOS radar platform enables many high level signal processing integration options and even allows for custom IP integration enabling designers to differentiate their systems. A highly integrated power management companion chip accompanies the platform. This system brings Tier 1 and OEMs the high performance required to build robust solutions for emerging autonomous driving applications.

5G Millimeter Wave

Analog Devices brings a strong contribution to the 5G microwave effort with our unique bits to microwave capability. Our broad technology portfolio and continued RF technology advances combined with our rich history in radio systems engineering put ADI in a leading position to pioneer new solutions for our customers at microwave and millimeter wave frequencies for the emerging 5G systems.

Sefa Tanis

Sefa Tanis [sefa.tanis@analog.com] is a senior RF systems engineer at Analog Devices specializing in digital predistortion algorithm development for small cell transceivers, researching signal processing techniques for automotive radars and evaluating system in a package RF modules for wireless infrastructures. Prior to joining ADI in 2012, he held a lead RF engineer role for an F-16 aircraft electronic warfare program, AN/ALQ-178 V(5)+, jointly developed by ASELSAN of Turkey and BAE Systems in North America. He has 15+ years of expertise in system-level design, and algorithm development, test, and integration of microwave products in telecommunications and the defense/aerospace industries. He received his B.S.E.E. from Cukurova University in Turkey in 2000.

Powering Infotainment Devices in Automotive Start/Stop Systems

By **Bruce Haug**

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Background

Automakers continue to tout stop/start systems that help save fuel. As its name implies, a stop/start system shuts off the engine instead of letting it idle at a stop, and then it rapidly restarts the engine once you need to drive away. If you do a lot of stop-and-go driving, you're reducing emissions and saving fuel by not idling the engine for extended periods of time. The concept is simple. As an example, if you're stopped at a red light or train crossing, you don't need the engine to be running; if the engine isn't running, you're not wasting any energy. As a result, the reduction in fuel consumption can be as much as 8% in city traffic compared to a car without such a system.

Driving comfort and safety are not compromised by an auto start/stop function, since it is not activated until the engine has reached an ideal running temperature. The same applies if the air conditioner has not yet brought the cabin to the desired temperature, if the battery is not adequately charged, or if the driver moves the steering wheel.

The auto start/stop function is coordinated by a central control unit that monitors data from all relevant sensors, including the starter motor and the alternator. If necessary for comfort or safety, the control unit will automatically restart the engine—for example, if the vehicle begins to roll, the battery charge falls too low, or condensation forms on the windshield. Furthermore, most systems recognize the difference between a temporary stop and the end of the trip. It will not restart the engine if a driver's seat belt is undone, or if the door or trunk is open. If desired, the auto start/stop function can be completely deactivated with the press of a button (for now, at least).

However, when the engine restarts and there is an infotainment system turned on or another electronic device requiring greater than 5 V, there is a possibility that the 12 V battery can dip to below 5 V, causing these systems to reset. Some navigation and infotainment systems operate from a 5 V and higher input voltage. When the input voltage dips to below 5 V during an engine restart, these systems will reset when the dc-to-dc converter only has the capability to step down the input voltage. Obviously, it is not acceptable to have a music player or the navigation system reset when the car restarts.

Solution

Analog Devices recently introduced a triple output dc-to-dc controller, the Power by Linear® LTC7815, that combines a boost controller and two step-down controllers in a single package. The high efficiency synchronous boost feeds the two downstream synchronous step-down converters, avoiding an output voltage dropout when the car battery voltage droops—a very useful feature in automotive start/stop systems. In addition, when the input voltage from the car battery is higher than its programmed boost output voltage, the boost controller runs at 100% duty cycle and simply passes the input voltage directly to the step-down converters, minimizing power loss.

Figure 1 shows an LTC7815 schematic with the boost converter supplying 10 volts to the step-down converters. In addition to powering the two step-down converters, which produce 5 V/7 A and 3.3 V/10 A, respectively, the boost converter can be used as a third output that can provide an additional 2 A. This circuit maintains 2.1 MHz operation at up to 28 V_{IN} and skips cycles above 28 V.

The LTC7815 operates from an input voltage of 4.5 V to 38 V during startup and maintains operation down to 2.5 V after startup. The synchronous boost converter can produce output voltages up to 60 V and can run with the synchronous switch fully on to pass through the input voltage when it is high enough to maximize efficiency. The two step-down converters can produce output voltages from 0.8 V to 24 V, with the entire system achieving efficiency as high as 95%. Its low 45 ns minimum on-time enables high step-down conversions while switching at 2 MHz, thus avoiding critical noise-sensitive frequency bands such as AM radio and allowing for smaller external components.

The LTC7815 can be configured for Burst Mode® operation, which reduces quiescent current to 28 µA per channel (38 µA when all three channels are on) while regulating the output voltage at no load, a useful feature for preserving battery run times in always-on systems. The powerful 1.1 Ω on-board all N-channel MOSFET gate drivers minimize switching losses and provide output current of more than 10 amps per channel, limited only by external components. Furthermore, the output current for each converter is sensed by monitoring the voltage drop across the inductor (DCR) or by using a separate sense resistor. The LTC7815's constant frequency current-mode architecture enables a selectable frequency from 320 kHz to 2.25 MHz or it can be synchronized to an external clock over the same range.

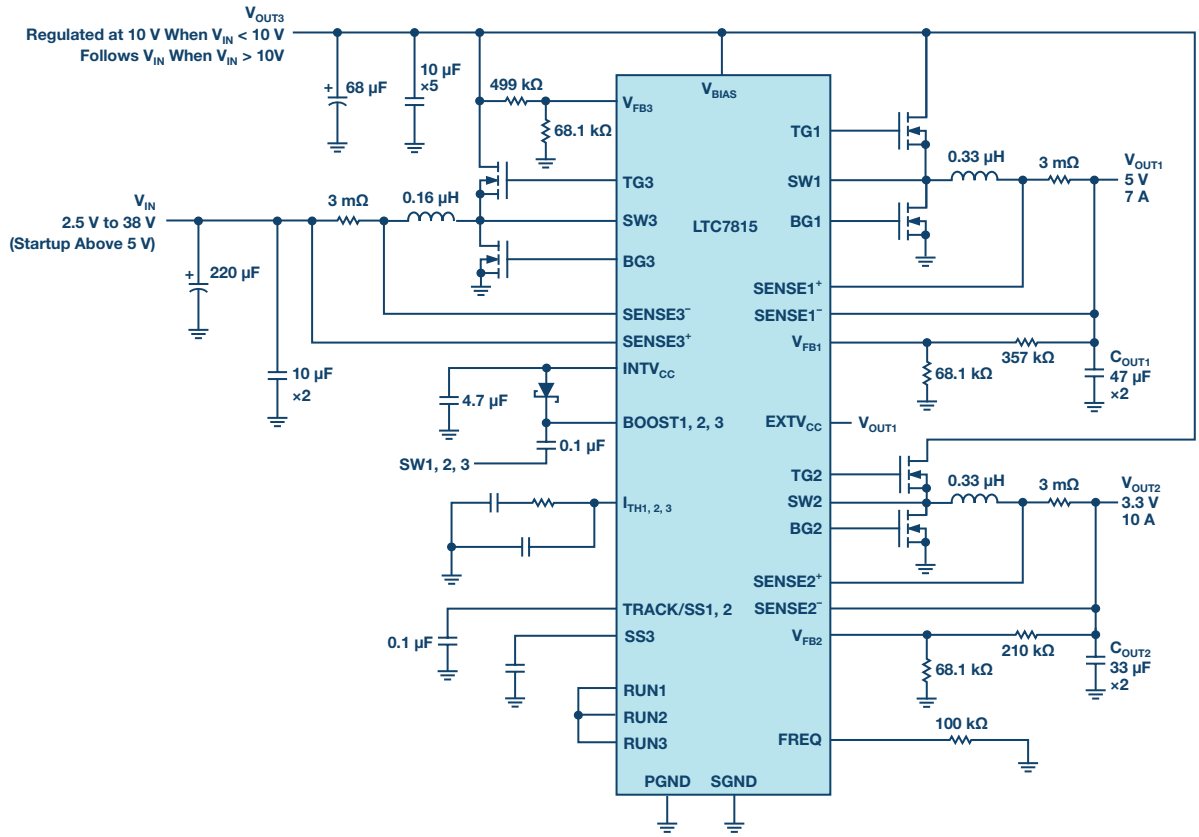

Figure 1. LTC7815 start/stop application schematic operating at 2.1 MHz.

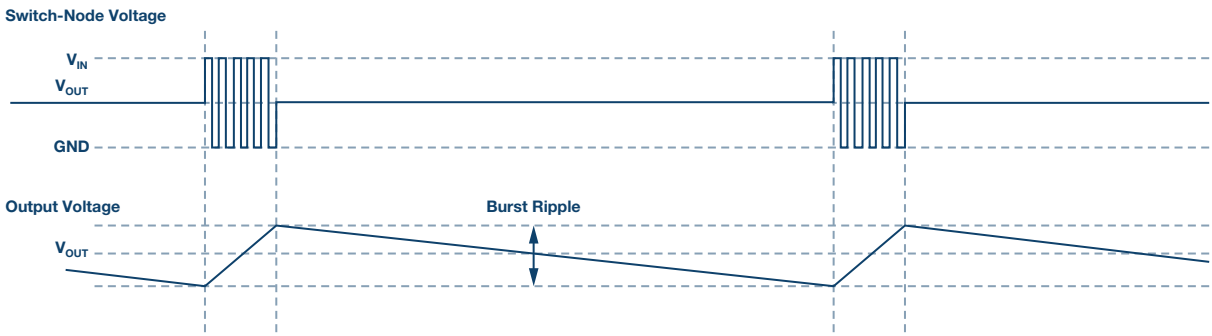

Figure 2. Burst Mode operation voltage diagram for the LTC7815.

Extending Battery Run Times

Any battery-powered system that requires an always-on power bus while the rest of the system is turned off must conserve battery energy. This state is commonly referred to as sleep, standby, or idle mode and requires these systems to have very low quiescent current. The need for low quiescent current to conserve battery energy is especially important in automotive applications that can have several electrical circuits such as telematics, CD/DVD players, remote keyless entry, and multiple always-on bus lines. The collective current consumption of these systems during standby mode needs to be as low as possible and the pressure continues to mount for battery energy conservation as cars become more dependent on electronic systems for their operation.

The LTC7815 draws a mere 28 µA when in sleep mode with the boost converter and one of the buck converters on. With all three channels on and in sleep mode, the LTC7815 draws only 20 µA, which significantly extends battery run times when in idle mode. This is done by configuring the part to enter high efficiency Burst Mode operation, where the LTC7815 delivers short bursts of current to the output capacitor followed by a sleep period where the output power is delivered to the load by the output capacitor only. Figure 2 shows the conceptual timing diagram of how this works.

In sleep mode, much of the internal circuitry is turned off except for the critical circuitry needed to respond quickly. When the output voltage drops enough, the sleep signal is activated and the controller resumes normal Burst Mode operation by switching on the top external MOSFET. Alternatively, there are instances when the user will want to operate in forced continuous or constant frequency pulse skipping mode at light load currents. Both modes are easily configurable and have a higher quiescent current.

Efficiency/Solution Size

The efficiency for the 5 V output as referenced in the Figure 1 schematic is about 90% as shown in Figure 3. A 3% to 4% higher efficiency can be attained if the operating frequency is reduced from 2.1 MHz to 300 kHz.

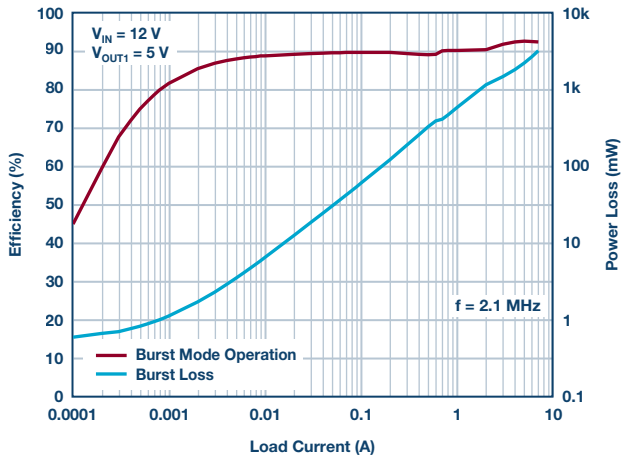

Figure 3. LTC7815 efficiency vs. load current for different converter sections.

Figure 4 shows the demo board for the LTC7815 (schematic shown in Figure 1) with the tallest part at 48 mm high.

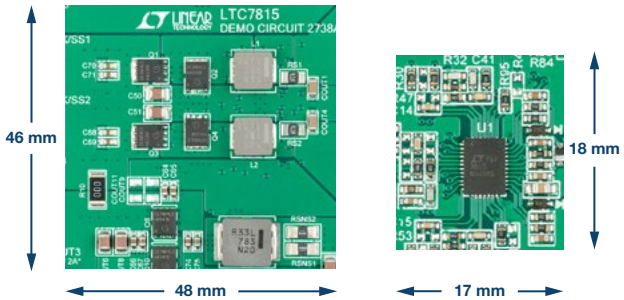

Figure 4. Size and layout of LTC7815 demo board top and bottom sides.

Protection Features

The LTC7815 can be configured to sense the output current by using DCR (inductor resistance) or a sense resistor. The choice between the two current sensing schemes is largely a trade-off between cost, power dissipation, and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. The sense resistor, however, is a more accurate way of sensing current.

On-board comparators monitor the buck output voltages and signal an overvoltage condition when the output is greater than 10% of its nominal value. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the overvoltage condition persists. If the output voltage returns to a safe level, normal operation automatically resumes.

At higher temperatures, or in cases where the internal power dissipation causes excessive self heating on-chip, the overtemperature shutdown circuitry will shut down the LTC7815. When the junction temperature exceeds approximately 170°C, the overtemperature circuitry disables the on-board bias LDO, causing the bias supply to drop to 0 V and effectively shutting down the entire LTC7815 in an orderly manner. Once the junction temperature drops back to approximately 155°C, the LDO turns back on.

Conclusion

Automotive start/stop systems allow for fuel savings that will continue to evolve over the next several years. Care must be taken with regards to powering on-board infotainment and navigation systems that need up to, or can exceed 5 V. These systems can reset when the car battery voltage droops to less than 5 V with an engine restart. The LTC7815 provides a solution by boosting the battery voltage to a safe operating level. This, combined with two step-down controllers, makes it ideal for powering many automotive electronic devices in cars that have a start/stop system.

Bruce Haug [bruce.haug@analog.com] received his B.S.E.E. from San Jose State University in 1980. He joined Linear Technology (now a part of Analog Devices) as a product marketing engineer in April 2006. Bruce's past experience includes stints at Cherokee International, Digital Power, and Ford Aerospace. He is an avid sports participant.

Bruce Haug

Phase-Locked Loop (PLL) Fundamentals

By **Ian Collins**

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Abstract:

Phase-locked loop (PLL) circuits exist in a wide variety of high frequency applications, from simple clock clean-up circuits, to local oscillators (LOs) for high performance radio communication links, and ultrafast switching frequency synthesizers in vector network analyzers (VNA). This article explains some of the building blocks of PLL circuits with references to each of these applications, in turn, to help guide the novice and PLL expert alike in navigating part selection and the trade-offs inherent for each different application. The article references the Analog Devices ADF4xxx and HMCxxx family of PLLs and voltage controlled oscillators (VCOs), and uses ADIsimPLL (Analog Devices in-house PLL circuit simulator) to demonstrate these different circuit performance parameters.

Basic Configuration: Clock Clean-Up Circuit

In its most basic configuration, a phase-locked loop compares the phase of a reference signal (F_{REF}) to the phase of an adjustable feedback signal (RF_{IN}) F_0, as seen in Figure 1. In Figure 2 there is a negative feedback control loop operating in the frequency domain. When the comparison is in steady-state, and the output frequency and phase are matched to the incoming frequency and phase of the error detector, we say that the PLL is locked. For the purposes of this article we shall only consider a classical digital PLL architecture as implemented on the Analog Devices ADF4xxx family of PLLs.

The first essential element in this circuit is the phase frequency detector (PFD). The PFD compares the frequency and phase of the input to REF_{IN} to the frequency and phase of the feedback to RF_{IN}. The ADF4002 is a PLL that can be configured as a standalone PFD (with the feedback divider N = 1). As such, it can be used with a high quality voltage controlled crystal oscillator (VCXO) and a narrow low-pass filter to clean up a noisy REF_{IN} clock.

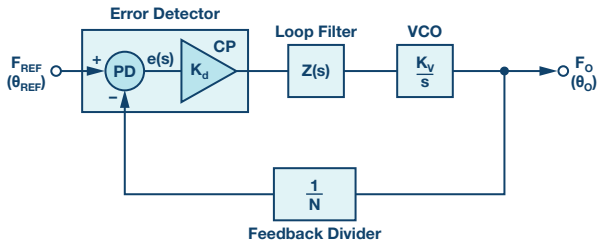

Figure. 1 Basic PLL configuration.

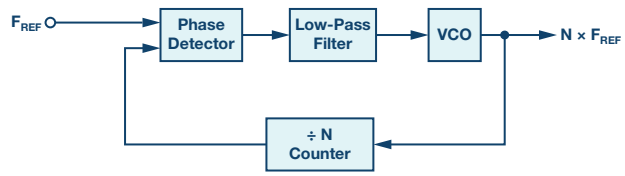

Figure 2. Basic PLL configuration.

Phase Frequency Detector

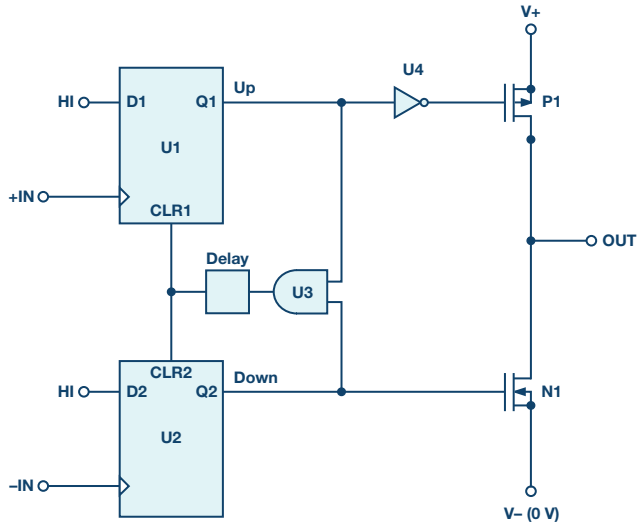

Figure 3. Phase frequency detector.

The phase frequency detector in Figure 3 compares the input to F_{REF} at +IN and the feedback signal at –IN. It uses two D-type flip flops with a delay element. One Q output enables a positive current source, and the other Q output enables a negative current source. These current sources are known as the charge pump. For more details on PFD operation, consult "Phase-Locked Loops for High Frequency Receivers and Transmitters."

Using this architecture, the input to +IN below is at a higher frequency than the –IN (Figure 4), and the resultant charge pump output is pumping current high, which, when integrated in the PLL low-pass filter, will push the tuning voltage of the VCO up. In this way, the –IN frequency will increase as the VCO increases, and the two PFD inputs will eventually converge or lock to the same frequency (Figure 5). If the frequency to –IN is higher than +IN, the reverse happens.

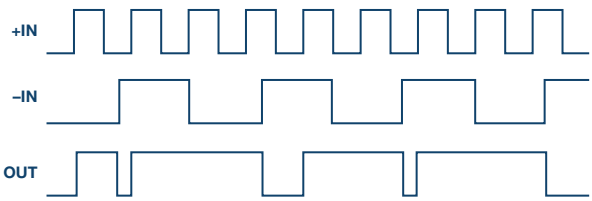

Figure 4. A PFD out of phase and frequency lock.

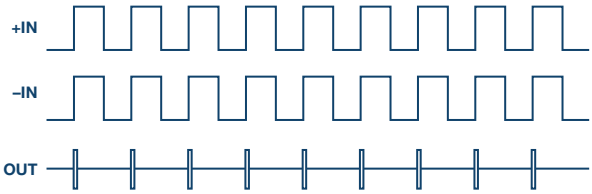

Figure 5. Phase frequency detector, frequency, and phase lock.

Returning to our original example of the noisy clock that requires cleaning, the phase noise profile of the clock, free running VCXO, and closed-loop PLL can be modeled in ADIsimPLL.

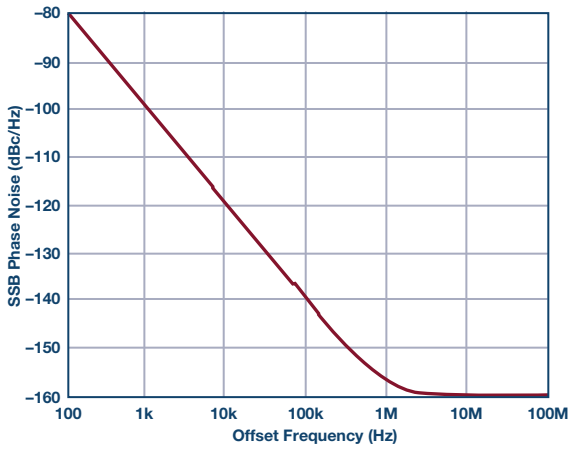

Figure 6. Reference noise.

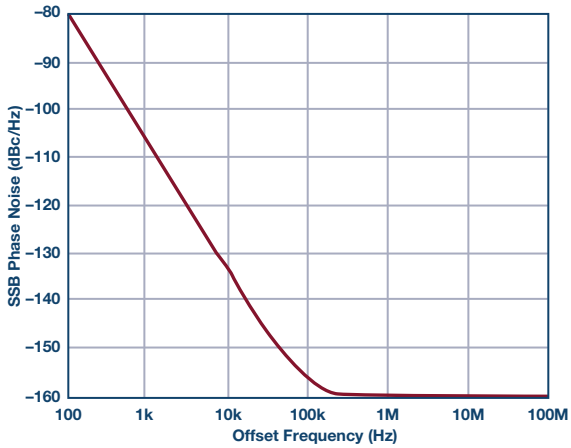

Figure 7. Free running VCXO.

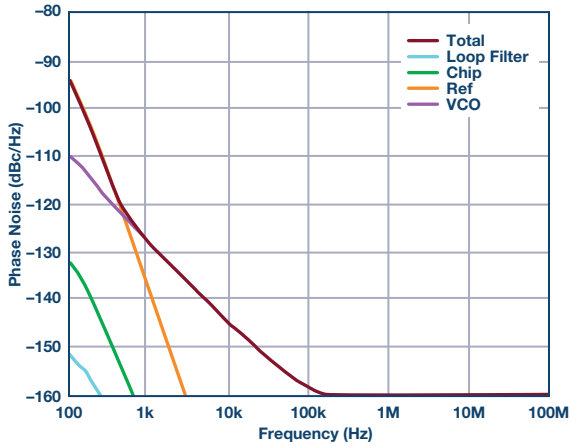

Figure 8. Total PLL noise.

As can be seen with the ADIsimPLL plots shown, the noisy phase noise profile of the REF_{IN} (Figure 6) is filtered by the low-pass filter. All the in-band noise contributed by the PLL reference and PFD circuitry is filtered out by the low-pass filter, leaving only the much lower VCXO noise (Figure 7) outside the loop bandwidth (Figure 8). When the output frequency is equal to the input frequency it creates one of the simplest PLL configurations. Such a PLL is called a clock clean-up PLL. For clock clean-up applications such as these, narrow (<1 kHz) low-pass filter bandwidths are recommended.

High Frequency Integer-N Architecture

To generate a range of higher frequencies, a VCO is used, which tunes over a wider range than a VCXO. This is regularly used in frequency hopping or in spread spectrum frequency hopping (FHSS) applications. In such PLLs, the output is a high multiple of the reference frequency. Voltage controlled oscillators contain a variable tuning element, such as a varactor diode, which varies its capacitance with input voltage, allowing a tuneable resonant circuit, which permits a range of frequencies to be generated (Figure 9). The PLL can be thought of as a control system for this VCO.

A feedback divider is used to divide the VCO frequency to the PFD frequency, which allows a PLL to generate output frequencies that are multiples of the PFD frequency. A divider may also be used in the reference path, which permits higher frequency references to be used than the PFD frequency. A PLL like this is the ADF4108 from Analog Devices. The PLL counters are the second essential element to be considered in our circuit.

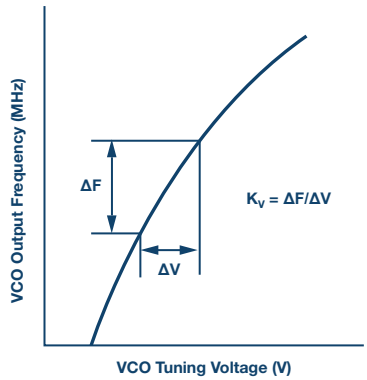

Figure 9. Voltage controlled oscillator.

The key performance parameters of PLLs are phase noise, unwanted by-products of the frequency synthesis process, or spurious frequencies (spurs for short). For integer-N PLLs, spurious frequencies are generated by the PFD frequency. A leakage current from the charge pump will modulate the tuning port of the VCO. This effect is lessened by the low-pass filter and the narrower this is, the greater the filtering of the spurious frequency. An ideal tone would have no noise or additional spurious frequency (Figure 10), but in practice phase noise appears as a skirtaround a carrier, as shown in Figure 11. Single sideband phase noise is the relative noise power to the carrier in a 1 Hz bandwidth, specified at a frequency offset from the carrier.

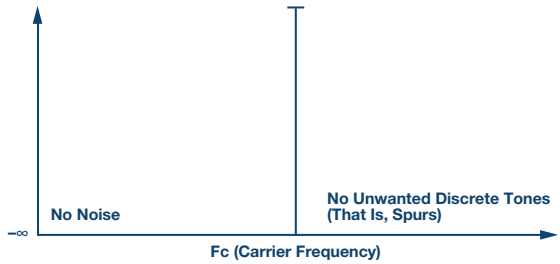

Figure 10. Ideal LO spectrum.

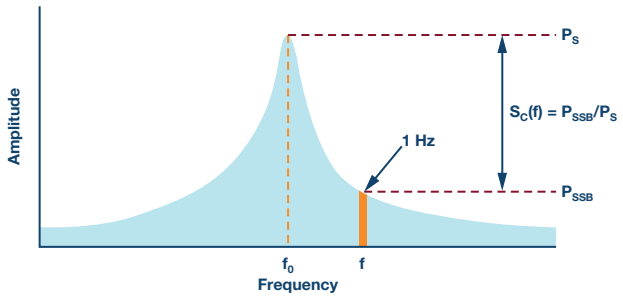

Figure 11. Single sideband phase noise.

Integer-N and Fractional-N Divider

For narrow-band applications, the channel spacing is narrow (typically <5 MHz) and the feedback counter, N, is high. Gaining high N values with a small circuit is achieved by the use of a dual modulus P/P + 1 prescaler, as seen in Figure 12, and allows N values to be computed with the calculation of N = PB + A, which, using the example of an 8/9 prescaler and an N value of 90, computes a value of 11 for B and 2 for A. The dual modulus prescaler will divide by 9 for A or two cycles. It will then divide by 8 for the remaining (B-A) or 9 cycles, as described in Table 1. The prescaler is generally designed using a higher frequency circuit technology, such as bipolar emitter coupled logic (ECL) circuits, while the A and B counters can take this lower frequency prescaler output and can be manufactured with lower speed CMOS circuitry. This reduces circuit area and power consumption. Low frequency clean up PLLs like the ADF4002 omit this prescaler.

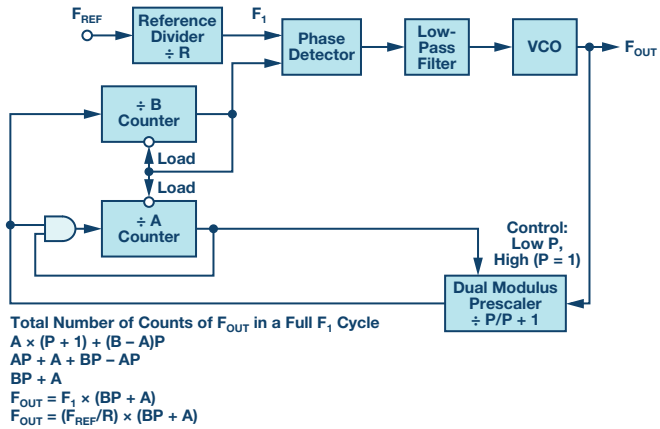

Figure 12. PLL with dual modulus N counter.

Table 1. Dual Modulus Prescaler Operation

N Value	P/P + 1	B Value	A Value
90	9	11	2
81	9	10	1
72	8	9	0
64	8	8	0
56	8	7	0
48	8	6	0
40	8	5	0
32	8	4	0
24	8	3	0
16	8	2	0
8	8	1	0
0	8	0	0

The in-band (inside the PLL loop filter bandwidth) phase noise is directly influenced by the value of N, and in-band noise is increased by 20log (N). So, for narrow-band applications in which the N value is high, the in-band noise is dominated by the high N value. A system that permits a much lower N value, but still permits fine resolution is enabled by a fractional-N synthesizer, such as the ADF4159 or HMC704. In this manner, the in-band phase noise can be greatly reduced. Figures 13 through 16 illustrate how this is achieved. In these examples, two PLLs are used to generate frequencies suitable for a 5G systems local oscillator (LO) in a range between 7.4 GHz to 7.6 GHz, with 1 MHz of channel resolution. The ADF4108 is used in an integer-N configuration (Figure 13) and the HMC704 is used in a fractional-N configuration. The HMC704 (Figure 14) can be used with a 50 MHz PFD frequency, which lowers the N value and, hence, the in-band noise, while still permitting a 1 MHz (or indeed smaller) frequency step size—an improvement of 15 dB (at 8 kHz offset frequency) is noted (Figure 15 vs. Figure 16). The ADF4108, however, is forced to use a 1 MHz PFD to achieve the same resolution.

Care needs to be taken with fractional-N PLLs to ensure that spurious tones do not degrade system performance. On PLLs such as the HMC704, integer boundary spurs (generated when the fractional portion of the N value approaches 0 or 1, like 147.98 or 148.02 are very close to the integer value of 148) generate the most concern. This can be mitigated by buffering the VCO output to the RF input, and/or careful frequency planning in which the REF_{IN} can be changed to avoid these more problematic frequencies.

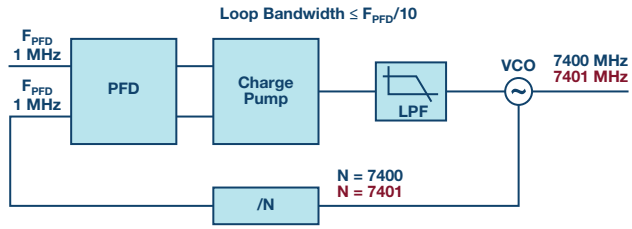

Figure 13. Integer-N PLL.

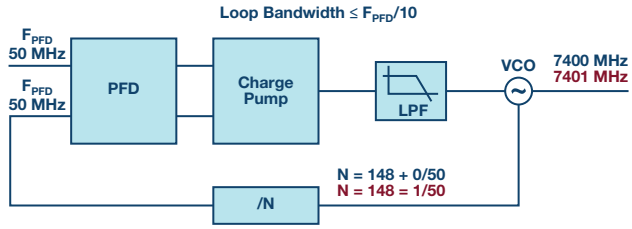

Figure 14. Fractional-N PLL.

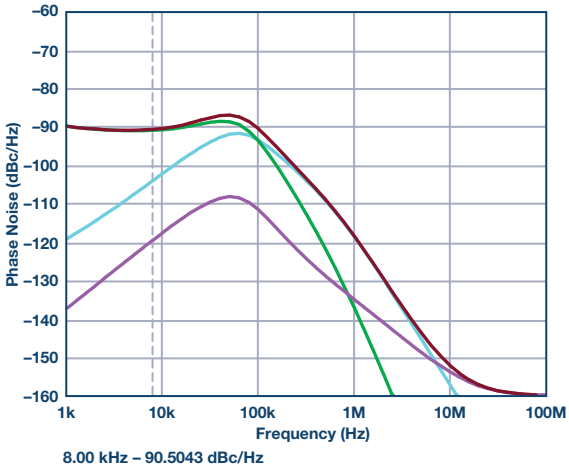

Figure 15. Integer N PLL in-band phase noise.

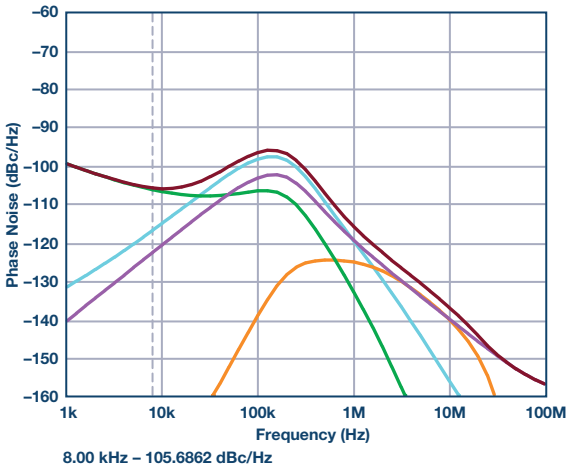

Figure 16. Fractional-N PLL in-band phase noise.

For the majority of PLLs the in-band noise is highly dependent on the N value, and also on the PFD frequency. Subtracting 20log (N) and 10log (F_{PFD}) from the flat portion of an in-band phase noise measurement yields the figure of merit (FOM). A common metric for choosing PLLs is to compare the FOM. Another factor that influences the in-band noise is the 1/f noise, which is dependent on the output frequency of the device. The FOM contribution and the 1/f noise, together with the reference noise, dominate the in-band noise of a PLL system.

Narrow-Band LO for 5G Communications

For communication systems, the chief specifications from the PLL perspective are error vector magnitude (EVM) and VCO blocking specifications. EVM is similar in scope to integrated phase noise, which considers the noise contribution over a range of offsets. For the 5G system listed earlier, the integration limits are quite wide, starting at 1 kHz and continuing to 100 MHz. EVM can be thought of as a percentage degradation of a perfectly modulated signal from its ideal point expressed as a percentage (Figure 17). In a similar manner, integrated phase noise integrates the noise power at different offsets from the carrier and expresses this can be configured to calculate the EVM, integrated phase noise, and rms phase error and jitter. Modern signal source analyzers will also include these numbers at the push of a button (Figure 18). As modulation schemes increase in density, EVM becomes critical. For 16-QAM, the required minimum EVM according to ETSI specification 3GPP TS 36.104 is 12.5%. For 64-QAM, the requirement is 8%. However, since EVM is comprised of various other nonideal parameters due to power amplifier distortion and unwanted mixer products, the integrated noise (in dBc) is usually defined separately.

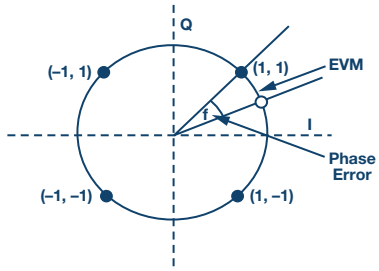

Figure 17. Phase error visualization.

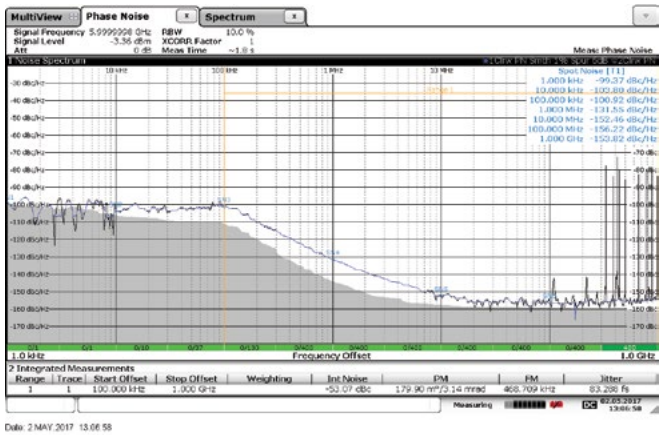

Figure 18. Signal source analyzer plot.

VCO blocking specifications are very important in cellular systems that need to account for the presence of strong transmissions. If a receiver signal is weak, and if the VCO is too noisy, then the nearby transmitter signal can mix down and drown out the wanted signal (Figure 19). The illustration in Figure 19 demonstrates how the nearby transmitter (800 kHz away) transmitting at –25 dBm power could, if the receiver VCO is noisy, swamp the wanted signal at –101 dBm. These specifications form part of a wireless communications standard. The blocking specifications directly influence the performance requirement of the VCO.

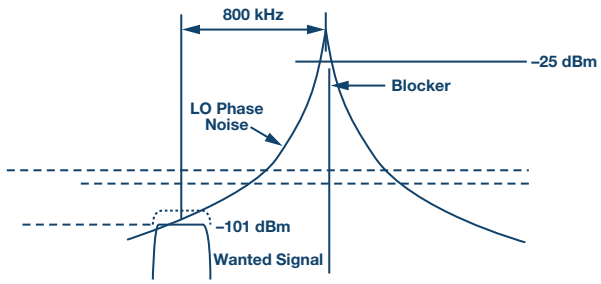

Figure 19. VCO noise blockers.

Voltage Controlled Oscillators (VCOs)

The next PLL circuit element to be considered in our circuit is the voltage controlled oscillator. With VCOs, a fundamental trade-off between phase noise, frequency coverage, and power consumption is necessary. The higher the quality factor (Q) of the oscillator, the lower the VCO phase noise is. However, higher Q circuits have narrower frequency ranges. Increasing the power supply will also lower the phase noise. Looking at the Analog Devices family of VCOs, the HMC507 covers a range of 6650 MHz to 7650 MHz and the VCO noise at 100 kHz is approximately –115 dBc/Hz. By contrast, the HMC586 covers a full octave from 4000 MHz to 8000 MHz, but has higher phase noise of –100 dBc/Hz. One strategy for minimizing phase noise in such VCOs is to increase the voltage tuning range of the V_{TUNE} to the VCO (up to 20 V or greater). This increases PLL circuit

complexity, as most PLL charge pumps can only tune to 5 V, so an active filter using operational amplifiers is used to increase the tuning voltage of the PLL circuit on its own.

Multiband Integrated PLLs and VCOs

Another strategy to increase frequency coverage without degrading VCO phase noise is to use a multiband VCO, in which overlapping frequency ranges are used to cover an octave of frequency range, and lower frequencies can be generated by using frequency dividers at the output of the VCO. Such a device is the ADF4356, which uses four main VCO cores each with 256 overlapping frequency ranges. The internal reference and feedback frequency dividers are used by the device to choose the appropriate VCO band, a process known as VCO band select or autocalibration.

The wide tuning range of the multiband VCOs makes them suitable for use in wideband instrumentation, in which they generate a wide range of frequencies. The 39 bits of fractional-N resolution also makes them ideal candidates for these precise frequency applications. In instruments such as vector network analyzers, ultrafast switching speed is essential. This can be achieved by using a very wide low-pass filter bandwidth, which tunes to final frequency very quickly. The automatic frequency calibration routine can be bypassed in these applications by using a look-up table with the frequency values directly programmed for each frequency, true single core wideband VCOs like the HMC733 can also be used with less complexity.

For phase-locked loop circuits, the bandwidth of the low-pass filter has a direct influence on the settling time of the system. The low-pass filter is the final element in our circuit. If settling time is critical, the loop bandwidth should be increased to the maximum bandwidth permissible for achieving stable lock and meeting phase noise and spurious frequency targets. The narrow-band demands in a communications link mean the optimal bandwidth of the low-pass filter for minimum integrated noise (between 30 kHz to 100 MHz) is about 207 kHz (Figure 20) using the HMC507. This provides approximately –51 dBc of integrated noise and achieves frequency lock to within 1 kHz error in about 51 µs (Figure 22).

By contrast, the wideband HMC586 (covering from 4 GHz to 8 GHz) achieves the optimum rms phase noise with a wider bandwidth closer to 300 kHz bandwidth (Figure 21), achieving –44 dBc of integrated noise. However, it achieves frequency lock to the same specification in less than 27 µs (Figure 23). Correct part selection and the surrounding circuit design are all critical for achieving the best outcome for the application.

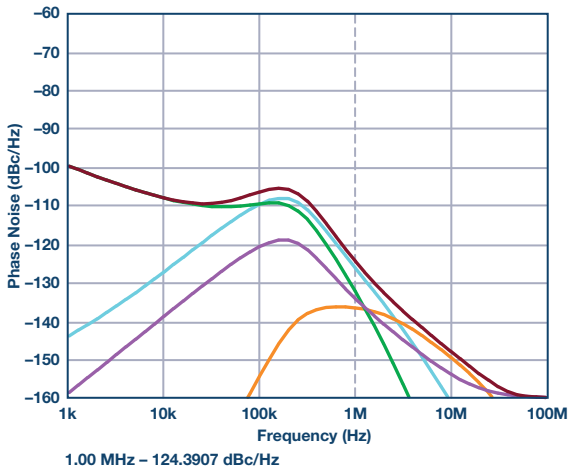

Figure 20. Phase noise HMC704 plus HMC507.

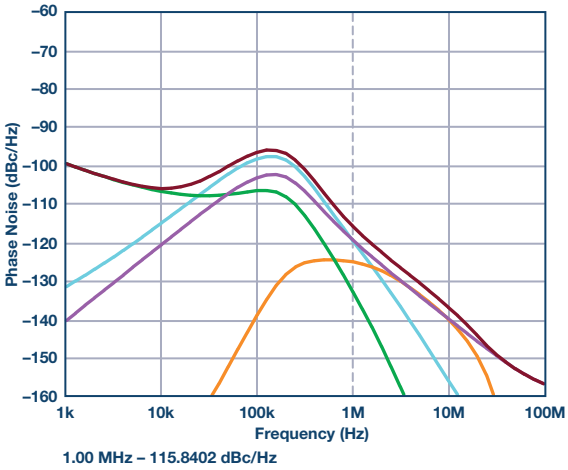

Figure 21. Phase noise HMC704 plus HMC586.

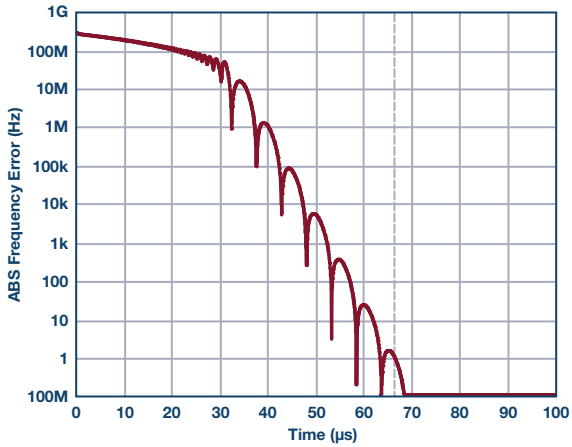

Figure 22. Frequency settling: HMC704 plus HMC507.

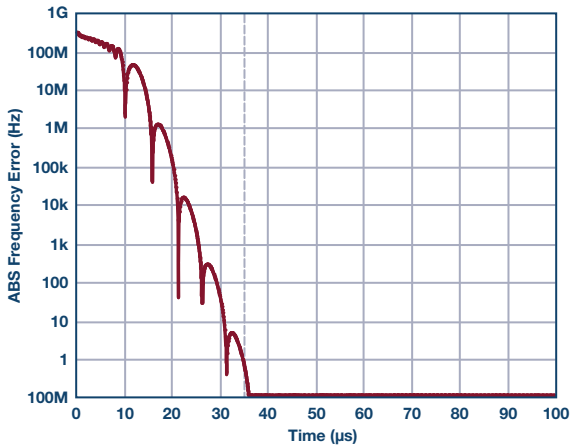

Figure 23. HMC704 plus HMC586.

Low Jitter Clocking

For high speed digital-to-analog converters (DACs) and high speed analog-to-digital converters (ADCs), a clean low jitter sampling clock is an essential building block. To minimize in band noise a low N value is desired; but to minimize spurious noise, integer-N is preferred. Clocking tends to be fixed frequency so the frequencies can be chosen to ensure

that the REF_{IN} frequency is an exact integer multiple of the input frequency. This ensures the lowest in-band PLL noise. The VCO (whether integrated or not) needs to be chosen to ensure that it is sufficiently low noise for the application, paying particular attention to the wideband noise. The low-pass filter then needs to be carefully placed to ensure that the in-band PLL noise will intersect with the VCO noise—this ensures lowest rms jitter. A low-pass filter with phase margin of 60° ensures lowest filter peaking, which minimizes jitter. In this manner, low jitter clocking falls in between the clock clean-up application of the first circuit discussed in this article, and the fast switching capability of the last circuit discussed.

For clocking circuits, the rms jitter of the clock is the key performance parameter. This can be estimated using ADIsimPLL or measured with a signal source analyzer. For high performance PLL parts like the ADF5356, a relatively wide low-pass filter bandwidth of 132 kHz, together with an ultralow REF_{IN} source like a Wenxel OCXO, allows the user to design clocks with rms jitter below 90 fs (Figure 26). Manipulating the placement of the PLL loop filter bandwidth (LBW) shows how decreasing it too much has an effect in which VCO noise begins to dominate at small offsets (Figure 24) where the in-band PLL noise would in fact be lower, and increasing it too much means the in-band noise is dominating at offsets where the VCO noise would instead be significantly lower (Figure 25).

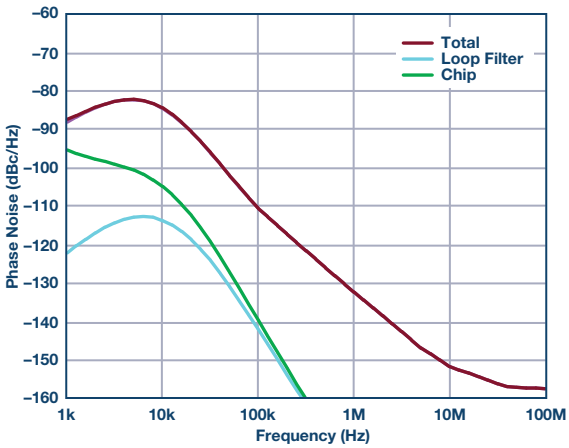

Figure 24. LBW = 10 kHz, 331 fs jitter.

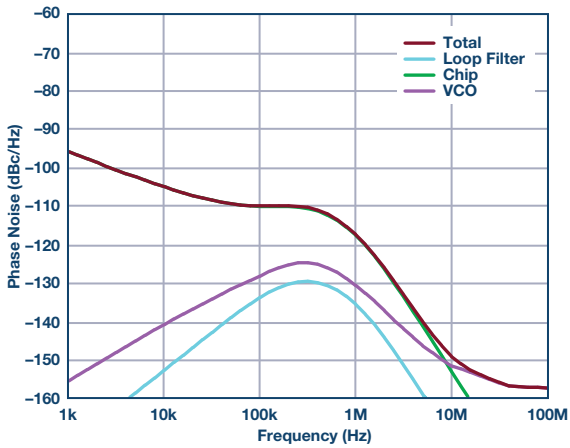

Figure 25. LBW = 500 kHz, 111 fs jitter.

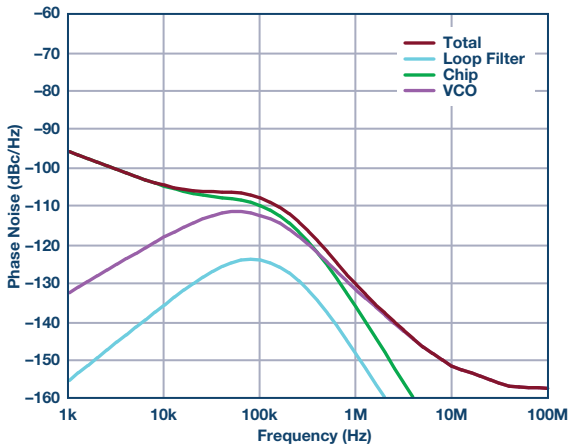

Figure 26. LBW = 132 kHz, 83 fs jitter.

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Curtin, Mike and Paul O'Brien. "Phase-Locked Loops for High Frequency Receivers and Transmitters." *Analog Dialogue*, Vol. 33, 1999.

Ian Collins [ian.collins@analog.com] graduated from University College Cork with a degree in electrical and electronic engineering and has worked in the RF and Microwave Group of Analog Devices since 2000. He is currently applications manager of the Microwave Frequency Generation Group, which focuses mainly on phase-locked loop (PLL) and voltage controlled oscillator (VCO) products. When not spending time at work or with his young family, Ian enjoys photography and the theater (both on- and off-stage), reading, and listening to music.

Ian Collins

Rarely Asked Questions—Issue 155
Home on the Range: Getting Multiple Gain Ranges With Instrumentation Amplifiers

By **Scott Hunt**

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Question:

I have an instrumentation amplifier, but I need wider dynamic range than I can get with a single gain. Can I multiplex gain resistors to get programmable gain?

Answer:

In order to maximize dynamic range in precision sensor measurements, it may be necessary to use a programmable gain instrumentation amplifier (PGIA). Because most instrumentation amplifiers (in-amps) use an external gain resistor (R_G) to set the gain, it would seem the desired programmed gains can be achieved with a set of multiplexed gain resistors. While this is possible, there are three major issues to consider before implementing a system this way with a solid-state multiplexer: supply and signal voltage limitations, switch capacitance, and on-resistance.

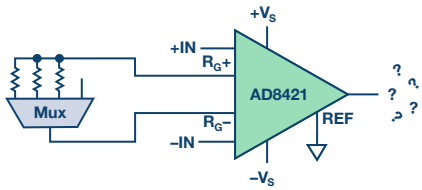

Figure 1. AD8421 PGIA with multiplexer.

Staying Within the Signal Range

Solid-state CMOS switches require a power supply. When the source or drain voltage exceeds the supply, fault current can flow and cause an incorrect output. The voltage at each R_G pin is typically within a diode drop of the voltage at the corresponding input; therefore, the signal voltage range of the switch must be greater than the input range of the in-amp.

Considering the Capacitance

The switch capacitance is similar to hanging a capacitor on one of the R_G pins and leaving the other R_G pin alone. A large enough capacitor could cause peaking or instability, but the more overlooked issue is the effect on the common-mode rejection ratio. In board layout, ground plane is generally removed from beneath the R_G pins, because capacitive imbalance less than 1 pF greatly reduces the ac CMRR. The switch capacitance can be in the tens of picofarads, causing large errors. Taking the simple case with an in-amp with perfect CMRR, no R_G present, and capacitance at only one R_G pin, the CMRR due to the capacitance can be approximated by:

$$CMRR(f) = -20 \times \log_{10}(f \times 2\pi \times RF \times C_{RG})$$

For example, if the internal feedback resistance, RF = 25 kΩ, and C_{RG} = 10 pF, the CMRR at 10 kHz is only 36 dB. This suggests using a low capacitance switch or a balanced switching architecture like the one shown in Figure 2 with SPST switches.

Regarding the Resistance

Finally, the on resistance of the switch impacts the gain directly according to the gain equation of the in-amp. If the on-resistance is low enough that the desired gain is still achievable, this might be okay. However, the on resistance of the switch changes with the drain voltage, specified as $R_{FLAT(ON)}$. The change in the switch resistance creates both a gain dependence on the common-mode voltage and a gain nonlinearity effect. For example, using an R_G of 1 kΩ and a switch with 10 Ω $R_{FLAT(ON)}$, there will be a 1% gain uncertainty over the common-mode range. A certain portion of that will translate to the differential signal (for example, a 2 Ω change would be 2000 ppm nonlinearity). This suggests using a low on resistance switch, which is contrary to the suggestion of a low capacitance switch because low on resistance is achieved with large transistor device

size whereas low capacitance is achieved with small transistors. The ADG5412F fault-protected, quad SPST switch provides a good solution in many cases. The architecture of these fault-protected switches allows them to provide 10 Ω on resistance that is very flat across the signal range and only 12 pF off capacitance.

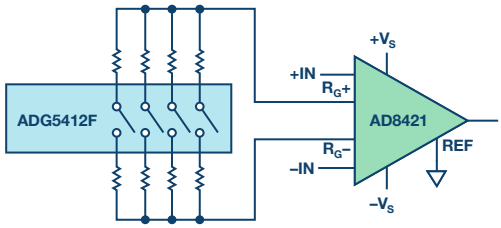

Figure 2. Balanced PGIA with ADG5412F quad SPST and AD8421.

Acknowledging the Alternatives

There are also other ways to implement the programmable gain in-amp function if these circuits don't meet the design requirements. It is highly recommended to choose an integrated PGIA if there is one that is appropriate. Integrated PGIAs are designed for high performance, have a smaller footprint, and fewer parasitics than discrete solutions, and the specifications include the effects from the internal switches. Some good examples of integrated PGIAs are AD8231, AD8250/AD8251/AD8253, and LTC6915. Additionally, there are solutions with higher levels of integration that include this function, such as AD7124-8 and ADAS3022.

Conclusion

In-amps are high precision components that are made as balanced as possible at the silicon level in order to reject common-mode. It is possible to build a programmable gain in-amp using solid-state switches, but it is also very easy to throw off the balance that defines the in-amp and reduce the precision of the circuit. The nonideal effects of the switches need to be considered in order to make the necessary trade-offs. Balanced switching architectures and modern switches like ADG5412F are great tools to optimize these designs. Integrated PGIAs are recommended because the effects of the switches are already included in the specifications.

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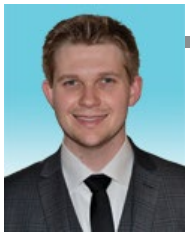

Scott Hunt

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How to Stay Out of Deep Water when Designing with Bridge Sensors

Volume 48, Number 1

Some Recent Developments in the Art of Receiver Technology: A Selected History on Receiver Innovations over the Last 100 Years

By **Brad Brannon**

Part 1: The Early Days

While there were many contributors to the early days of wireless, Guglielmo Marconi is one of the more prominent. While he is known for his wireless technology, many people are less familiar with the business he built around wireless technology at the turn of the 19th century. For about 20 years after the start of the 1900s, he built a critical business that launched the world of wireless toward what we have today.

Figure 1. Marconi demonstrating his technology.

While his commercialized technology was not the most up to date, it was good enough despite rapid technological changes because he figured out how to use the technology available to him to enable a new industry. Marconi set out to deploy a worldwide network capable of sending and relaying messages wirelessly at a time when the world was in turmoil at the end of colonialism and the wars and disasters that pockmarked the start of the 1900s, including the sinking of the RMS Titanic in April of 1912. The role that wireless played in both the rescue of survivors and the dissemination of the news of that accident reinforced the importance of this fledgling technology. The importance of wireless technology wasn't missed by either the public or the military, notably Joseph Daniels, who later became the secretary of the U.S. Navy. In the U.S. and elsewhere, leaders such as Daniels felt that the military should nationalize radio to ensure that they had access to it during wartime. It must be kept in mind that during this period, the only usable spectrum was below 200 kHz or so. At least for a while things moved this direction, but after World War I, the government's control of wireless weakened, but not before the formation of the government sanctioned monopoly that created the Radio Corporation of America (RCA).[1]

By our expectations, the radios of Marconi's days were quite primitive. The transmitters employed spark gap devices (only later did they employ mechanical alternators) to generate the RF, but on the receiving end, the systems were fully passive and consisted of an antenna, resonant LC tuner, and some sort of detector. These detectors will be covered shortly, but they were either mechanical, chemical, or organic. Some of these systems employed a battery simply to bias them, but not to provide any circuit gain as we might recognize today. The output from these systems was supplied to some sort of headset to convert the signal to audio, which was always very weak and just a simple click or buzz at best.

Because these systems provided no gain on the receiving end, range was determined by the amount of transmitted power, the quality of the receiver, the experience of the operator to adjust it, and, of course, atmospheric conditions. What Marconi realized was that given a reasonably predictable range, a network of stations could be built that could be utilized to reliably communicate information across both continents and oceans. This included installations both on land and at sea. Marconi set off to install his wireless stations across the globe and at sea, both on passenger ships and cargo ships. By installing systems on seafaring ships, he not only enabled them to communicate with their commercial interests on shore, but this also allowed Marconi to fill critical gaps in his network by providing relay and redundancy where needed.

One of the technologies that Marconi possessed was that of early vacuum tubes. John Ambrose Fleming, the recognized inventor of the vacuum tube, worked for the Marconi Corporation, but Fleming and Marconi's analysis at the time was that their existing technology was sufficient at detecting radio signals. Furthermore, they felt that the benefit of his discovery wasn't worth the additional expense or the batteries to run the valve tubes. Marconi already possessed several technologies that could detect a signal and didn't require the high power to run the filament and plate that a tube needed. Thus, they passed on this technology initially.

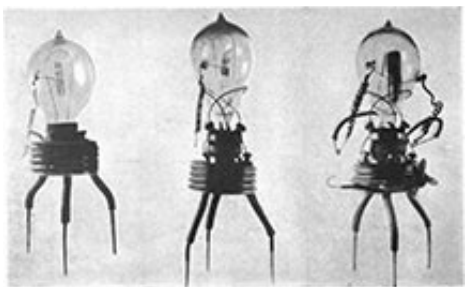

Figure 2. The first Fleming valve prototypes.

However, the so-called Father of Radio, Lee de Forest, took this technology and realized what the potential was. By insertion of a screen grid between the filament and the plate, he could not only rectify a signal, he could also control the amount of current in the plate. This enabled amplification. Even though there is evidence that he didn't understand how his Audion tube worked, he did realize the potential and did his best to capitalize on his invention both as a technology and as a value-added service similar to that created by Marconi. Through various business ventures, de Forest attempted to both manufacture and sell his vacuum tubes and to set up wireless networks like Marconi's. However, these ventures were doomed to failure not because of bad technology, but because de Forest's business partners were often less than honest, and often left him standing alone answering for the wrong doing of others. In the end, de Forest had to sell the rights to his own invention for others to profit from its capabilities.

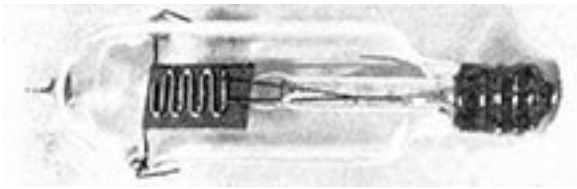

Figure 3. First audio triode de Forest tube.

One of those who early on realized the vacuum tube's possibilities was Edwin Armstrong. While he was still in high school, a family friend gave him one of de Forest's tubes to play with. Armstrong had already developed a reputation as an expert in wireless and, having built his own wireless station in the family home, quickly figured out how to utilize the device to develop a better receiver. While in college he continued to develop this technology, and developed the regenerative receiver that provided superior performance compared to the passive systems employed by all wireless stations of the day.

David Sarnoff was a senior figure in the American Marconi Corporation. His rise within the company was a direct result of a long-cultivated relationship with Marconi himself and a dedicated work ethic. Sarnoff began his career as an errand boy for AMC and by chance met Marconi on one of his visits to America. Sarnoff so impressed Marconi that he enabled him to rise to power within the company, with Sarnoff eventually taking senior leadership in both AMC and later in RCA. While visiting engineering labs around New York, he chanced across Armstrong. Armstrong's knowledge of wireless and the capabilities of his regenerative receiver helped forge a long-term professional and personal relationship between the two.

When WWI came, Armstrong felt the call of duty to enlist. By this time, however, he had developed a reputation as a wireless expert and, instead of being assigned combat duties, was assigned the role of inspecting and installing radios for combat services throughout France. His duties allowed him access to equipment and labs, as well as various technologies that enabled him to continue his research activities on the side. During an air raid in early 1918, he made a series of discoveries that led him to synthesize the superheterodyne receiver. Throughout 1918 he developed his concept and, by November, met with a close group of friends to demonstrate a prototype of the superheterodyne radio. They were impressed and urged him to continue his developments. By the end of 1918 the war was ending and, prior to returning to the U.S., Armstrong filed for a French patent on December 30, 1918. On returning to the U.S., he spent a few weeks recovering from an illness that delayed his filing for a U.S. patent. Eventually, he filed a U.S. patent for the superheterodyne receiver on February 8, 1919.

While Marconi's vision for wireless focused only on commercial information carried by telegraphy between two parties, Sarnoff had a much broader vision—to send a signal to many parties. Sarnoff's vision was not shared broadly early on, but eventually others realized that this new technology offered a means by which news and entertainment could easily be delivered over great distances, including the rural reaches of America. To help drive his vision, Sarnoff and his team conceived of broadcasting the Dempsey vs. Carpentier boxing match on July 2, 1921. The success of this broadcast enabled others to see the potential of broadcast radio as we know it today.

However, the real challenge of the time was technical. Early radios were difficult to use and didn't function very well. This is where the story continues for Armstrong, Sarnoff, and the Radio Corporation of America. Through the relationship developed earlier and the patents that RCA had acquired, including that of the superheterodyne, radio technology had been simplified enough to make it both portable and easy enough for anyone to use. From a technology point of view, the superheterodyne architecture was key to this success and this largely remains true today.

Figure 4. Edwin Armstrong and his wife Marion on their honeymoon with the first portable radio.

Detectors

A radio must have some way of producing an output that conveys meaningful information. In the early days, this was a sympathetic spark created in the receiving loop antenna. It was quickly realized that a more sensitive way of converting the radiated energy into a meaningful signal was required. Early technology was quite limited and often leveraged a wide range of properties including chemical, mechanical, and electrical.

In the very beginning, one of the first detectors used was called a coherer detector and was based on the discoveries of a Frenchman named Édouard Branly. The coherer consisted of two metal plates closely spaced with a supply of metal filings. As the RF signal presented itself to the plates, the metal filings adhered to the plates, closing an electrical circuit. This worked quite well for the detection, but once the RF signal was removed, the filings tended to remain attached to the plates. To solve this problem, some sort of tapper was arranged to hit the side of the device to force the filings to dislodge. This crude detector was effective yet bulky to use and operate because of this. Despite this, it was in use as late as 1907.

Figure 5. Coherer device.

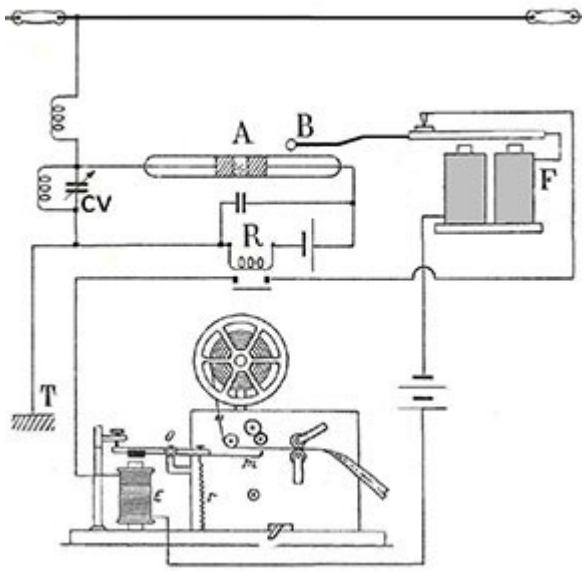

Figure 6. Coherer receiver schematic.[2]

A more practical solution was the electrolytic detector. This device consisted of a very fine platinum wire immersed in a solution of sulfuric or nitric acid. A battery was used to bias this circuit just to the point of electrolysis. This formed gas bubbles on the surface of the platinum wire, causing the current to drop. If the RF current was coupled into this circuit, it would modulate the electrolysis and cause the current to vary in relation to the strength of the coupled RF signal. This technique was developed by Fessenden and in common use from 1903 until 1913. One variation of this developed by de Forest was the responder, which consisted of two metal plates immersed in a solution of lead peroxide.

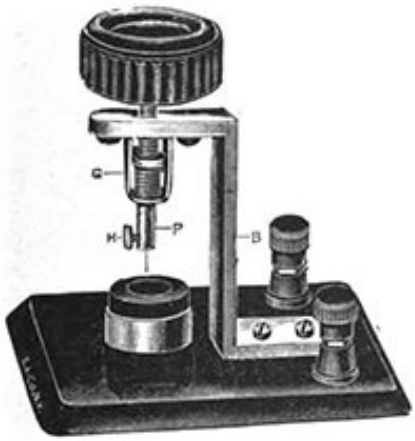

Figure 7. Electrolytic detector.

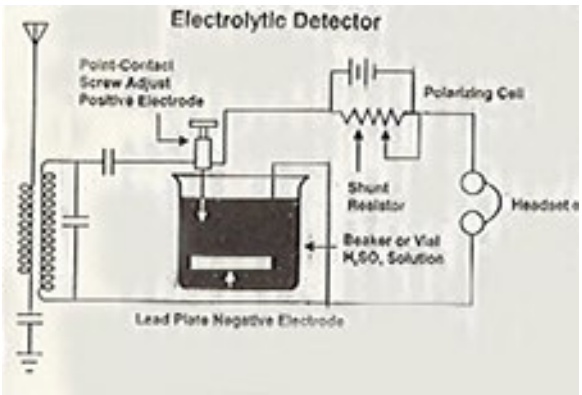

Figure 8. Electrolytic radio receiver.

Marconi preferred another approach called the magnetic detector. These devices were affectionately referred to as Maggies by their users. They worked by creating an endless loop of steel wire that was magnetized by permanent magnets while being circularly rotated. This magnetized portion of the wire was passed through a loop of wire connected to an antenna. The RF field in this coil would demagnetize the wire according to the received signal level present. The variations in the magnetic field in the wire was then picked up by another coil that was connected to an ear piece that provided an audible version of the RF signal. This approach was used by all Marconi installations until 1912, including on the RMS Titanic.

Figure 9. Magnetic detector as Marconi would have used.[3]

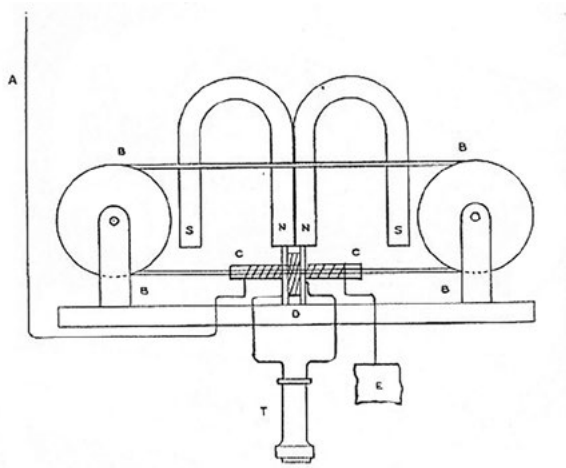

Figure 10. Schematic of a magnetic detector radio.

Another common type detector was the crystal detector, which remained popular until around 1925. This type of popular device was often referred to as a cat whisker and was basically an early semiconductor junction fashioned out of various types of mineral. Typical minerals included galena (PbS), iron pyrite (FeS_2), molybdenite (MoS_2), and carborundum (SiC). Small samples of these rocks were fashioned in a metal cup with a fine wire making a point contact on the rock. This contact could be moved and placed at various locations on the rock in search of the best operation. Crystal radios are still available today; the circuit is identical to that available 100 years ago, with the exception that a manufactured semiconductor diode replaces the cat whisker. One advantage of crystal detectors is that these devices provide more of a linear detection, which became important as AM broadcast began. This made voice communication possible, while earlier transmissions were only sent by Morse code.

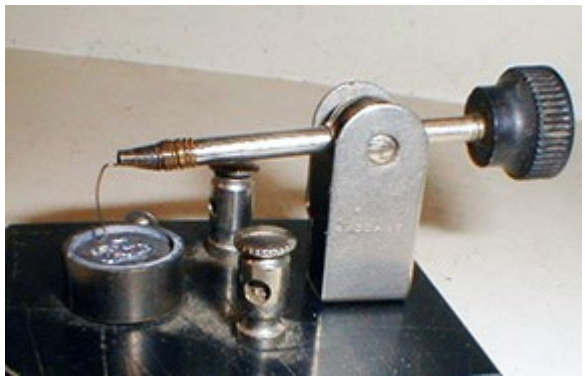

Figure 11. Galena cat whisker detector.

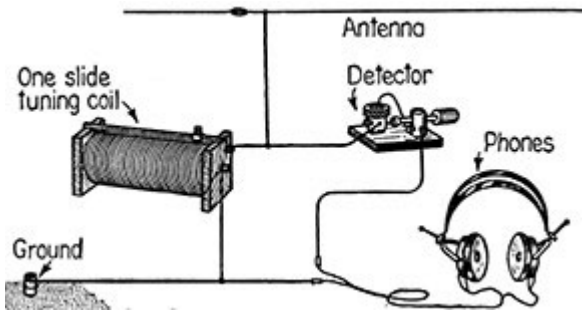

Figure 12. Typical crystal radio schematic.[4]

Another type of detector was created in 1904 by an engineer working for Marconi. John Ambrose Fleming discovered that by adding a plate to an Edison incandescent bulb he had created a rectifier or valve as it is often called. Marconi and Ambrose believed that their existing solution for

detection, typically a Maggie, was better than that offered by the Fleming valve and they temporarily discontinued their efforts to find a better solution until after 1912. Others, including de Forest, however, did see the immediate value and picked up where Fleming and Marconi left off by adding a screen grid between the filament and plate. This work was patented and published in 1906. While de Forest realized the value of his invention for improved radios, he was not able to capitalize on this, partly due to his business partner's misdeeds and partly due to various infringement cases against his patent.

Part 2: Receiver Architectures

One key point early radio pioneers like de Forest and Armstrong understood was that their successes were determined by a solid, reliable detector; in the early days, this was largely the wireless operator whose technical and auditory skills made it possible. However, as the industry grew, other aspects became important, such as including linearity and bandwidth.

In 1912, to address these issues, de Forest figured out regeneration and how a receiver could benefit from this technique. At nearly the same time, Armstrong made similar discoveries, and he noted that if energy was coupled from the plate circuit back into the screen tuner, significant amplification occurred as the amplifier response peaked prior to free oscillation. These discoveries set off a multidecade long patent dispute as each inventor claimed their invention came first.

Regardless, the key advantage of the regenerative receiver was that, in addition to the very high levels of gain achieved, the receiver facilitated connecting the output to a speaker as opposed to a small headphone with a weak audio output as had previously been used. Armstrong noted that, with this arrangement, he could easily copy Marconi's installation in Ireland from his New York lab, whereas Marconi typically required a relay station to achieve transatlantic coverage. After he was satisfied with his results, Armstrong invited Sarnoff to his lab to share his discoveries. With his regenerative setup, they spent the night DXing and received signals from the West Coast and into the Pacific with ease. This was a major enhancement for detector technology. The biggest challenge for the regenerative receivers was adjusting the feedback for proper operation; a challenging task even for an experienced operator. As early models of the regenerative and super-regenerative radios were put into productions, this challenge became apparent and required resolution before radio technology could be put into widespread usage.

World War I eventually drew the U.S. into the engagement and Armstrong received duty in France, where he was responsible for installing technology in the field. This afforded him the opportunity to continue his research where he conceived of the superheterodyne architecture in February of 1918 after working with colleagues in both France and Britain. Eventually, this architecture resolved many of the tedious adjustments required in prior architectures like the super-regenerative type without sacrificing performance.

Armstrong continued to develop the superheterodyne architecture throughout 1918, which solved many of the challenges of the regenerative and the super-regenerative receivers. This development enabled easy to operate radios consistent with those in production today. While a superheterodyne receiver is not strictly a detector, it does facilitate better, more consistent detection by including gain and additional selectivity, and by presenting a fixed IF regardless of the RF frequency being monitored. This allows the detector to be optimized without concern of degradation as a function of the desired RF frequency, which was a huge challenge of early radio and continues to challenge radio designers today, albeit at much higher frequencies even as we continue to explore new architectures including zero-IF and direct RF sampling.

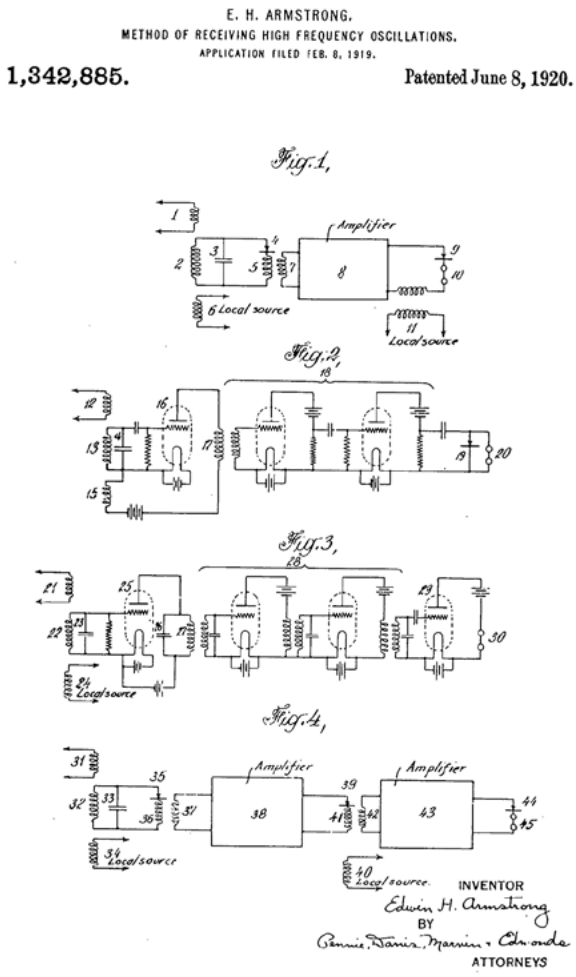

Figure 13. Superheterodyne patent figures.

These advantages have cemented the importance of heterodyne architectures, and this continues today. While the implementing technology has moved from tube to transistor to integrated circuit, the architecture remains key to many modern systems.

Outside of the shifting of technology types, little changed in radio architectures until the 1970s, with the advent of general-purpose DSPs and FPGAs. Detector functions moved from linear detector elements like diodes, discriminators, and PLLs to analog-to-digital converters followed by digital signal processing. This enabled significantly more capability not possible with older technology. While data converters followed by DSP can and do perform traditional AM and FM[5] demodulation, use of digital processing techniques enables complex digital demodulation used widely for digital television, HD Radio® in the United States, and DAB in Europe and other regions around the world.

In early digital systems, the IF stage was typically converted to a baseband signal with an I/Q demodulator and then digitized by dual low frequency ADCs, as shown in Figure 14. These early ADCs were relatively low bandwidth and therefore radios tended to be narrow-band systems. While these systems are workable for low bandwidth systems, they suffered from quadrature mismatches that caused image rejection issues that had to be corrected for by analog and later digital techniques. Because early systems were not highly integrated, it was difficult to maintain balance between I/Q, which resulted in image errors (quadrature). This was complicated due to

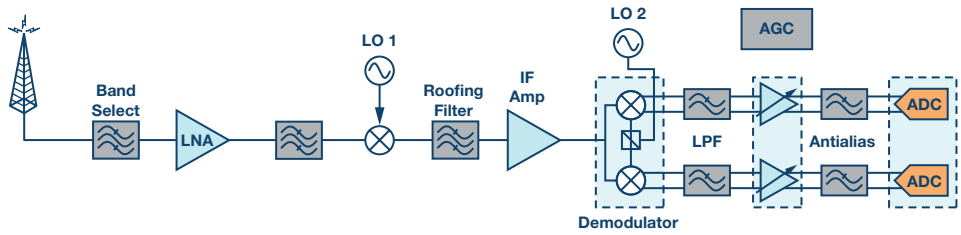

Figure 14. Dual conversion baseband sampling.

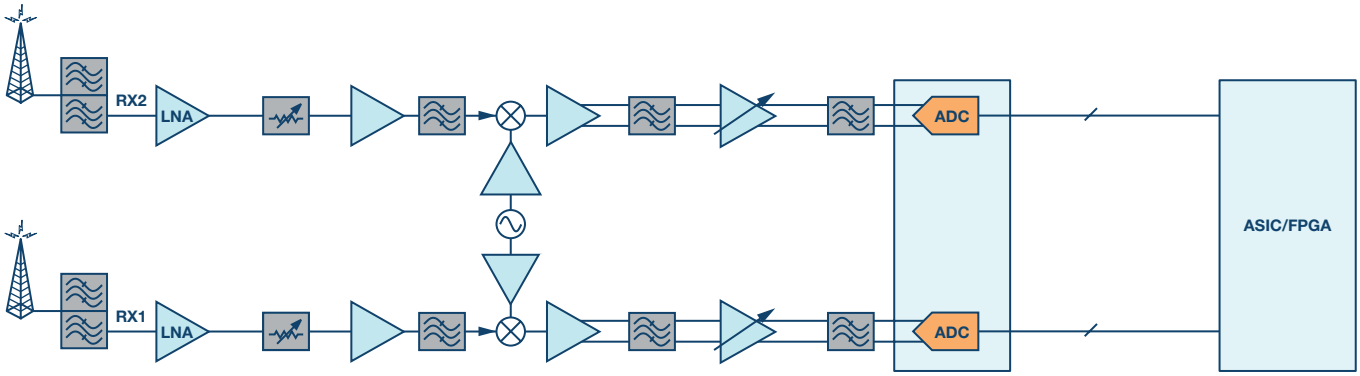

Figure 15. Typical IF sampling architecture.

shifts over time and temperature that had to be carefully accounted for. Even in highly integrated systems, I/Q balance is typically limited to 40 dB or worse image rejection without some sort of corrective algorithm.

By the mid-'90s, converter technology began to improve enough that baseband I/Q sampling could be replaced with IF sampling. This had several advantages. First, the demodulator and baseband converter pair could be eliminated and replaced with a single ADC saving power and board space. More importantly, the errors associated with analog I/Q extraction could be eliminated. Of course, complex data was still required for DSP processing, but it could easily be extracted digitally by using digital downconverters (DDCs) like the AD6624 that provide perfect quadrature that doesn't drift over time or temperature.

Initially these IF sampling converters were narrow band, but in the late '90s, wideband IF sampling converters became available, including devices like the AD9042 and AD6645. These new devices could sample IF frequencies as high as 200 MHz and provide a signal bandwidth of up to 35 MHz. This became interesting enough that many high performance receivers began adopting IF sampling to both simplify the radio and to improve performance. One of the many advantages of this technique is that one receiver signal path could process multiple RF carriers.[6] This had the effect of allowing one radio to replace many analog narrow-band radios and greatly reduce the cost of ownership in many telecommunications applications. Any application that processed multiple independent (or dependent) RF signals could benefit from this type of architecture, which allowed for a reduction in cost, size, and complexity. Individual RF carriers are easily sorted out in the digital data stream where they could be independently processed as required. Each signal could be modulated differently with unique information or the signal bandwidth could be widened to increase the data throughput. Integrated mixer technology, including the ADRF6612 and ADRF6655, continues to move IF sampling heterodyne radios forward by providing highly integrated and low cost solutions when combined with new IF sampling converters like the AD9684 and AD9694. These new ADCs include digital downconverters (DDCs) that not only digitally filter unneeded spectrum, but that also digitally extract out the I/Q components.

Side by Side: Then and Now

Armstrong's patent[7] states that "It is well known that all detectors rapidly lose their sensitiveness as the strength of the received signal is decreased, and that when the strength of the high frequency oscillation falls below a certain point, the response of a detector becomes so feeble that it is impossible to receive signals." Armstrong claimed that as amplitude fell or as frequency increased, detector sensitivity was reduced. He and others sought a method to extend the usefulness of radio to higher frequencies and to improve overall performance.

Based on earlier work with tubes such as the Audion tube and regeneration, Armstrong realized that he could convert the incoming frequency to one that worked more efficiently with the detectors available. Furthermore, gain could be applied to increase not only the RF signal level, but the audio signal level provided to the user.

Figure 16 shows one of the patent's diagrams, which "illustrates in detail the utilization of [Armstrong's] method using a tuned amplifier system wherein 21 is the source of the incoming oscillations (signals), and a vacuum tube rectifying system 22-23-25 converts the combined oscillations of the incoming and those from the separate heterodyne 24 (local oscillator). The circuit 26-27 is tuned to the converted combination of the two oscillations (desired mixer product). A multitube high frequency amplifier 28 amplifies the resulting energy heterodyned and detected by the vacuum tube system 29 and indicated by the telephones 30."[7] By using this method, Armstrong was able to take the RF energy and shift the frequency to one that could easily and efficiently be detected as well as provide sufficient amplification for a comfortable audio level. In his patent, he goes on to show that multiple stages of heterodyning can be applied, which has the advantage of providing additional selectivity and higher levels of gain without the concern of uncontrolled feedback causing oscillation—a problem that plagued earlier radio architectures such as the regenerative receiver.

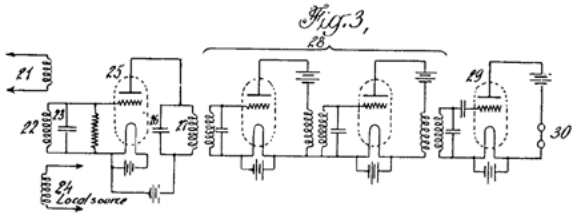

Figure 16. Armstrong's superhet diagram.

The following figures help to better compare tube technology to a contemporary implementation and show how modern designs remain similar to the original design proposed 100 years ago.

Figure 17 shows both circuits placed side by side. The first tube stage, according to Armstrong's patent, consists of a vacuum tube rectifying system. This first stage combines the mixing of the desired signal with the LO by taking advantage of the rectifying properties of the tube to produce the typical mixing products. Armstrong suggested 10 MHz (shown in Figure 18) as an RF because this was beyond what detectors of his time could respond to and because it represented a technical challenge to him during the period when he was developing the superheterodyne receiver. Modern receivers typically include at least one RF amplifier prior to the mixer to provide lower noise and better sensitivity as is shown in the lower signal chain. These devices are typically very low noise FET designs optimized for the frequency range of operation. The only fundamental difference between what Armstrong originally patented and modern designs is the separate RF amplifier placed before the mixer. By WW2, it was common to find tube type designs with front-end amplifiers equivalent to today's FET front ends.

He suggested that this incoming RF signal could be combined with an LO of perhaps 10.1 MHz to produce a new tone at 0.1 MHz during the first stage. We recognize this as the sum and difference products of a typical mixer, as shown in Figure 19. In the tube schematic in Figure 18, the LO was coupled directly into the input circuitry where the nonlinear behavior of the tube produced these products. One challenge this original design would have posed would have been unintended radiation of the LO by way of the direct coupling to the antenna. Contemporary designs are less susceptible to this radiation, although not completely, because, as shown in Figure 19, the LO is coupled into a mixer isolated from the input by the front-end amplifier. One improvement Armstrong proposed was that Amplifier 1 could also be used as the local oscillator in addition to the detector by taking advantage of feedback from the plate into the grid circuit similar to what he and de Forest had accomplished with the regenerative receiver. This would have created a compact front-end function. In today's circuitry, the mixer, local oscillator, and RF and IF amplifiers are often included on a single IC. These devices are widely available for many different applications from consumer to industrial needs.

For both the tube and monolithic front ends, the mixing process produces sum and differences between the RF and LO. In Armstrong's case, this meant 0.1 MHz and 20.1 MHz. In addition, it is common to have both RF and LO leakage to the output as well. The unwanted terms created by the mixer must be filtered out in order to receive the desired signal. Since the bandwidth of the detector was limited, Armstrong focused in the difference term, 100 kHz. It is likely that his 2-stage IF amplifier provided some filtering of the other terms in addition to the resonant L-C structures he included. A contemporary IF amplifier will include some sort of IF filter as well. Figure 19 shows a basic LC filter, but, often, some form of high Q filter is used. Narrow-band radios often use quartz or ceramic filters for the IF stage; wider band designs often take advantage of SAW or BAW depending on the requirements. Often, this filter is referred to as a roofing filter and is used to protect following stages from strong out-of-band signals.

With a well filtered and strong IF signal, Armstrong could now easily detect what were once weak RF signals outside of the bandwidth of his detector. Now at an IF, they easily matched what detectors were capable of. In the case of the tube, these signals were rectified and then amplified so that they could drive a speaker directly, at least for amplitude modulated signals. In contemporary receivers, an analog-to-digital converter samples the analog IF and produces a digital equivalent, which is then processed digitally (including demodulation). In the case of an audio application, it can then be converted back to analog with a digital-to-analog converter to drive a speaker if necessary.

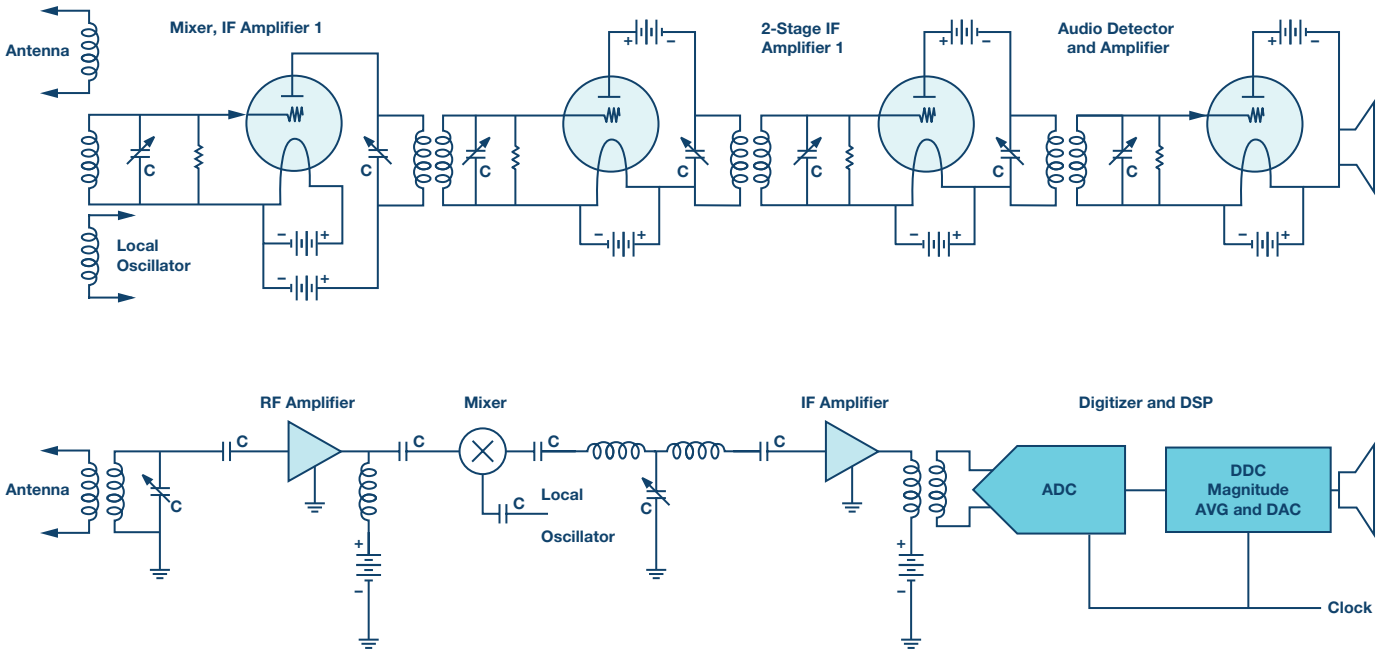

Figure 17. Tube vs. contemporary superhet.

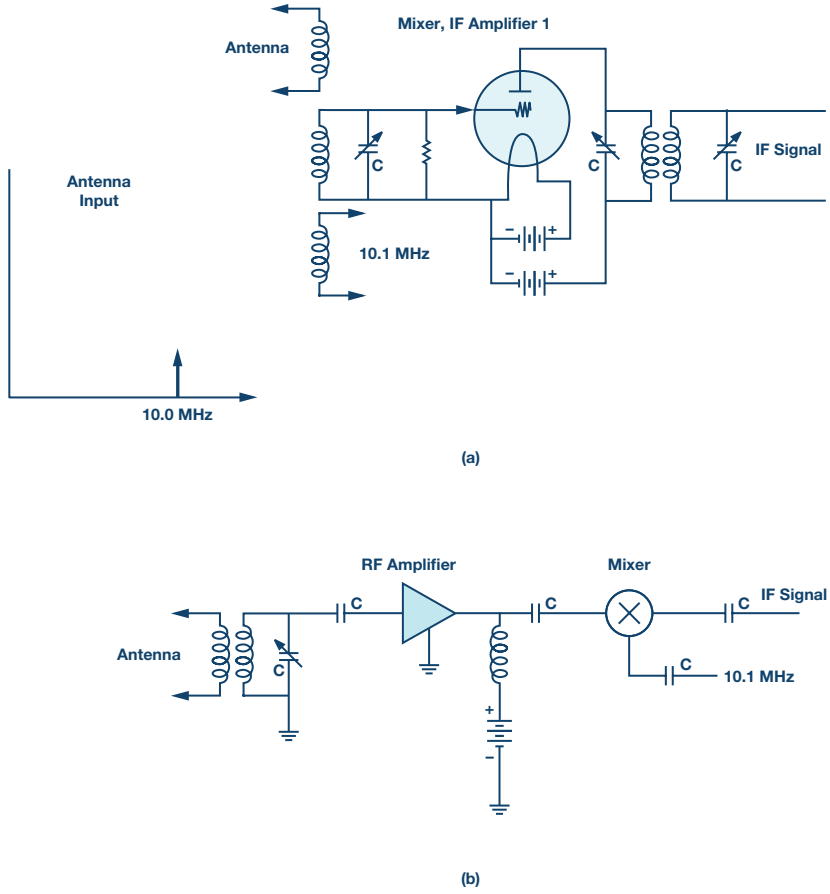

Figure 18. (a) Tube front end, (b) front end.

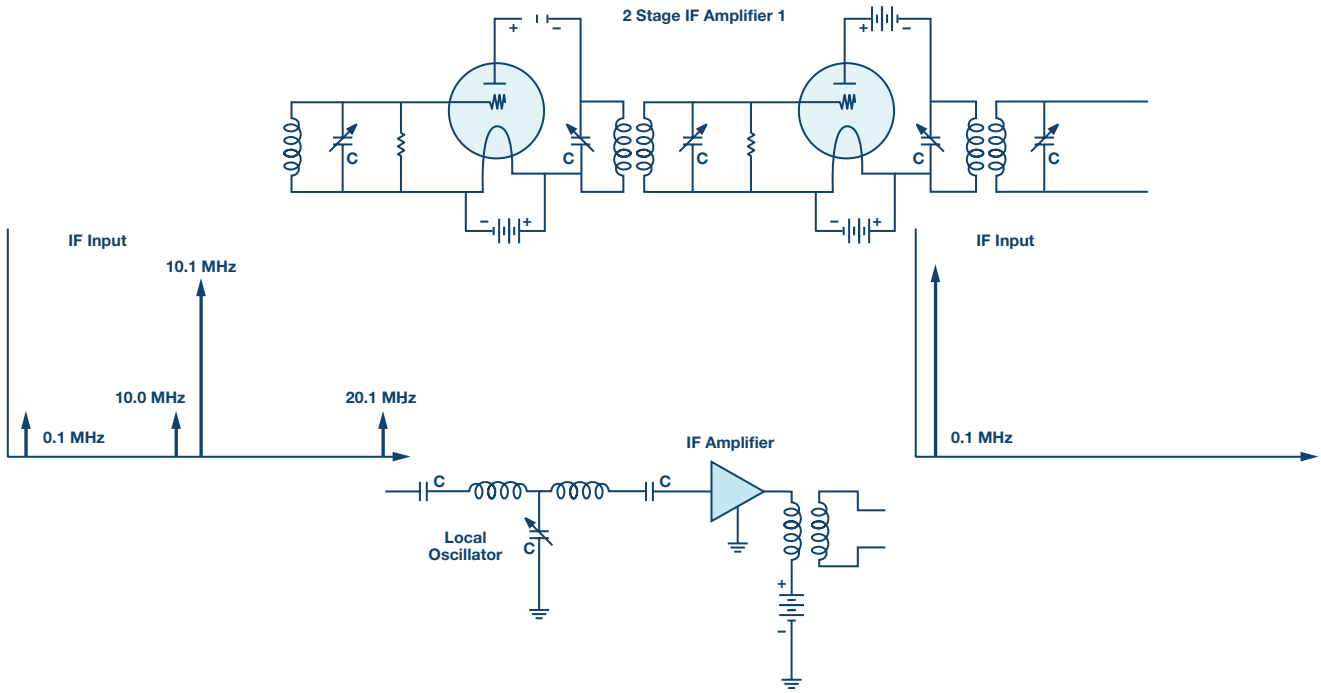

Figure 19. IF amplifier stage.

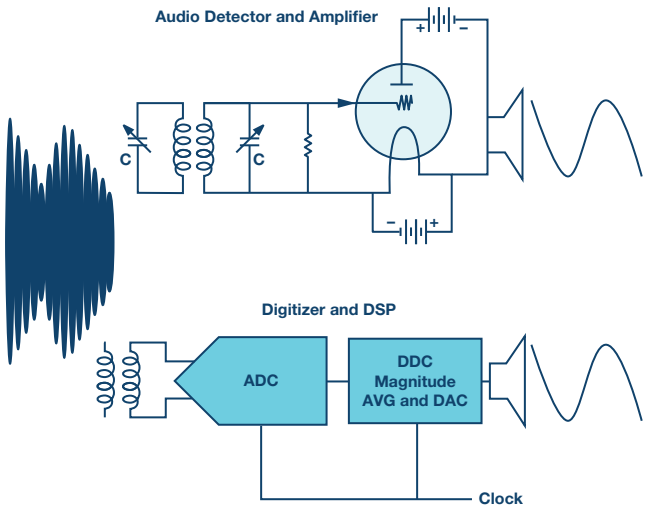

Figure 20. Detector.

While both tube and transistor versions of these radios can achieve a similar result, contemporary designs have a range of advantages. Notably, modern designs are much smaller and the power requirements are greatly reduced. While portable tube radios existed from the beginning, transistors enabled pocket size radios. Integrated circuits enabled single-chip radios for a wide range of applications from short-range wireless like the ADF7021 through high performance offered by way of AD9371. In many cases, this includes both the receiver and the transmitter.

Since monolithic radios typically utilize analog-to-digital and digital-to-analog converters, these readily facilitate complex modulation. Tube type radios historically were limited to basic modulation types such as AM and FM. When data converters are added to the radio, as is typically done on monolithic radios, new forms of modulation can be introduced by way of digital techniques including spread spectrum and OFMD, which are at the heart of most modern communications (digital TV, HD Radio, DAB, cell phones) that we rely on daily.

As radio technology continues to evolve, more advancements will come that may enable radio architectures or provide functions not currently possible. Today we have a wide selection of IF sampling superheterodyne and zero-IF architectures in highly integrated forms. Other architectures on the horizon include direct RF sampling where the signal is directly converted to digital without analog downconversion. As radio technology continues to evolve, the number of available options will grow. However, it is likely that some form of heterodyne will be with us for some time to come.

Conclusion

In the 100 years of the superheterodyne radio, little has changed in the architecture except the implementation technology. We have witnessed many changes through the years in the medium on which radios have been constructed as we've seen technology migrate from tubes to transistors to monolithic integrated circuits. These changes have enabled possibilities that were only a daydream to the early radio pioneers and on which our daily lives are so closely tied to.

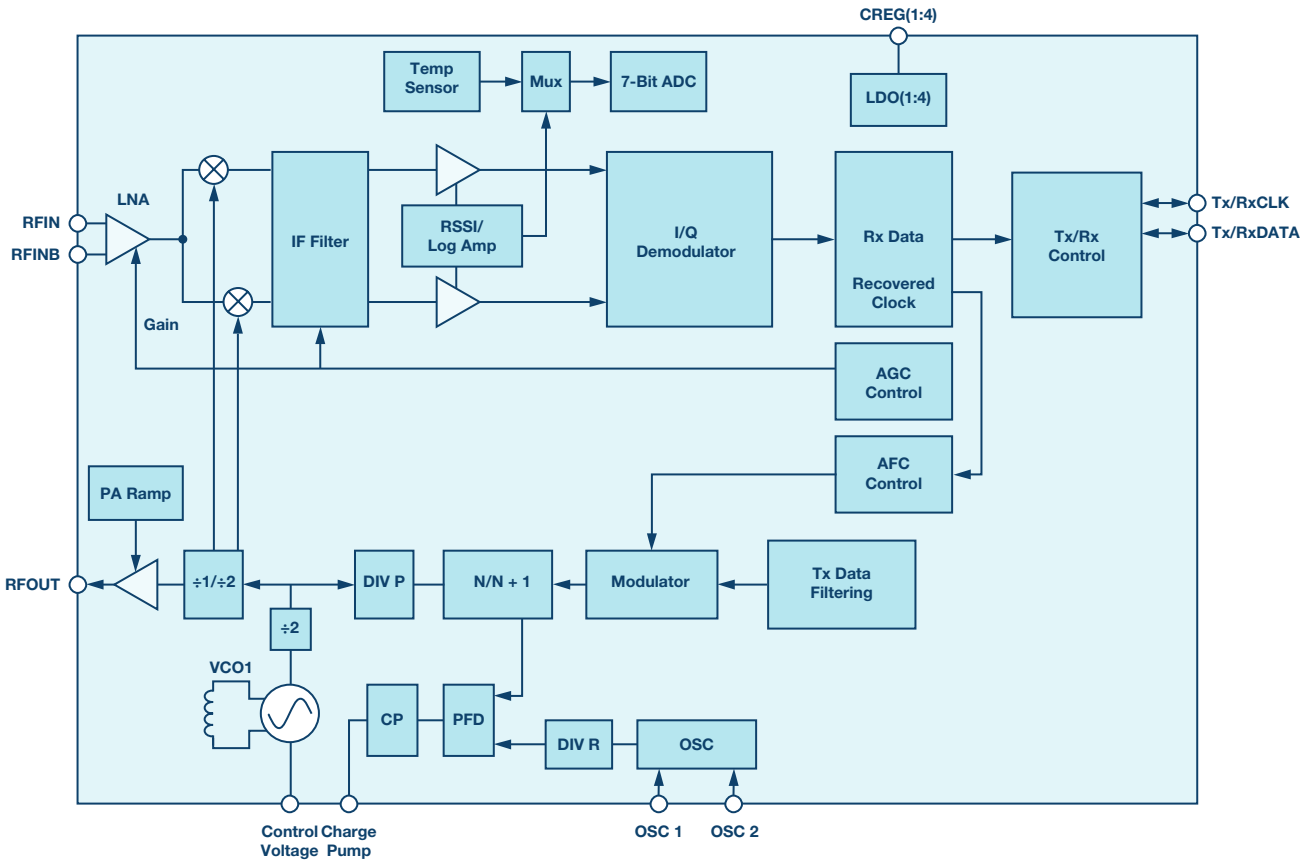

Figure 21. ADF7021 short-range wireless (simplified).

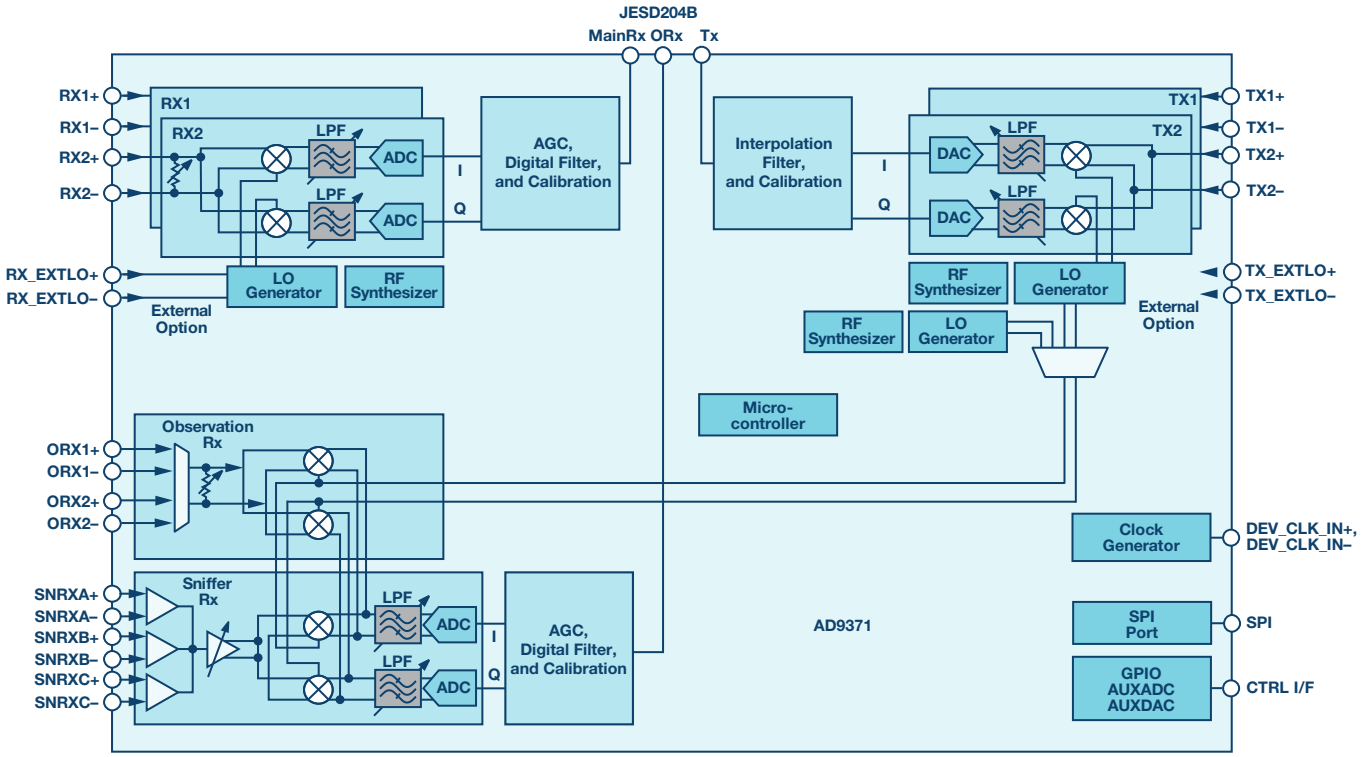

Figure 22. AD9371 ZIF transceiver.

One of the key elements that has made this possible is the detector fulfilled by the high speed ADC in today's radio technology. Improvements over the last few years in data converter and other technology has ushered in our connected world, which is changing our daily lives and the fabric of modern society. The exciting part is that this core technology is continuing to evolve, which will continue to enable new wireless solutions that may not be known today. The next 100 years carry as much potential to the next generation of wireless as Armstrong and Levy's inventions provided to the last 100 years.

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Brad Brannon

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Volume 50, Number 3

The Many Uses of a 200 mA Precision Voltage Reference

By **Michael Anderson**

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The LT6658 is not a run-of-the-mill reference or regulator, as it performs both functions equally well. Moreover, due to its unique architectural arrangement, it does much more than simply supply a precise voltage with plenty of current. The following circuits, which will be discussed throughout this article, demonstrate a wide range of circuit possibilities. While there are quite a few applications illustrated, there will undoubtedly be applications that LT6658 would make a compelling solution, but have not been explicitly implemented here. As a product that is both a voltage reference and regulator, LT6658 is referred to as the Refulator™.

The Refulator is intended for designs that require a precision reference and the ability to power associated signal chain components, such as data converters, amplifiers, bridge transducers, and other high performance circuit devices.

Introduction

This listing of key specifications and feature illustrates LT6658's performance. Key reference specifications include drift at 10 ppm/°C and initial accuracy at 0.05%. Key regulator specifications are load regulation at 0.25 µV/mA with two outputs sourcing current at 150 mA and 50 mA. Outstanding PSRR, low noise, output tracking, and a noise reduction pin combine to bring together the best of both the reference and regulator worlds into a single package.

Dual Outputs:

- Source current: 150 mA and 50 mA
- Sink current: 20 mA/buffer
- Drift: 10 ppm/°C
- Accuracy: 0.05%
- Load regulation: 0.25 µV/mA
- Output tracking: ±150 µV
- PSRR: >100 dB at 10 Hz
- 0.1 Hz to 10 Hz noise: 1.5 ppm p-p
- Maximum supply: 36 V
- Noise reduction pin
- Output disable pin
- Current protection
- Thermal protection
- Small footprint
- Temperature range: –40°C to +125°C

The typical application for the LT6658 is shown in Figure 1. The internal block diagram illustrates the band gap function followed by an optional filter function, followed by two buffers with their noninverting inputs tied together. In this application, the inverting inputs to the buffers, V_{OUT1_S} and V_{OUT2_S}, are tied to the outputs V_{OUT1_F} and V_{OUT2_F} as a voltage follower with Kelvin sense.

The LT6658 differs from many references and regulators in that it has a class A/B output stage that actively sinks, as well as sources current. In addition, it is designed to drive capacitive loads from 1 µF to 50 µF or higher. Large capacitive loads are stable when a 1 µF ceramic capacitor is placed on the output in parallel with a large capacitance.

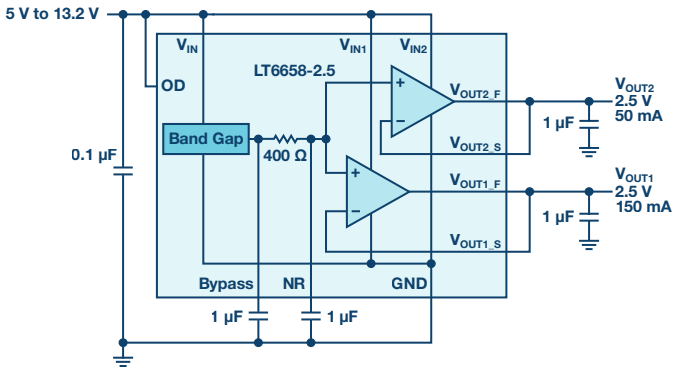

Figure 1. The LT6658 typical application.

The output buffers are trimmed to minimize drift resulting in excellent tracking over operating and load conditions. The complete data sheet with specifications can be found here.

Simple Output Configurations and Applications

Since the inverting inputs are available they can be arranged for nonunity gain, as shown in Figure 2. An LT5400-4 has 0.01% matching maintaining the precision of the LT6658. This example provides a precise 5 V and 2.5 V rail and can be used as a ±2.5 V regulator application with a split supply ground provided by the 2.5 V output. Nonunity gain can be applied to both outputs to generate any output voltage between 1 V and 6 V.

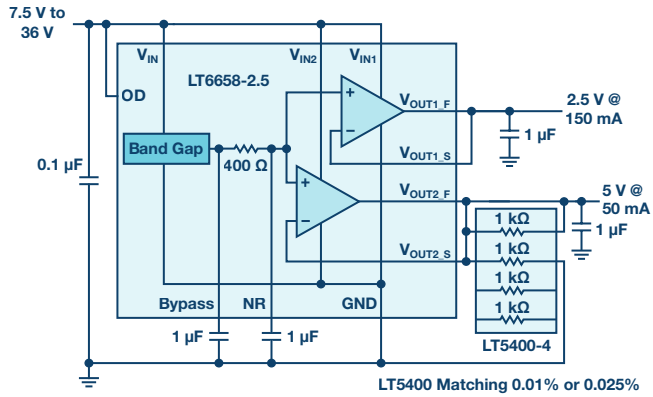

Figure 2. Simple, nonunity gain circuit creating a ±2.5 V split supply with ground.

A lower output voltage can be generated from a higher output voltage using the inverting input. Figure 3 demonstrates how a 3.3 V output can be used to generate a 1.8 V output. Since the noninverting inputs are tied to 2.5 V, it's simple to create a lower output voltage. The expression for V_{OUT2_F} is

$$V_{OUT2\_F} = 2.5\ \text{V}\left(1 - \frac{R_{F1}R_{F2}}{R_{IN1}R_{IN2}}\right)$$

where R_{F1} and R_{F2} are the buffer feedback resistors and R_{IN1} and R_{IN2} are the buffer input resistors.

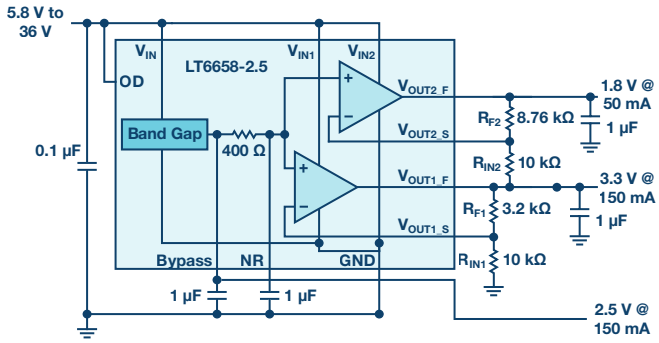

Figure 3. An application with gain and inversion.

The only parameter that is compromised in this application is accuracy, which is dependent on the ratios of R_F/R_{IN}. In addition, this application illustrates how the BYPASS output can be used as a ±10 mA source and sink output. Note that any change on the BYPASS pin will directly affect the V_{OUT1} and V_{OUT2} outputs.

The output voltages can be trimmed to values between 2.5 V and 6 V, as shown in Figure 4. The trims can be accomplished with mechanical trim or digital trim pots. Digital trim is especially helpful to correct for ADC and DAC errors. The trim pots can be ganged to produce the same output voltage or the outputs voltages can be independently controlled.

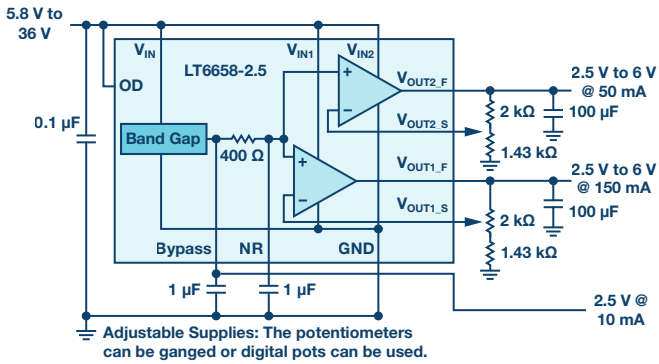

Figure 4. Adjustable gain.

Having two output buffers provides flexibility where one output can provide a necessary voltage, and the other output can provide a precision current source, as shown in Figure 5.

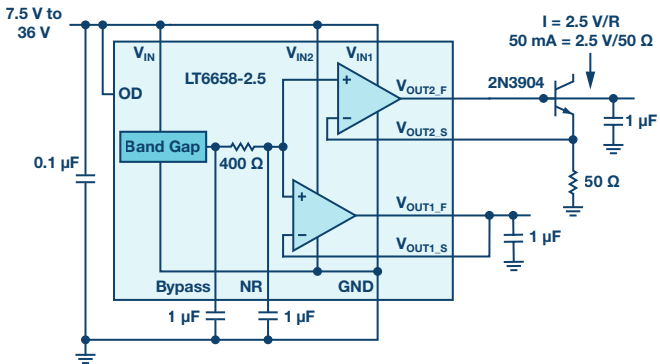

Figure 5. A precision voltage source and a precision current source application.

Note that the output V_{OUT2_F} pin will be one V_{BE} higher than the sense line. The supply voltage should be adjusted to accommodate the higher output voltage on V_{OUT2_F}. Since each output has an independent supply input, they can be driven separately to improve channel-to-channel isolation or to accommodate different output voltages without consuming excessive power.

Typically, when one mentions a voltage reference and oscillation in the same sentence, they are referring to undesirable behavior. However, to highlight the unique architecture of the LT6658, the multivibrator circuit in Figure 6a is introduced, along with the resulting waveforms in Figure 6b. Here a 2.2 µF capacitor and 1 kΩ resistor set the time constant. The 400 Ω external positive feedback resistor and 400 Ω internal resistor set the hysteresis and affect the output frequency, which is roughly f = 1/2.2 RC. The value of the internal resistor is 400 Ω ±15%, which will affect the output frequency.

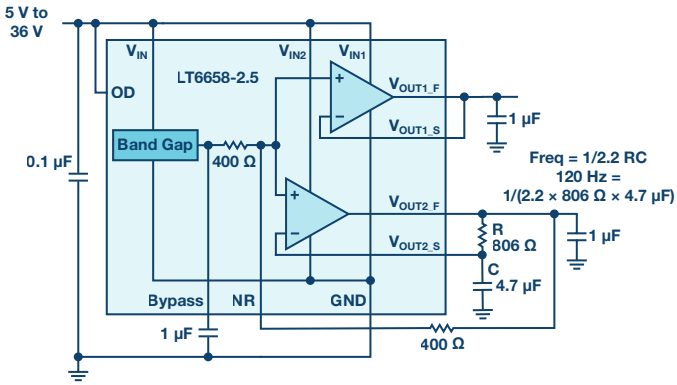

Figure 6a. Multivibrator application.

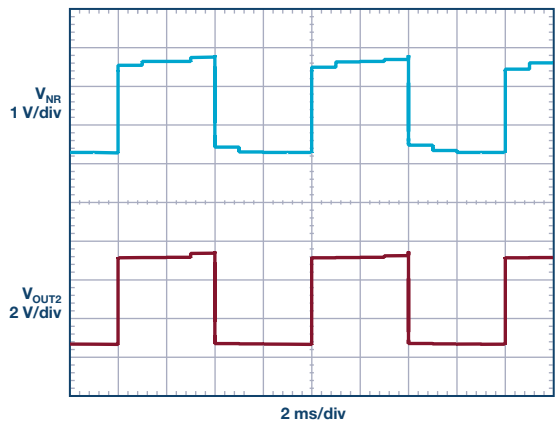

Figure 6b. Multivibrator output.

This circuit example shows the output voltage swing is slightly less than 4 V where the output low voltage goes down to 0.9 V and the output high voltage reaches to V_{IN} – 2.5 V. V_{IN} in this example is 6 V and the output is not fully loaded. As V_{IN} increases past 8.5 V, the output will clamp around 6 V and the output duty cycle will reduce to about 40%.

Since current is flowing through the 400 Ω internal resistor, the voltage at the NR pin varies, causing V_{OUT1} to also oscillate synchronously with V_{OUT2}.

Another dynamic circuit that is usually not associated with a voltage reference is the audio amplifier. The dual class A/B outputs can be arranged to drive 8 Ω and 16 Ω speakers, as shown in Figure 7. A single-ended source drives the inverting input of V_{OUT1}, which drives the inverting input of V_{OUT2}. The band gap sets a precision common mode, while the outputs act as a differential driver. To improve slew rate, use the minimum output capacitance on the LT6658.

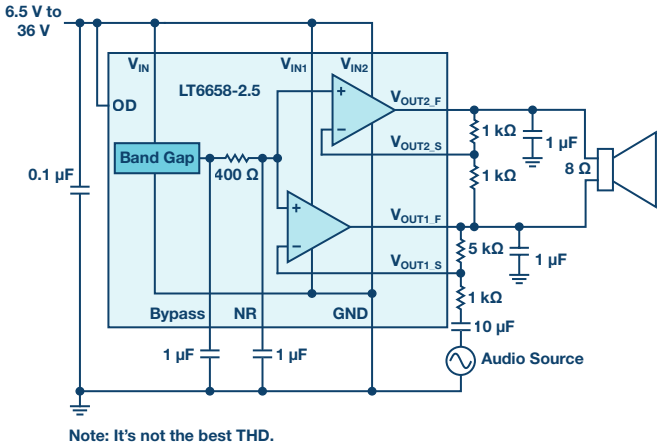

Figure 7. An audio application circuit.

With the addition of complementary discrete BJT output devices, the circuit in Figure 8 can supply more power. The circuit shows only one amplifier circuit, though two speakers can be driven by the two outputs to create stereo. While there are better audio amplifier choices, these applications demonstrate the flexibility of the LT6658 architecture.

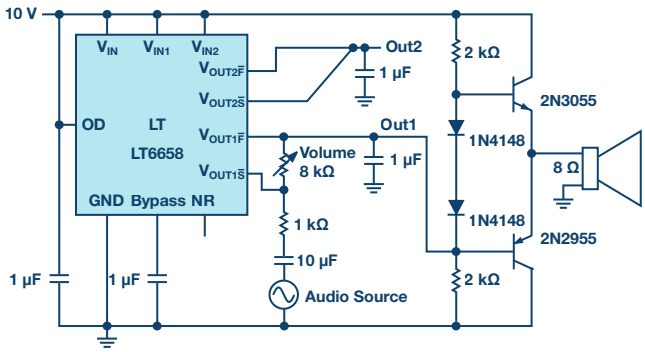

Figure 8. An audio application circuit using discrete BJTs.

Strain Gage Applications

The LT6658 can act as a regulator and a reference, as shown in the following strain gage application (Figure 9). The LT6658 provides the reference voltage and supply voltage to four LTC2440, and the 2.5 V rail biases the four strain gages. Each strain gage draws 7.5 mA totaling 30 mA, which is well within V_{OUT2}'s 50 mA output specification and provides the ADC reference input. V_{OUT1} supplies 8 mA to each LTC2440 for a total of 32 mA.

Figure 10 shows a bridge circuit application with three load cells. The LT6658 provides a precise and stable operation even though the total load resistance is only 82 Ω requiring 60 mA. The high gain buffer will maintain a precise voltage capable of driving the load cells. The second output can drive another strain gage or supply power to the ADC converter downstream.

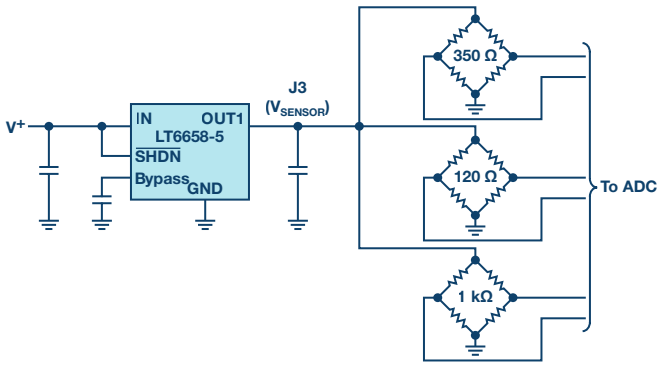

Figure 10. A bridge circuit application.

Data Acquisition Applications

For precision applications that use a DAC where the reference current is code dependent, it is important to pay special attention to board layout and parasitic resistance. To maintain an INL <0.1 LSB with the LTC2641, load regulation needs to be <19 ppm/mA. Further, reference output impedance and PCB resistance needs to be <48 mW. The LT6658 has a dc output resistance of about 0.2 mW, leaving a 47.8 mW error budget for PCB resistance.

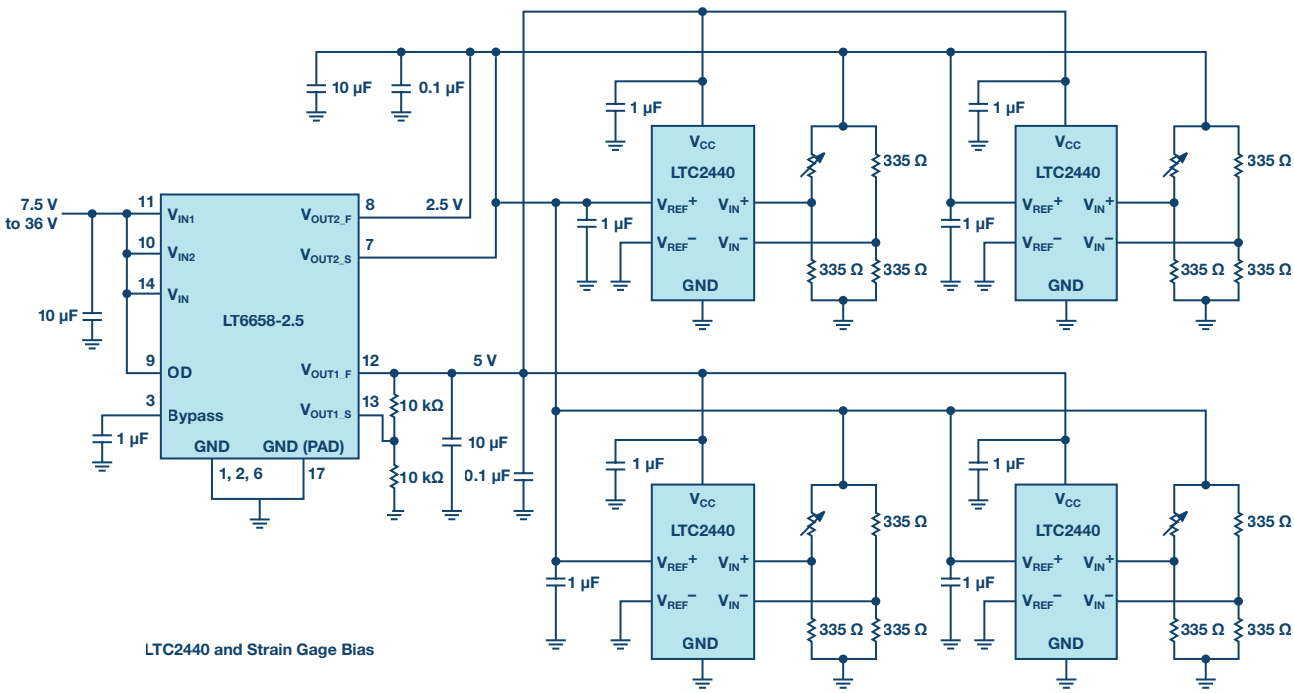

Figure 9. The LT6658 as a reference and regulator for a strain gage application.

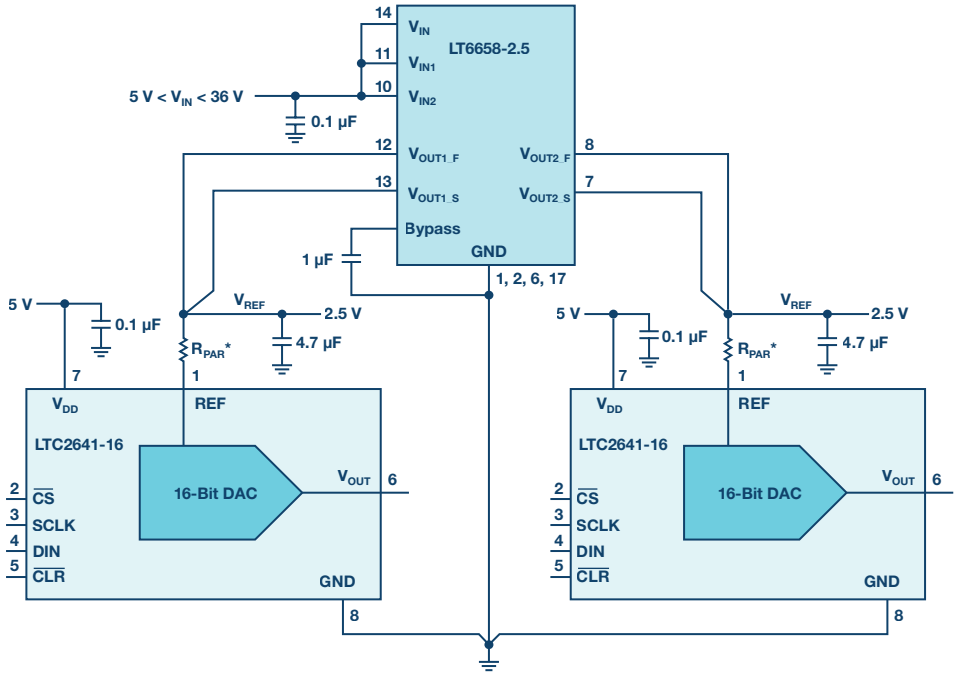

Figure 11. The LT6658 driving two code dependent DAC reference inputs.

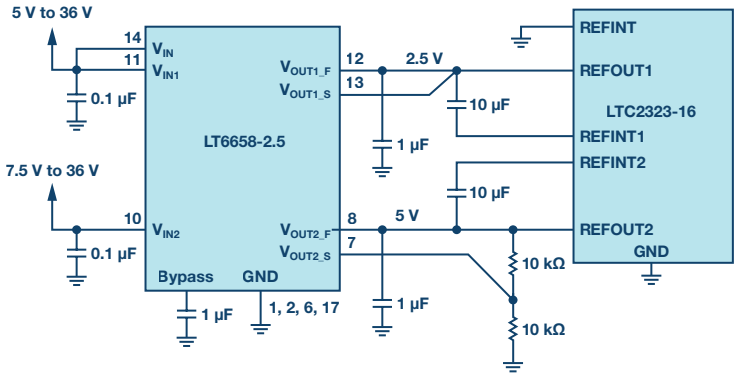

Figure 12. The LT6658 driving the LTC2323-16 dual ADC with independent voltage references.

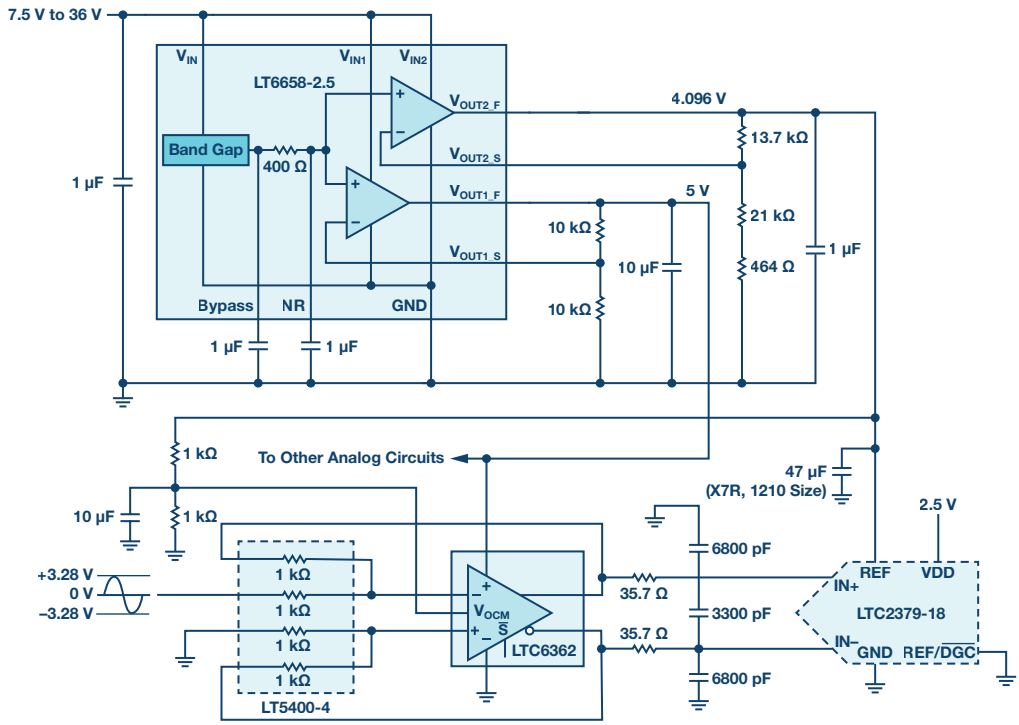

Figure 13. An 18-bit data acquisition application.

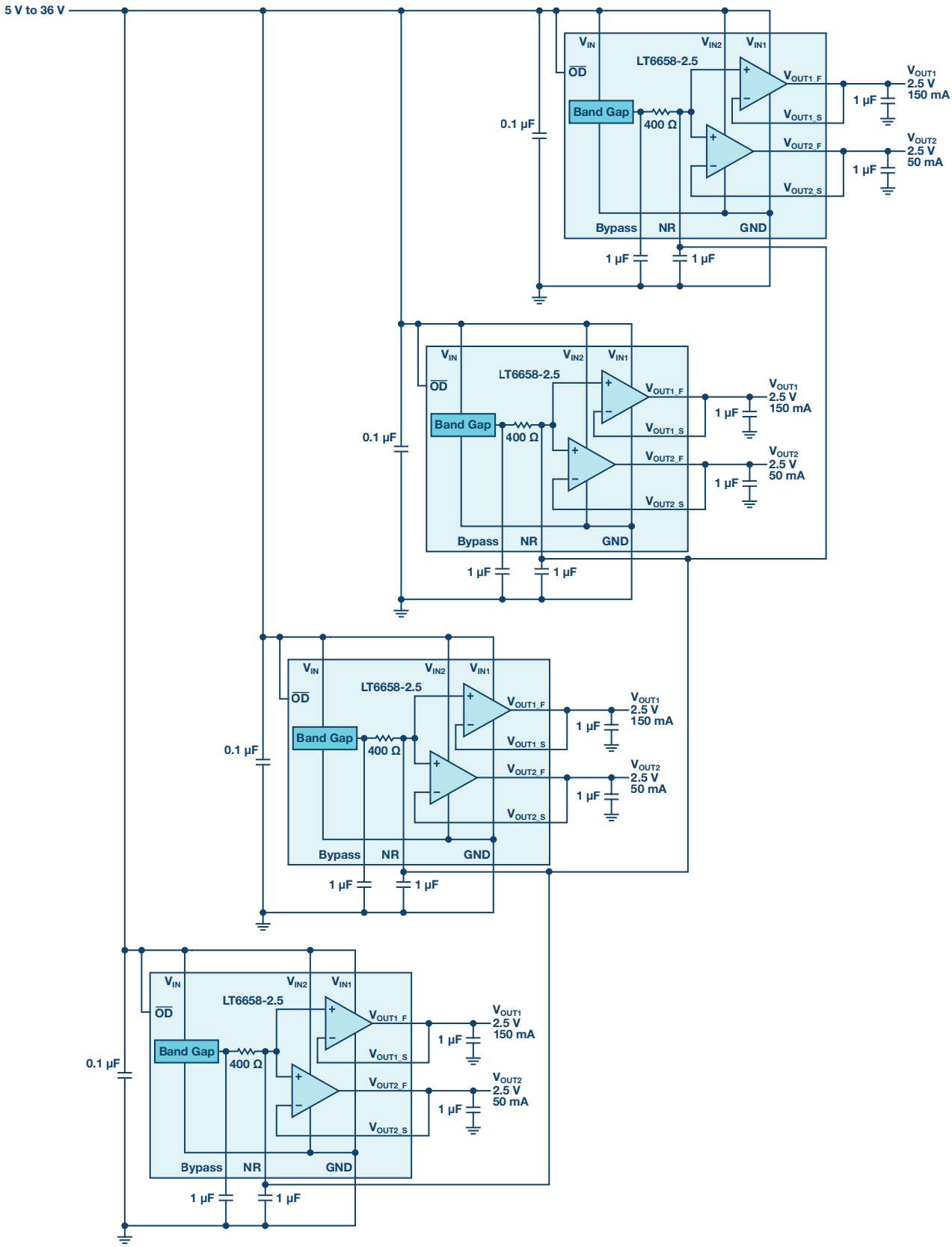

Figure 14. Paralleled NR pins for multichannel supplies with output tracking.

Figure 11 shows an application with two LTC2641 precision, 16-bit DACs. Since the reference current of the LTC2641 is code dependent, the two DAC reference inputs require a separate reference. The exception tracking of LT6658 output buffers translates into exceptional tracking of the DACs.

If only one DAC is required, the second output of the LT6658 can supply the input voltage to the DAC and other precision analog circuitry.

The LTC2323-16 is a dual, 16-bit ADC with separate reference inputs. This allows for a different reference voltage for each ADC. Figure 12 shows one arrangement where 2.5 V and 5 V reference voltages drive the separate reference inputs. Again, the LT6658 output buffers track well maintaining conversion results that also track.

Precision signal processing and conditioning can involve multiple integrated circuits. Figure 13 is an example where the LT6658 functions as a supply voltage and reference voltage for an 18-bit converter. A capacitive SAR converter is constantly charging and discharging an array of internal capacitors. The dynamic reference current of a SAR converter can wreak havoc on a voltage reference. The LT6658 can maintain stability by providing a precise voltage, while the second output can supply precision power. Moreover, the LT6658 has the current driving ability to supply voltage to multiple reference inputs. Another way to put this is the LT6658 has a large reference fan out ability.

The buffers in the preceding applications provided a reference voltage to precision circuits. A valid concern is whether activity on the output of one buffer will affect the output of the other buffer. Supply rejection is >100 dB at dc continuing beyond 1 kHz when there is a 10 µF capacitor on the NR pin. This is when the V_{IN1} and V_{IN2} pins are connected together. See the LT6658 data sheet for details on ac PSRR. The channel-to-channel isolation supply to output is >130 dB at dc to 100 Hz.

Multichannel Output Supply with Tracking

The NR pins of several LT6658s can be tied together creating a multichannel precision supply with tracking. In the example shown in Figure 14, four LT6658s have their NR pins tied together. The resulting supply has eight tracking outputs. That is, since all the NR pins are tied together, the output buffers in each of four LT6658s will track over temperature. Figure 15a shows how the precision trimmed outputs track over a wide temperature range. The seven traces in this plot are referred to the first V_{OUT1}. This demonstrates the low offset voltage and the low temperature drift of the output buffers.

By tying the NR pins together, the input voltage to the buffers are the same, and the C_{NR} capacitors will combine to a larger value reducing the noise bandwidth coming of the band gap circuits. The resulting noise density spectrum at the output buffer is shown in Figure 15b, where the noise is dominated by the output buffer and the band gap noise rolls at less than 10 Hz.

This example shows all the channels configured as unity gain. The output voltages can be configured for a variety of output voltage values. While these devices share the NR pin and supply voltage, they retain excellent PSRR, load isolation, and load regulation.

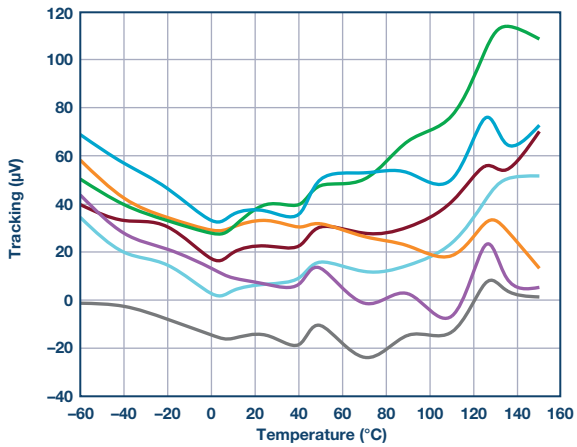

Figure 15a. Tracking.

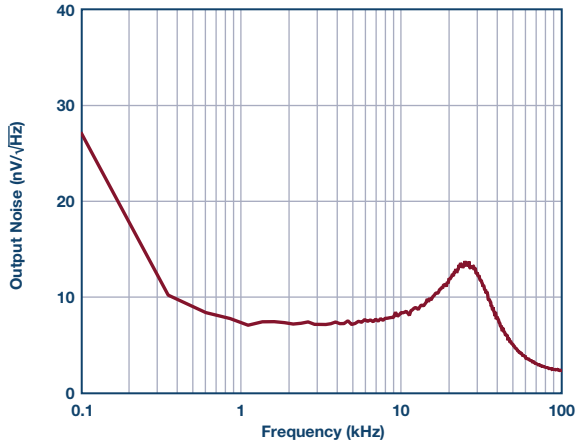

Figure 15b. Output voltage noise density.

High Current, Low Temperature Coefficient Circuit

Figure 16 illustrates how an LTC6655-2.5 low noise reference can overdrive the NR pin of the LT6658. The result is a dual output, low temperature coefficient (TC), high current reference. A variation of this circuit includes adding gain to one of the channels and driving the LTC6655's V_{IN} pin. The LTC6655-2.5 requires 500 mV headroom, necessitating a minimum 3 V output from one of the LT6658's buffers.

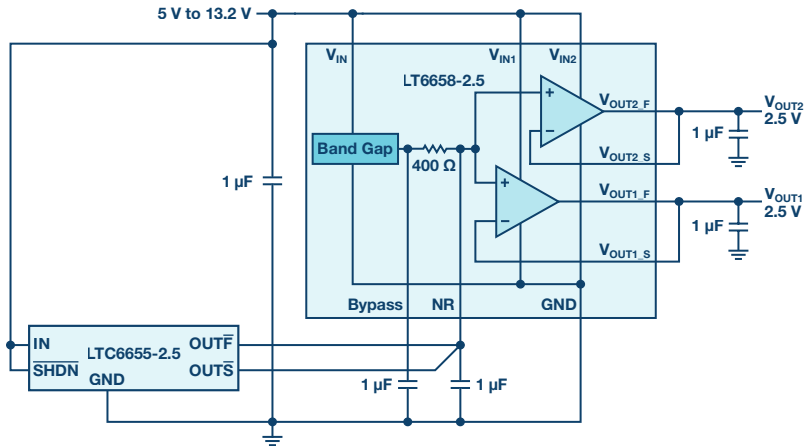

Figure 16. A low drift, high current application.

Power Applications

The buffer outputs can be combined to provide a single 200 mA output. The resistors allow the outputs to be connected together without wreaking havoc. The load regulation of the circuit in Figure 17 is limited by the value of the resistors and is 3 ppm/mA. This is in addition to the typical load regulation of the part at 0.25 µV/mA. The resistors can also be scaled to reduce the load regulation. And, since the resistance values are so low, power dissipation is not an issue.

The resistors can be constructed from a printed circuit board trace. One or two ounce copper can be used, or a combination of 0.01 Ω resistors can be arranged. This circuit will also sink current with the same ratios it sources current.

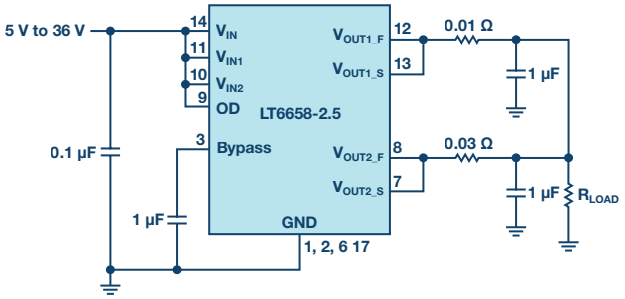

Figure 17. Parallel outputs for 200 mA output.

The two outputs will try to compensate each other requiring some resistance between them. There can be up to ±70 µV difference between the two outputs. Using the shown values of 0.01 Ω and 0.03 Ω, there are up to a few milliamps of current flowing between the output buffers. As the resistor values increase this shared current decreases. However, large isolation resistors mean a larger load regulation error as shown in Table 1.

Table 1. Load Regulation as a Function of Output Resistors.

R1 (Ω)	R2 (Ω)	Load Regulation (ppm/mA)
0.01	0.03	3
0.02	0.06	6
0.03	0.09	9
0.04	0.12	12
0.05	0.15	15

For applications that require lots of precision current, the LT6658 can be combined with a few transistors and ballast resistors to create a precision low noise, 5 A fixed dc supply, as shown in Figure 18.

A variable supply can be derived from Figure 18 with a few modifications, as shown in Figure 19. A blog article discusses this design, which can be found here.

Supplying Power to a RF Circuit

The application in Figure 20 has the LT6658 providing power where one output is increased to 3 V and the other output is decreased to 1.4 V. This provides power to an I and Q signal amplifier/filter and modulator. The 3 V output supplies power to the filters and modulator, while the 1.4 V output sets the common mode. The LT6658's OD pin is used to toggle the circuit between transmit and standby.

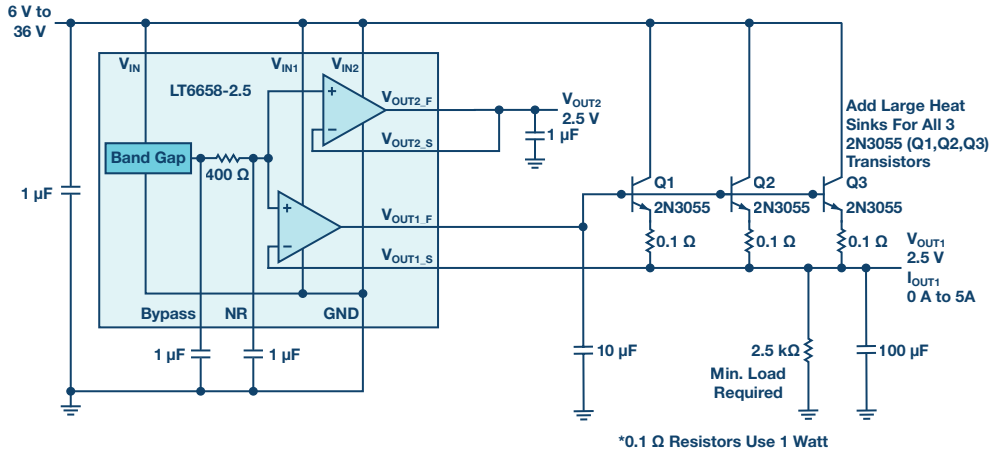

Figure 18. A precision, low noise fixed, 2. 5 V, 5 A supply circuit.

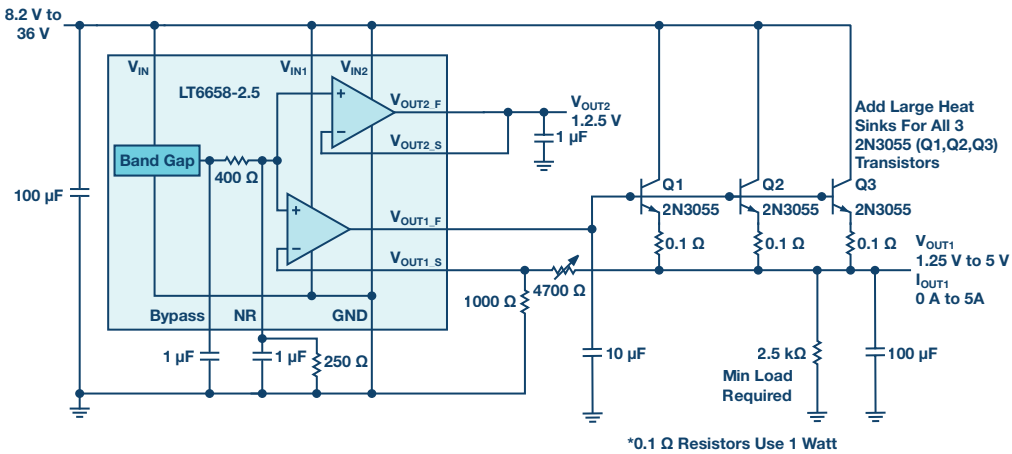

Figure 19. Precision, low noise variable, 1 V to 5 V, 5 A supply.

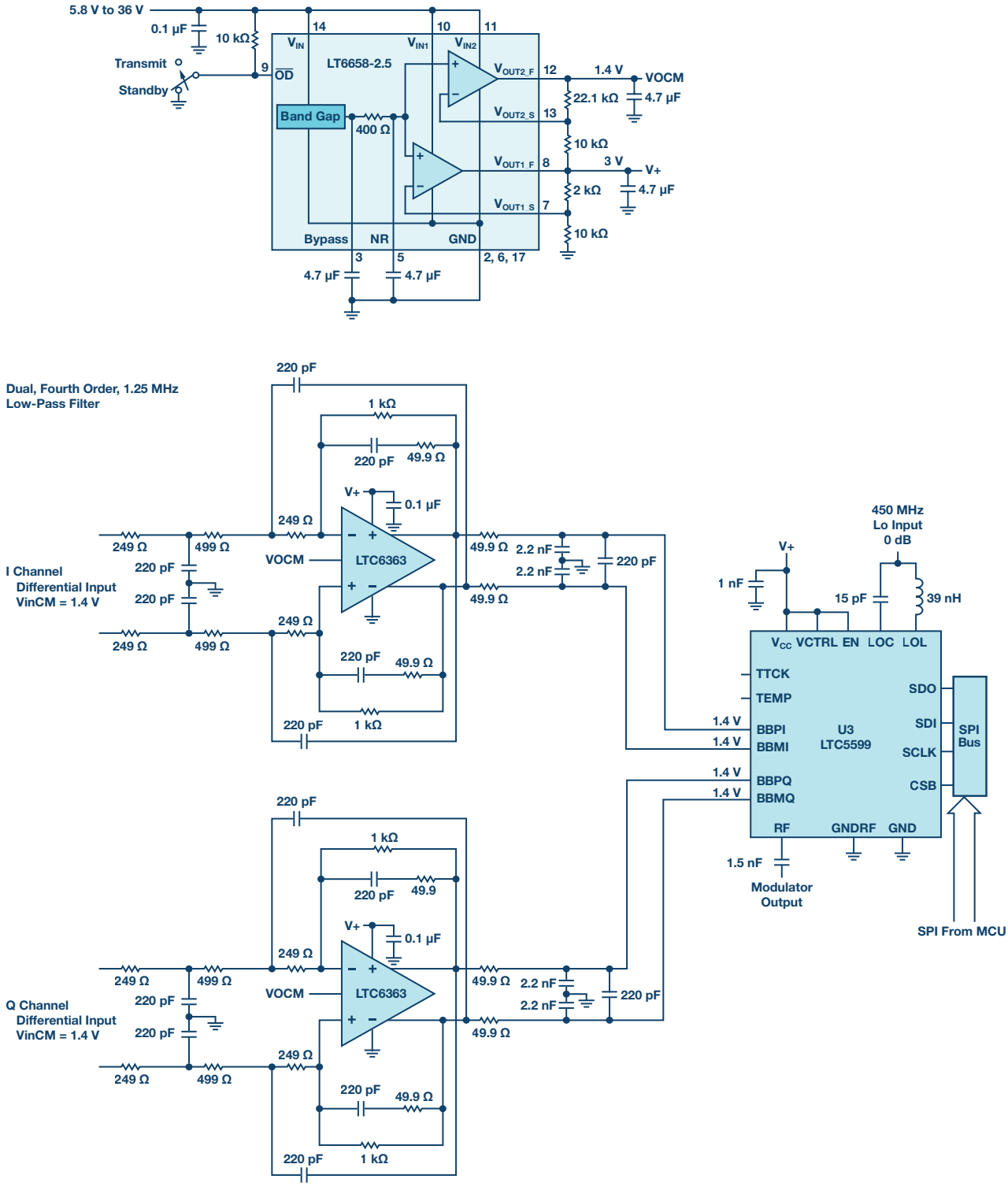

Figure 20. A low power, low noise I and Q signal amplifier/filter and modulator.

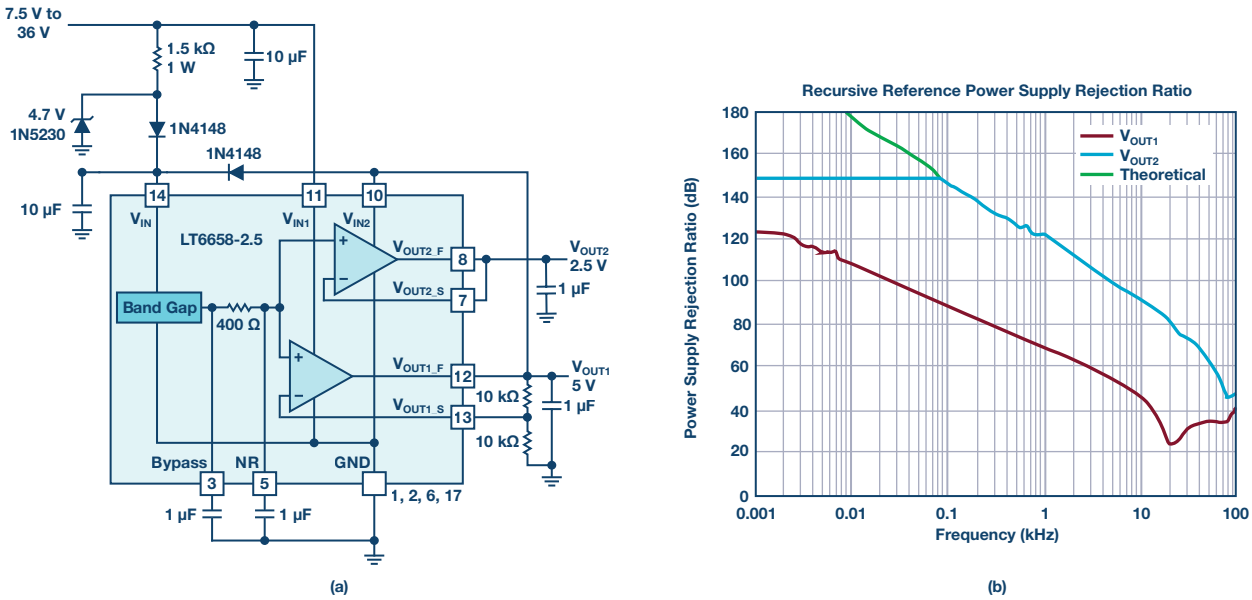

Figure 21. a) Extreme supply rejection circuit, b) AC power supply rejection ratio of the recursive reference.

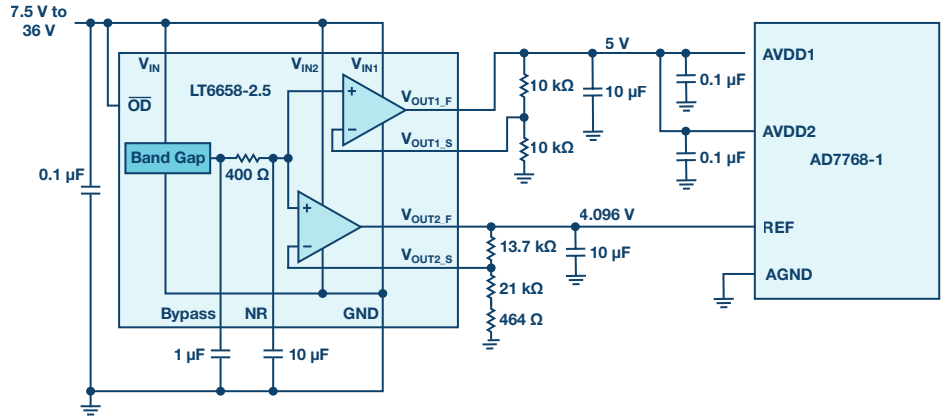

Figure 22. A 24-bit, simultaneously sampling Σ-Δ converter powered by the LT6658.

Recursive Reference

While the LT6658 has exceptional power supply rejection, Figure 21 takes power supply rejection to the next level. The recursive reference shown in Figure 21 creates an output on V_{OUT2} that is extremely isolated from the supply voltage. V_{IN1} and V_{IN} are driven by the external supply and creates a 5 V supply on V_{OUT1}. Once active, V_{OUT1} then takes over powering V_{IN} and subsequently, V_{IN2}, isolating those supply inputs from the external supply.

As the plot in Figure 21b shows, the measurable low frequency supply rejection is over 140 dB at the limit of our test setup. A theoretical trace is included that indicates the more likely supply rejection.

A 24-Bit, High Resolution ADC Application

The AD7768-1 is a precision, 24-bit Σ-Δ converter designed for wide bandwidth, high density instrumentation, energy, and healthcare equipment. The AD7768-1 is a demanding converter that requires a low noise, precise, and solid voltage reference to drive its reference input pin. For this application, one output of the LT6658 provides 5 V to the analog supply pins AVDD1 and AVDD2. The other output provides 4.096 V to the reference input.

The resulting FFT with a 1 kHz input tone and the fastest available sampling rate is shown below in Figure 23. To put this in perspective, the 4.096 V reference is divided down to an LSB size of 488 nV. Any noise, ripple, or feedthrough becomes readily apparent in the measurement results.

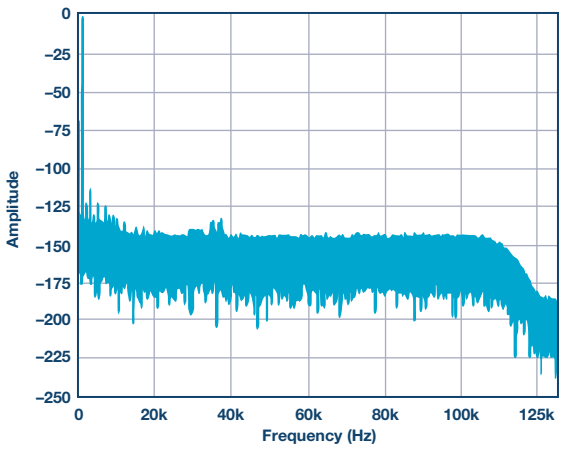

Figure 23. FFT of the AD7768-1 and LT6658 application.

Conclusion

The versatility and flexibility of the LT6658 is considered with a few applications. While the applications shown here use the 2.5 V variant, there are five other voltage options available, namely 1.2 V, 1.8 V, 3 V, 3.3 V, and 5 V. All six options share the same exacting specifications and rigorous testing Analog Devices is known for.

The LT6658 was conceived to satisfy customers who want more supply current from a voltage reference. Having two outputs seemed sensible and the aforementioned architecture emerged. As demonstrated in the preceding pages, this architecture can be exploited for various applications. Undoubtedly our customers will find many other innovative ways to apply the LT6658.

For more information on the capabilities of the LT6658 visit our website and look up the *Analog Dialogue* article "The Refulator: The Capabilities of a 200 mA Precision Voltage Reference."

Acknowledgements

The circuits in the article were contributed, built, and tested from a wide source of talented people here at ADI. I would like to thank Philip Karantzalis, Noe Quintero, Niall McGinley, Robert Keily, and Tom Westenberg. I'd also like to thank Aaron Schultz and Catherine Chang for their helpful feedback on the article. And thanks to Brendan Whelan for his comments and support.

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Michael Anderson

Also by this Author:

The Refulator: The Capabilities of a 200 mA Precision Voltage

Volume 52, Number 2

60 V and 100 V, Low I_Q Boost/SEPIC/Inverting Converters for Compact, Efficient, Low EMI Power Supplies

By **Joey Yurgelon**, **Jesus Rosales**, and **Mark Marosek**

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Automotive and industrial markets demand cool running power supplies that fit tight spaces and meet low EMI standards. The LT8362, LT8364, and LT8361 switching regulators meet these demands in boost, SEPIC, or inverting topologies. Each supports a wide, 2.8 V to 60 V input range for industrial or automotive environments, low I_Q Burst Mode® capability, and optional SSFM for reduced EMI. With built-in rugged power switches of 60 V/2 A, 60 V/4 A, and 100 V/2 A, including efficient operation up to 2 MHz, these devices can deliver high power in small spaces while meeting stringent thermal and EMI requirements.

Automotive Input Transients and Preboost

With the dramatic increase of electronic content in today's automobiles, the number of power supplies has multiplied with many required to directly convert a wide ranging battery voltage to a usable regulated output. With a minimum input voltage of 2.8 V, all members of the LT836x family can operate during cold crank or stop-start events; the maximum input voltage capability of up to 60 V handles high input voltage transients such as load dump.

This wide input voltage range makes the LT836x family ideal for automotive preboost applications. Automotive buck regulators require a preboost stage in applications where battery input voltage can drop below the buck output voltage. The LT8361, LT8362, and LT8364 provide the necessary boosting during low battery levels, and turn off with minimal power consumption during normal or load dump battery voltages.

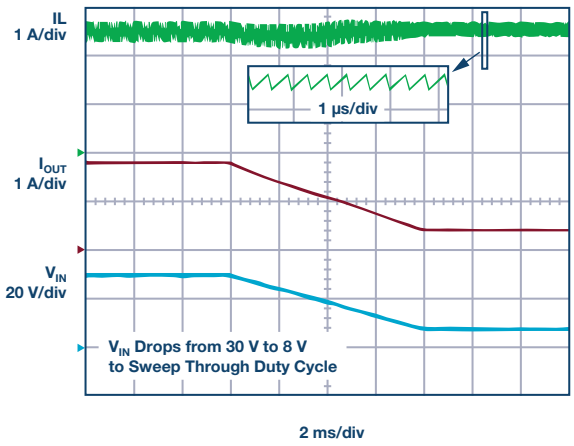


Figure 1. LT836x converters provide the full slope compensation necessary for proper operation at peak switch current limit, without the dc reduction of peak switch current limit vs. duty cycle.

Rugged Power Switches

A key requirement for any switching regulator is to provide enough power for a given application over the entire input voltage range while also guaranteeing reliability. Rugged power switches with voltage/peak current offerings of 60 V/2 A (LT8362), 60 V/4 A (LT8364), and 100 V/2 A (LT8361) enable a wide range of applications. The high power switch voltage ratings of the LT836x family extend output voltage capability in addition to extending the input voltage range for SEPICs and inverting converters.

Maximizing Power Delivery: Flat Current Limit vs. Duty Cycle

To maximize power delivery over the entire input voltage range, the power switches of the LT836x family maintain their peak switch current limit over the entire duty cycle range. The advertised current of the switch is available without compromise. This is a significant advantage over converters that may exhibit a fall of 30% or more in peak switch current limit at high duty cycles.

Current-mode dc-to-dc converters typically add slope compensation to their peak switch current limit to avoid subharmonic oscillations when that peak switch current limit is met. The drawback is a reduction of peak switch current limit as duty cycle increases (as input voltage lowers). The LT836x family provides the full slope compensation necessary for proper operation at peak switch current limit, without the dc reduction of peak switch current limit vs. duty cycle.

2 MHz Operation: Compact Power Supplies Above AM Band

To meet the demand for compact power supplies, dc-to-dc converters use high switching frequencies to minimize component size and cost. Furthermore, the requirements for operation above the AM band in automotive applications has driven frequencies to 2 MHz.

Traditionally, high switching frequencies result in increased switching losses and limited duty-cycle range. The LT836x family minimizes ac switching losses using fast power switch drivers and features low minimum on- and off-times, enabling support of a wide conversion range even at 2 MHz. For instance, the LT836x family can achieve lower losses and a higher duty-cycle range than many applications that would traditionally run at 400 kHz to maximize efficiency. Thermal performance for each of the covered topologies—inverting, boost, and SEPIC—is shown in Figure 2.

Burst Mode Operation: High Efficiency at Light Load

High efficiency at light loads is a critical feature in automotive environments where extending battery life is of utmost importance. The LT836x family offers high efficiency at light loads with optional Burst Mode operation—selectable using the SYNC/MODE pin (see Table 2). Burst Mode operation uses single-switch pulses spaced evenly at a lower switching frequency to reduce switching losses, while minimizing output voltage ripple. The LT836x family can draw as little as 9 µA from the input pin when in deep sleep or in pass through mode in a preboost application.

SSFM Mode: Three Topologies Passing CISPR 25 Class 5

The LT836x family is capable of meeting CISPR 25 Class 5 standards using spread spectrum frequency modulation (SSFM) mode and proper board layout with some filtering.

Designers have traditionally avoided using switching regulators throughout EMI sensitive environments. A switcher's large capacitors and troublesome hot loops elevate the importance of PCB layout to achieve good EMI performance and small solution size, placing a burden on board design and manufacture. The available factory demonstration circuits for the LT8362, LT8364, and LT8361 include the requisite input/output filters and feature exemplary PCB layout to meet CISPR 25 Class 5 standards (as tested) when SSFM mode is selected (see Table 2). By essentially removing the converter from the EMI equation, application development time and cost are reduced. Figure 4 shows EMI test results for a boost solution.

Best of Both: Burst Mode Operation and SSFM

Until recently, selecting SSFM mode for low EMI meant having to use the less efficient pulse-skipping mode at light load, but the LT836x family does not require this trade-off. By simply adding a 100 kΩ resistor from SYNC/MODE pin to ground (see Table 2), the LT836x family seamlessly transitions from SSFM mode to Burst Mode operation when loads become light. The result is low EMI and high efficiency over all loads.

Packages, Pin Compatibility, and Temperature Grades

For customers who prefer leaded packages, each part is offered in a pin compatible 16(12)-lead MSE TSSOP with four pins removed for HV pin spacing. For a smaller solution size, the LT8362 and LT8364 are also offered in DFN packages. The LT8362 (3 mm × 3 mm) 10-lead DFN is pin compatible with the LT8364 by placing it onto the (4 mm × 3 mm) LT8364 12-lead DFN PCB space (see Figure 6). All packages include a thermally enhanced exposed ground pad and are offered in E, I, and H temperature grades.

Boost/SEPIC/Inverting: FBX Pin for Positive or Negative Outputs

By offering a single FBX pin that allows for both positive and negative output voltages, all topologies are within reach. An inverting application is just as accessible as that of a boost or SEPIC, reducing design time and effort.

Boost Converters

For applications requiring output voltages greater than the input, the LT836x family is ideal for many boost converter applications given the 2.8 V to 60 V input capability and range of power switch ratings. For large conversion ratio designs, operating in discontinuous conduction mode (DCM) might be the best solution; continuous conduction mode (CCM) can deliver higher output power.

The converter in Figure 7 shows an LT8364 low I_Q, low EMI, 2 MHz, 24 V boost converter with SSFM that passes CISPR 25 Class 5 radiated and conducted EMI (Figure 4). With an input of 12 V, this application easily reaches a peak efficiency of 94%.

SEPIC Converters

Automotive and industrial applications often operate from input voltages that can be above and below the required output voltage. For applications where the dc-to-dc converter is required to both step-up and step-down its input, a SEPIC topology is often the solution. SEPICs support applications that require output disconnect, ensuring no output voltage during shutdown and tolerating output short-circuit faults since there is no dc path from input to output. With switch ratings of 60 V/100 V, and low minimum on- and off-times, wide input voltage ranges are achievable. The LT836x family offers an optional BIAS pin, which serves as a second input supply for the $INTV_{CC}$ regulator for improved efficiency.

The SEPIC converter in Figure 8 uses the LT8361 to showcase the versatility of a 100 V rated switch. The switch voltage rating must be greater than the addition of maximum input and output voltages. With a 48 V input to 24 V output, the switch can easily handle the required 72 V. With use cases where the input is greater than the output, the BIAS pin can offer improved efficiency when connected to V_{OUT}. Operating with SSFM, this application passes CISPR 25 Class 5 radiated and conducted EMI (Figure 9). Peak efficiency with a 12 V input is 88%.

Inverting Converters

Negative supplies are commonly used in today's electronics. However, many applications only have a positive input voltage from which to operate. The LT836x family, when configured in the inverting topology, can regulate from a positive input voltage that is above or below the magnitude of the negative output voltage. As with the SEPIC topology, the high 60 V/100 V switch ratings and low minimum on- and off-times allow wide input voltage ranges.

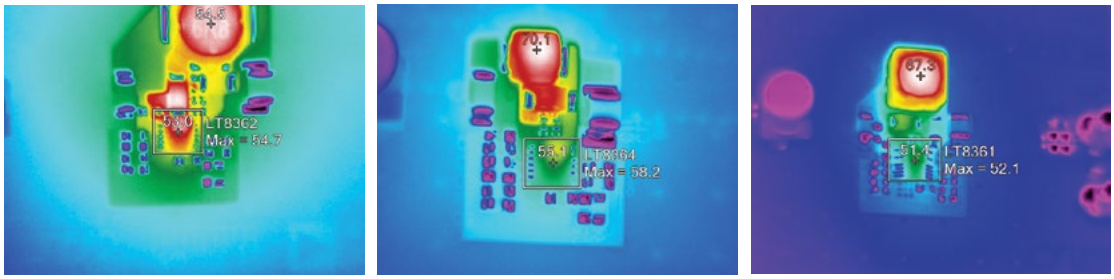
Operating at 2 MHz, the LT8362 offers an easy way to create a negative voltage from a positive input supply, as shown in Figure 10—a low I_Q, low EMI, 2 MHz, –12 V inverting converter with SSFM. With the rugged 60 V switch, this application can operate with inputs up to 42 V ($|V_{OUT}| + V_{IN}$ 60 V). With a V_{IN} of 12 V, a peak efficiency of 85% can be achieved. Operating with SSFM, this application passes CISPR 25 Class 5 radiated and conducted EMI (Figure 11).

Conclusion

To satisfy the automotive and industrial market demand for compact, efficient, low EMI power supplies, the LT836x family provides the rugged LT8362 (60 V/2 A), LT8364 (60 V/4 A), and LT8361 (100 V/2 A) switching regulators for boost, SEPIC, and inverting topologies. These devices are a significant improvement over alternatives due to low I_Q Burst Mode operation, flat switch current limit over duty cycle, low loss switching for 2 MHz operation, and a wide 2.8 V to 60 V input range.

Low EMI performance is achieved through proper demo board layout and filter design with SSFM mode to meet CISPR 25 Class 5 EMI standards.

Design development is simplified with 16(12)-lead MSE pin compatibility for all parts and footprint compatibility for LT8362 (3 mm × 3 mm, 10-lead DFN) and LT8364 (4 mm × 3 mm, 12-lead DFN. All members of the LT836x family are available in E, I, and H temperature grades.



(a) LT8362 DC2517A Inverting Converter. (b) LT8364 DC2716A Boost Converter. (c) LT8361 DC2599A SEPIC Converter.

Figure 2. Thermal performance of LT8362 Cuk inverting, LT8364 boost, and LT8361 SEPIC solutions.

(a) LT8362 low EMI Inverting Converter. (b) LT8364 Low EMI Boost Converter (c) LT8361 Low EMI SEPIC Converter.

Figure 3. Compact, EMI friendly converter solutions.

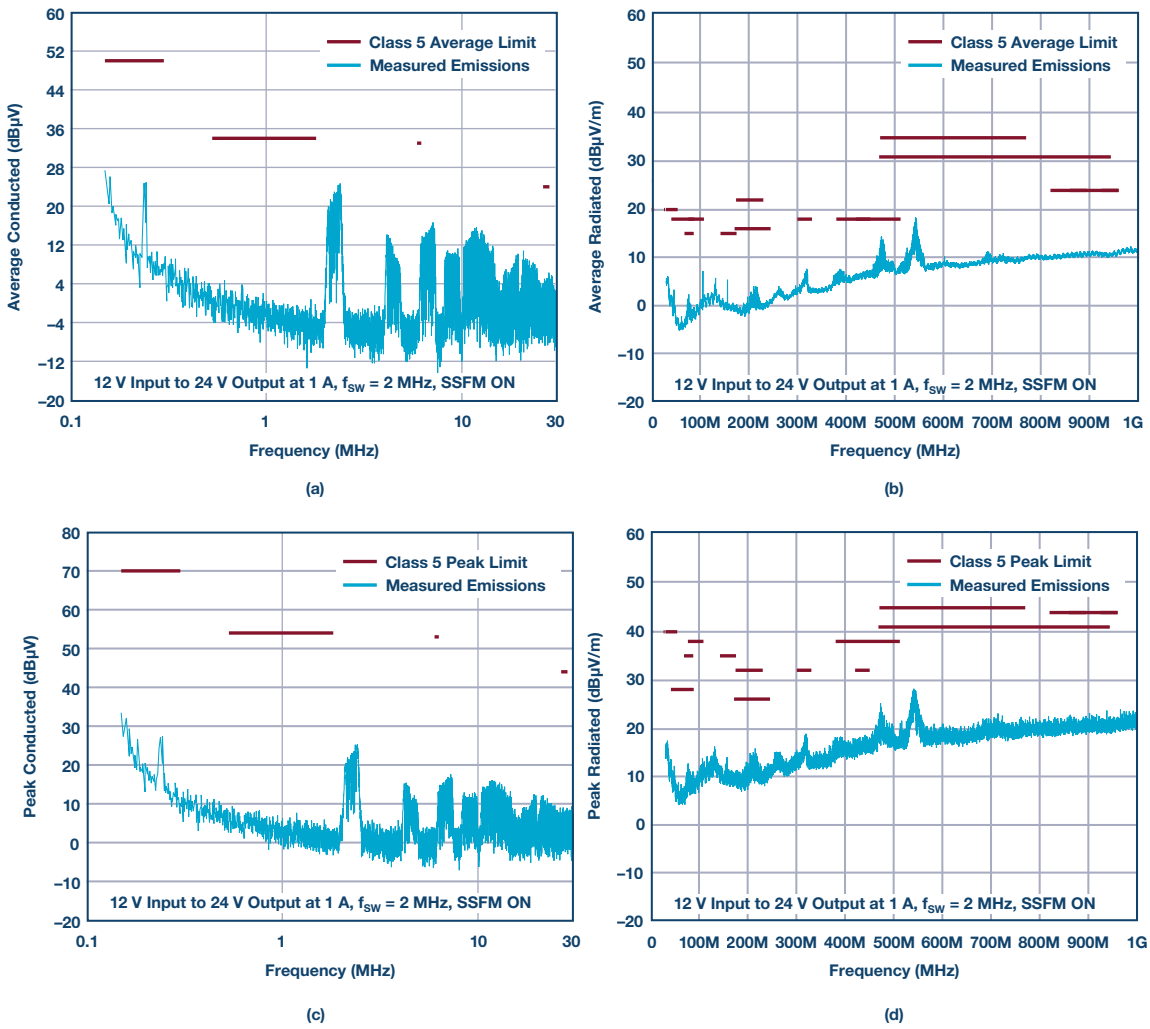


Figure 4. EMI test results for LT8364 boost solution.

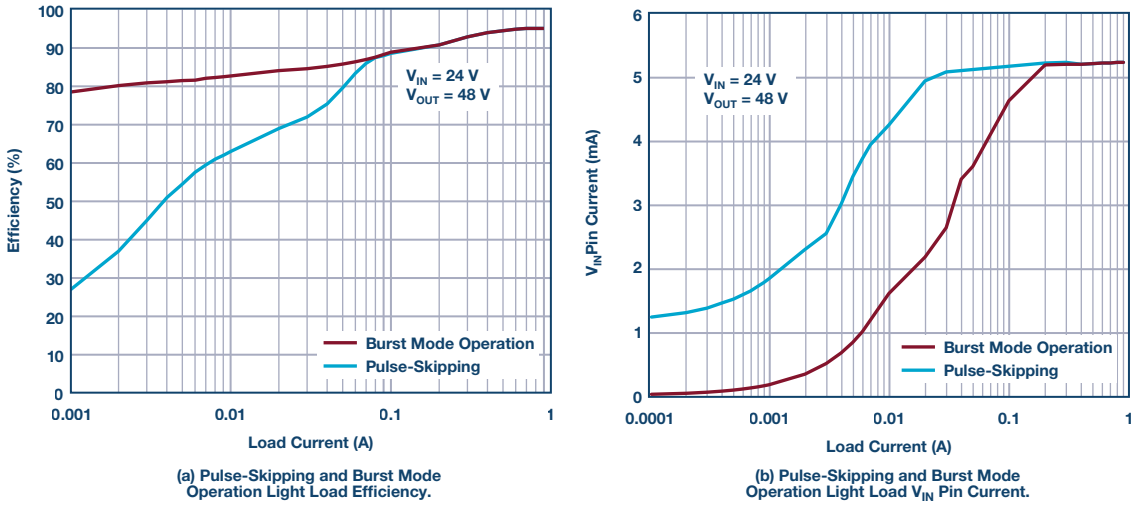


Figure 5. Pulse-skipping vs. Burst Mode operation for LT8362 boost solution (24 V input to 48 V output).

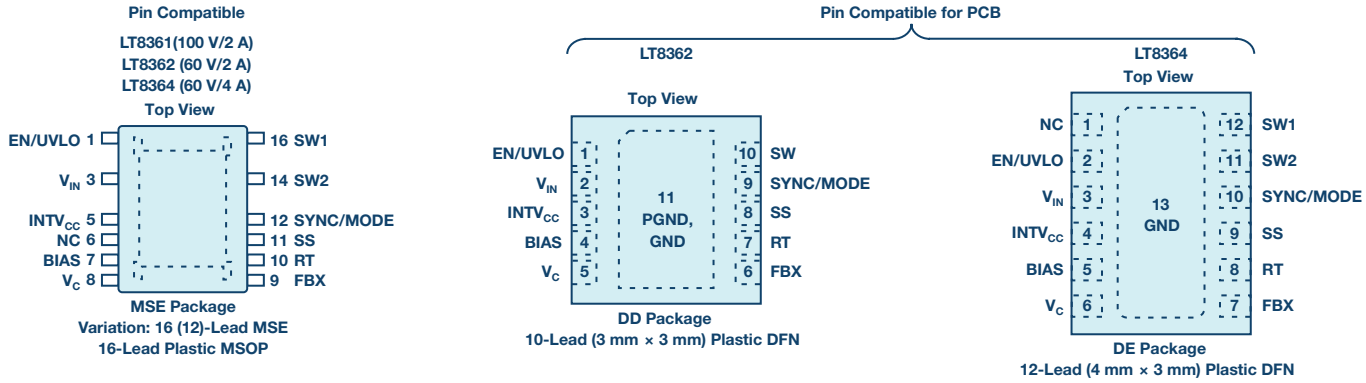


Figure 6. Pin compatibility of packages for the LT8361, LT8362, and LT8364.

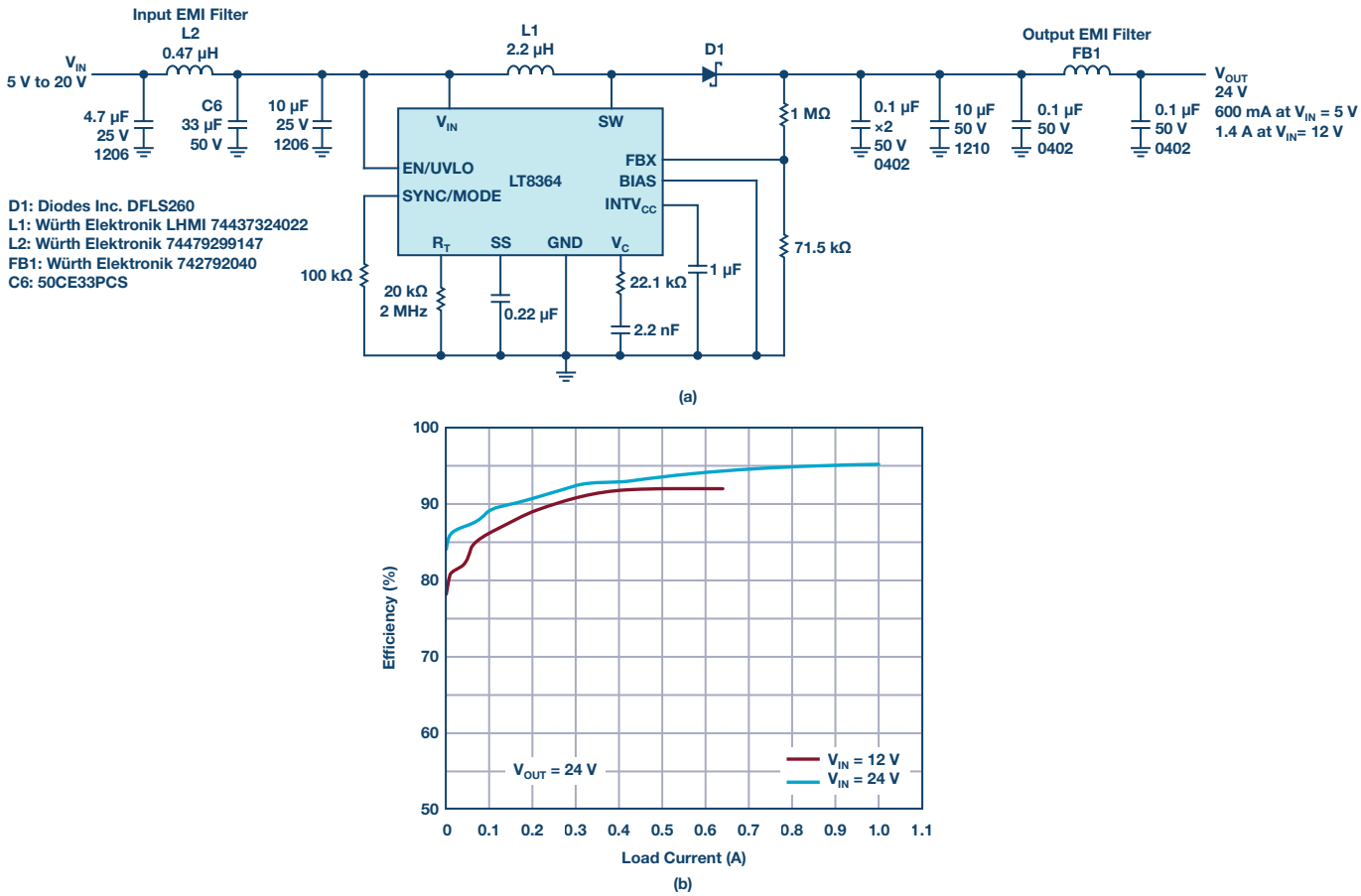


Figure 7. LT8364, 2 MHz, 24 V output boost converter passes CISPR 25 Class 5 EMI (see Figure 4).

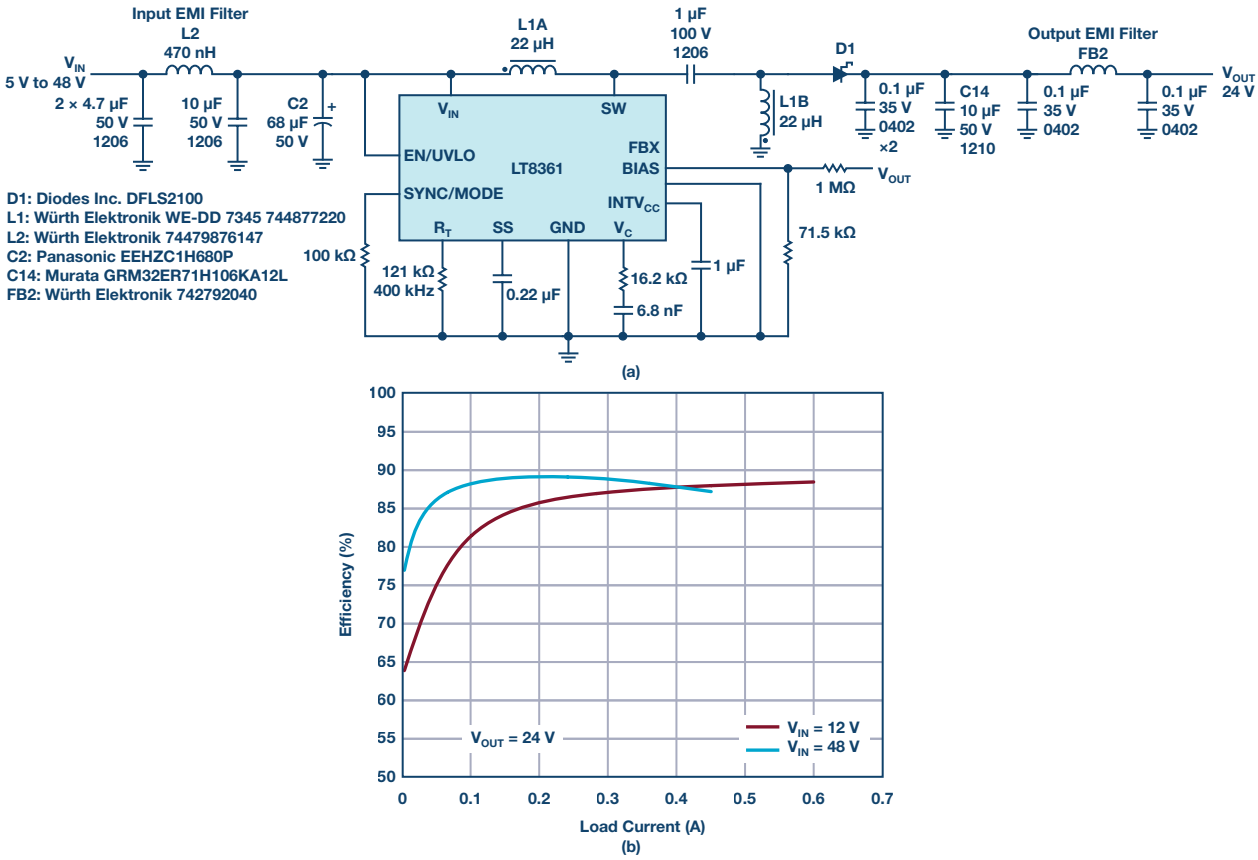


Figure 8. LT8361, 400 kHz, 24 V output SEPIC converter passes CISPR 25 Class 5 EMI.

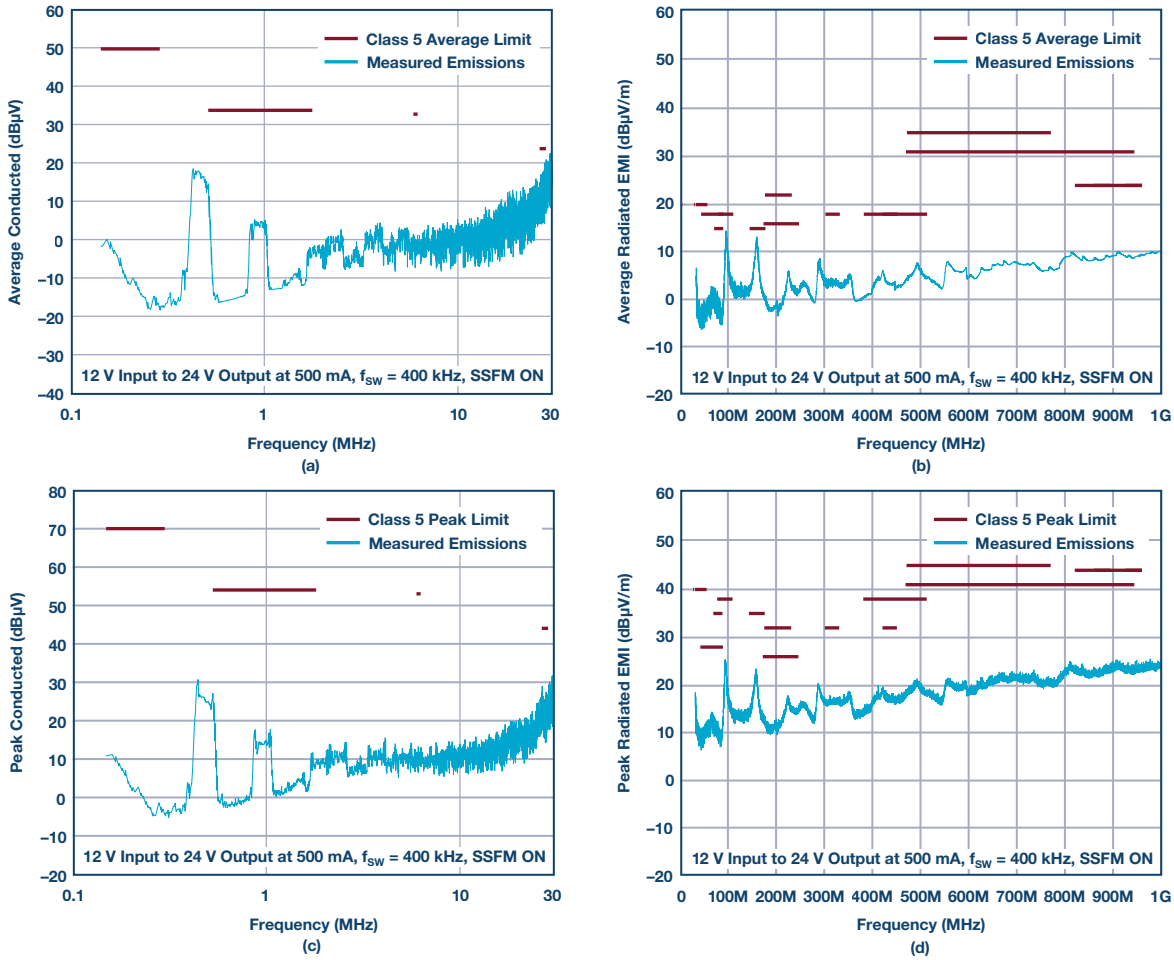


Figure 9. EMI test results for LT8361 SEPIC solution.

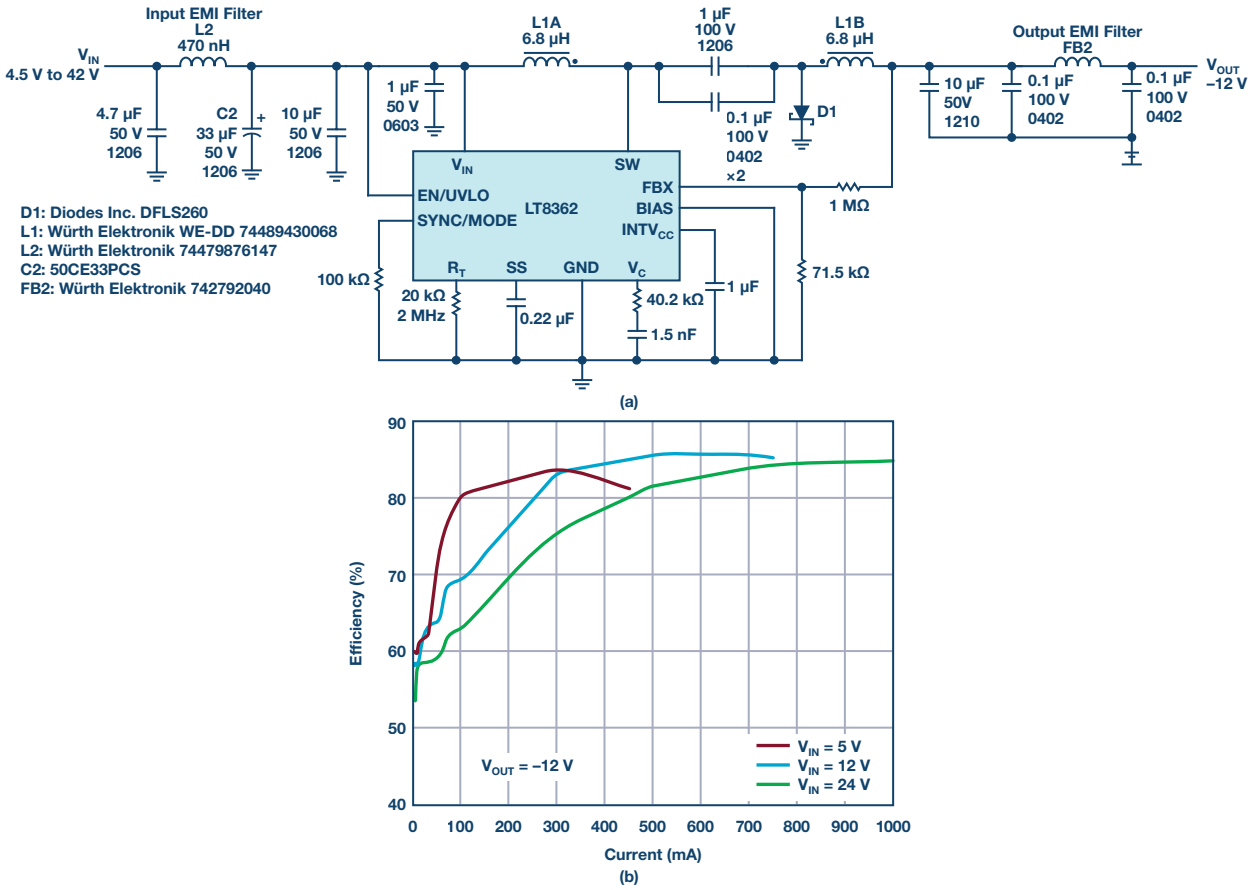


Figure 10. LT8362, 2 MHz, –12 V output, inverting converter passes CISPR 25 Class 5 EMI.

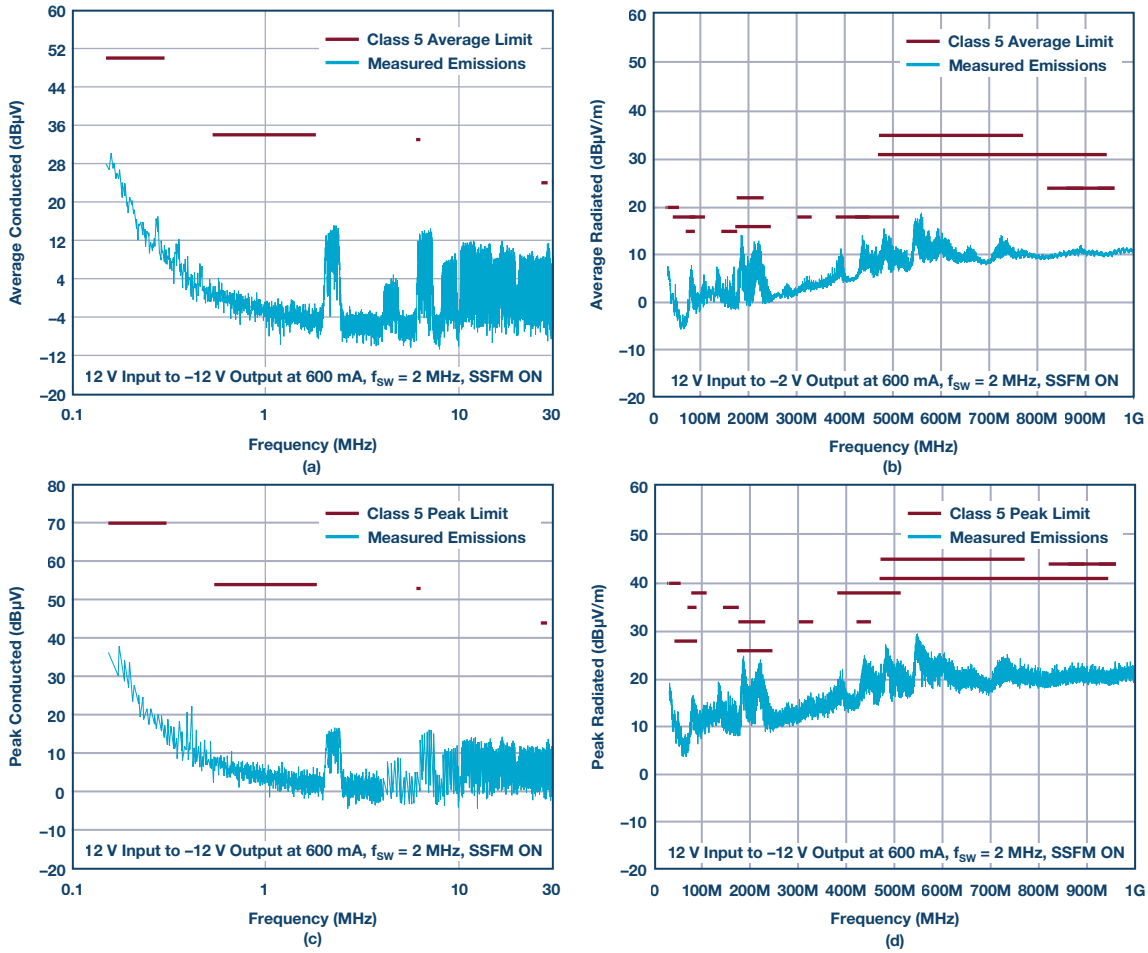


Figure 11. EMI test results for LT8362 inverting solution.

Table 1. Low I_Q Boost/SEPIC/Inverting Converters; Devices Described in this Article Are Highlighted.

	LT8362	LT8364	LT8361	LT8330	LT8331	LT8335
Bust Mode I_Q (µA)	9	9	9	6	6	6
Input Voltage Range (V)	2.8 to 60	2.8 to 60	2.8 to 60	3 to 40	4.5 to 100	3 to 25
Programmable, Fixed, Switching Frequency	300 kHz to 2 MHz	300 kHz to 2 MHz	300 kHz to 2 MHz	2 MHz	100 kHz to 500 kHz	2 MHz
Spread Spectrum Frequency Modulation for Low EMI	Yes	Yes	Yes			
Power Switch Voltage/ Current	60 V/2 A	60 V/4 A	100 V/2 A	60 V/1 A	140 V/0.5 A	28 V/2 A
Package	3 mm × 3 mm DFN, 16(12)-lead MSE	4 mm × 3 mm DFN, 16(12)-lead MSE	16(12)-lead MSE	3 mm × 2 mm DFN, TSOT- 23	16(12)-lead MSE	3 mm × 2 mm DFN
Temperature Grades	E, I, H	E, I, H	E, I, H	E, I, H	E, I, H	E, I, H

Table 2. LT836x Family Capable Modes of Operation.

SYNC/MODE Pin Input	Capable Modes of Operation
(1) GND or <0.14 V	Burst Mode operation
(2) External clock	Pulse-skipping/sync
(3) 100 kΩ resistor to GND	Burst/SSFM
(4) Float (pin open)	Pulse-skipping
(5) $INTV_{CC}$ or > 1.7 V	Pulse-skipping/SSFM
Temperature Grades	E, I, H

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Rarely Asked Questions—Issue 156 Optimized Power Supply Measurement Setup

By **Frederik Dostal**

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Question:

How can I make sure I'm testing my switching regulator as efficiently as possible?

Answer:

Before a circuit designer decides on a particular power supply, he or she will first want to test it carefully. The data sheet for a switching regulator IC provides valuable information on how the complete power supply could behave in real life, as well as how its respective behavior is always obtained through the testing of a circuit in the lab. Circuit simulations, such as with LTspice®, are useful and can be helpful in circuit optimization. However, simulation does not take the place of hardware testing. With respect to this, parasitic effects are either difficult to estimate or hard to simulate.

Power supplies are thus thoroughly tested in the laboratory. Either a prototype developed in-house or, in most cases, an existing evaluation board from the manufacturer of the respective power supply IC is used for this.

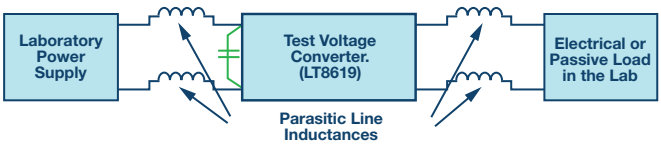

Figure 1. Connections for operation of a power supply.

When connecting the test circuit, a few points should be considered. Figure 1 shows a schematic of the test setup. The design under test must be connected to a power supply on the input side and a load on the output side. This sounds trivial, but there are some important details that must be heeded.

Minimization of Line Inductances

Figure 1 shows a schematic of the setup for evaluation of a power converter. We want to test the behavior of the power circuit and not the effect of the connection lines between the test board and the lab power supply or the load at the output. Two important measures should be taken to reduce the effects of these connection lines. For one, the connection lines should be kept as short as possible. Short lines have lower line inductance values than long lines do. Second, minimization of the current path area further reduces the parasitic inductance. An obvious way to accomplish this is to twist the lines. This results in the current path area only being dependent on the line length and the thickness of the stranded wire sheath. Figure 2 shows the connection of a test voltage converter with twisted connection lines for reduced parasitic line inductances.

Figure 2. Practical operational setup with short twisted cables.

In power supplies based on switching regulators, ac is found both on the input side and on the output side. Depending on the circuit topology, a pulsed current can occur at the input side, for example, in step-down converters (buck controllers). The start-up behavior and operation under load transients must also be tested. Under these operating conditions, the connection lines in the test setup also carry ac.

Addition of a Local Energy Storage Device on the Input

If a power supply is tested with respect to how quickly it can respond to load transients, sufficient energy must be available at the design under test. The energy source on the input side of the design under test should not be the limiting factor. To ensure that this is not the case, placement of a larger bulk capacitor at the voltage supply input is recommended. This is shown in green in Figure 1. It ensures that load transient tests can be performed properly.

However, it must be ensured that the later use of the power supply is subject to very specific conditions. The effect of the energy storage device at the input must be well understood so that the input capacitor for the power supply can be dimensioned correctly.

Another aspect of the bulk capacitor in Figure 1 must also be considered. If voltage transients need to be applied at the input of the power supply to test the resulting behavior, the bulk capacitor would considerably slow down the voltage transients seen by the circuit under test. Thus, for these tests, the capacitor should be removed.

In conclusion there are quite a few things that must be considered in apparently simple tasks related to the design of the voltage supply—for example, connecting a circuit to the laboratory bench. Power lines to the circuit under test, as well as power lines away from the circuit under test, need to be treated as ac circuits and, thus, these cables need to be short and twisted to reduce parasitic inductance in these connecting cables. It is not more effort for the circuit designer to do so and the test results come close to what we actually intend to test. If influences from the test setup are reduced, the rest results will have more value. Over time, experienced power supply engineers have developed methods that optimize the evaluation of circuits. If all the tips in this article are followed, evaluation can be performed smoothly.

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Also by this Author:

Power Management for FPGAs

Volume 52, Number 1

Introduction to SPI Interface

By **Piyu Dhaker**

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Serial peripheral interface (SPI) is one of the most widely used interfaces between microcontroller and peripheral ICs such as sensors, ADCs, DACs, shift registers, SRAM, and others. This article provides a brief description of the SPI interface followed by an introduction to Analog Devices' SPI enabled switches and muxes, and how they help reduce the number of digital GPIOs in system board design.

SPI is a synchronous, full duplex master-slave-based interface. The data from the master or the slave is synchronized on the rising or falling clock edge. Both master and slave can transmit data at the same time. The SPI interface can be either 3-wire or 4-wire. This article focuses on the popular 4-wire SPI interface.

Interface

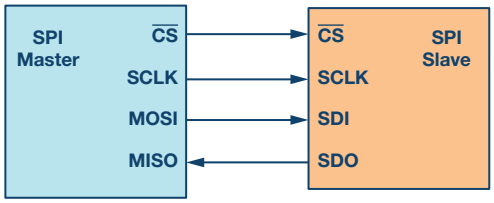

Figure 1. SPI configuration with master and a slave.

4-wire SPI devices have four signals:

- Clock (SPI CLK, SCLK)
- Chip select (CS)
- Master out, slave in (MOSI)
- Master in, slave out (MISO)

The device that generates the clock signal is called the master. Data transmitted between the master and the slave is synchronized to the clock generated by the master. SPI devices support much higher clock frequencies compared to I^2C interfaces. Users should consult the product data sheet for the clock frequency specification of the SPI interface.

SPI interfaces can have only one master and can have one or multiple slaves. Figure 1 shows the SPI connection between the master and the slave.

The chip select signal from the master is used to select the slave. This is normally an active low signal and is pulled high to disconnect the slave from the SPI bus. When multiple slaves are used, an individual chip select signal for each slave is required from the master. In this article, the chip select signal is always an active low signal.

MOSI and MISO are the data lines. MOSI transmits data from the master to the slave and MISO transmits data from the slave to the master.

Data Transmission

To begin SPI communication, the master must send the clock signal and select the slave by enabling the CS signal. Usually chip select is an active low signal; hence, the master must send a logic 0 on this signal to select the slave. SPI is a full-duplex interface; both master and slave can send data at the same time via the MOSI and MISO lines respectively. During SPI communication, the data is simultaneously transmitted (shifted out serially onto the MOSI/SDO bus) and received (the data on the bus (MISO/SDI) is sampled or read in). The serial clock edge synchronizes the shifting and sampling of the data. The SPI interface provides the user with flexibility to select the rising or falling edge of the clock to sample and/or shift the data. Please refer to the device data sheet to determine the number of data bits transmitted using the SPI interface.

Clock Polarity and Clock Phase

In SPI, the master can select the clock polarity and clock phase. The CPOL bit sets the polarity of the clock signal during the idle state. The idle state is defined as the period when CS is high and transitioning to low at the start of the transmission and when CS is low and transitioning to high at the end of the transmission. The CPHA bit selects the clock phase. Depending on the CPHA bit, the rising or falling clock edge is used to sample and/or shift the data. The master must select the clock polarity and clock phase, as per the requirement of the slave. Depending on the CPOL and CPHA bit selection, four SPI modes are available. Table 1 shows the four SPI modes.

Table 1. SPI Modes with CPOL and CPHA

SPI Mode	CPOL	CPHA	Clock Polarity in Idle State	Clock Phase Used to Sample and/or Shift the Data
0	0	0	Logic low	Data sampled on rising edge and shifted out on the falling edge
1	0	1	Logic low	Data sampled on the falling edge and shifted out on the rising edge
2	1	1	Logic high	Data sampled on the falling edge and shifted out on the rising edge
3	1	0	Logic high	Data sampled on the rising edge and shifted out on the falling edge

Figure 2 through Figure 5 show an example of communication in four SPI modes. In these examples, the data is shown on the MOSI and MISO line. The start and end of transmission is indicated by the dotted green line, the sampling edge is indicated in orange, and the shifting edge is indicated in blue. Please note these figures are for illustration purpose only. For successful SPI communications, users must refer to the product data sheet and ensure that the timing specifications for the part are met.

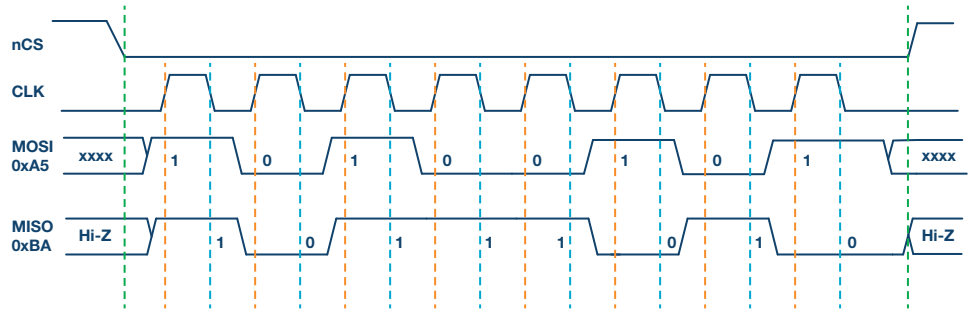

Figure 2. SPI Mode 0, CPOL = 0, CPHA = 0: CLK idle state = low, data sampled on rising edge and shifted on falling edge.

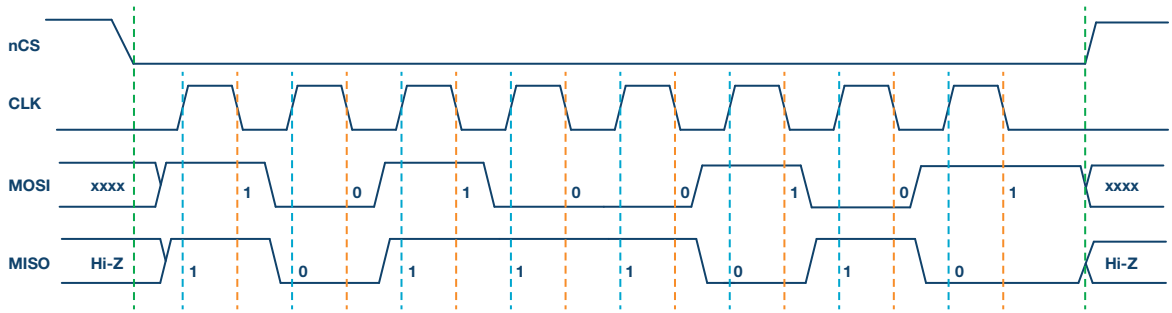

Figure 3. SPI Mode 1, CPOL = 0, CPHA = 1: CLK idle state = low, data sampled on the falling edge and shifted on the rising edge.

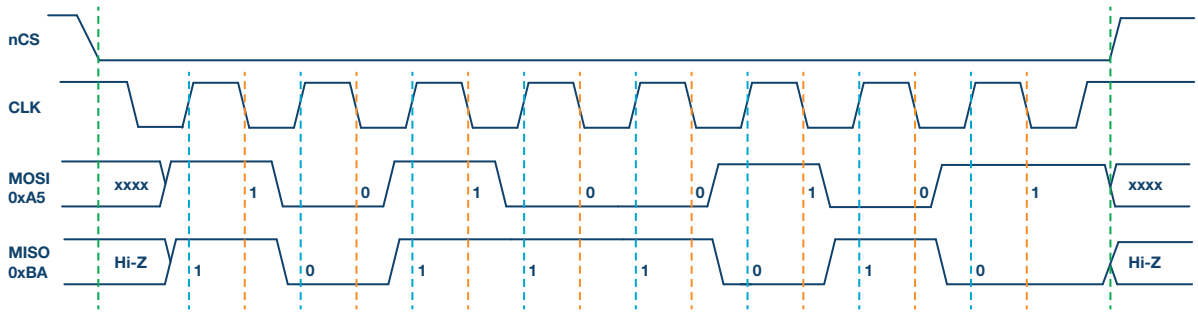

Figure 4. SPI Mode 2, CPOL = 1, CPHA = 1: CLK idle state = high, data sampled on the falling edge and shifted on the rising edge.

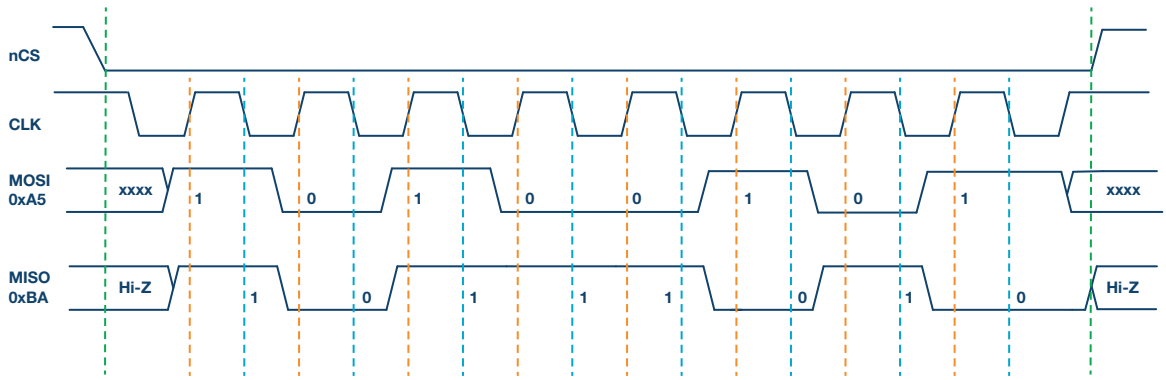

Figure 5. SPI Mode 3, CPOL = 1, CPHA = 0: CLK idle state = high, data sampled on the rising edge and shifted on the falling edge.

Figure 3 shows the timing diagram for SPI Mode 1. In this mode, clock polarity is 0, which indicates that the idle state of the clock signal is low. The clock phase in this mode is 1, which indicates that the data is sampled on the falling edge (shown by the orange dotted line) and the data is shifted on the rising edge (shown by the dotted blue line) of the clock signal.

Figure 4 shows the timing diagram for SPI Mode 2. In this mode, the clock polarity is 1, which indicates that the idle state of the clock signal is high. The clock phase in this mode is 1, which indicates that the data is sampled on the falling edge (shown by the orange dotted line) and the data is shifted on the rising edge (shown by the dotted blue line) of the clock signal.

Figure 5 shows the timing diagram for SPI Mode 3. In this mode, the clock polarity is 1, which indicates that the idle state of the clock signal is high. The clock phase in this mode is 0, which indicates that the data is sampled on the rising edge (shown by the orange dotted line) and the data is shifted on the falling edge (shown by the dotted blue line) of the clock signal.

Multislave Configuration

Multiple slaves can be used with a single SPI master. The slaves can be connected in regular mode or daisy-chain mode.

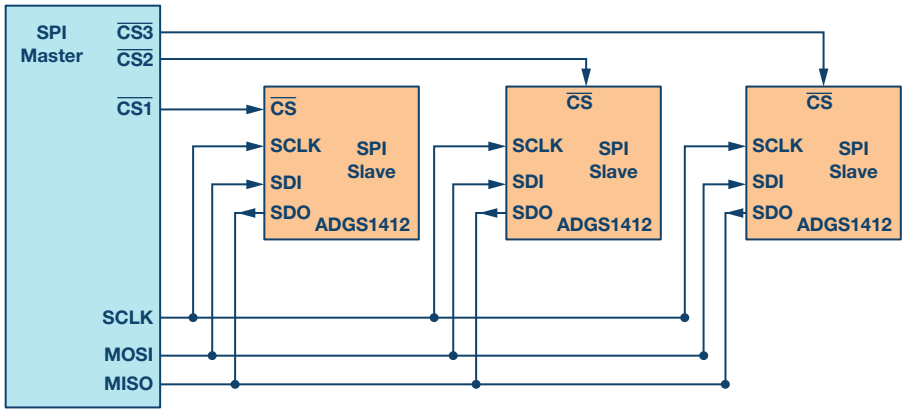

Figure 6. Multislave SPI configuration.

Regular SPI Mode:

In regular mode, an individual chip select for each slave is required from the master. Once the chip select signal is enabled (pulled low) by the master, the clock and data on the MOSI/MISO lines are available for the selected slave. If multiple chip select signals are enabled, the data on the MISO line is corrupted, as there is no way for the master to identify which slave is transmitting the data.

As can be seen from Figure 6, as the number of slaves increases, the number of chip select lines from the master increases. This can quickly add to the number of inputs and outputs needed from the master and limit the number of slaves that can be used. There are different techniques that can be used to increase the number of slaves in regular mode; for example, using a mux to generate a chip select signal.

Daisy-Chain Method:

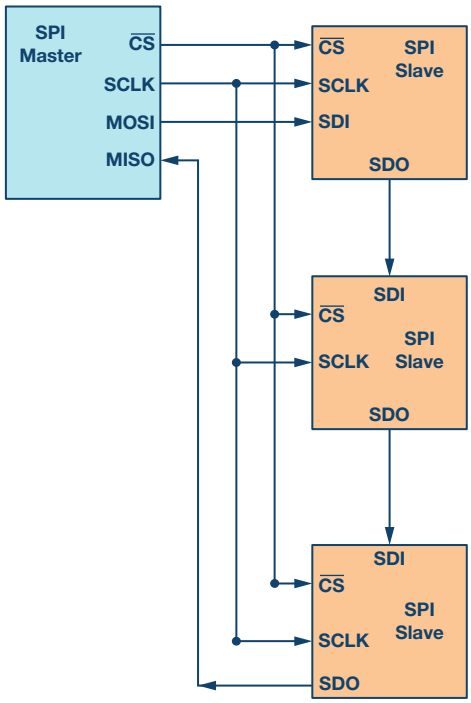

Figure 7. Multislave SPI daisy-chain configuration.

In daisy-chain mode, the slaves are configured such that the chip select signal for all slaves is tied together and data propagates from one slave to the next. In this configuration, all slaves receive the same SPI clock at the same time. The data from the master is directly connected to the first slave and that slave provides data to the next slave and so on.

In this method, as data is propagated from one slave to the next, the number of clock cycles required to transmit data is proportional to the slave position in the daisy chain. For example, in Figure 7, in an 8-bit system, 24 clock pulses are required for the data to be available on the 3rd slave, compared to only eight clock pulses in regular SPI mode. Figure 8 shows the clock cycles and data propagating through the daisy chain. Daisy-chain mode is not necessarily supported by all SPI devices. Please refer to the product data sheet to confirm if daisy chain is available.

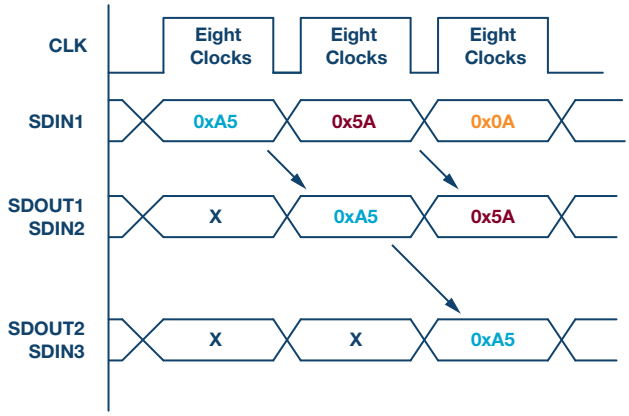

Figure 8. Daisy-chain configuration: data propagation.

Analog Devices SPI Enabled Switches and Muxes

The newest generation of ADI SPI enabled switches offer significant space saving without compromise to the precision switch performance. This section of the article discusses a case study of how SPI enabled switches or muxes can significantly simplify the system-level design and reduce the number of GPIOs required.

The ADG1412 is a quad, single-pole, single-throw (SPST) switch, which requires four GPIOs connected to the control input of each switch. Figure 9 shows the connection between the microcontroller and one ADG1412.

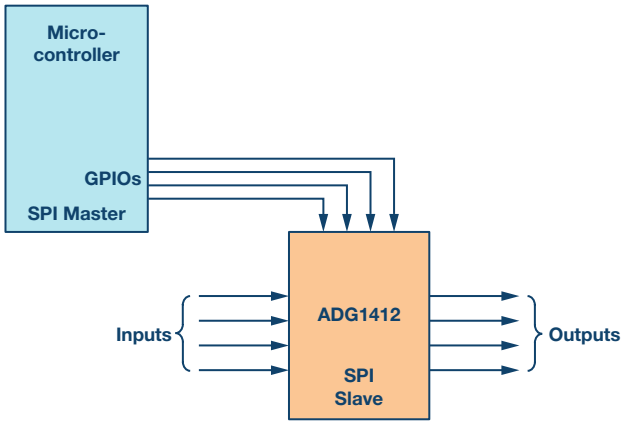

Figure 9. Microcontroller GPIO as control signals for the switch.

As the number of switches on the board increases, the number of required GPIOs increases significantly. For example, when designing a test instrumentation system and a large number of switches are used to increase the number of channels in the system. In a 4 × 4 cross-point matrix configuration, four ADG1412s are used. This system would require 16 GPIOs, limiting the available GPIOs in a standard microcontroller. Figure 10 shows the connection of four ADG1412s using the 16 GPIOs of the microcontroller.

One approach to reduce the number of GPIOs is to use a serial-to-parallel converter, as shown in Figure 11. This device outputs parallel signals that can be connected to the switch control inputs and the device can be configured by serial interface SPI. The drawback of this method is an increase in the bill of material by introducing an additional component.

An alternative method is to use SPI controlled switches. This method provides the benefit of reducing the number of GPIOs required and also eliminates the overhead of additional serial-to-parallel converter. As shown in Figure 12, instead of 16 microcontroller GPIOS, only seven microcontroller GPIOs are needed to provide the SPI signals to the four ADGS1412s.

The switches can be configured in daisy-chain configuration to further optimize the GPIO count. In daisy-chain configuration, irrespective of the number of switches used in the system, only four GPIOs are used from the master (microcontroller).

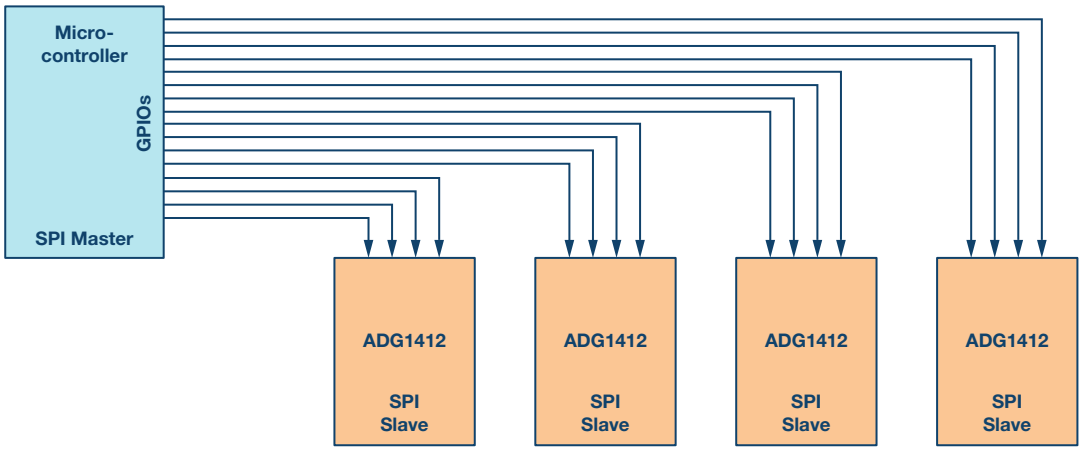

Figure 10. In a multislave configuration, the number of GPIOs needed increases tremendously.

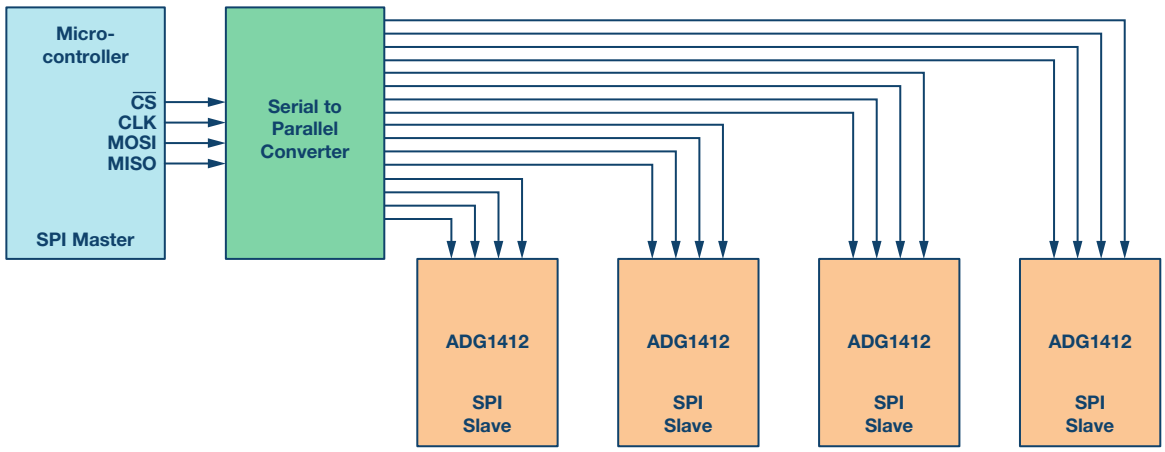

Figure 11. Multislave switches using a serial-to-parallel converter.

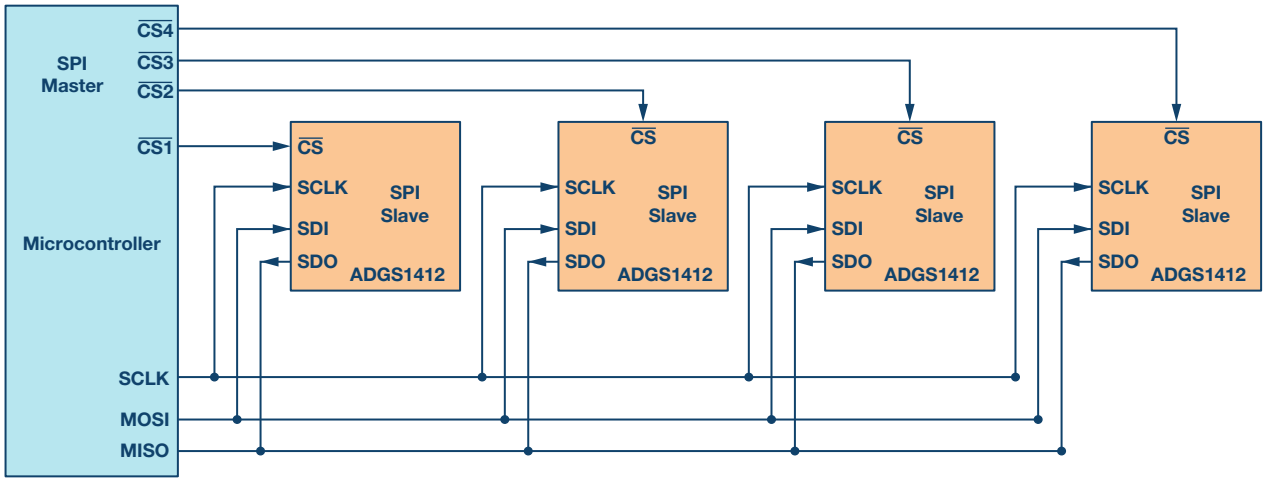

Figure 12. SPI enabled switches save up microcontroller GPIOs.

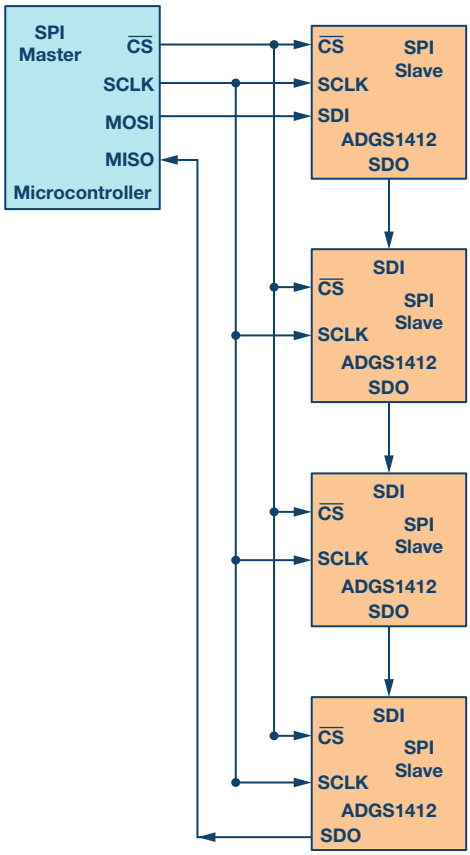

Figure 13. SPI enabled switches configured in a daisy chain to further optimize the GPIOs.

Figure 13 is for illustration purposes. The ADGS1412 data sheet recommends a pull-up resistor on the SDO pin. Please refer to the ADGS1412 data sheet for further details on daisy-chain mode. For the sake of simplicity, four switches have been used in this example. As the number of switches increase in a system, the benefits of board simplicity and space saving is significant. The ADI SPI enabled switches provide a 20% overall board space reduction in a 4 × 8 crosspoint configuration with eight quad SPST switches on a 6-layer board. The article "Precision SPI Switch Configuration Increases Channel Density" provides detail on how precision SPI switch configuration increases channel density.

Analog Devices offers several SPI enabled switches and multiplexers. For more information visit here.

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Piyu Dhaker

Antialiasing Filtering Considerations for High Precision SAR Analog-to-Digital Converters

By **Patrick Butler**

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Introduction

At a time when IoT, big data, and the cloud are all the rage in the trade press, it is worth it to cast an eye toward the technological advances that enable the digitization of our analog world. Feeding the cloud requires data it's already digitized? The analog-to-digital converter (ADC) is the device that straddles these worlds and is key in defining the quality and accuracy of big data. Advances in ADC design approaches continue to push boundaries that provide the precision digital representation of the world around us. Speeds and resolutions can be pushed in a way that burns through historical metrology benchmarks.

High performance precision ADC has been pervasive across many application areas. Process control, programmable controllers, electric motor control, and distribution of electrical energy are distinct examples. Adding the less everyday domains of instrumentation where testing, research, development, and qualification of all styles of technologies relies on high precision digital conversion. Several ADC architectures compete at present in terms of precision and, depending on their needs, the choices align with analog-to-digital conversion principles, such as successive approximation register (SAR) vs. Σ-Δ, which are respectively capable of resolutions of up to 24 bits and more for a few MSPS, and 32 bits at several hundred kSPS.

When faced with these levels of resolution and precision where the useful dynamics offered by these converters easily exceed the magical barrier of 100 dBFS (full scale), users face a real challenge in the design of analog conditioning circuitry for the signals to be digitized, as well as the associated antialiasing filters. Sampling rates and filtering techniques have evolved significantly over the past two decades and it is now possible to use a combination of analog and digital filters to achieve a better compromise between performance and complexity.

Figure 1 shows a typical example of this kind of partition for a data acquisition system. After conditioning the differential or nondifferential signals (amplification, scaling, adaptation and translation of levels, etc.), the latter is filtered before digitization to satisfy the Nyquist criterion. Depending on the oversampling rate of the ADC(s), additional digital filtering is used to comply with the specifications of the acquisition system.

Many of the aforementioned applications employ state-of-the-art, high resolution ADCs due to the increased demand for very wide input dynamics. With the increased dynamics, one can expect system performance improvements along with a resulting compaction of the analog conditioning chain and a reduction in congestion and energy consumption, or even material costs.

Oversampling and Its Benefits

Before the advent of very fast, high resolution analog-to-digital converters, the dynamics problem was solved at the conditioning chain level by using fast programmable gain amplifiers, even faster comparators, and/or the paralleling of several ADCs, topped off with suitable digital processing to enable digitization of strong signals and discriminate small amplitudes near the noise level. In these antiquated and now obsolete architectures, this translated into complex circuits that were difficult to develop and were limited in terms of linearity, bandwidth, and sampling frequency. Today's alternative is to apply oversampling techniques by exploiting the high sampling rates offered by modern and more economical ADCs. The action of sampling a signal at an F_{SE} rate higher than the minimum imposed by the Nyquist theorem enables performing a gain operation through processing and increasing the signal-to-noise-noise ratio of an encoder, and consequently increasing the number of effective bits. Indeed, the quantization noise and thermal noise are assimilated into a white noise that spreads uniformly over the entire Nyquist band and beyond. After oversampling, restricting the useful band by filtering and operating strictly at the minimum required sample rate, or 2 × BW, permits a reduction of noise energy by 3 dB for each octave of band reduction, as indicated in Figure 2. In other words, an oversampling factor of 4 ideally provides a theoretical increase in the signal-to-noise ratio of 6 dB; that is, one additional bit, as expressed by Equation 1:

$$\frac{S}{B} = 6.02 \times N + 1.76 + 10 \times log\left(\frac{F_{se}}{2 \times BW}\right) \quad (1)$$

In summary, oversampling has two advantages: namely, an improvement in the signal-to-noise ratio, and a relaxation of the demands placed on the antialiasing analog filter before the ADC.

Antialiasing Filter: The Partition Dilemma

Ideally, the filters associated with the ADCs, and particularly those tasked with the problem of aliasing the spectrum, must have an amplitude response with the flattest possible bandwidth compared to their precision, as well as an out-of-band attenuation adequate to their dynamics. The transition band should generally be as steep as possible. Thus, these antialiasing, low-pass filters must have characteristics that enable them

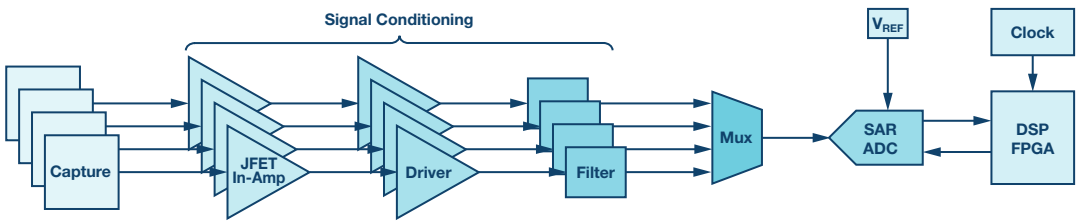

Figure 1. Typical measurement signal chain.

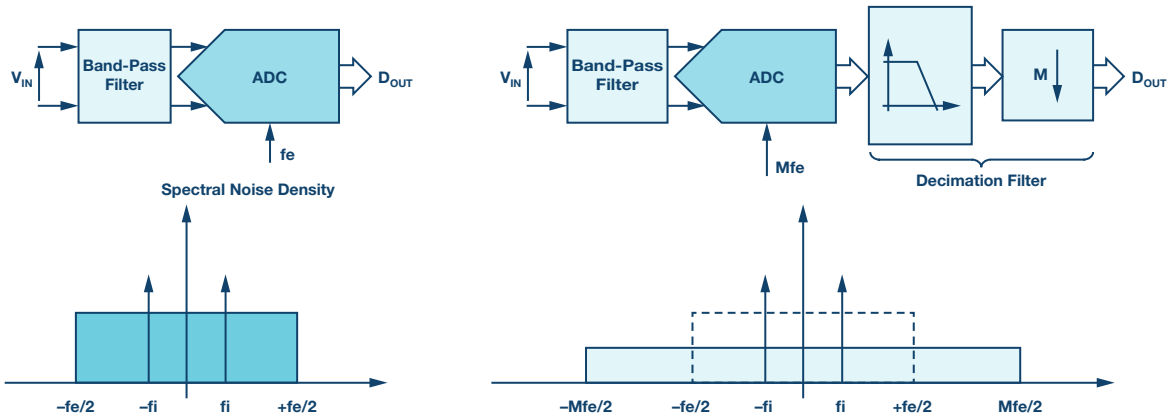

Figure 2. Comparison of the spectral noise density by adding a digital decimation filter.

to eliminate parasitic images, noise, and other spurious tones. Depending on the application, significant attention should also be given to the phase response, and any excessive phase shift should be compensated. Many recommendations are considered elementary, but become very difficult to implement when they must be combined with the requirements of a specified 24- or 32-bit converter with an integral nonlinearity error of only a few LSBs and other similar static and dynamic parameters.

The interest in oversampling, as stated earlier, assumes its full importance here due to its beneficial effects not only on the signal-to-noise ratio, but also on the accompanying relaxation of the specifications for the analog antialiasing filter and its cutoff frequency. As shown in Figure 3c, oversampling spreads the transition band between the cutoff frequency at –3 dB and the beginning of the stop band. The order of the analog antialiasing filter is inversely proportional to the oversampling ratio. Data in Table 1 illustrates the relationship between the oversampling ratio and the analog antialiasing filter order for a given rejection target.

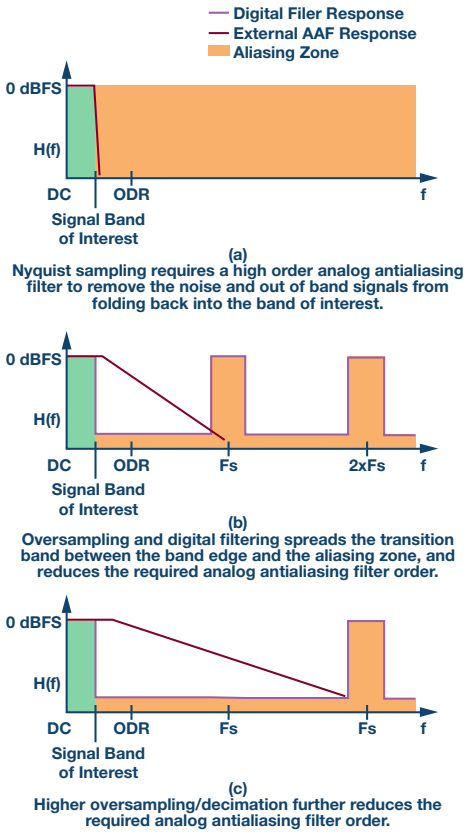

Figure 3. Oversampling, digital filtering, and decimation reduces the required analog antialiasing filter order.

The current technology provides for highly precise SAR ADC conversion rates that have increased considerably in recent years, and currently reach from over 1 MSPS up to 15 MSPS for 18-bit resolution. By comparison, the wideband Σ-Δ ADCs offer higher resolution at lower throughput rate with very high over sampling ratio. Looking at the Σ-Δ converters at equivalent (18-bit resolution) input bandwidth of hundreds of kHz is possible, but with the added functionality of digital filtering being built-in.

Σ-Δ ADCs with equivalent resolution can have a bandwidth in the hundreds of kHz range with the added benefit of a selection of digital filters built-in. These ADCs are fundamentally characterized by their overall metrological precision, which relates both to the static (dc) and dynamic (ac) parameters, and therefore the converters and the accompanying analog conditioning circuitry in these systems must have top tier specifications.

Conversely, most SAR ADCs do not include a digital filter except for the oversampling SARs such as LTC2512 and LTC2500-32, and their operation is therefore not impeded or limited by some unavoidable digital low-pass filtering that results in a compromise between computational accuracy, band-pass ripple, attenuated band rejection, propagation time, and power consumption. Meanwhile, some of the new wideband Σ-Δ ADCs such as the AD7768-1 are more flexible to allow a certain level of user programmability on its digital filter coefficients.

The LTC2378-20: First 20-Bit SAR ADC on the Market

In the race for performance, Linear Technology (now part of Analog Devices) provided the first SAR ADC with 20-bit resolution and nothing less than linearity. The LTC2378-20 is an exceptional converter that still holds its own against the best of all other competitors that are closing in on MSPS.

The AD4020, Analog Devices' first 20-bit SAR ADC, took a slightly different path. While combining low noise and low energy consumption, the AD4020 has sought to make the signal chain easier for the customer. Low noise and low energy at 1.8 MSPS are the traditional vectors. However, there are some key extras that help make it easier for hardware designers to achieve the necessary performance. The ability to quiet the analog front-end sampling is one example. The charging/discharging at the inputs as the converter transitions back to acquisition has always been a difficult problem. The typical knock on effect was that much higher speed driver amplifiers were required. With AD4020, high-Z mode, low power precision amplifiers that equate to the actual signal bandwidth of interest can now be employed, improving measurement precision. Limiting the conversion time to 350 ns allows for the extension of acquisition time, which also makes choosing the amplifier easier and, on the digital side, allows for slower serial data clocks to be used when reading data on the serial interface. In isolated applications, slower serial clocks reduce EMI effects and current consumption of the isolator. Holding the 10-lead MSOP or 10-lead QFN casing shared by the AD7980 family and the other 16- to 18-bit members of the AD40xx family means there is an easy upgrade of platform

design choice for the hardware designer. Powered at 1.8 V, it consumes only 15 mW at 1.8 MSPS. This low component power consumption coupled with features that reduce current consumption of the supporting blocks in the signal chain means that exceptional performance is achieved with the lowest possible thermal dissipation.

With sampling rates of 1 MSPS and 1.8 MSPS respectively, the LTC2378-20 and AD4020 offer significant possibilities for oversampling, particularly with respect to the audio band or beyond. To do this, a customized decimation filter must be implemented in an external FPGA or DSP. As mentioned earlier, the latter can be bypassed to reduce the latency to its minimum if necessary. With these primary sampling rate values and in considering the 0 kHz to 25 kHz band, the respective oversampling factors are approximately 16 or 32, and processing gains of 12 dB to 18 dB result along with a simplification of the antialiasing, low-pass filter with regard to conventional operation strictly according to Nyquist theorem.

ADC to DSP Link: Everything Is Serial

In recent years, the semiconductor industry and its coterie of designers have had an obvious penchant for a reduction in component sizes, leading to a real deflation of the casing pins and conditioning almost all the digital inputs or outputs in serial form, which are required to be interfaced with SPI buses, synchronous serial ports, etc. The converters in question here are not left with their serial interfaces used both to extract the samples and control the various functional options of the ADC. These serial interfaces are qualified to be compatible with SPI or with the DSP serial ports, but are not really so. At best, they hide the shift registers that set the rhythm of a clock signal for extracting data from the device, or to inject it during configuration. Like all of these SAR ADCs, the LTC2378-20 and AD4020 have frequency requirements for the serial clock (SCK) to recover 20 bits of data at the nominal sampling rate. As the phase of data reading is strictly limited to the duration of the acquisition time, which is of the order of some 300 ns, the digital activities on external access must be reduced to total silence during the conversion period, and a clock frequency of more than 60 MHz is necessary to recover all the bits from a sampling over the allotted time while respecting the sampling rate of 1 MSPS. This is a severe constraint imposed on the interface of the controller in charge of collecting the data from the ADCs, both for generating such clock frequencies, but also with respect to the time specifications to be achieved by the receiver side. The minimum SCK signal frequency of 64 MHz required by the LTC2378-20 means that it cannot be interfaced with just any general-purpose microcontroller or most DSPs with synchronous serial ports (SPORTs) that exceed the maximum frequency of barely 50 MHz, except for some members of the Blackfin® family, such as the ADSP-BF533 or ADSP-BF561 that can reach 90 Mbps. Therefore, there is concern that the use of a large CPLD or FPGA associated with low jitter clock generation circuitry is essential. Most of the digital interfaces for the serial output SAR ADCs share more or less the same timing and logic signal patterns as shown in Figure 4. As for the SDI configuration input, apart from the cascade modes, it is sought at much lower frequencies. The equivalent full cycle time for the ADC sampling period is

$$t_{cyc} = t_{conv} + t_{acq} \quad (2)$$

thus defining the maximum sampling frequency, consists of:

$$F_s = \frac{1}{t_{cyc}} \quad (3)$$

which itself is conditioned by the reading rate of the output data with

$$t_{acq} = \frac{1}{F_{sck}} \quad (4)$$

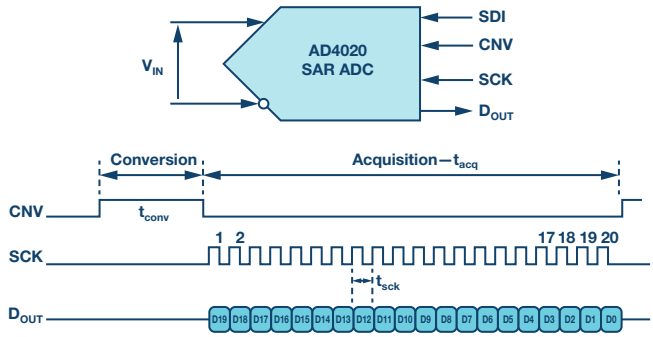

Figure 4. Timing diagram for the AD4020.

Fortunately, the AD4020, with its very short conversion time of 325 ns and a sampling rate of 1 MSPS, allows an acquisition time of 675 ns and consequently a serial data read frequency of less than 33 MHz; a frequency that matches that of the DSP synchronous serial ports, such as the SHARC® ADSP-21479; and very low energy consumption.

The LTC2512 and LTC2500-32 oversampling SARs reduce the serial data read frequency requirement by allowing the user to read out the contents of the filtered output register over multiple conversions. The wideband Σ-Δ ADCs further relax the serial interface clock timing by not requiring an interface quiet time during the ADC conversion.

An Ultra Low Power Multichannel Acquisition System

For reasons of energy consumption, precision, and flexibility in choice of operating modes, but also for commercial reasons, FPGA-based solutions cannot be considered in these areas. Only DSP floating-point processors are retained for the processing of the serial outputs from these 20-bit ADCs and for realizing optimized decimation filters.

Today, there are many data acquisition systems capable of simultaneous sampling over a large number of channels. This translates into many ADCs operating in parallel, while being governed by the same controller that also has the task of collecting the data and storing it in memory for subsequent analysis.

A system constructed around SAR ADCs associated with the capabilities of a SHARC ADSP-21479, or one of its fast ADSP-21469 or ADSP-21489 versions clocked at 450 MHz, is not only conceivable but presents itself as the most pertinent in terms of performance, development time, energy consumption, and compactness. These processors have all the functions and peripherals needed to support 8 analog-to-digital digitization channels, from synchronous serial interfaces to the generation of different clock signals and triggering conversion. Among all SHARC processors, the ADSP-21479 is the only 32-/40-bit floating-point DSP to be manufactured with a low leakage, 65 nm CMOS process, which has the advantage of substantially reducing leakage or static currents, and the evolution of the junction temperature is almost exponential. The dynamic current, which is a function of the frequency and activity of the processor and its peripherals, is also lower than that for standard or fast CMOS manufacturing processes. The flipside is a maximum CPU frequency reduced by about 30% to 40% compared to conventional versions, nevertheless largely sufficient for the needs of such an application.

The ADSP-21479 has many peripherals including a special block called a serial input port (SIP), that is capable of simultaneously receiving streams from eight external serial port transmitters in synchronous operation with clock and synchronization signals. In fact, it is possible to directly connect eight ADCs similar to the AD4020 directly to this interface, and thus to the processor. As shown in Figure 5, the 8 channels have their own IDP_SCK clock, IDP_FS synchronization, and IDP_DAT input signals, and their data, once deserialized, are automatically multiplexed into a 32-bit, 8-word FIFO memory before being transferred to the SHARC internal RAM, through either a 64-bit DMA packet or a read performed by the CPU. In

a DMA transfer operation, the SIP is served by a double-indexed DMA channel operating in automatic ping-pong mode. In addition, the ADSP-21479 features four precision clock generators (for their low jitter) or PCGs capable of generating independent pairs of clock and synchronization signals from an internal or external source (TCXO). The frequency, period, pulse width, and phase of these stimuli are obtained by programming 20-bit internal dividers. Each PCGx generation unit provides a pair of CLK/FS signals shared by a pair of AD4020 converters, but the clock must be silent during the conversion phase, which accounts for the presence of a logic gate that combines the IDP_FS and IDP_SCK signals to create the SCK clock. The time diagram in Figure 5 shows that once the conversion time t_{conv} has elapsed, the 20 bits from the current sample must be read as quickly as possible, that is, at the rate of 33.3 MHz to maintain the 1 MSPS magical barrier in the sampling frequency. About 600 ns later, the data is transferred to one of the SIP buffers and a new conversion cycle can be started using the IDP_FS or CNV signal to trigger a new conversion of the AD4020. Having a maximum 325 ns conversion time for the latter will correspond to the pulse width of the CNV signal, that is, 12 IDP_SCK clock periods or 360 ns. In summary, as shown in the timing diagram of Figure 5, 32 IDP_SCK signal periods, or a total of 960 ns, are required for a complete scan cycle, resulting in a maximum sampling rate of 1.040 MSPS.

Similarly, the ADC LTC2378-20 can be associated with an ADSP-21489 since it is capable of operating at the clocks of higher peripheral clock frequencies up to 50 MHz, and the sampling rate in this case will be 900 kSPS, as shown in Table 1. Unfortunately, the static supply current (I_{ddint}), or leakage of the latter, is much higher than the dynamic current, which makes an unacceptably high overall consumption for this configuration by exceeding the available wattage.

Decimation Filtering

Assuming that these converters are used in oversampling mode, it is necessary to provide a decimation filter tailored for the band of interest with the aforementioned performance requirements, minimizing the impact on the DSP in terms of required computing power and energy consumption. Currently, the procedure for changing the sampling rate has become a standard digital signal processing operation, and these are performed using interpolators and digital decimators. For reasons of linearity in the phase response, the low-pass decimation filter uses a finite impulse response (FIR) topology, and different topologies can be used according to the degree of efficiency sought:

- Direct or optimized FIR filters for decimation
- Cascaded multirate FIR filters (half band)
- Polyphase FIR filters

Polyphase filters, whether of the FIR or IIR type, are one of the most efficient implementations of decimation or interpolation filters. Nevertheless, digital processing orthodoxy requires filtering before decimation. On this assumption, a 1/M decimation filter consists of a low-pass filter followed by a sampling frequency reduction stage (Figure 6a). The signal is filtered beforehand to avoid the aliasing of spectrum, then the samples are periodically eliminated at the rate of M – 1. However, the direct implementation of these decimation filters of the conventional FIR or other structures is wasteful of resources knowing that the rejected samples result from a few tens or even hundreds of multiplication-accumulations (MACs). The use of polyphase filters decomposed into several banks of filters, or filters optimized for decimation, leads to the production of efficient filters based on certain identities such as that illustrated in Figure 6b.

With their SIMD architecture and hardware accelerator dedicated to FIR filtering, and an instruction set optimized for digital signal processing, the SHARC ADSP-21479 is particularly well positioned for implementing these types of filters. Each SHARC processing element has a 32-/40-bit multiplier-accumulator capable of providing 533 MACs per second in fixed or floating point at a CPU frequency of 266 MHz. However, for some applications with a significant delay (room equalization or sound effects), increased computing power is necessary to free up the core from intensive and sustained multiplication operations, such as FIR, IIR, or FFT filtering, tasks that are performed by dedicated hardware accelerators. Thus, the user will have complete freedom to utilize the CPU for the calculation of more complex algorithms that require the full sophistication of the instruction set. The accelerator dedicated to FIR filtering has its own local memory for storing data and coefficients, and has the following characteristics:

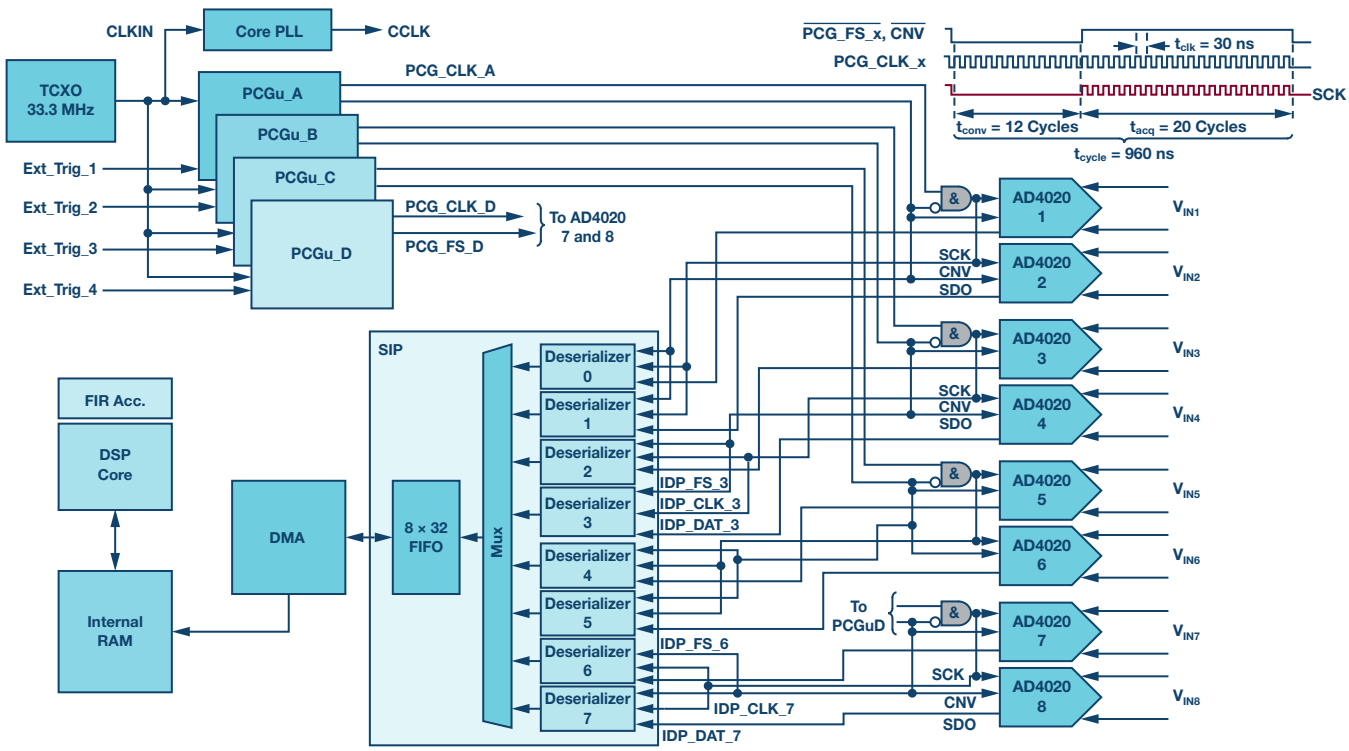

Figure 5. Connection of 8, 20-bit, 1 MSPS SAR ADCs to a SHARC DSP using deserialization and DMA transfer into the DSP internal RAM.

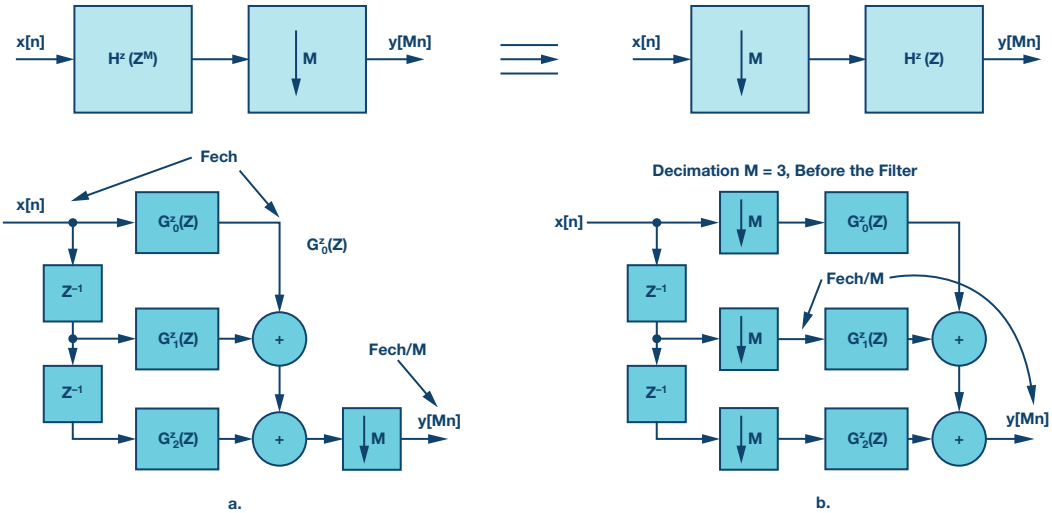

Figure 6a and 6b. Conventional decimation filter and a decimation filter using the polyphase approach.

- It supports IEEE-754 fixed-point or floating-point 32-bit arithmetic formats
- It has four multiplication-accumulation units operating in parallel
- It can operate in monorate or multirate processing modes (decimation or interpolation)
- It can handle up to 32 FIR filters for a total of 1024 coefficients in a simple iteration

The accelerator of the ADSP-21479 is clocked at the rate of the system clock or PCLK peripherals, half of the CCLK clock frequency of the CPU; that is, 133 MHz. This results in a total computing capacity of 533 MAC per second. The accelerator does not call for the execution of instructions; its operation is dictated by the configuration of specific registers and relies exclusively on DMA transfers for moving data between the internal and/or external memories.

Obviously, this accelerator will perform the implementation of multirate filters (interpolation or decimation) in an optimized way. Since a simple decimation filter provides only one output result for M input signals, the output rate is 1/M times lower than the input rate. Without resorting to the sophistication of the polyphase filter banks, which are complicated to implement because of the number of memory pointers required, the implementation of such an optimized FIR filter simply exploits the setting aside of the output from M – 1 samples to avoid doing those calculations, and only calculates the data for those that produce useful samples. This eliminates waste and, consequently, the number of operations is reduced in an M – 1 ratio—that is, 15 in the present example—resulting in a considerable saving of CPU cycles. However, for such a decimation ratio and short calculation window, the accelerator is not as effective as the core with its two calculation units, and is adversely affected by its DMA channels being reprogrammed during the passage from one filter to another. As implemented by a single calculation unit in SISD mode, the cost of such a filter in terms of the number of CCLK cycles is expressed as:

$$FIR\_Decim\_Cycles = N + 2 \times M + 19 \quad (5)$$

N is the number of coefficients for the filter and M is the decimation ratio.

The implementation of such a decimation filter for a single iteration amounts to about 150 cycles for an FIR filter (source to assembler 21k) corresponding to the ripple specifications of ± 0.00001 dB in the band (0 kHz to 24 kHz) and an out-of-band attenuation of –130 dB for a sample rate of 62,500 SPS. The response of this filter, which has 97 coefficients (quantized in 32-bit FP IEEE-754 format) is shown in Figure 7 with MATLAB® Filter Designer. It is repeated on DMA interrupt occurrences at the rate of this sampling frequency for each active channel of the connected SIP or ADC.

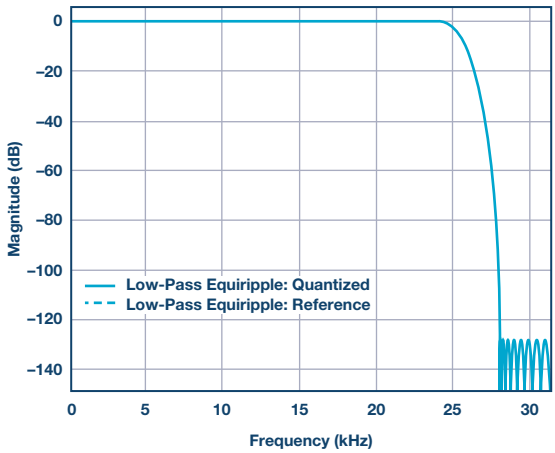

Figure 7. Filter response of a decimation filter.

For the real-time and the DSP load, the filtering operation is repeated at the frequency of 62.5 kSPS, which represents 9,375,053 CCLK cycles, and a little more than 8 times more with the 8 ADC conversion channels because of the saving and restoration of the memory pointer values of each filter, stored in the SHARC data address generators. This translates into 80 million execution cycles per second or 80 MIPS of a SHARC DSP in SISD mode and half that in SIMD mode, with the two processing elements running in parallel. The execution of these eight decimator FIR filters occupies the ADSP-21479 clocked at 266 MHz at the rate of 30% and 15% respectively, according to the aforementioned modes.

Finally, Energy Consumption

While the energy consumption of the converters can be evaluated quite easily and accurately from their specifications, that of the processors is more difficult because of the number of parameters entering the equation of this consumption and its great variability according to the constraints of real time and the modes of operation. Without going into details that the reader can easily find in the technical notes relating to the estimation of the energy consumption of the various constituents of ADSP-214xx and ADSP-21479 processors in particular, where account is taken of the activity of functional blocks, junction temperature for static current, supply voltage values, number of input-output pins used, various external frequencies, and capacitive loads. The energy consumption corresponding to the activity of the DSP for this type of decimation filtering application, in accordance with the functional description of Figure 5, is given for several combinations of DSP and ADCs. These associated DSP variants with four or eight ADCs are established according to the functional capacities, the number of adequate inputs/outputs, and computing power of the proces-

sors, as well as the overall performance of the ADCs. Owing to its very low static current, the solution constructed around the ADSP-21479 and its cluster of eight SAR ADCs is one that consumes the least energy while offering full latitude in the choice of filtering algorithms and other digital functions with an overall performance that is at best excellent.

This multichannel data acquisition system (DAQ) example also demonstrates that the use of FPGA is not mandatory for handling digital signal processing tasks and floating-point DSPs are a better fit for high precision SAR ADCs, especially when the power consumption is a hot concern.

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Table 1. Comparison of Different SAR ADCs in Comparison with a DSP

Parameters	AD4020 and ADSP-21479	LTC2378 and ADSP-21489	AD4020 and ADSP-BF532	LTC2378 and ADSP-BF532	LTC2512 -24	LTC2500 -32	AD7768 -1 Medium Mode	AD7768 -1 Fast Mode
Conversion A/N	SAR	SAR	SAR	SAR	SAR	SAR	WB-Σ-Δ	WB-Σ-Δ
Resolution	20	20	20	20	24	24 + 8	24	24
Oversampling	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
In-Band Ripple (dB)	±0.00001	±0.00001	±0.00001	±0.00001	±0.001	±0.001	±0.003 programmable	±0.003 programmable
Stop Band Att (dB)	<–130	<–130	<–120	<–120	<–65	<–65	–110 programmable	–110 programmable
Decimation Filter	Opt. FIR	Opt. FIR	Opt. FIR	Opt. FIR	FIR	FIR	FIR	FIR
Sampling Frequency (MSPS)	1	0.91	1.8	1	1	1	4	8
Effective Oversampling Ratio	16	16	32	16	16	16	128	256
First Aliasing Zone (MHz)	1	1	2	1	1	1	8	16
Frequency After Decimation (kSPS)	62.5	62.5	62.5	62.5	62.5	62.5	62.5	62.5
AAF Order Required to Achieve –110 dB of Aliasing Rejection	5	5	4	5	5	5	3	3
Aliasing Rejection with the Filter Order Above (dB)	–123.4	–123.4	–123.4	–123.4	–123.4	–123.4	–130	–147.5
SNR at 3 kHz with 5 V Reference (dBFS)	112	116	115	116	114	116	113.7	116.9
SFDR at 2 kHz (dBc)	122	128	122	128	120	128	128	128
THD at 20 kHz (dBFS)		–113		–113		–115	–120	–120
Digital Filter Bypass	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Frequency SCK/SDO (MHz)	33.3	50	61.5	64.1	1.5	1.5	1.5	1.5
ADC Consumption (mW)	10.8	24.8	15	24.8	32	30	19.7	36.8
DSP Consumption (mW)	185	832	70	75				
Number of Channels	8	8	4	4	1	1	1	1
Total Energy Consumption (Typically at Tj = 55°C) (mW)	272	1030	130	175				
Energy Consumption per Channel (mW)	34	129	33	43	32	30	19.7	36.8
ADC Operating Temperature Range (°C)	–40 to +125	–40 to +85	–40 to +125	–40 to +85	–40 to +85	–40 to +85	–40 to +125	–40 to +125

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Patrick Butler

Automotive USB Type-C Power Solution: 45 W, 2 MHz Buck-Boost Controller in a 1 Inch Square

By **Kyle Lawrence**

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USB Type-C is a relatively new, high power USB peripheral standard used in computer and portable electronic devices. The USB Type-C standard has driven changes in the USB power delivery specification, allowing for increased bus voltages (up to 20 V) and current delivery capability (up to 5 A) from the long-standing 5 V USB standard. Connected USB-C devices can recognize each other and negotiate a bus voltage—from the default 5 V USB output to several higher preset voltage steps—for faster battery charging and higher power delivery where needed, up to 100 W.

The simple, compact buck regulators and linear regulators used in battery chargers that require only USB 5 V at 500 mA to 2 A do not sufficiently cover the full range of Type-C USB power. The increased voltage range, 5 V to 20 V, of Type-C USB power delivery requires more than just step-down voltage conversion from 9 V to 36 V (or 60 V) automotive batteries, or other charging sources. An adjustable buck-boost converter is needed with the ability to both step-up and step-down the input-to-output voltage.

Additionally, for high power automotive USB chargers, a buck-boost converter should support a 10 A or higher peak switch current rating and offer low EMI performance. The ability to set the switching frequency outside the AM radio band and maintain a small solution size are sought-after features. High voltage monolithic converters (with onboard switches) are not capable of sustaining such high peak switch currents without burning up.

The LT8390A is a unique 2 MHz, synchronous 4-switch buck-boost controller. At 2 MHz switching frequency, it can deliver output voltages between 5 V and 15 V (up to 45 W at 3 A) to provide power to a connected USB-C device from a car battery. This high controller switching frequency keeps the solution size small, the bandwidth high, and the EMI outside of the AM radio band. Both spread spectrum frequency modulation and low EMI current-sense architecture help LT8390A applications pass the rigors of the CISPR 25 Class 5 automotive EMI standard.

High Power Density Conversion: Size (and Power), Efficiency, Heat

The design of a voltage regulator system operating in an automotive or portable electronics environment is constrained by the space required for the circuit, as well as the heat it generates during operation. These two factors impose an upper bound of achievable power levels while operating within the given design constraints.

Increasing the switching frequency of a design allows for the use of smaller inductors, which is often the largest footprint component in wide input voltage 4-switch buck-boost voltage regulator designs. The LT8390A's 2 MHz switching frequency capability enables the use of a much smaller inductor size than a 150 kHz or 400 kHz design. A complete design is shown in Figure 1. Along with a smaller inductor, this solution uses only ceramic output capacitors, eliminating the need for bulky electrolytic capacitors. All the components necessary for this design, including the IC, are contained within a small, 1" inch square footprint, as shown in Figure 1.

Figure 1. Efficient, low EMI USB Type-C power solution that fits in a 1" square.

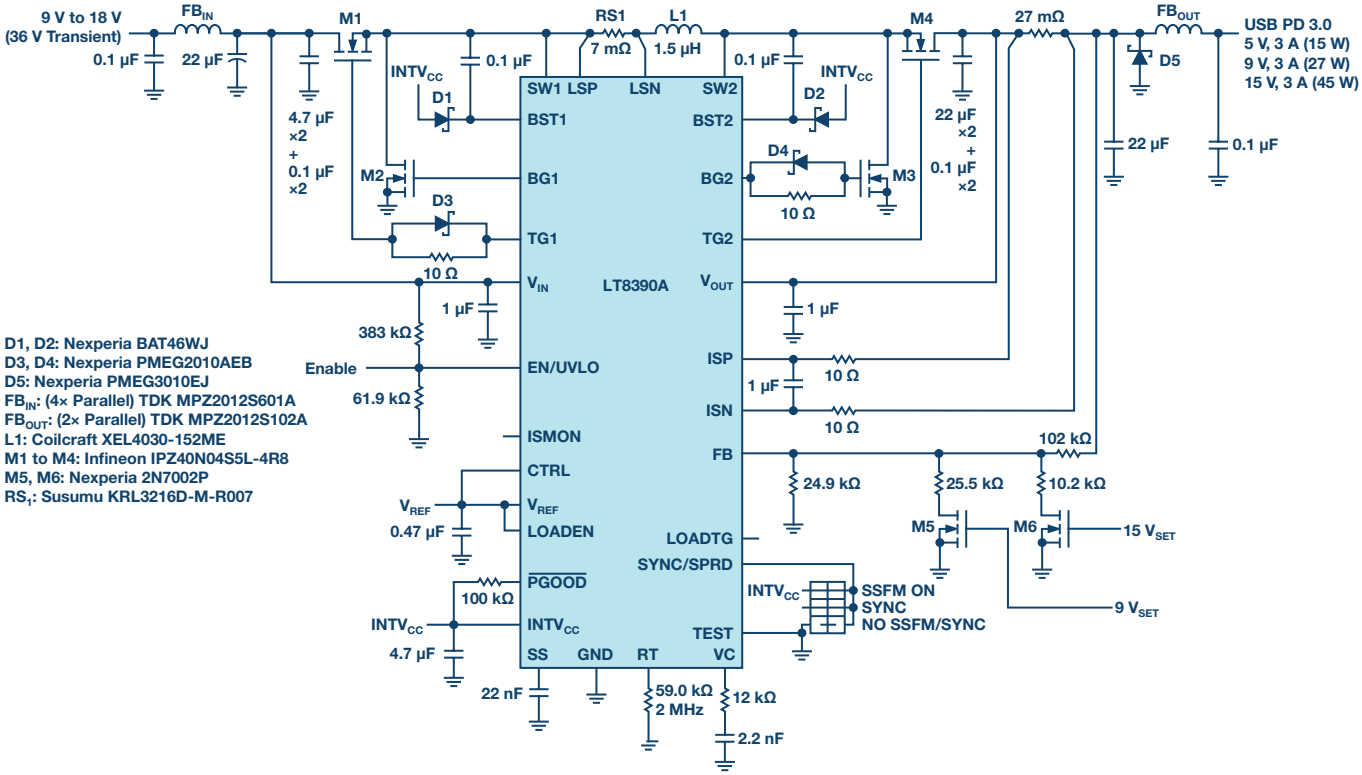

Figure 2. This LT8390A voltage regulator solution provides up to 3 A at selectable 5 V, 9 V, or 15 V low EMI outputs using AEC qualified MOSFETs, magnetics, and capacitors.

Figure 2 shows a 45 W LT8390A solution using AEC qualified components. This design experiences a maximum temperature increase of 65°C from the ambient temperature, as shown in Figure 3. Even with the small solution size, the LT8390A system boasts a peak efficiency of 94% while delivering a 45 W output, and deviates in efficiency by less than 10% over the input range for each output voltage created, shown in the graphs in Figure 4.

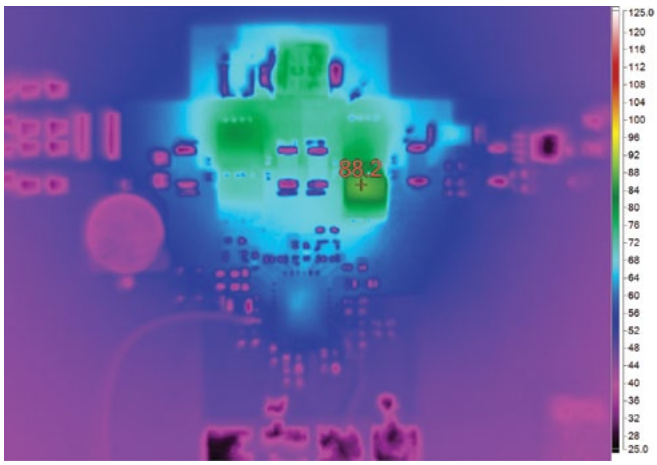

Figure 3. While generating 45 W of output power, this small circuit's greatest temperature rise is only 65ºC above ambient temperature.

Low EMI for Automotive Applications

The LT8390A has several unique EMI mitigating features that enable high power conversion with low noise performance, which simplifies its implementation in automotive systems. A notable difference between LT8390A and alternative 4-switch controllers is the placement of the inductor current sensing resistor. Most 4-switch buck-boost controllers tend to use a ground-referred current sensing scheme to obtain switch current information, whereas the LT8390A places its current sense resistor in-line with the inductor. By placing the sensing resistor in-line with the inductor, it is effectively removed from both the buck and boost hot loops, shrinking the loops in size and improving the EMI performance.

Along with the architectural advantage of the inductor sensing resistor placement, the LT8390A has built-in spread spectrum frequency modulation to further reduce EMI generated by the controller. Furthermore, the switching edge rate is controlled on both the buck and boost power switches using only a few discrete components to slow the turn-on of the MOSFETs, ensuring the proper balance of high frequency EMI reduction and temperature rise in the power switches. With these EMI-reducing features, the only filtering needed to meet CISPR 25 compliance is taken care of by small ferrite filters on the input and output rather than large ferrite cases and bulky LC filters. The solution shown in Figure 1 was designed using only AEC-Q100 components.

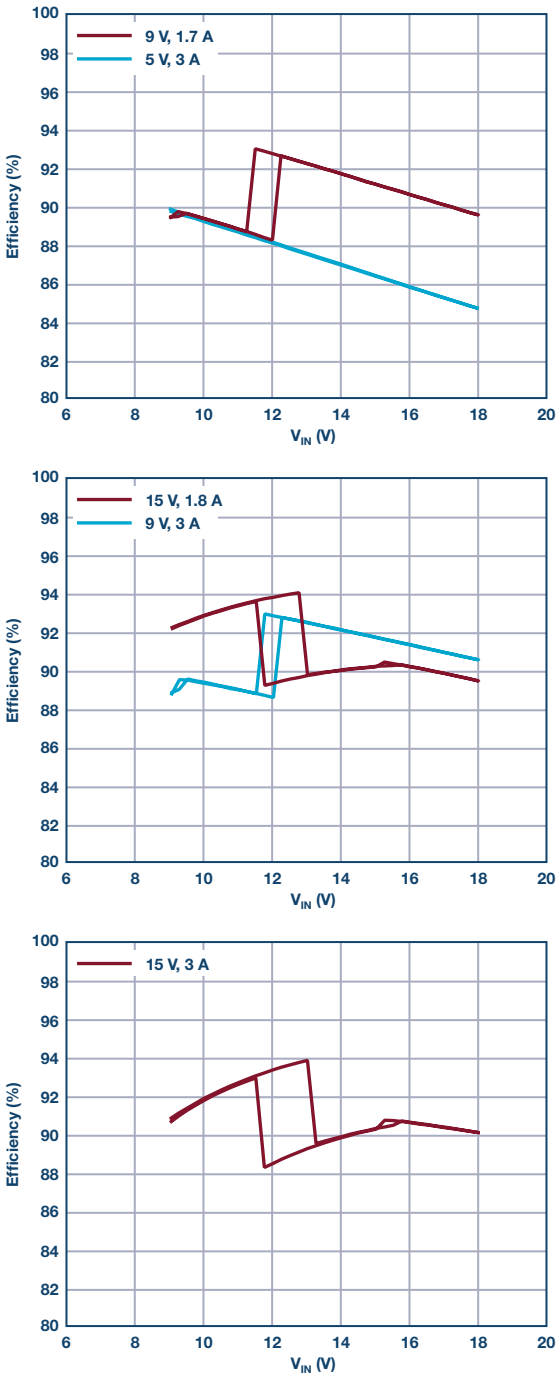

Figure 4. The LT8390A voltage regulator system remains in the 94% to 84% efficiency range across all output voltages generated when powered from an automotive SLA battery.

Seamless Output Voltage Transitions

The LT8390A's output voltage can be adjusted without shutting down the converter by using logic-level signals to drive MOSFETs that adjust the resistor divider off the output to change the set voltage. A USB PD source controller device with GPIO pins can be used in conjunction with the LT8390A system to facilitate the negotiation process between host and USB-connected device and to set the desired bus voltage.

Figure 5 demonstrates how smoothly the output of the LT8390A system transitions from one output voltage to another. When powered from a 12 V input source, each transition to an increased output voltage takes at most 150 µs to settle, as measured from the rising edge of the digital control signal. During these changes in the output voltage, the buck-boost controller goes through mode transitions—between buck, boost, and buck-boost operation—depending on the relation of input to output voltages. These mode transitions are performed in a controlled manner, preventing excessive overshoot or sagging of the output voltage.

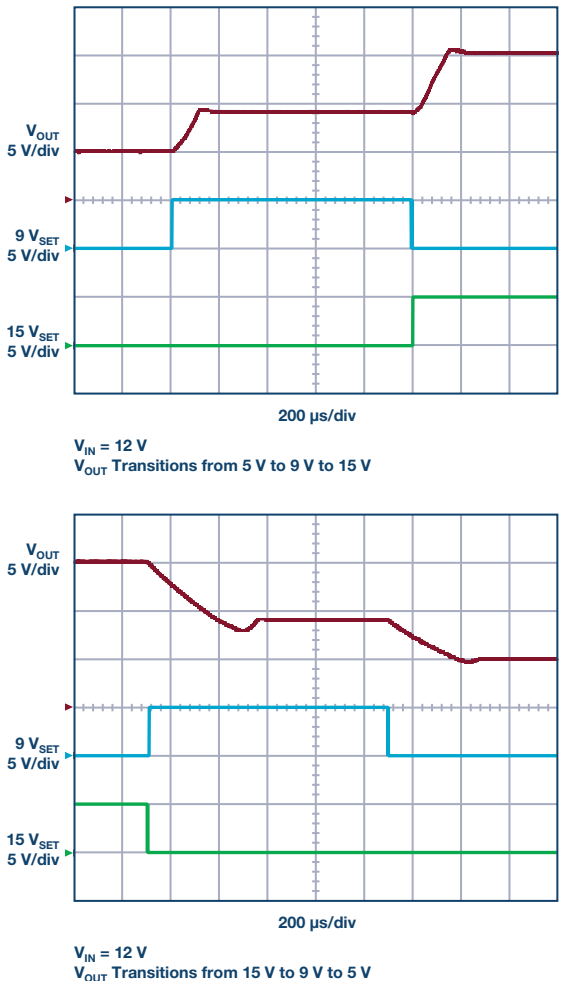

Figure 5. The output of the LT8390A system smoothly transitions between 5 V, 9 V, and 15 V outputs while maintaining continuous power delivery to the output.

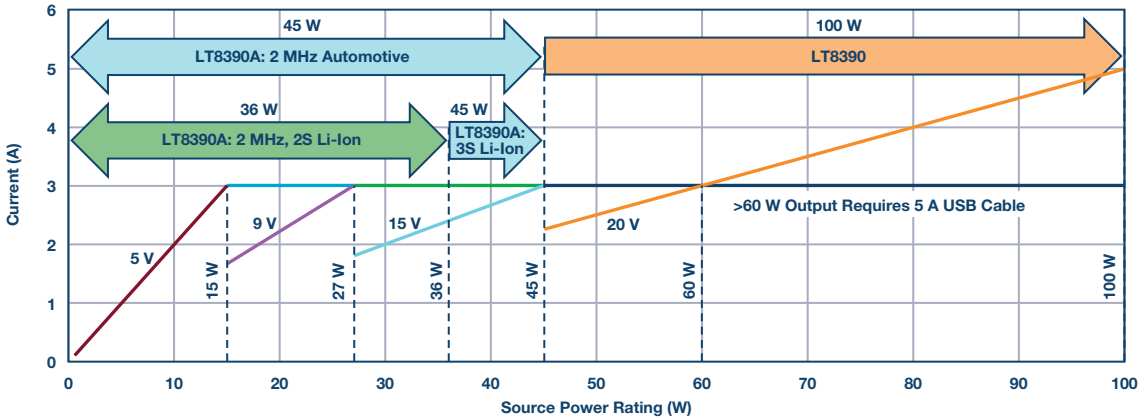

Figure 6. The LT8390A and LT8390 cover a wide range of output power levels for USB power delivery.

Expanding Beyond 45 W

To push the output power level beyond 45 W requires operating at a lower switching frequency to reduce switching losses, which might otherwise thermally stress the MOSFETs at this power level. As an alternative to the LT8390A, the LT8390 operates between 150 kHz and 600 kHz with the same feature set as LT8390A—allowing low EMI, high power buck-boost designs. A 400 kHz LT8390 system, utilizing a larger inductor and output capacitor, easily achieves 100 W of output power from an automotive battery input with acceptable temperature rise. Figure 6 illustrates the power capabilities of the LT8390A and LT8390 product line from various battery-powered inputs.

Conclusion

The new USB standard for voltage regulators powering connected devices permits higher power transfer by increasing the output voltage range and current delivery that regulators can provide. Portable and automotive battery-powered USB-C charger devices require a wide V_{IN}/V_{OUT} buck-boost regulator to deliver a bus voltage above or below the input voltage. The LT8390A provides up to 45 W of output power in a small footprint, made possible by its 2 MHz switching frequency. For power levels exceeding 45 W, the LT8390 can be used with a slightly larger solution size and lower switching frequency.

Kyle Lawrence [kyle.lawrence@analog.com] is an applications engineer at Analog Devices. He is responsible for the design and testing of a variety of dc-to-dc converters, including 4-switch buck-boost voltage regulators and LED drivers targeting low EMI automotive applications. Kyle received his B.S. degree in electrical engineering from the University of California, Santa Cruz in 2014.

Kyle Lawrence

Also by this Author:

LED Driver for High Power Machine Vision Flash

Volume 52, Number 2

Rarely Asked Questions—Issue 157 Overvoltage Protection for RTD-Based Measurement Systems

By **Yao Zhao**

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Question:

Is it possible to design a complete RTD module with overvoltage protection?

Answer:

Introduction

RTDs (resistance temperature detectors) can provide excellent stability and accuracy, and reduce the impacts of noise and interference. RTD sensors can be made up of either 2-wire, 3-wire, or 4-wire versions, and require an excitation current to produce an output voltage. AD7124-4/AD7124-8 contain two well matched current sources, a PGA, reference buffers, and diagnostic functions, which are ideally suited for high reliability RTD modules.

Incorrect operations, careless connections, and exposed wires usually lead to overvoltage faults in industrial circumstances, which will damage the electronic devices and cause undesirable consequences that may flow from the damage. Overvoltage protection ability is a key specification for an RTD module. Outside of transient overvoltage protection, durable overvoltage protection must be considered during actual production.

This article will focus on how to provide a total solution for multiwire RTD modules with overvoltage protection function, which is based on AD7124, and overvoltage protection and detection multiplexers and channel protectors. This article can help designers understand this method and choose appropriate devices.

For overvoltage protection functions, here are three optional solutions:

- Using series resistors in front of the pins of an ADC can help protect the AD7124 easily. These pins include analog input and excitation output pins, but the resistors will limit compliance voltage.
- The protection of current source can be realized by discrete components. This solution can achieve higher overvoltage protection and larger voltage compliance. However, the switches and multiplexers are still externally exposed.
- ADI's overvoltage protection and detection switches, multiplexers, and channel protectors (ADG52xxF and ADG54xxF) can be used for RTD module protection and different wires RTD sensor switching. These parts can provide ±55 V fault voltage protection in both the powered and unpowered mode, and can implement fault detection with latch-up immunity. Their high density package occupies a much smaller PCB area than traditional solutions.

RTD Module Based on AD7124

Ratiometric measurement is widely used in RTD modules, as it can remove the error and drift of the excitation current source. Figure 1 shows the typical diagram for 4-wire RTD measurement based on AD7124-8.

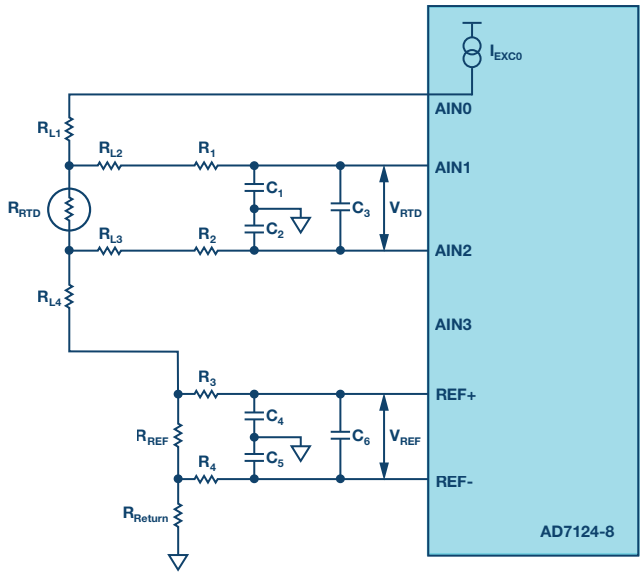

Figure 1. 4-wire RTD ratiometric measurement based on AD7124-8.

AIN0 provides the excitation current, and the AD7124 integrated reference buffer and PGA, REF_{IN} and A_{IN} are high impedance inputs, so the same current flows through the RTD sensor and reference resistor. The ADC conversion result is the ratio between input voltage (V_{RTD}) and reference voltage (V_{REF}), which is equal to the ratio between R_{RTD} and R_{REF}. If R_{REF} is a known, high precision, and stable reference resistor, R_{RTD} can be calculated by the R_{REF} value and ADC conversion result.

By using a 4-wire RTD configuration, the system can achieve high accuracy and reliability and the error due to lead wire resistance can be removed. Accordingly, the cost is higher than a 3-wire or 2-wire configuration. Figure 2 shows the 3-wire RTD measurement based on AD7124, which is a compromise between performance and cost.

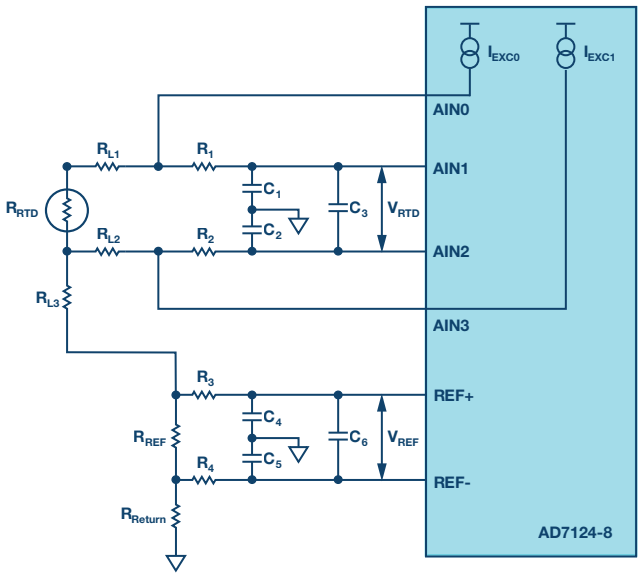

Figure 2. 3-wire RTD ratiometric measurement based on AD7124-8.

Two integrated, well matched current sources are helpful for 3-wire RTD measurement. V_{REF} and V_{RTD} can be expressed by the following two functions:

$$V_{REF} = (I_{EXC0} + I_{EXC1}) \times R_{REF}$$
$$V_{RTD} = I_{EXC0} \times R_{RTD} + I_{EXC0} \times R_{L1} - I_{EXT1} \times R_{L2} \quad (1)$$

AD7124 has two well matched current sources, which means I_{EXC0} is near or equal to I_{EXC1} and the lead resistors RL1 and RL2 are very similar. The functions can be expressed as:

$$V_{RTD} = I_{EXT0} \times R_{RTD}$$
$$V_{REF} = 2 \times I_{EXC0} \times R_{REF} \quad (2)$$

Express the conversion code as a composition of these two functions:

$$Code/Code_{FS} = V_{RTD}/V_{REF} = \frac{R_{RTD}}{(2 \times R_{REF})} \quad (3)$$

According to this function, the RTD resistor value can be calculated by the conversion result and reference resistor value. Please refer to CN-0383 for details.

For a 2-wire RTD, the error due to lead resistance can't be cancelled, but the cost of these type RTD sensors is lower than the others, and AD7124-8 can be configured as a 2-wire RTD sensor, as seen in Figure 3.

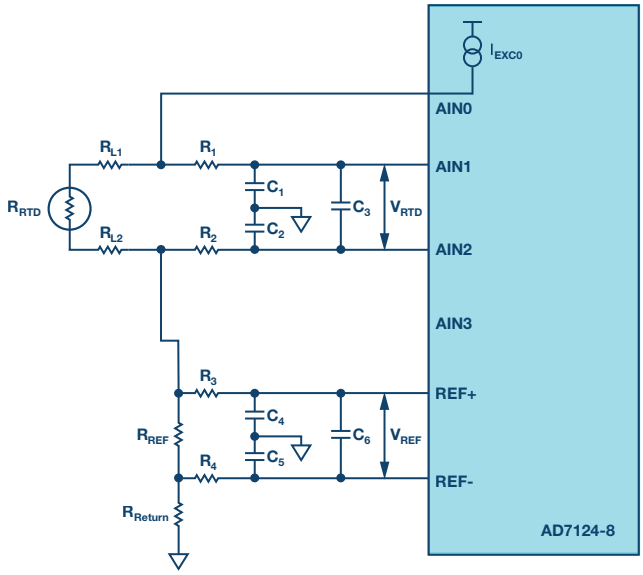

Figure 3. 2-wire RTD ratiometric measurement based on AD7124-8.

In practice, many industrial customers ask for the same port of an RTD module to many different types of RTD sensors, which is convenient for balancing RTD sensors' cost and performance. Figure 4 shows a universal interface of an RTD module, which can support different wires RTD sensors.

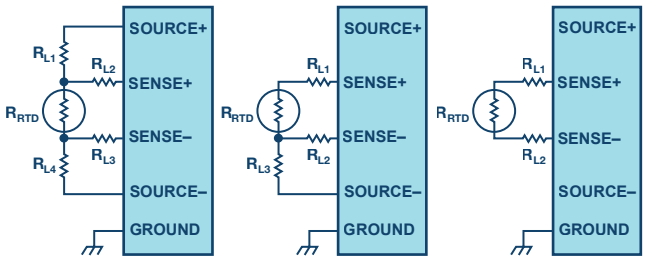

Figure 4. RTD interface for different wire sensors.

Due to this requirement, this type of RTD module needs to be configured by firmware for differently wired RTD sensors easily. Figure 5 shows the block diagram for different wire RTD sensors based on one piece of the AD7124-8 and its switches. AD7124-8 can support a 4-channel, 2-wire/3-wire/4-wire RTD measurement.

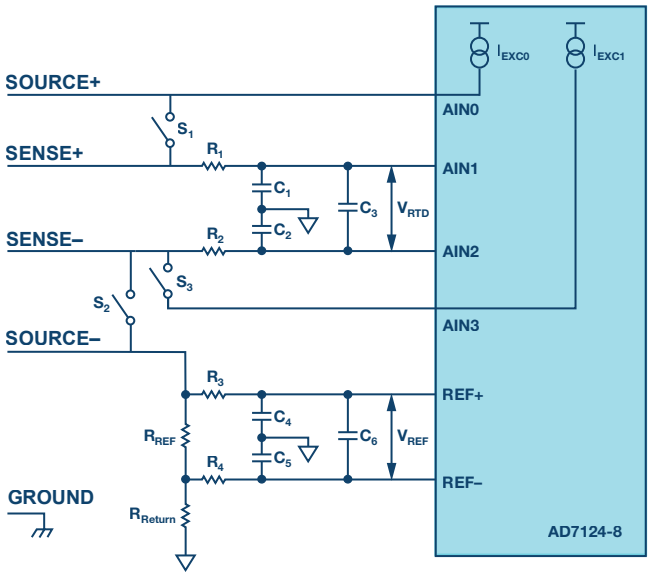

Figure 5. Different wire RTD sensors measurement based on AD7124-8.

Using a controller can change the configuration for different sensors easily, and Table 1 shows switches and current source status for different configurations.

Table 1. Switch and I_{EXT} Status for Different Wire RTD Sensors

	S1	S2	S3	I_{ETX1}	I_{ETX2}
2-wire RTD	Closed	Closed	Open	Enable	Disable
3-wire RTD	Closed	Open	Closed	Enable	Enable
4-wire RTF	Open	Open	Open	Enable	Disable

Choosing appropriate resistor and capacitor value by calculation can optimize the noise performance. The article "Analog Front-End Design Considerations for RTD Ratiometric Temperature Measurements" can provide guidance. If, in addition to an optimized noise performance, overvoltage protection is needed in the field, the additional requirement will cause a lot of additional trouble.

First, some analog pins of AD7124 are directly exposed to outside environments, and according to the absolute maximum ratings of AD7124 under 25°C, the analog input voltage to AVSS should between −0.3 V to AVDD +0.3 V, which means this module can't defend high overvoltage occur. Secondly, three switches need to bear high voltage.

Adding Current Limiting Resistors

Adding current limiting resistors on every pin of AD7124 can provide overvoltage protection for AD7124 easily.

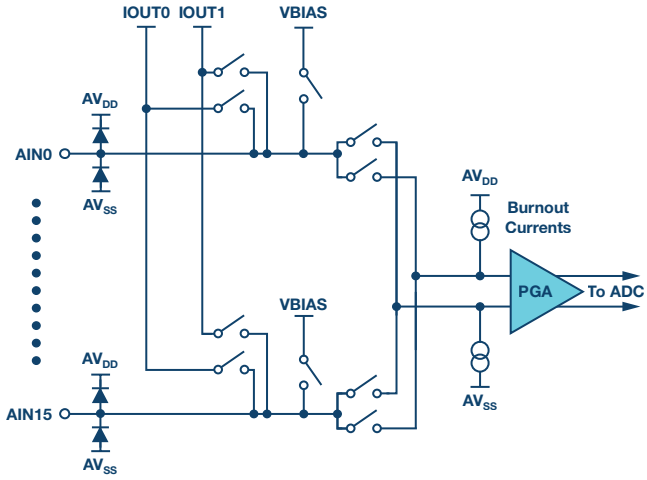

Figure 6. AD7124-8 analog pin internal architecture.

Figure 6 shows the AD7124 analog pin architecture. There are two clamping diodes on every analog pin and we can use these diodes to implement protection directly without introducing any other leakage current.

Figure 7 shows the diagram of this method—R1 to R4 are in front of AIN1, AIN2, REF+, and REF– separately. This setup is used for noise elimination. These resistors can be used for current limit at the same time and adding current limiting resistors in front of AIN0 and AIN3 can protect the rest of exposed analog pins of AD7124.

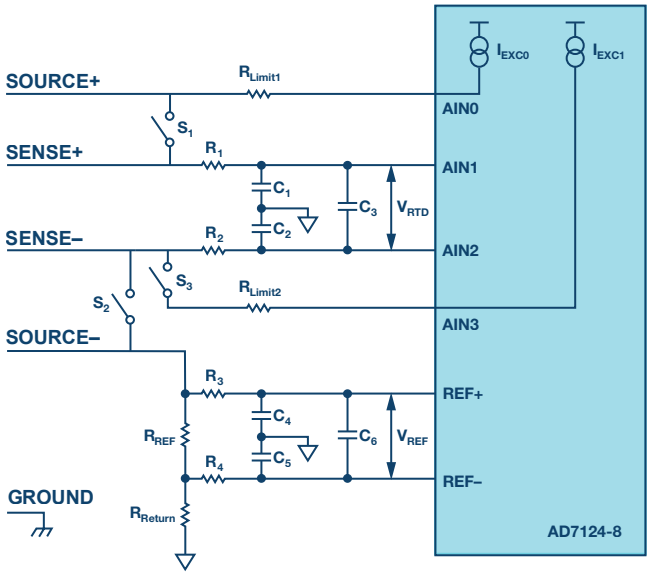

Figure 7. Adding current limiting resistors in front of ADC input pins.

These resistors and the internal clamping diodes can protect against some level of positive and negative overvoltage. When positive or negative overvoltage fault occurs, the current will flow through the resistors and internal clamping diodes to AVDD or AVSS. The current value must be limited to less than 10 mA, according to the absolute specification of AD7124. If R_{Limit} is equal to 3 kΩ, this module can prevent ±30 V durable overvoltage.

However, there would be a voltage drop on R_{LIMIT} when this module works in a normal mode. If the excitation current was 500 µA, the voltage drop on R_{LIMIT} would be 1.5 V, the resistance of sensor and R_{REF} would be limited. Increasing R_{LIMIT} can get better protection, but the resistance range will be smaller. The compliance voltage will decrease along with the increasing overvoltage protection requirement based on this protection method. If the power consumption of R_{REF} and R_{Return} is taken care of, the fault voltage will directly drop on these two resistors.

Except for AD7124-8 analog pins, the switches are exposed under the high voltage too, so we should choose the parts that can defend ±30 V voltage. In the past few years, photo MOS and relay have been used in these situations, but the high price and large package limit the sphere of application.

Using Discrete Transistors to Protect the Current Source

The biggest weakness of using limit resistors is that the compliance voltage on SOURCE+ is low. Using discrete transistors and diodes can implement overvoltage protection and increase the max allowed voltage on SOURCE+ pin. Figure 8 shows the diagram for this method.

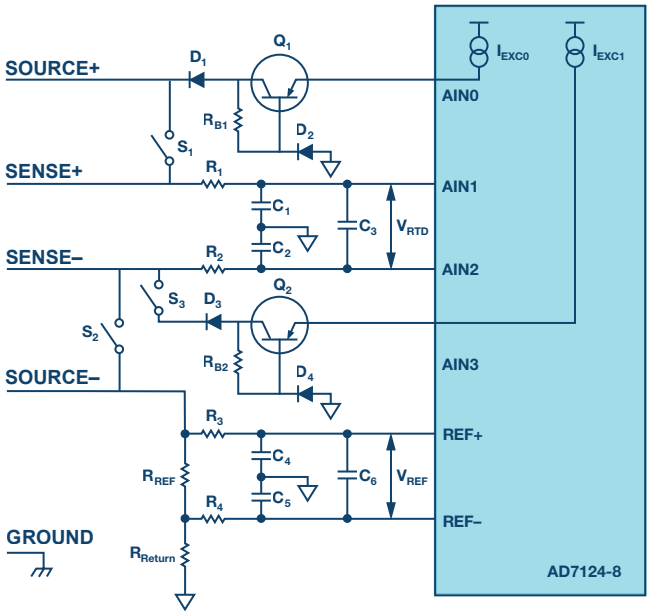

Figure 8. Using discrete transistors and diodes for overvoltage protection.

This architecture can keep the excitation current flow to the RTD sensor in a normal situation and defend against high overvoltage damage. The other analog input pins can be protected by current limiting resistors, since analog input pins have no compliance voltage limitation.

If a large positive voltage is applied to this RTD sensor, D1 prevents the current source from positive high voltage. If a large negative voltage is applied to this RTD sensor, the PN junction between Q1's collector and base is in reverse biased, causing high voltage drops on R_{B1} and this PN junction, which can prevent damage to AIN0.

In the normal mode, D2 functions as a reverse biased diode, which keeps the current flow through this part very small. There is very little current flow throw Q1's emitter to base, so the voltage drop on R_{B1} can be neglectful. This method can keep compliance voltage higher than using current limiting resistors and defend much higher fault voltage.

Using Analog Switches and Multiplexers with Overvoltage Protection Function

The weaknesses of using discrete components to protect this high precision RTD module are obvious—it's not easy to choose appropriate components; these parts makes the protection circuit complicated; and they occupy a large PCB area.

Even though the leakage current of AD7124 analog input pins is quite small, the large resistor series on these pins, such as R_1 and R_2, will produce notable error, and the thermal noise of these resistors decrease the resolution. In an actual design, the RTD module may have multiple channels, the current source would switch from one channel to the other, a large resistor value increases the settling time of analog input RC combination, and a RTD module should spend more time on charging the capacitors, such as C_1, C_2, and C_3. It's hard to balance protection functions and accuracy. And the switches still need to protect against high overvoltage too.

In this case, using analog switches and multiplexers with fault protection can provide switch and overvoltage protection. Figure 9 shows an example.

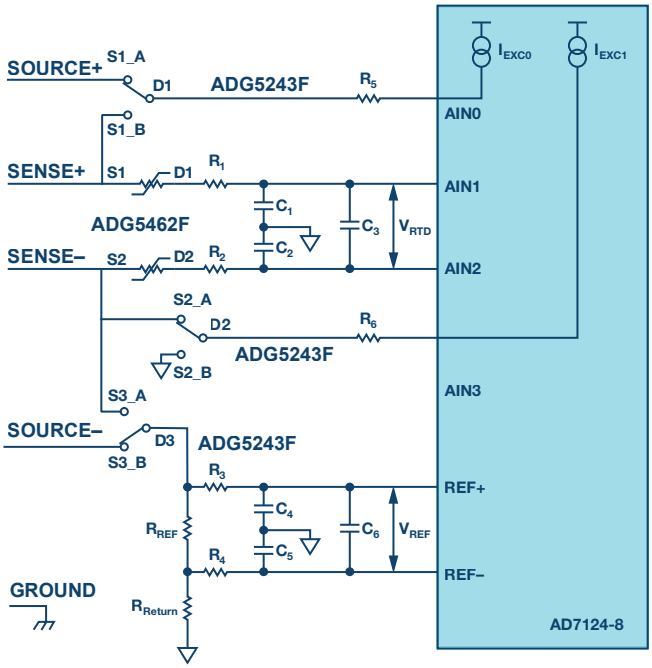

Figure 9. Analog switches and multiplexers with fault protection.

In Figure 9, there are three SPDT switches using the ADG5243F in front of the AD7124, and two variable resistors using ADG5462F in front of AIN1 and AIN2. These components can be implemented by using ADG5243F and ADG5462F, which have user-defined fault protection and detection functions.

The highlight feature of these parts are:

- The source pins are protected against voltages greater than the secondary supply rails, from –55 V and +55 V.
- The source pins are protected against voltages between –55 V and +55 V in an unpowered state.
- Overvoltage detection with the digital output indicates the operating state of the switches.
- Trench isolation guards against latch-up.
- Optimized for low charge injection and on-capacitance.
- The ADG5243F can be operated from a dual supply of ±5 V to ±22 V or a single power supply of 8 V to 44 V.

Latch-up immunity with low leakage current and industry-leading R_{ON} flatness are the advantages of these parts too. Low leakage and low conductive resistance can improve the accuracy and noise performance of this RTD module.

If a positive or negative voltage is applied to the RTD interface, the voltage on the drain pins will be clamped at POSFV + V_T or NEGFV – V_T. If the POSFV is set to 4.5 V and the NEGFV is set to AGND, the resistor series in the route, which is used for protecting AD7124, is much easier to choose. If the overvoltage occurs during unpowered state, the switches stay in a high impedance state and help prevent damage to the parts.

The detection function of these parts can be used for system diagnostics. The voltages on the source inputs of ADG5243F and ADG5462F are continuously monitored. An active low digital output pin, FF, indicates the state of the switches. The voltage on the FF pin indicates if any of the source input pins are experiencing a fault condition. AD7124 offers many strong diagnostic functions for system safety. The processor can combine the diagnostic functions of these parts to build a much more robust system.

Summary

The functional blocks and diagnostic functions in AD7124 improve the accuracy and robustness. After comparing three overvoltage protection methods in RTD module, using analog switches and multiplexers with overvoltage protection functionality has many advantages:

- Making RTD modules endure higher fault voltage
- Low leakage current, low noise, and short settling time
- Replacing traditional relay and photo MOS, saving PCB area and cost
- Diagnostic functionality enhances system robustness
- Easy to use

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Yao Zhao

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