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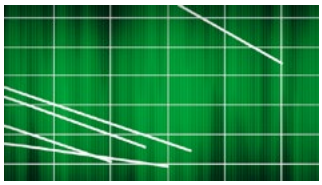

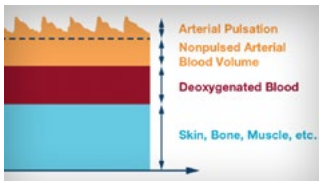

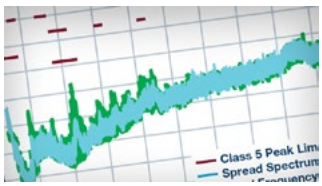

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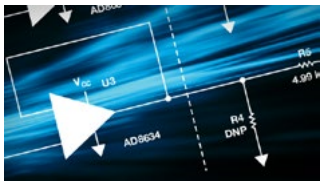

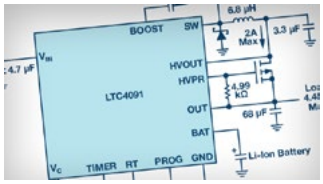

Bernhard Siegel, Editor

Bernhard became editor of *Analog Dialogue* in March 2017, when the preceding editor, Jim Surber, decided to retire. Bernhard has been with Analog Devices for over 25 years, starting at the ADI Munich office in Germany.

Bernhard has worked in various engineering roles including sales, field applications, and product engineering, as well as in technical support and marketing roles.

Residing near Munich, Germany, Bernhard enjoys spending time with his family and playing trombone and euphonium in both a brass band and a symphony orchestra.

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AnalogDialogue

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Preventing Start-Up Issues Due to Output Inrush in Switching Converters

By **Fil Paulo Balat, Jefferson Eco,** and **James Macasaet**

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Abstract

Switching converters on applications demanding reduced output noise may encounter delayed startup, or may not startup at all, due to excessive output inrush. Output inrush current, attributed to inappropriate design of output filters and its impact, can be minimized by increasing the soft start time, increasing the switching frequency, or decreasing the output capacitance. In this article, practical design considerations toward preventing start-up issues due to excessive output inrush will be presented.

Introduction

Many switching converter designs are driven by stringent output noise requirements. The demand for low output noise has pushed designers to implement heavy output filtering, such as using several capacitors at the output. With increased capacitance across the output rail, excessive inrush current may become an issue during startup that can potentially lead to inductor saturation or damage of the power switch.

The power switch of a monolithic switching regulator is internal to the chip, as opposed to a switching controller. This is an ideal approach on point-of-load switching converter applications, because of advantages like smaller PCB footprint and better design of the gate-drive circuit. This means that protection against overcurrent becomes a necessity to avoid damaging not only the switch, but the regulator chip itself. The ADP5070 dual, high performance dc-to-dc monolithic switching regulator is an example, as illustrated in Figure 1.

To prevent damage during output overload condition or startup when high current flows through the internal switch, switching regulator manufacturers employ different current-limiting techniques on monolithic switching regulators. Despite the existence of current-limit protection, the switching regulator may not properly operate as intended, especially during startup. For instance, with hiccup mode as the current-limit protection, at initial power-up when the output capacitor is still fully discharged, the switching regulator may enter hiccup mode, causing a longer start-up time or

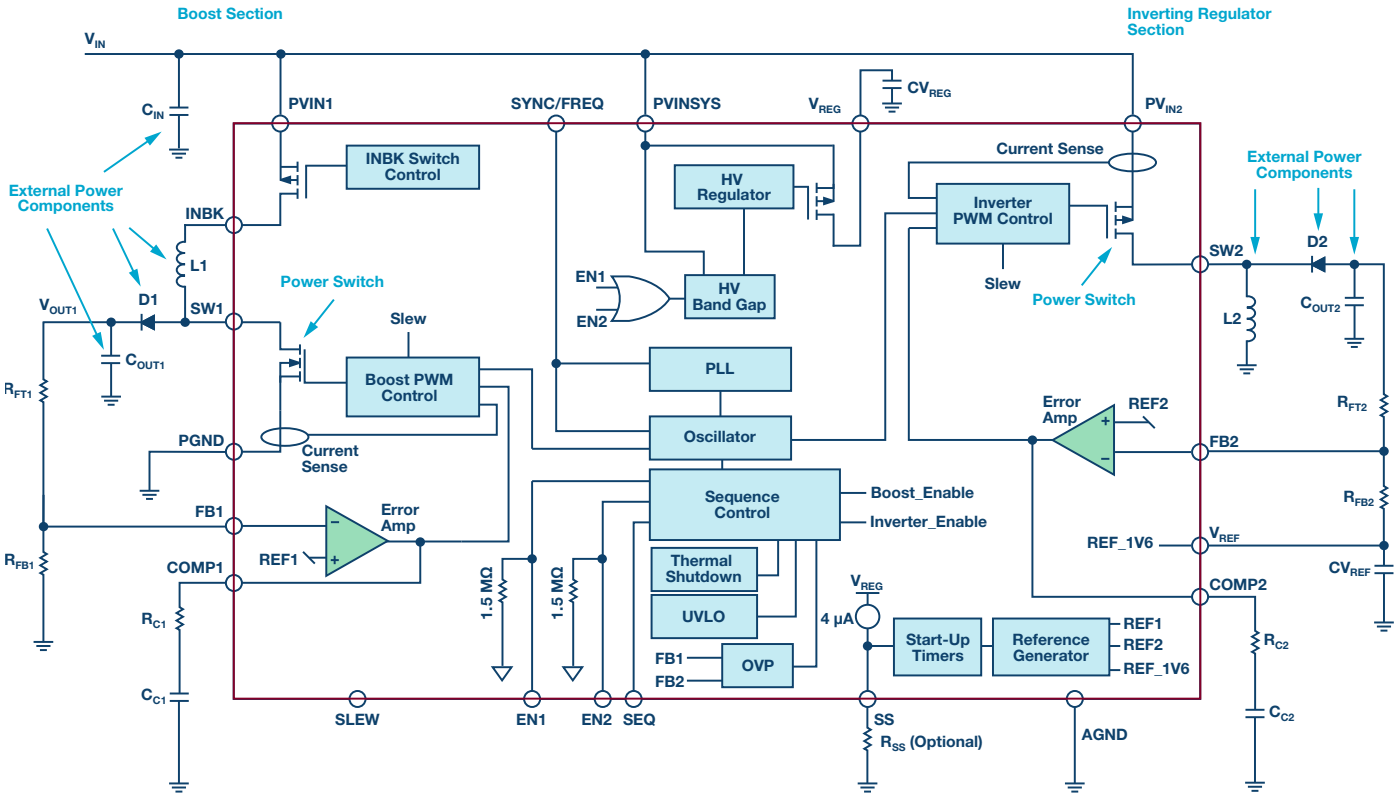


Figure 1. Switching converter using ADP5070 regulator.

potentially not starting up at all. The output capacitor may pull excessive inrush current that, in addition to the load, causes the inductor current to go high and hit the hiccup mode current-limit threshold.

Overcurrent Protection Schemes

Integrating the power switch inside switching converters makes the current-limiting protection a basic function. Three commonly used current-limiting schemes are: constant current-limiting, foldback current-limiting, and hiccup mode current-limiting.

Constant Current-Limiting

For a constant current-limiting scheme, the output current is held constant to a specific value (I_{LIMIT}) when an overload condition occurs. As a result, the output voltage drops. This scheme is implemented by using cycle-by-cycle current-limiting that utilizes the peak inductor current information through the power switch to detect the overload condition.

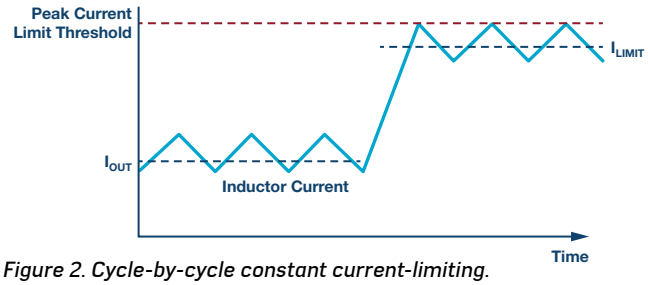


Figure 2. Cycle-by-cycle constant current-limiting.

Figure 2 shows a typical inductor current of a buck converter during normal and overload conditions for the peak current-limiting scheme. During overload condition, as illustrated by I_{LIMIT}, the switching cycle is terminated when the peak current detected is greater than the predetermined threshold.

In the constant current-limiting scheme, the output current is maintained at I_{LIMIT}, resulting in high power dissipated in the regulator. This power dissipation causes the junction temperature to increase, which may exceed thermal limits.

Foldback Current-Limiting

The foldback current-limiting scheme partially solves the issue with constant current-limiting, helping to keep the transistor in its safe operating area under fault or overload conditions. Figure 3 shows the comparison of the V_{OUT} vs. I_{OUT} response curves between the constant and foldback current-limiting schemes. The reduction in output current (I_{OUT}), as opposed to constant current-limiting, reduces power dissipation, thus reducing the thermal stress on the switching converter.

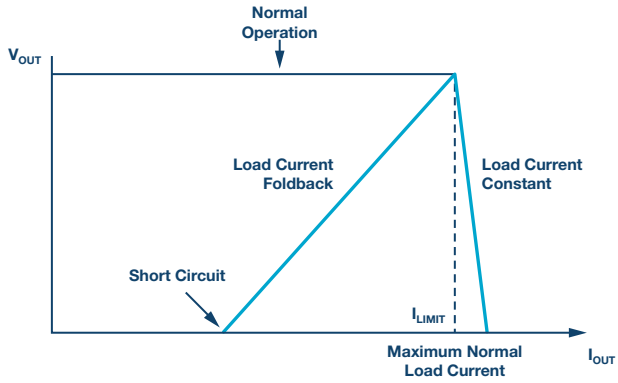


Figure 3. V_{OUT} vs. I_{OUT} curve of constant and foldback schemes.

The disadvantage of this scheme is that it is not fully self-recoverable. Due to its foldback nature and depending on the nature of the load, the operating point could fall into the foldback region toward the short circuit operating point once the current-limit threshold was reached or exceeded. This would require power cycling the part or re-enabling the part to get back to the normal operating condition.

Hiccup Mode Current-Limiting

In a hiccup mode current-limiting scheme, the converter switching goes into a series of short burst of pulses followed by sleep time—hence the name hiccup. Once an overload condition occurs, the switching converter enters hiccup mode, where sleep time refers to the switch being turned off for a predefined period of time. At the end of the sleep time, the switching converter attempts to start again from soft start. If the current limit fault is cleared, the device resumes normal operation—otherwise, it re-enters hiccup mode.

The hiccup mode current-limiting scheme overcomes the drawbacks of the two overcurrent protections discussed. Firstly, it solves the thermal dissipation problem, as the sleep time reduces the average load current that allows the converter to cool down. Secondly, it allows smooth autorecovery once the overload condition is removed.

However, some issues may arise if the hiccup mode detector is active during startup. Excessive inrush current, in addition to the load current, may cause the inductor current to go beyond the current limit threshold, which triggers hiccup mode and prevents the converter from starting up. For example, the negative output of the inverting regulator of ADP5071, configured to have an output voltage of –15 V and 100 mA output current with around 63 µF of total output capacitance, is not starting up after powering from a 3.3 V power supply. The negative rail is under hiccup mode, as shown in Figure 4, which is triggered by the large output inrush current. Inductor current peak goes to around 1.5 A, exceeding the typical current-limit threshold of around 1.32 A.

Figure 4. ADP5071 inverting regulator in hiccup mode.

Also, if there's excessive inrush due to large output capacitance, the converter may get unexpected longer start-up time, as shown in Figure 5.

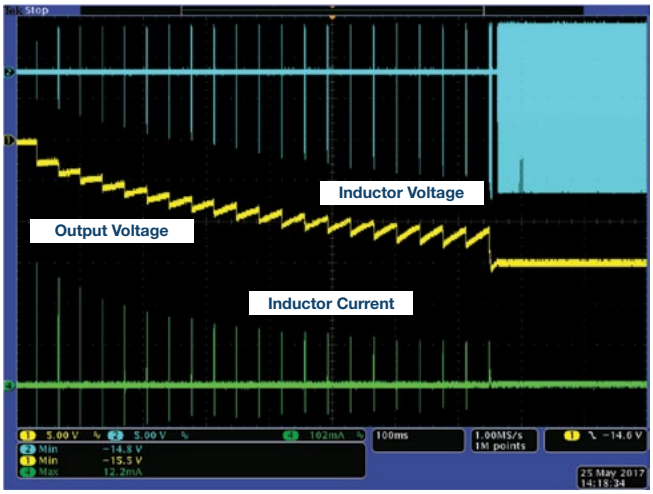


Figure 5. ADP5070 inverting regulator delayed startup.

Inductor Current in Switching Converters

Inductor Current Average

In nonisolated switching converters, the location of the inductor defines the converter topology. With a common ground reference between input and output, there are just three distinct rails possible for the position of the inductor: the input, the output, and the ground rails.

Refer to the three basic switching topologies shown in Figure 6. When the inductor is at the output rail, the topology is a buck. When it is at the input rail, the topology is a boost. And when the inductor is at the ground rail, the topology is an inverting buck-boost.

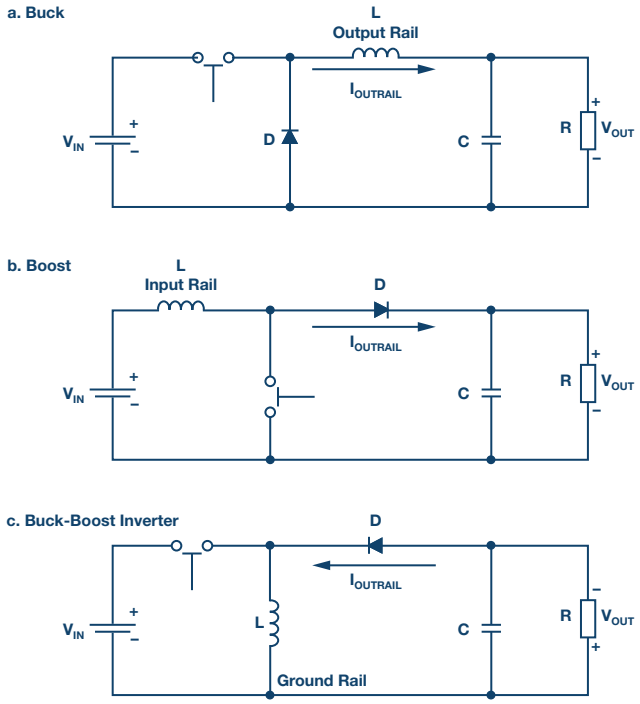


Figure 6. Basic switching topologies

During steady-state condition, the average current ($I_{OUTRAIL}$) on the output rail must be equal to the output current since the average current on the capacitor is zero. For a buck topology, $I_{L\text{-}AVE} = I_{OUT}$. However, for the boost and the inverting buck-boost topologies, $I_{D\text{-}AVE} = I_{OUT}$.

For boost and inverting buck-boost topologies, it is only during switch-off time that current flows through the diode. Therefore, $I_{D\text{-}AVE} = I_{L\text{-}AVE}$ during switch turn off. Refer to Figure 7 in deriving the average inductor current with respect to the output current. The rectangular area in green during switch-off time is the average diode current $I_{D\text{-}AVE}$, with height equal to $I_{L\text{-}AVE}$, and width equal to T_{OFF}. This current all goes to the output and, therefore, can be translated into a rectangular area averaged to a width of T and with height I_{OUT}.

$$I_{L\text{-}AVE} \times (T - T_{ON}) = I_{OUT} \times T$$
$$I_{L\text{-}AVE} = \frac{I_{OUT}}{(1-D)} \text{ where, } D = \frac{T_{ON}}{T} \quad (1)$$

Table 1. Average Inductor Current and Duty Cycle Inductor Current Peak

Topology	Inductor Current	Duty Cycle
Buck	$I_{L\text{-}AVE} = I_{OUT}$	$D = \frac{V_{OUT}}{V_{IN}}$
Boost	$I_{L\text{-}AVE} = \frac{I_{OUT}}{(1-D)}$	$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$
Buck-boost inverter		$D = \frac{\lvert V_{OUT}\rvert}{\lvert V_{OUT}\rvert + V_{IN}}$

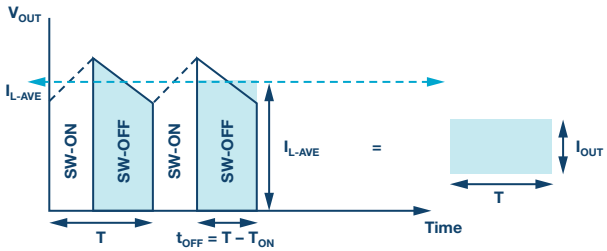


Figure 7. Diode current of boost or buck-boost inverter.

Table 1 shows a summary of the average inductor current $I_{L\text{-}AVE}$ and switching duty cycle D. Based on the equations, the inductor current will be at its maximum when the input voltage is at its minimum providing maximum duty cycle and when the output current is at its maximum.

Inductor Current Peak

Figure 8 shows inductor voltage and current waveforms of a buck-boost inverter in a steady-state condition in continuous conduction mode of operation. As to any switching topology, the amount of inductor current ripple (ΔI_L) can be derived according to the ideal inductor Equation 2.

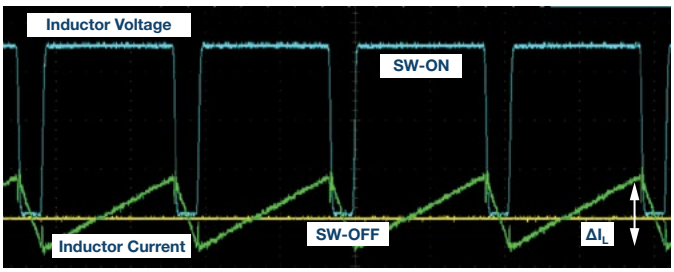


Figure 8. Swing of the inductor current.

$$V_L = L \times \frac{dI_L}{dt} \quad (2)$$

In switching converter applications where the inductor current is triangular and exhibits a constant rate of change, and therefore constant induced voltage, ($\Delta I_L/\Delta t$) can be used in the inductor equation, as found in the rearranged Equation 3. Inductor current ripple is determined by the applied voltseconds to the inductor and the inductance.

$$\Delta I_L = \frac{V_L \times \Delta t}{L} \quad (3)$$

Switch turn-on time can be easily related to duty cycle and switching frequency, as in Equation 4. It is therefore more convenient to use voltsecond products during switch turn-on than switch turn-off in the succeeding formula.

$$t_{ON} = \frac{t_{ON}}{T} \div \frac{1}{T} = \frac{D}{f_{SW}} \quad (4)$$

Table 2 shows a summary of the inductor current ripple in the three different topologies. The voltseconds product term t_{ON}, based on Equation 3, is replaced by Equation 4, and the term $V_{L\text{-}ON}$ is replaced by the induced voltage across the inductor according to topology.

Table 2. Inductor Current Ripple

Topology	Inductor Current Ripple
Buck	$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times fsw}$
Boost	$\Delta I_L = \frac{V_{IN} \times D}{L \times fsw}$
Buck-boost inverter	

Looking back at the steady-state inductor current in Figure 8, it will be observed that the inductor current average simply lies at the geometrical center of the ramp or the swinging of waveform at the point $\Delta I_L/2$. Therefore, the inductor current peak is the sum of inductor current average and half of the inductor current ripple, as shown in Equation 5.

$$I_{L-PK} = I_{L-AVE} + \frac{\Delta I_L}{2} \quad (5)$$

Capacitor Inrush Current

The charging current or displacement current equation of the capacitor is defined in Equation 6. It states that current flows through a capacitor in correspondence to a rate of change of voltage across it.

$$I_C = C \times \frac{dV_C}{dt} \quad (6)$$

The capacitor charging current should be considered when choosing output capacitor values for switching converters. At startup, assuming that the capacitor voltage is equal to zero or no capacitor charge, the output capacitor will begin to charge and draw as much current depending on the total capacitance and rate of change of the capacitor voltage, until the capacitor voltage reaches steady-state.

The rising of the output voltage in switching converters is a controlled ramp with constant slope so the rate of change equation can be simplified, as shown in Equation 7. Change in output voltage (ΔV) corresponds to the output voltage at steady-state and Δt corresponds to the time it takes for the output to reach its final value during startup, or what is commonly called soft start time.

$$I_{CAP} = C_{OUT} \times \frac{\Delta V}{\Delta t} = C_{OUT} \times \frac{V_{OUT}}{t_{SS}} \quad (7)$$

If there is too much output capacitance (C_{OUT}) or if the soft start time is small, the current demanded from the regulator I_{CAP} may be too high, which may cause problems with the converter operation. This large amount of current impulse is referred to as the inrush current. Figure 9 shows capacitor inrush current and output voltage during the startup of an inverting buck-boost converter with an output of 15 V, 10 µF output capacitor, and 4 ms soft start time.

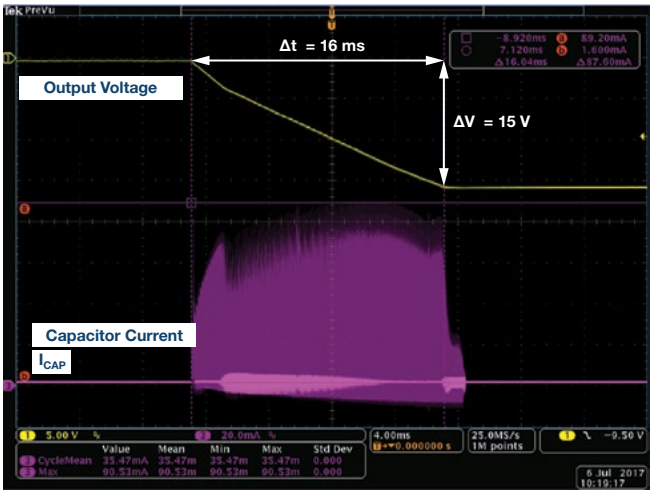


Figure 9. Output capacitor inrush current.

Inductor Current Peak at Startup

A simple boost converter circuit is shown on Figure 10. When the transistor switch is on close switch, current flows through the inductor while no current flows through the output rail. It is the discharging phase of C_{OUT} where the discharging current (I_{CAP}) goes to the output, while none goes through the reverse-biased diode. When the transistor's open switch is off, current I_D flows through the diode.

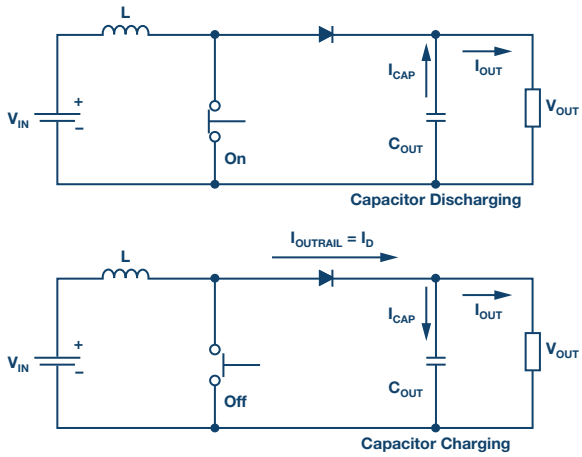


Figure 10. Boost dc-to-dc converter circuit.

By Kirchhoff's current law, the current through the output rail (I_D) must be equal to the sum of the current flowing through the output capacitor (I_{CAP}) and output load (I_{OUT}). This is described by Equation 8.

$$I_{OUTRAIL} = I_D = I_{CAP} + I_{OUT} \quad (8)$$

This equation applies during every charging phase or when voltage is rising across the capacitor. Therefore, it is also applicable during the startup of a switching converter when the initial state of the output capacitor is discharged or when the output voltage is not yet in the steady-state value.

The inductor current peak during startup can be defined using Equation 5 and includes the impact of inrush current due to output capacitor. Equation 8 will be applied into the $I_{L\text{-}AVE}$ equations in Table 1, replacing I_{OUT} with $I_{OUT} + I_{CAP}$. Inductor current peak equations during startup are summarized in Table 3.

Table 3. Inductor Current Peak at Startup

Topology	Inductor Current Peak
Buck	$I_{L-PK} = \left(C_{OUT} \times \frac{V_{OUT}}{t_{ss}}\right) + I_{OUT} + \frac{(V_{IN} - V_{OUT}) \times D}{2 \times L \times fsw}$
Boost	$I_{L-PK} = \frac{\left(C_{OUT} \times \frac{V_{OUT}}{t_{ss}}\right) + I_{OUT}}{(1-D)} + \frac{V_{IN} \times D}{2 \times L \times fsw}$
Buck-boost inverter	

For any of the three topologies, the inductor current peak is proportional to I_{OUT}. In terms of output current, the output capacitor must be designed at full load conditions.

Most applications require operation within a range of input voltage. So against input voltage, there is a difference between the buck and the other two topologies in terms of the magnitude of the dc and ac components voltage of the inductor current. This can be understood better through Figure 11. For the buck, as input voltage goes up, ac component voltage goes up. Average current is equal to output current, so the dc component voltage remains constant. Inductor current peak is therefore maximum at maximum input voltage.

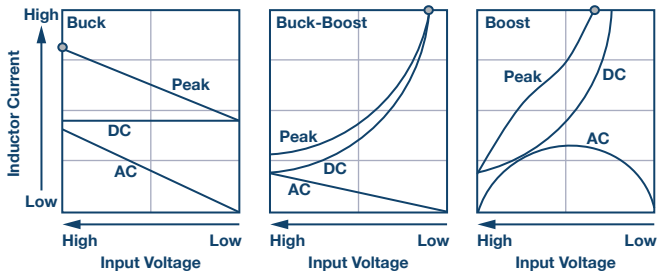


Figure 11. Inductor current against input voltage.

For the boost and buck-boost inverter, as input voltage goes up, ac component voltage goes up—but dc component voltage goes down because of the impact to the average current by the duty cycle, as shown in Table 1. The dc component voltage dominates, so the inductor peak current is at its maximum rating at minimum input voltage. In terms of input voltage, design of the output capacitor must be done at the maximum input voltage for buck and at minimum input voltage for boost and buck-boost inverter.

Mitigating Impact of Inrush

Output Capacitor Filter

As shown in previous sections, too much capacitance at the output causes high inrush current that may cause the inductor current peak to reach the current-limit threshold during startup. Therefore, the right amount of capacitance is necessary to achieve smallest output voltage ripple, while maintaining good converter start-up performance.

For buck converters, the relationship between C_{OUT} and the peak-to-peak voltage ripple is defined by Equation 9.

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUTripp_{pk-pk}}} \quad (9)$$

Where:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{f_{SW} \times L}$$

For boost and inverting buck-boost converters, the relationship between C_{OUT} and the peak-to-peak ripple is defined by Equation 10.

$$C_{OUT} = \frac{I_{OUT} \times D}{f_{SW} \times V_{OUTripp_{pk-pk}}} \quad (10)$$

Note that these equations neglect the effect of parasitic elements on the capacitors and inductors. These, in line with the rated specifications of the converter, can help the designer in limiting the capacitors added to the output. A good balance of filtering level and output inrush current are key considerations.

Second-Stage LC Filter

In certain cases, switching transients occur on the output voltage, as shown in Figure 12. If the magnitude is significant, it becomes an issue to the output load. The switching spikes are primarily caused by the switching transitions of the current on the output rail, which is the diode current for boost and buck-boost inverters. They can be magnified due to the stray inductance on the PCB copper traces. Because the spikes are in much higher frequency than the switching frequency of the converter, the peak-to-peak ripple cannot be reduced by the output filter capacitor alone—additional filtering is needed.

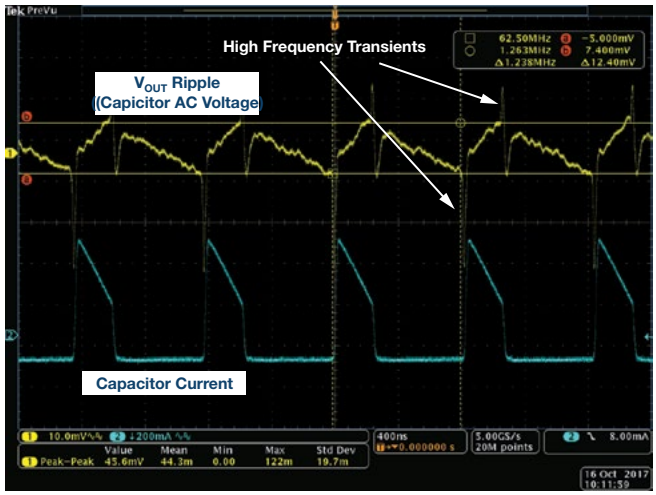


Figure 12. Output voltage ripple with switching transients.

Figure 12 shows the periodic switching action of the inductor in a boost converter represented by the blue trace, and the output voltage ripple represented by the yellow trace. High frequency transients are observed within the ripple voltage upon the switching transitions of the inductor current.

A great article on analog.com that provides more insight on how to reduce the high frequency transients by second-stage LC filtering is "Designing Second Stage Output Filters for Switching Power Supplies" by Kevin Tompsett.

Ripple Measurement

The right measurement method is also important when getting the output voltage ripple. Incorrect measurement setup can result in inaccurate and high voltage ripple readings, potentially leading to over-design of the output capacitor. It is easy to make the mistake of putting too much capacitance at the output in the hopes of reducing voltage ripple without realizing the tradeoffs.

An application note written by Aldrick Limjoco entitled "Measuring Output Ripple and Switching Transients in Switching Regulators" should be of help. See the references for details.

Soft Start Feature

For boost and inverting buck-boost, a bigger impact is dictated by the increase of the dc component voltage of the inductor current. At lower input voltage, the increase in the duty cycle causes a big increase in the inductor current average as shown in the (1-D) factor in equations in Table 3—this is also illustrated in Figure 11. This means that the inrush current of the output capacitor has to be significantly reduced. It is achieved by increasing the soft start time (t_{SS}) in Equation 7.

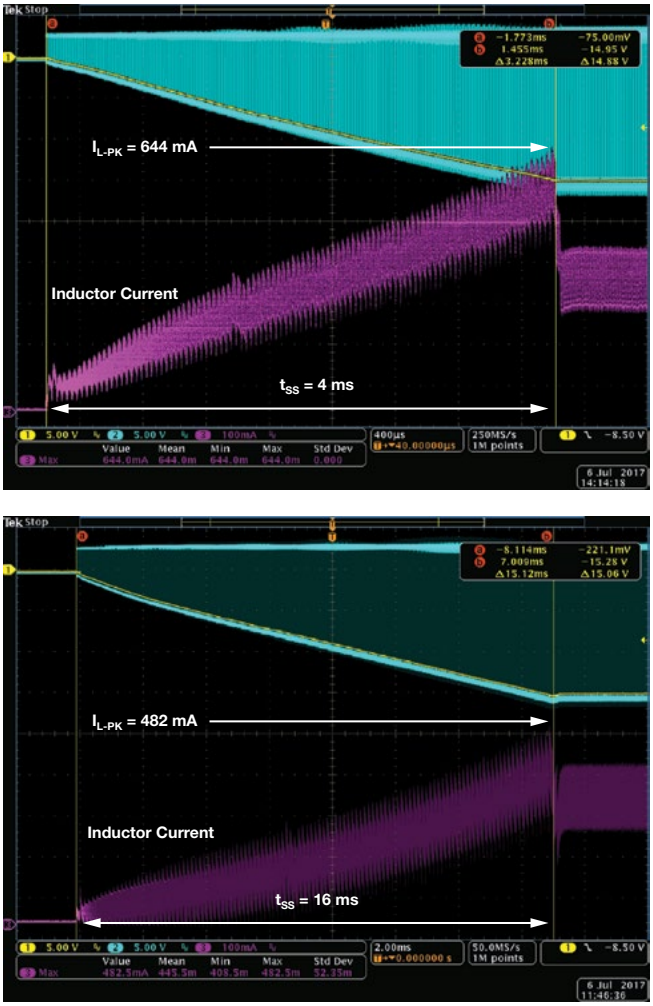


Figure 13. Inductor current vs. soft start time.

Most switching regulators (t_{SS}) have a soft start feature that refers to its capability, in order to give designers the option to adjust the rise time of output voltage during startup. Changing the value of a single resistor is often the convenient method of adjusting the soft start time. Figure 13 shows the start-up waveforms of a buck-boost inverter. A significant 25% decrease in inductor current peak can be seen by a change in soft start time from 4 ms to 16 ms.

Increasing the Switching Frequency

Figure 14 illustrates the impact to inductor current by change switching frequency (f_{SW}). Assuming that duty cycle D and output current are constant, the ac component voltage of the inductor current or $\Delta I_L/2$ is affected by change in f_{SW}, while the dc component voltage is not. Inductor current peak being inversely proportional is therefore lower at higher switching frequencies.

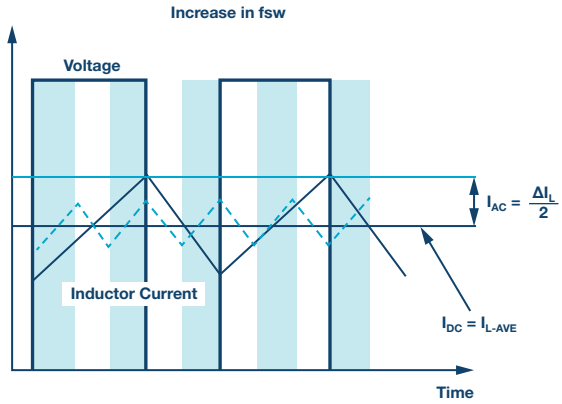


Figure 14. Factors affecting inductor current peak.

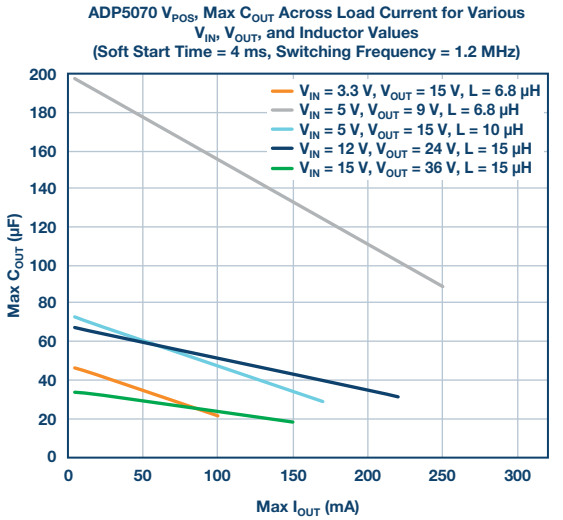
ADP5070: An Example

How Large Can the Output Capacitance Be?

ADP5070 is a monolithic, dual-boost and inverting buck-boost regulator with hiccup mode current-limiting scheme as the overcurrent protection. Some customers forgot to consider the trade-off of putting too much capacitance at the output, especially at high duty cycle operating condition or at the minimum input voltage. This usually has led to start-up issues at the inverting output, because the inverting buck-boost regulator is designed with lower current-limit threshold than the boost regulator.

Figure 15 can be used as an aid for application engineers as to how much capacitance is allowed at the output of ADP5070 to avoid start-up issues. Max C_{OUT} is shown vs. max I_{OUT} on different input and output voltage combinations, using the direct relationship of inductor peak current to output current, including inrush in Table 3's equation. It will help in the design limits of the output capacitor values after having considered the optimum V_{OUT} ripple performance using either Equation 9 or Equation 10.

Both graphs were computed based on the shortest t_{SS} and the current-limit threshold of the regulator. External components were chosen to be of much higher current handling capability than the regulator. In other words, the numbers in these graphs will definitely increase in magnitude if the t_{SS} were increased.



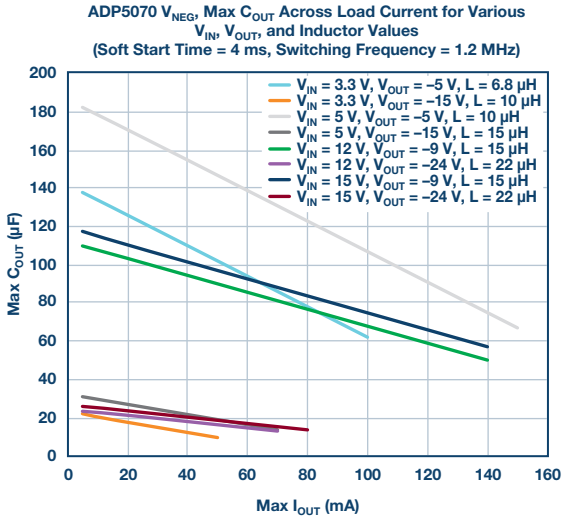


Figure 15. Maximum C_{OUT} vs. maximum load current.

For applications requiring higher output load current, ADP5071 should be considered. ADP5071 is designed with higher current-limit threshold than ADP5070 for both boost and inverting buck-boost regulators.

Computed vs. Measured Data

Figure 16 shows the start-up waveforms of the inductor induced voltage and current of the inverting regulator, while the data that follows in Figure 17 show the inductor current data both by computation using equation in Table 3 and measured bench data.

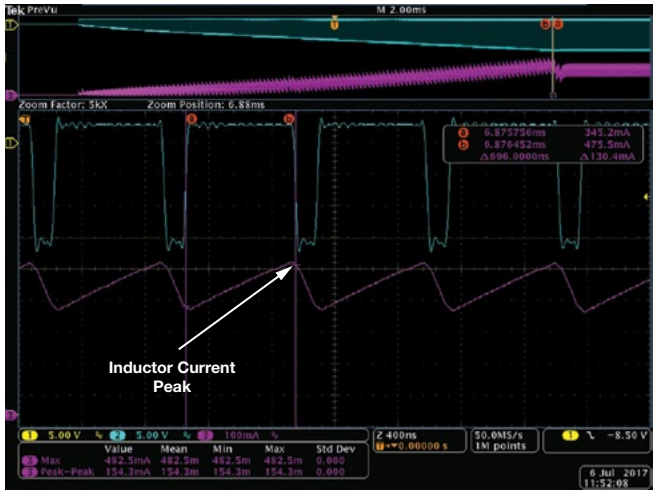


Figure 16. Inductor current and induced voltage at startup.

Input Parameters:

V_N =	3.3 V	V_{OUT} =	–15 V
f_{SW} =	1.2 MHz	I_{OUT} =	50 mA
L =	15 µH	V_{DIODE} =	0.5 V
		C_{OUT} =	10 µF

t_{SS} = 3.22ms

Data	DUTY (%)	I_{CAP} (mA)	I_{L-PK} (mA)	I_{L-PP} (mA)
Computed	82.4	46.6	625.8	151.2
Measured	84.1	46.8	644	161.4

t_{SS} = 15.14ms

Data	DUTY (%)	I_{CAP} (mA)	I_{L-PK} (mA)	I_{L-PP} (mA)
Computed	82.4	9.9	416.9	151.2
Measured	83.5	7.6	481.6	149.7

t_{SS} = 30.32ms

Data	DUTY (%)	I_{CAP} (mA)	I_{L-PK} (mA)	I_{L-PP} (mA)
Computed	82.4	4.9	388.6	151.2
Measured	84.3	5.2	465.6	147.4

Figure 17. Inductor current: Computed vs. measured.

The data proves that inrush current is greatly reduced if t_{SS} is increased, thereby lowering inductor peak current. At 4 ms t_{SS}, the inverting regulator is already hitting the current-limit threshold of 0.6 A and has a tendency of having start-up issues. The remedy is to increase t_{SS} to 16 ms to give enough inductor peak current margin.

Conclusion

This article has shown that careful design of the output filter capacitor is important in designing switching converters. Good knowledge of the factors influencing the inductor peak current during startup helps avoid start-up issues. Boost and inverting buck-boost converters are more prone to these issues, especially those using the hiccup mode current-limiting scheme.

A direct relationship between the inductor peak current and output inrush current has been provided. It will prove to be useful when designing the output capacitors while keeping track of the inductor peak current against current-limit threshold. For the same output conditions, output inrush current can be minimized by increasing the soft start time or the converter switching frequency.

This article acts as a reference material when designing a dc-to-dc switching converter using the ADP5070/ADP5071/ADP5073/ADP5074/ADP5075 series of monolithic switching regulators of Analog Devices.

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Ferrite Beads Demystified

Volume 50, Number 1

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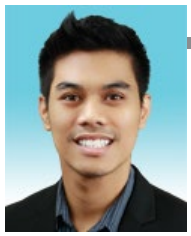

James Macasaet

MUSIC-Based Algorithm for On-Demand Heart Rate Estimation Using Photoplethysmographic (PPG) Signals on Wrist

By **Foroohar Foroozan**

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Imagine a world in the next few decades where your grandchildren didn't know about the word *hospital* and all your health information was recorded and monitored remotely through sensors. Imagine your home equipped with different sensors to measure air quality, temperature, noise, light, and air pressure, and, based on your personal health information, systems adjust the relevant environmental parameters to optimize your well-being at home. Analog Devices holds a unique position to make this happen by providing sensors, software, and algorithms that complement each other, which increases its share of the digital health market.

Heart rate (HR) monitoring is a key feature in many existing wearable and clinical devices. These devices generally measure photoplethysmography (PPG) signals, which are obtained by illuminating human skin using LEDs and measuring intensity changes due to blood flow in the reflected light by a photodiode. The PPG signal morphology is similar to the arterial blood pressure (ABP) waveform, which makes this signal popular within the scientific community as a potential noninvasive HR monitoring tool. The periodicity of the PPG signal corresponds to cardiac rhythm. Therefore, HR can be estimated from the PPG signals. However, the HR estimation performance can be degraded by poor blood perfusion, ambient light, and, most importantly, motion artifacts (MA).[1] Many signal processing techniques have been proposed to remove the MA noise, including the ADI motion rejection and frequency tracking algorithm, by using a 3-axis acceleration sensor placed close to the PPG sensor. When there is no motion, it is desirable to have an on-demand algorithm provide a fast and more accurate estimate of the HR to tracking algorithms. This article adapts the multiple signal classification (MUSIC) frequency estimation algorithm for high precision, on-demand HR estimation using the PPG signals from the wrist, using the ADI healthcare watch platform using the block diagram in Figure 1. The details of the figure will be explained in later sections.

What Does a PPG Signal from ADI's Healthcare Watch Look Like?

As light is emitted by the LED, blood levels and tissues absorb various amounts of photons, causing different detections sensed by the photodetector. The photodetector measures the variations in blood pulsations and outputs a current that is then amplified and filtered for further analysis.

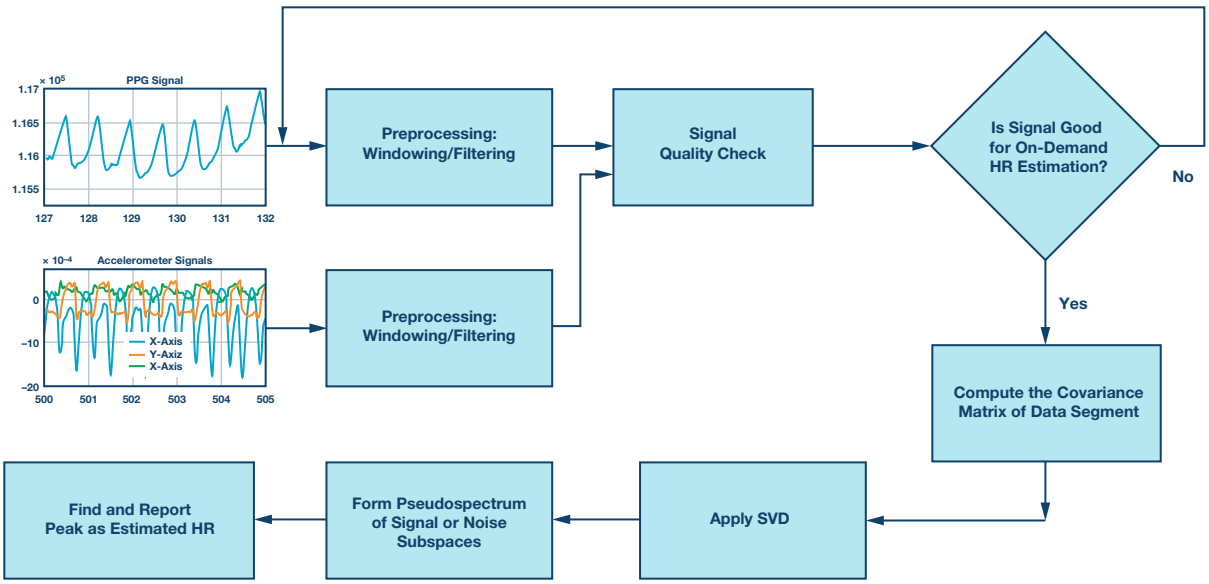

Figure 1. MUSIC-based on-demand HR estimation algorithm from PPG signals on wrist.

Figure 2a shows a general PPG signal consisting of alternating current (ac) and direct current (dc) components. The dc component of the PPG waveform detects the optical signal reflected from the tissue, bone, and muscle, and also the average blood volume of both arterial and venous blood. The ac component, on the other hand, demonstrates changes in the blood volume that occurs between the systolic and diastolic phases of the cardiac cycle, where the fundamental frequency of the ac component depends on the HR. Figure 2b is the PPG signal from the ADPD107 watch, which was introduced in previous *Analog Dialogue* articles. The goal of the ADI multisensory watch is to measure multiple vital signs on the human wrist. The ADI watch has PPG, an electrocardiogram (ECG), electrodermal activity (EDA), an accelerometer (ACC), and temperature sensors. This article focuses only on the PPG and ACC sensors.

Now let's have a close look into the similarity of the PPG and ABP waveforms. The ABP waveform is created due to the ejection of blood from the left ventricle. The main pressure travels down the systemic vascular network and reaches several sites, causing reflection due to significant changes in arterial resistance and compliance. The first site is the juncture between the thoracic and abdominal aorta, which causes the first reflection, commonly known as the late systolic wave. The second reflection site is the juncture between the abdominal aorta and common iliac arteries. The main wave is reflected back once again, which makes a small dip, called the dicrotic notch, which can be observed between the first and second reflections. There are other additional minor reflections, which are smoothed in the PPG signals.[2] The focus of this article is on the HR estimation, which only depends on the periodicity of the PPG signals and the exact morphology of the PPG is not taken into consideration for the purpose of this algorithm.

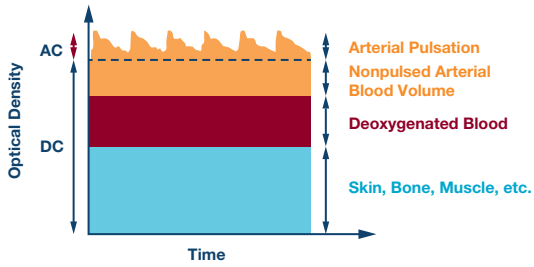

Figure 2a. Typical PPG signal with ac and dc parts.

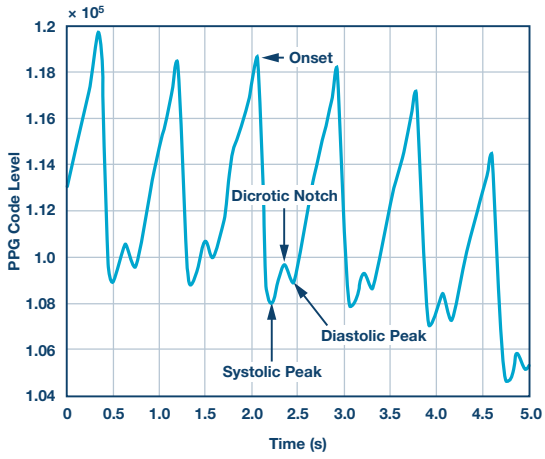

Figure 2b. ADI healthcare watch PPG signal.

Preprocessing of PPG Signals

The susceptibility of the PPG signal to poor blood perfusion of the peripheral tissues and motion artifact is well known.[1] In order to minimize the influence of these factors in the subsequent phases of the PPG analysis for HR estimation, a preprocessing stage is required. A band-pass filter is required to remove both high frequency component (such as power sources) of the PPG signals, as well as low frequency components, such as changes in capillary density and venous blood volume, temperature variations, and so on. Figure 3a shows a PPG signal after filtering. A set of signal quality metrics is used to find the first window of PPG signal appropriate for the on-demand algorithm. The first check involves the ACC data and the PPG signal to determine whether a segment of motion free data can be detected—then, the other signal quality metrics are measured. Estimates from such a window of data are rejected by the on-demand algorithm if there is motion above a certain threshold of the absolute value of the ACC data in three directions. The next signal quality check is based on certain autocorrelation having features of the data segment. One example of the autocorrelation of the filtered PPG signal is shown in Figure 3b. Autocorrelation of acceptable signal segments exhibits properties such as having at least one local peak and not more than a certain number of peaks corresponding to the highest possible HR; having the local peaks in a descending order with increasing lags; and a few others. Autocorrelation is only computed for lags that correspond to meaningful heart rates within a margin of range, from 30 bpm to 220 bpm.

When enough data segments pass the quality checks consecutively, the second stage of the algorithm extracts an accurate HR using the MUSIC-based algorithm.

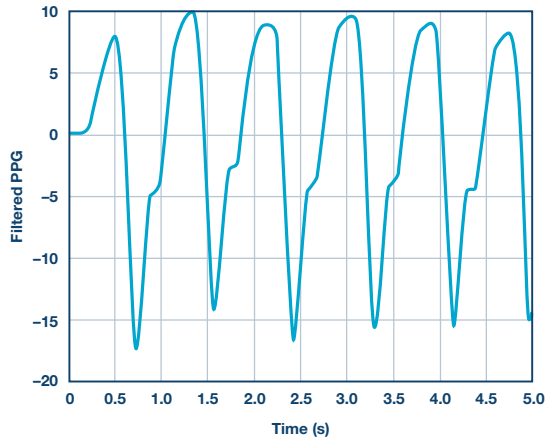

Figure 3a. Band-pass filtered PPG signal from Figure 1b.

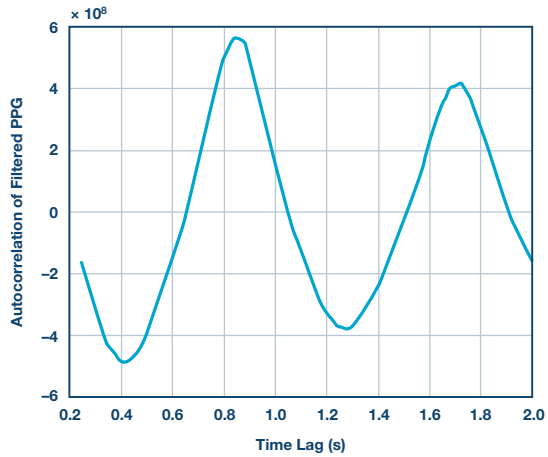

Figure 3b. Autocorrelation of the signal plot from Figure 2a.

MUSIC-Based Algorithm for On-Demand HR Estimation

MUSIC is a subspace-based method using a model of harmonic signals that can estimate frequency with high precision.[3] When it comes to the PPG signals corrupted with noise, Fourier transform (FT) may not behave well, as we are seeking a high resolution HR estimation algorithm. Also, FT distributes time-domain noise uniformly throughout the frequency domain, limiting the certainty of estimation. It is difficult to observe a small peak in the vicinity of a large peak using FT.[4] Therefore, in this study, we used the MUSIC-based algorithm for frequency estimation of the HR. The key idea behind MUSIC is that the noise subspace is orthogonal to the signal subspace, so zeroes of the noise subspace will indicate signal frequencies. The following steps show a summary of this algorithm used for the HR estimation:

- Remove the mean and linear trend from the data
- Compute the covariance matrix of the data
- Apply the singular value decomposition (SVD) to the covariance matrix
- Compute the signal subspace order
- Form the pseudospectrum of the signal or noise subspaces
- Find the peaks of the MUSIC pseudospectrum as the HR estimate

MUSIC has to apply a singular value decomposition and has to search spectral peaks in the full range of frequencies. Let's look at some math in order to make the above steps more clear. Assume a window of length m of the filtered PPG signal, which is denoted as $\boldsymbol{x}_m$ and $m \leq L$ (with L being the total samples of the filtered PPG signal in a given window). Then, the first step is to form the sample covariance matrix as follows:

$$\hat{R} = \frac{1}{L-M} \sum_{m=1}^{M} x_m x_m^T$$

Then, an SVD is applied to the sample covariance matrix as given below:

$$\hat{R} = U \Lambda V = U_s \Lambda U_s^T + U_n \Lambda U_n^T$$

where U is the left eigenvectors, Λ is the diagonal matrix of the eigenvalues, and V is the right eigenvectors of the covariance matrix. The subscripts s and n stand for the signal and noise subspaces. As we mentioned before, the MUSIC-based algorithm is modified for HR estimation using prior knowledge that the signal has passed the signal quality checking stage—so the only frequency content in the signal after the preprocessing step is the HR frequency. Next, we form the signal and noise subspaces, assuming the model order only contains one single tone, as follows:

$$U_s = U(1{:}\, p, :);\ U_n = U(p+1{:}\, end, :)$$

where $p = 2$ is the model number. The frequencies within the meaningful HR limits are considered only. This reduces the computations significantly and makes it feasible for real-time implementation for embedded algorithms. The search frequency vector is defined as:

$$a(k) = [1, e^{-1 \times \frac{2\pi j(k-1)}{L}}, e^{-2 \times \frac{2\pi j(k-1)}{L}}, e^{-3 \times \frac{2\pi j(k-1)}{L}}, \ldots$$

$$e^{-(m-1) \times \frac{2\pi j(k-1)}{L}}]\hat{}T$$

where k is the frequency bin within the frequency range of interest for HR, and L is the window length for the data in $\boldsymbol{x}_m(t)$. Then, the following pseudospectrum takes the noise subspace eigenvectors to find the peaks of the MUSIC as follows.

$$\Phi(k) = \frac{1}{a^H U_n U_n^H a}$$

The word pseudospectrum is used here because it indicates the presence of sinusoidal components in the studied signal, but it is not a true power spectral density. One sample result of the MUSIC-based algorithm on a 5 second window of data is given in Figure 4, which shows a sharp peak at 1.96 Hz, and which translates to 117.6 bpm HR.

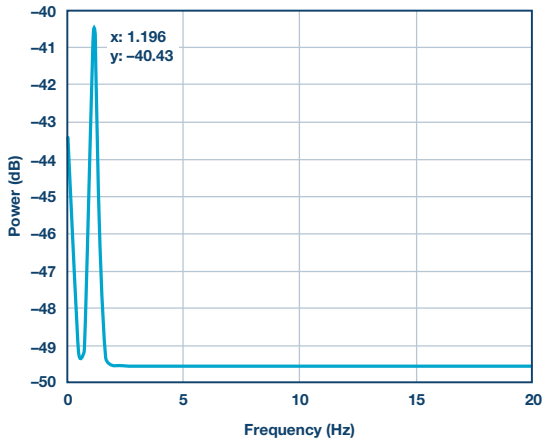

Figure 4. One sample of MUSIC-based estimation from the PPG data.

Results of the MUSIC-Based On-Demand Algorithm for HR Estimation

We have tested the performance of this algorithm on a dataset comprising of 1289 test cases (data1) and at the beginning of the data the test subjects are asked to stand at rest. Table 1 illustrates the result of the MUSIC-based algorithm and indicates if the estimated HR is within 2 bpm and 5 bpm of the reference (ECG), as well as the 50th percentile (median) and 75th percentile of the estimation times. The second row of Table 1 shows the performance of the algorithm when there is periodic motion (such as walking, jogging, running) over a dataset of 298 test cases (data2). The algorithm is considered to be successful if either the data is rejected as unreliable by sensing the motion or by accurately estimating the HR despite the motion. In terms of memory usage, assuming a buffer size of 500 (that is, 5 sec at 100 Hz), the total memory needed is around 3.4 kB with 2.83 cycle per call for the frequency range of interest (30 bpm to 220 bpm).

Table 1. Performance Numbers for the MUSIC-Based On-Demand HR Algorithm

Metric	2 bpm Accuracy	5 bpm Accuracy	50th Percentile	75th Percentile
Accuracy (data1)	93.7%	95.2%	5.00 sec	5.00 sec
Accuracy (data2)	93.4%	94.1%	5.00 sec	5.00 sec

Final Discussion

The MUSIC-based on-demand algorithm is one of the many algorithms proposed in the vital signs monitoring segment of the ADI healthcare business unit. The on-demand algorithm used in our healthcare watch is a different algorithm than the MUSIC-based method discussed here, because it is less computationally expensive. ADI delivers software and algorithm capabilities at both sensor (embedded) and edge nodes that distill data to extract valuable information by sending only the most important data to the cloud and allowing local decision making for our customers and partners. We choose applications where outcomes really matter for our customers and where we have unique measurement expertise. This article just provides a flavor of the algorithms we are working on at ADI. With our existing expertise in sensor design, and our efforts in biomedical algorithm development (both embedded and cloud), ADI will have a unique position to provide state-of-the-art algorithms and software to the global healthcare market.

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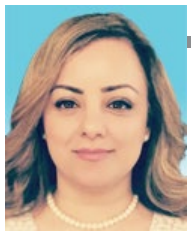

Foroohar Foroozan

Low EMI/EMC Emission Switching Converter Eases ADAS Designs

By **Tony Armstrong**

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Background

ADAS is an acronym for advanced driver assistance system, which is commonly found in many of today's new automobiles and trucks. These systems usually facilitate safe driving and can provide the driver with an alert if the system detects risks from surrounding objects such as errant pedestrians, cyclists, or even other vehicles on an unsafe trajectory! Furthermore, these systems typically provide dynamic features such as adaptive cruise control, blind spot detection, lane departure warning, driver drowsiness monitoring, automatic braking, traction control, and night vision. As a result, the increasing focus of consumers on safety, demands for comfort while driving, and the continued increase of government safety regulations are the main growth drivers of ADAS in automobiles for the latter half of this decade.

This growth does not come without challenges for the industry, which include pricing pressure, inflation, complexity, and difficulty in testing these systems. Moreover, it should come as no surprise that the European automotive industry is one of the most innovative automotive markets, and, as such, it has seen major market penetration and adoption of ADAS from its customers. Nevertheless, both the American and Japanese automotive makers are not far behind. The ultimate goal is an autonomous driving machine without the need for a human being behind the wheel!

System Challenges

Generally speaking, an ADAS incorporates some kind of microprocessor to gather all of the input from the numerous sensors within the vehicle and then processes them so that they can be easily presented to the driver in a way that it can be easily understood. Moreover, these systems are usually powered directly from the vehicle's main battery, which is a nominal 9 V to 18 V in a car, but could be as high as 42 V due to voltage transients within the system, and as low as 3.4 V during a cold-crank condition. Therefore, any dc-to-dc converters within these systems must be able to handle the wide input voltage range of 3.4 V to 42 V at a minimum. Furthermore, many dual battery systems, such as those commonly found in trucks, require an even broader input range, pushing the upper limit as high as 65 V. As a result, some ADAS manufacturers design their systems to cover a 3.4 V to 65 V input range so that they can be used in either cars or trucks; while gaining economies of scale during the manufacturing process.

Many ADASs use a 5 V and 3.3 V rail to power their various analog and digital IC content; correspondingly, the manufacturers of such systems prefer to use a single converter to address both the single and double battery configurations simultaneously. Furthermore, the system is usually mounted in a part of the vehicle that is both space and thermally constrained, thereby limiting the heat sinking available for cooling purposes. While it is commonplace to use a high voltage dc-to-dc converter to generate a 5 V and 3.3 V rail directly from the battery, in today's ADASs a switching regulator must also switch at 2 MHz or greater, rather than the historical switching frequency of sub-500 kHz. The key driving force behind this change is the need for smaller solution footprints while also staying above the AM frequency band to avoid any potential interference.

Furthermore, as if the designers' task is not already complicated enough, they must also ensure that the ADAS complies with the various noise immunity standards within the vehicle. In an automotive environment, switching regulators are replacing linear regulators in areas where low heat dissipation and efficiency are valued. Moreover, the switching regulator is typically the first active component on the input power bus line, and therefore has a significant impact on the EMI performance of the complete converter circuit.

There are two types of EMI emissions: conducted and radiated. Conducted emissions ride on the wires and traces that connect up to a product. Since the noise is localized to a specific terminal or connector in the design, compliance with conducted emissions requirements can often be assured relatively early in the development process with a good layout or filter design.

However, radiated emissions are another story altogether. Everything on the board that carries current radiates an electromagnetic field. Every trace on the board is an antenna and every copper plane is a resonator. Anything, other than a pure sine wave or dc voltage, generates noise all over the signal spectrum. Even with careful design, a power supply designer never really knows how bad the radiated emissions are going to be until the system gets tested—and radiated emissions testing cannot be formally performed until the design is essentially complete.

Filters are often used to reduce EMI by attenuating the strength at a certain frequency or over a range of frequencies. A portion of this energy that travels through space (radiated) is attenuated by adding metallic and

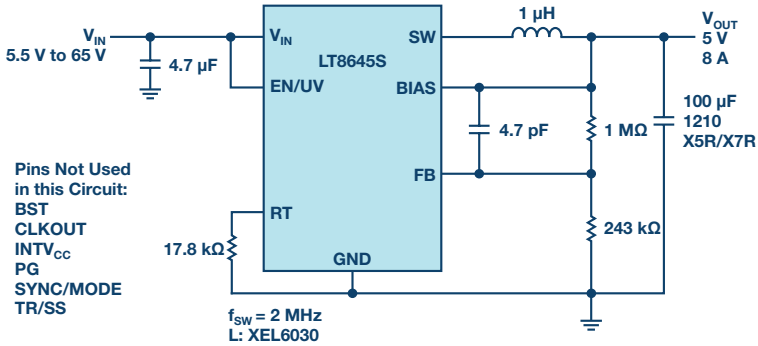

Figure 1. LT8645S schematic delivering 5 V at 8 A output at 2 MHz.

magnetic shields. The part that rides on PCB traces (conducted) is tamed by adding ferrite beads and other filters. EMI cannot be eliminated but can be attenuated to a level that is acceptable by other communication and digital components. Moreover, several regulatory bodies enforce standards to ensure compliance.

Modern input filter components in surface-mount technology have better performance than throughhole parts. However, this improvement is outpaced by the increase in operating switching frequencies of switching regulators. Higher efficiency, low minimum on- and off-times result in higher harmonic content due to the faster switch transitions. For every doubling in switching frequency, the EMI becomes 6 dB worse while all other parameters, such as switch capacity and transition times, remain constant. The wideband EMI behaves like a first-order, high-pass filter with 20 dB higher emissions if the switching frequency increases by 10 times.

Savvy PCB designers will make the hot loops small and use shielding ground layers as close to the active layer as possible. Nevertheless, device pinouts, package construction, thermal design requirements, and package sizes needed for adequate energy storage in decoupling components dictate a minimum hot loop size. To further complicate matters, in typical planar printed circuit boards, the magnetic or transformer style coupling between traces above 30 MHz will diminish all filter efforts since the higher the harmonic frequencies, the more effective unwanted magnetic coupling becomes.

High Voltage DC-to-DC Converter with Low EMI Emissions

It was because of the previously described application constraints that Analog Devices' Power by Linear™ Group developed the LT8645S—a high input voltage capable, monolithic, synchronous buck converter that also has low EMI emissions. Its 3.4 V to 65 V input voltage range makes it ideal for both automotive and truck applications, including ADAS, which must regulate through cold-crank and stop-start scenarios with minimum input voltages as low as 3.4 V and load dump transients more than 60 V. As seen in Figure 1, the device is a single-channel design delivering an 8 A output at 5 V. Its synchronous rectification topology delivers up to 94% efficiency at a switching frequency of 2 MHz, while Burst Mode® operation keeps quiescent current under 2.5 µA in no-load standby conditions, making it ideal for always on systems.

The LT8645S's switching frequency can be programmed from 200 kHz to 2.2 MHz and synchronized throughout this range. Its unique Silent Switcher® 2 architecture integrates internal input capacitors, as well as internal BST and $INTV_{CC}$ capacitors to reduce the solution footprint. Combined with very well controlled switching edges and an internal construction with an integral ground plane and the use of copper pillars in lieu of bond wires, the LT8645S's design dramatically reduces EMI emissions. Furthermore, its Silent Switcher 2 design also provides robust EMI performance on any printed circuit board (PCB), including 2-layer PCBs. Moreover, it is much less sensitive to the PCB layout when compared to other comparable converters. This new level of performance is due to the LT8645S's internal, dual-input, BST and $INTV_{CC}$ capacitors that minimize the area of the hot loops. It still requires dual external input capacitors, but the requirement of placing them as close to the input pins is greatly relaxed. Combined with the internal capacitors minimizing the area of the hot loops, the BT substrate's integrated ground plane significantly improves EMI performance (see Figure 2). The multilayer BT substrate also enables the I/O pins to use the exact same pattern as a QFN package, while enabling large grounded thermal pads. This laminate-based QFN (LQFN) package is more pliable and flexible than the standard QFN and has demonstrated much better performance in solder joint reliability during board level temperature cycle, allowing customers to use LQFN where previously they could only use leaded parts.

The LT8645S can easily pass the automotive CISPR25, Class 5 peak EMI limits over its entire load range. Spread spectrum frequency modulation is also available to lower EMI levels further (Figure 2). The LT8645S utilizes internal top and bottom high efficiency power switches with the necessary boost diode, oscillator, and control and logic circuitry integrated into a single die. Low ripple Burst Mode operation maintains high efficiency at low output currents while keeping output ripple below 10 mV p-p. Finally, the LT8645S is packaged in a small thermally enhanced 4 mm × 6 mm, 32-lead LQFN package.

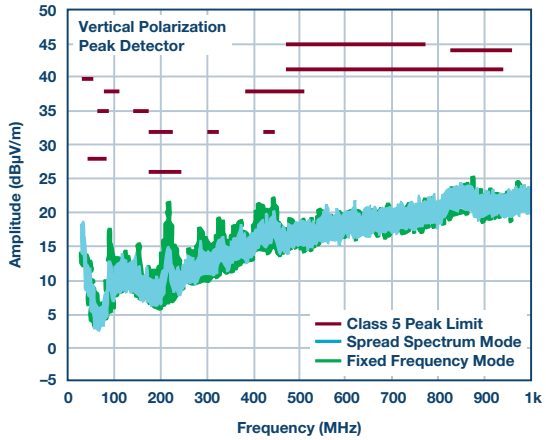

Figure 2. LT8640S radiated EMI performance graph.

Conclusion

The proliferation of ADASs in cars and trucks is not going to end anytime soon. It is also clear that finding the right power conversion device that meets all the necessary performance metrics so as not to interfere with the ADAS is not a simple task. Fortunately, the designers of these automotive systems can now have the high performance capabilities afforded by the Silent Switcher 2 dc-to-dc converters from Analog Devices. Not only do they greatly simplify power designers' tasks, they simultaneously deliver all the performance needed without requiring sophisticated layout or design techniques.

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Tony Armstrong

Also by this Author:

Maximize the Run Time in Automotive Battery Stacks Even as Cells Age

Volume 51, Number 4

Rarely Asked Questions—Issue 149 Intermediate Voltage to Increase Power Conversion Efficiency

By **Frederik Dostal**

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Question:

How do you increase the efficiency of a power converter with high voltage input and low voltage output?

Answer:

There are different solutions for applications that require conversion from a high input voltage down to a very low output voltage. One interesting example is the conversion from 48 V down to 3.3 V. Such a specification is not only common in server applications for the information technology market, but in telecommunications as well.

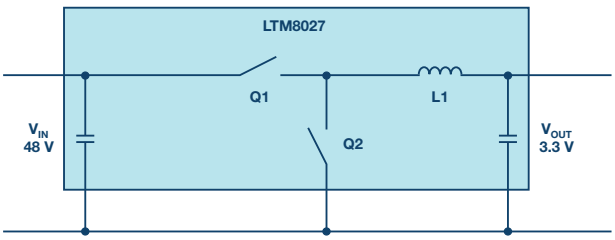

Figure 1. Conversion of a voltage from 48 V down to 3.3 V in one single conversion step.

If a step-down converter (buck) is used for this single conversion step, as shown in Figure 1, the problem of small duty cycles emerges. The duty cycle is the relationship between the on-time (when the main switch is turned on) and the off-time (when the main switch is turned off). A buck converter has a duty cycle, which is defined by the following formula:

$$Duty\ Cycle = \frac{Output\ Voltage}{Input\ Voltage}$$

With an input voltage of 48 V and an output voltage of 3.3 V, the duty cycle is approximately 7%.

This means that at a switching frequency of 1 MHz (1000 ns per switching period), the Q1 switch is turned on for only 70 ns. Then, the Q1 switch is turned off for 930 ns and Q2 is turned on. For such a circuit, a switching regulator has to be chosen that allows for a minimum on-time of 70 ns or less. If such a component is selected, there is another challenge. Usually the very high power conversion efficiency of a buck regulator is reduced when operating at very short duty cycles. This is because there is only a very short time available to store energy in the inductor. The inductor needs to provide power for a long period during the off-time. This typically leads to very high peak currents in the circuit. To lower these currents, the inductance of L1 needs to be relatively large. This is due to the fact that during the on-time, a large voltage difference is applied across L1 in Figure 1.

In the example, we see about 44.7 V across the inductor during the on-time, 48 V on the switch-node side, and 3.3 V on the output side. The inductor current is calculated by the following formula:

$$i_L = \frac{1}{L}\int u_L dt$$

If there is a high voltage across the inductor, the current rises during a fixed time period and at a fixed inductance. To reduce inductor peak currents, a higher inductance value needs to be selected. However, a higher value inductor adds to increased power losses. Under these voltage conditions, an efficient LTM8027 µModule® regulator from Analog Devices achieves power efficiency of only 80% at 4 A output current.

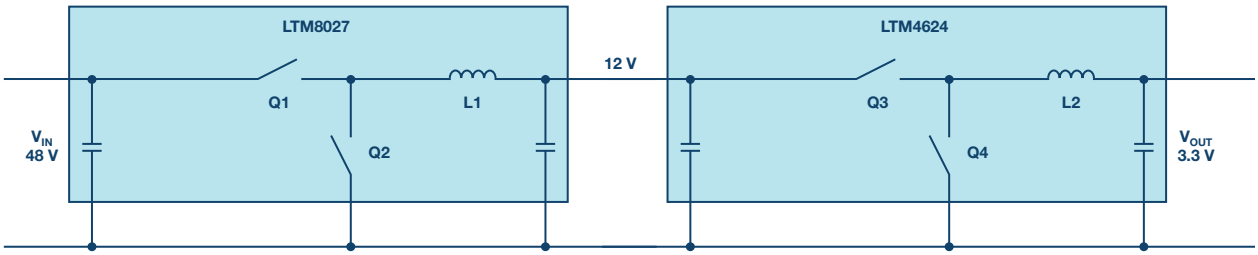

Figure 2. Voltage conversion from 48 V down to 3.3 V in two steps, including a 12 V intermediate voltage.

Today, a very common and more efficient circuit solution to increase the power efficiency is the generation of an intermediate voltage. A cascaded setup with two highly efficient step-down (buck) regulators is shown in Figure 2. In the first step, the voltage of 48 V is converted to 12 V. This voltage is then converted down to 3.3 V in a second conversion step. The LTM8027 µModule regulator has a total conversion efficiency of more than 92% when going from 48 V down to 12 V. The second conversion step from 12 V down to 3.3 V, performed with a LTM4624, has a conversion efficiency of 90%. This yields a total power conversion efficiency of 83%. This is 3% higher than the direct conversion in Figure 1.

This can be quite surprising since all the power on the 3.3 V output needed to run through two individual switching regulator circuits. The efficiency of the circuit in Figure 1 is lower due to the short duty cycle and the resulting high inductor peak currents.

When comparing single step down architectures with intermediate bus architectures, there are many more aspects to consider besides power efficiency. However, this article is only intended to look at the important aspects of power conversion efficiency. One other solution to this basic problem is the new LTC7821, hybrid step-down controller. It combines charge pump action with a step-down buck regulation. This enables the duty cycle to be $2\times V_{IN}/V_{OUT}$ and, thus, very high step down ratios can be achieved at very high power conversion efficiencies.

The generation of an intermediate voltage can be quite useful to increase the total conversion efficiency of a specific power supply. A lot of development is being done to increase the conversion efficiency in Figure 1 with such short duty cycles. For example, very fast GaN switches can be used, which reduce the switching losses and, as a result, increase the power conversion efficiency. However, such solutions are currently more costly than a cascaded solution, such as in Figure 2.

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Frederik Dostal

Also by this Author:

Synchronous Rectification on the Secondary Side

Volume 51, Number 4

How to Improve the Accuracy of Inclination Measurement Using an Accelerometer

By **Allen Fan**

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Typical Application of Tilt Measurement

This article discusses how to improve tilt measurement accuracy using an accelerometer like a combo part. Electric park brakes (EPBs) are used on passenger vehicles to hold the vehicle stationary on graded and flat roads. This is accomplished by measuring the inclination using a single-axis or dual-axis accelerometer. Typically, an X-/Y- or Z-axis low-*g* accelerometer is placed in a dedicated module of an EPB control unit. Now, more and more vehicles have ESC (electronic stability control) function with a combined low-*g* accelerometer and gyroscope in a single chip. This is done to prevent the vehicle from side slipping and rolling over, and now ESC function is demanded world-wide through legislation. If tilt measurement is accomplished by a combo part (single-chip, combined accelerometer and gyroscope), then it is not necessary to have a standalone EPB module on the vehicle, which would significantly reduce the cost of the car. Because a combo part is typically used for ESC it's not optimized for tilt sensing, and sometimes, the accuracy of the tilt measurement by a combo part could not meet the accuracy requirement. Because a combo is XY-axis or XYZ-axis, it typically uses the X-axis for tilt measurement and some of the traditional low-*g* accelerometers in EPB modules use the z-axis, because it's installed vertically in the engine compartment. The sensing axis should be placed perpendicular to gravity to achieve better accuracy—this will be discussed later.

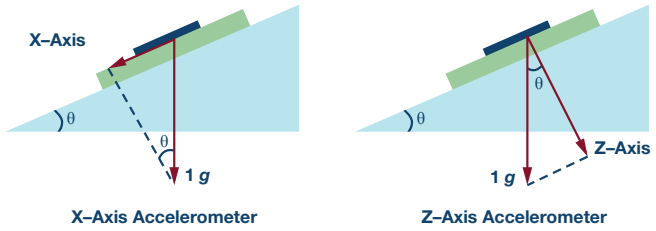

Figure 1. Installation illustration of X-axis and Z-axis accelerometer.

For tilt measurement on a vehicle, it's very important to evaluate the accuracy. Imagine that your car is parking on absolutely flat ground, so the angle calculated by the accelerometer should be 0°. If your car is parking on a ramp, the inclination should be accurately detected so that the braking system would be actuated correctly.

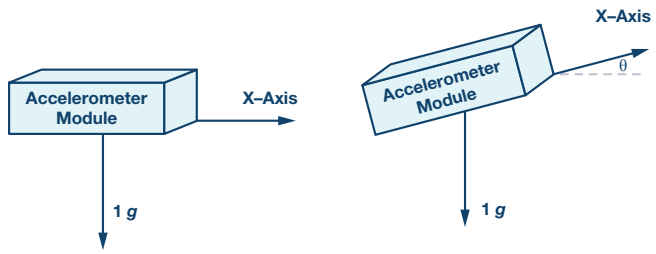

Figure 2. X-axis sensing tilt measurement illustration.

$$A_{OUT} = 1\ g \times \sin\theta$$

So

$$\theta = \sin^{-1}(A_{OUT}/g)$$

Where:

A_{OUT} is the output of the accelerometer in *g*.

θ is the inclination of the ramp in degrees.

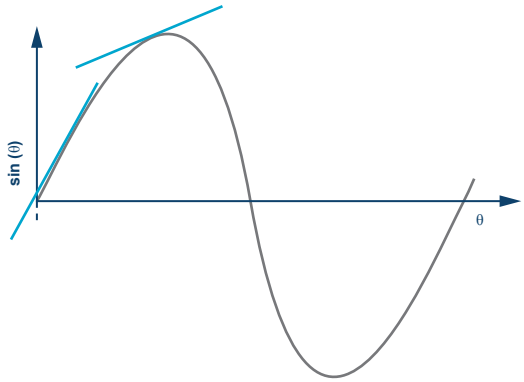

Figure 3. Sensitivity of sin θ to θ degrades as θ increases.

Because sin θ is a nonlinear function, the relationship between A_{OUT} and θ is nonlinear and it has the best linearity near zero, which means it has the best measuring accuracy. As θ increases, the measuring accuracy degrades. That's why the sensing axis should be placed perpendicular to gravity, because the road slope grade will be close to zero.

For tilt measurement on a vehicle, it's not necessary to consider the system with full ramp slope. The vast majority of ramp slope on the road in the real world would not exceed 30°. We only have to analyze the accuracy of contributions within the range of ±30°.

There are several contributions that would affect system-level measurement accuracy:

- Sensitivity error and initial absolute offset
- Nonlinearity
- Total offset variation from initial absolute offset
- Noise

Sensitivity Error and Initial Absolute Offset

Sensitivity Error

Sensitivity is the slope of the transfer function measured of inputs-outputs, usually at +1 *g* and –1 *g*. Sensitivity error is the part to part deviation of sensitivity. For example, some accelerometers' maximum sensitivity is 3%.

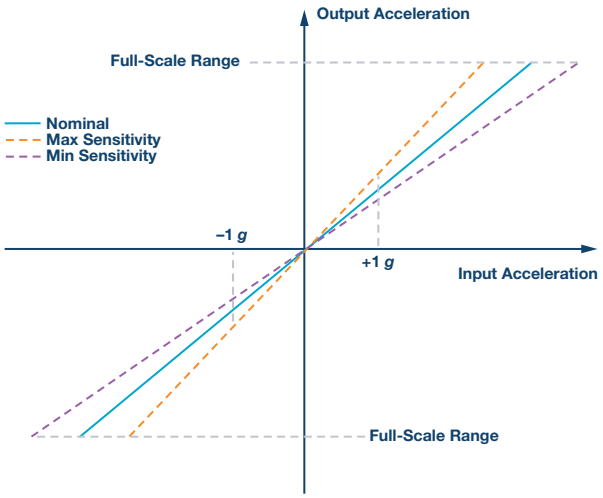

Figure 4. Sensitivity error of input-output acceleration.

Initial Absolute Offset

The offset within the range is around 25°C; for example, 25°C ± 5°C, measured immediately after completion of the module's manufacture. The initial absolute offset denotes the standard deviation of the measured offset values across a large population of devices.

Two-Point Calibration

For tilt measuring applications, the two main errors come from offset error and sensitivity error. These two errors lead to an unacceptable sensing result, so they should not be neglected. If we want to remove these two parts of error, the output of acceleration should be calibrated. Typically, there is a one-time calibration for offset and sensitivity of tilt measurement. If the offset and sensitivity error is considered, the relationship of input vs. output of the accelerometer is:

$$A_{OUTPUT} = A_{OFFSET} + Gain \times A_{ACTUAL}$$

Where:

A_{OUTPUT} is the offset error in *g*.

Gain is the gain of the accelerometer, the ideal value is 1.

A_{ACTUAL} is the real acceleration applied on the accelerometer in *g*.

There are two basic calibration techniques; one is single-point calibration. This calibration is done by applying a 0 *g* field on the accelerometer and then measuring the output. This kind of calibration could just be used for calibrating offset error and gain error could not be calibrated. Then, the resulting output in a 0 *g* field is subtracted from the real output value to remove the offset error. This is an easy method for calibration, but not for accuracy, because there's still sensitivity error. Another way is 1 *g* flip calibration, which would use two-point calibration at +1 *g* and –1 *g*, and in each field of +1 *g* and –1 *g* measure the acceleration output as below:

$$A_{+1\,g} = A_{OFFSET} + Gain \times A_{ACTUAL}$$
$$A_{-1\,g} = A_{OFFSET} - Gain \times A_{ACTUAL}$$

where the offset, A_{OFFSET}, is in *g*.

From this two-point information, offset and gain could be resolved as follows:

$$A_{OFFSET} = 0.5 \times (A_{+1\,g} + A_{-1\,g})$$
$$Gain = 0.5 \times \frac{A_{+1\,g} - A_{-1\,g}}{2}$$

Where the +1 *g* and –1 *g* measurements, $A_{+1\,g}$ and $A_{-1\,g}$, are in *g*.

After this one-time calibration, the actual acceleration could be calculated by following this equation, each time removing the offset and sensitivity error.

$$A_{ACTUAL} = \frac{A_{OUT} - A_{OFFSET}}{Gain}$$

Where A_{OFFSET} and A_{OUT} are in *g*.

Nonlinearity

The nonlinearity of the device is the maximum deviation of the measured acceleration (A_{MEA}) and the ideal linear output acceleration (A_{FIT}). The dataset of the acceleration measurement should include the full-scale range of the accelerometer. It's measured as $Max(|A_{MEA} - A_{FIT}|)$.

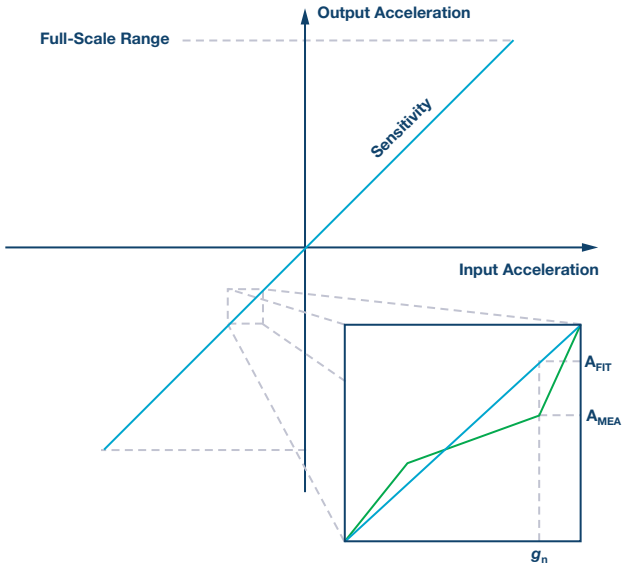

Figure 5. Nonlinearity of the device.

Where:

A_{MEA} is measured acceleration at a defined g_n.
A_{FIT} is predicted acceleration at a defined g_n.

Most accelerometer or combo parts have nonlinearity over a given input accelerometer range—for example, a range of 30 m*g* ± 2 *g*. For tilt measurement applications, the input ramp slope is within ±30°, which means the output acceleration range is within ±500 m*g* (±1 *g* × sin 30°), so the nonlinearity within this range should be reassessed. Because the nonlinearity is not linear across the whole input range, it's difficult to evaluate this part of error accurately and quantitatively. However, because the data sheet for this part is usually very conservative for a nonlinearity of 30 m*g* with an input range of ±2 *g*, it would be more reasonable to use 10 m*g* for the error calculation within ±500 m*g*.

Total Offset Variation from Initial Absolute Offset

Total offset variation from initial absolute offset is the maximum deviation of the offset as induced by temperature, stress, and aging effects. This deviation is measured relative to the initial absolute offset for a given device. This is the main contribution to the total error of accuracy.

Among all these factors like temperature, stress, aging, etc., variation vs. temperature accounts for the major percentage of total offset variation. Typically, the variation vs. temperature curve is a second-order curve, which is typically a rotated parabola. In order to eliminate this part of error, a three-point calibration at the system level could be performed. For a given device, the output variation drift vs. temperature could be calibrated as following steps.

Step 1:

The output response of the device is shifted by some value ΔN_0. The first step in the temperature calibration process is to cancel out the offset at ambient.

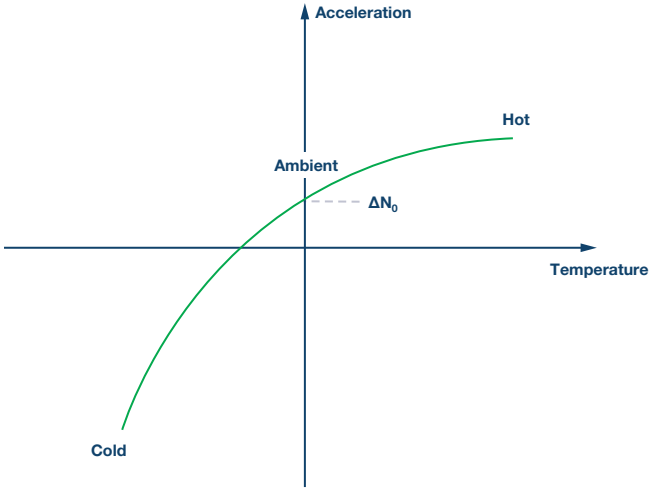

Figure 6. Step 1: cancel out the offset at ambient.

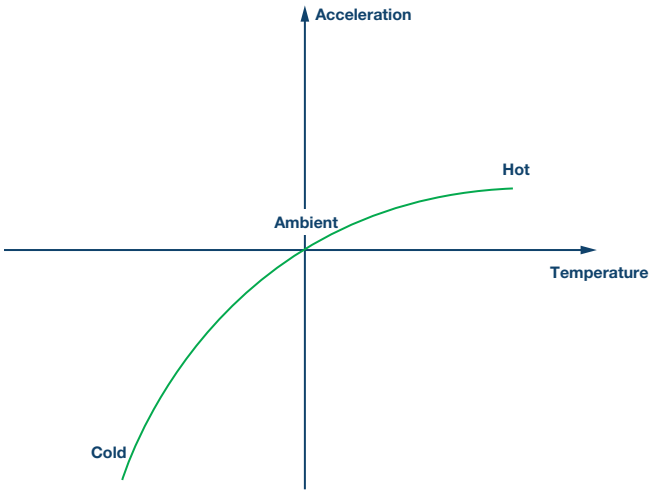

Figure 7. Step 2: after cancellation of the offset at ambient.

Step 2:

Next, the device is tested at a hot temperature and this new information is used to generate a linear equation for offset correction.

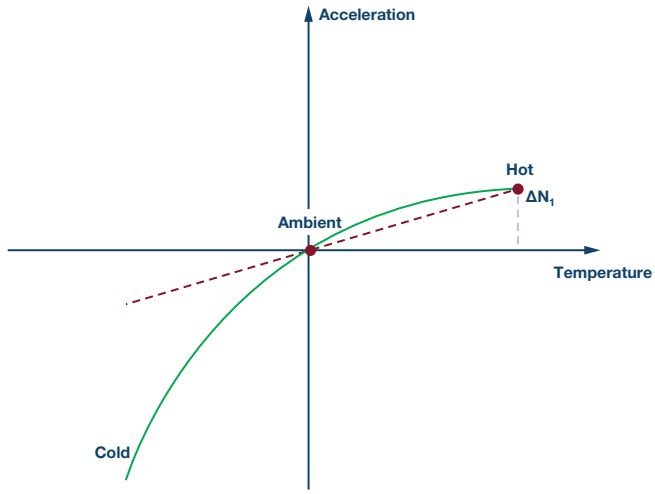

Figure 8. Step 3: cancel out the parabola rotation component at hot.

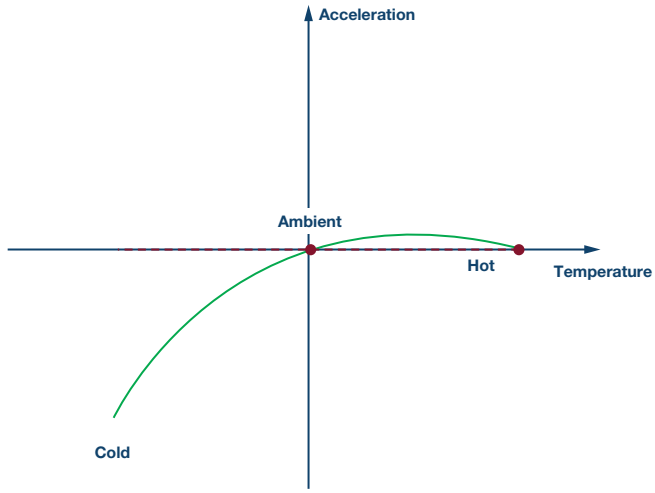

Figure 9. Step 4: after the cancellation of the parabola rotation component.

Step 3:

A second-order component is added to the existing equation in order to correct for the remainder of the offset. Assuming the second-order curve follows below equation:

$$A_{TEMP} = at^2 + bt + c$$

This is a second-order parabola formula and the rotation component has been cancelled through steps 1 and 2.

This second-order parabola has three solution of this equation:

$$(Temp_{COLD,}\ \Delta N_2), (Temp_{AMB,}\ 0), (Temp_{HOT,}\ 0)$$

Then we could get tempco ***a***, ***b***, ***c***.

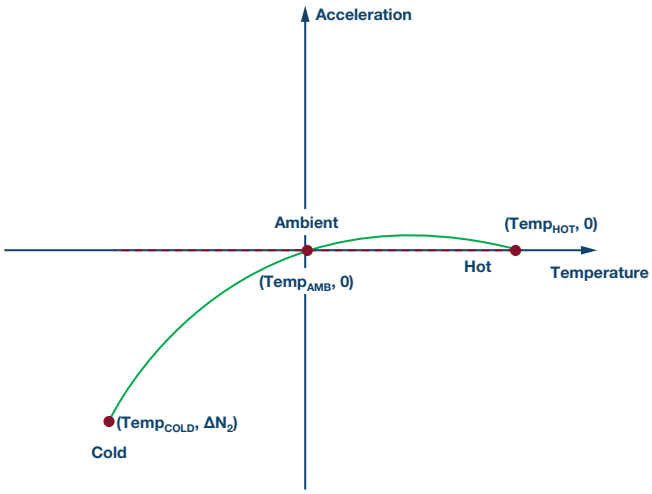

Figure 10. Step 5: adding a second-order component to cancel out the residual offset.

All the tempco information of ΔN_0, ΔN_1, ΔN_2, ***a***, ***b***, ***c*** should be stored in the system's nonvolatile memory and an on-board temperature sensor is needed. The system would calibrate the accelerometer routinely after each power on to ensure the cancellation of the variant drift vs. temperature.

Noise

To perform a tilt measurement based on a single sample of data may not be reliable. Even if the accelerometer had zero noise, tilt measurements are being made while the car is on, so any or all vibration caused by the engine, passing vehicles, or the passengers shifting around within the car will all need to be mitigated. The best way to do this is to average the data for as long as possible without falling below the minimum data rate requirements. This averaging will reduce the rms noise.

Assuming we sample the noise, we get a per-sample variance of

$$\mathrm{Var}(z) = E[z^2] = \sigma^2$$

Averaging a random variable leads to the following variance,

$$\mathrm{Var}\left(\frac{1}{n}\sum_{i=1}^{n} z_i\right) = \frac{1}{n^2}\mathrm{Var}\left(\sum_{i=1}^{n} z_i\right) = \frac{1}{n^2}\sum_{i=1}^{n}\mathrm{Var}(z_i)$$

Since noise variance is constant at σ^2,

$$N_{AVG} = \mathrm{Var}\left(\frac{1}{n}\sum_{i=1}^{n} z_i\right) = \frac{1}{n^2} n\,\sigma^2 = \frac{1}{n}\sigma^2$$

Demonstrating that averaging n realizations of the same, uncorrelated noise reduces noise power by a factor of n, and the rms noise would be reduced by $\sqrt{n}$.

Because random noise is subject to Gaussian distribution, rms noise is equivalent to the standard deviation of Gaussian distribution. The minimum population within 6σ is 97%.

For example, if you are averaging every 100 ms of data at 1 kSPS, then a max rms noise = 0.4 m*g*, meaning the calculation for peak noise at that point is only 2.4 m*g* if we use 6σ as the distance from the mean.

The factors that you are multiplying the rms value by depend on the statistical needs of the mission profile for the part. For example, if you choose 6 as the factor (peak-to-peak noise is 6 × RMS_Noise), the number of times will the algorithm is run over the lifetime of the part would impact the probability, exceeding the worst-case scenario of 6 × RMS_Noise. We can summarize this as:

$$E = M \times r$$

E is the expected times exceeding the worst case over lifetime, *M* is the lifetime running times, and *r* is the probability of exceeding the worst case. Based on this, we can evaluate a reasonable factor by multiplying the rms noise.

Summary

Taking ADI's ADXC1500/ADXC1501 (combined gyroscope and 2-axis/3-axis accelerometer) as an example, all the error contribution items are listed in Table 1 with or without calibration measures. We can assume total offset variation is the second curve and variation over temperature accounts for 80% of its total offset variation. Also, take 6 as the factor multiplied by the maximum rms noise.

This combination of a gyroscope and tri-axis accelerometer enables many new applications, especially in automotive safety systems and industrial automation applications. Minimizing these large error sources is mission critical to designing more reliable and accurate automotive safety systems, such as robust electronic stability control (ESC) and rollover detection. These build on traditional chassis control systems already in the vehicle, including the antilock braking system, traction control, and yaw control.

Table 1. Error Contributions With/Without Calibration

Error Contribution	Before Calibration	After Calibration	Calibration Measures
Sensitivity error	30 m*g*	0 m*g*	Two-point calibration
Initial absolute offset	15 m*g*	0 m*g*	Two-point calibration
Nonlinearity	10 m*g* over ±500 m*g*	10 m*g* over ±500 m*g*	None
Total offset variation	50 m*g*	10 m*g*	Three-point calibration
Noise	24 m*g*	2.4 m*g*	100× averaging
Total error	129 m*g*	22.4 m*g*	
Accuracy	7.4° (worst case)	1.28° (worst case)	In degree

Acknowledgements

I'd like to thank my two colleagues, Matthew Hazel and Brian Larivee, for providing many useful thoughts in this article.

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Solving IEC System Protection for Analog Inputs

By **David Forde**

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Introduction

External, high voltage transients that interact with a system's analog input and output nodes can damage the integrated circuits (ICs) within the system if they are not adequately protected. The analog input and output pins of a modern IC are typically protected against high voltage electrostatic discharge (ESD) transients. The human body model (HBM), machine model (MM), and charged device model (CDM) are the device-level standards used to measure a device's ability to withstand ESD events. These tests are designed so that a device can withstand the manufacturing and the PCB assembly process, which usually take place in a controlled environment.

Systems that operate in harsh electromagnetic environments are required to withstand high voltage transients on the input or output nodes—and when moving from device-level standards to system-level standards for high voltage transient robustness, there is a substantial difference in the energy levels transmitted to the pin of an IC. Therefore, ICs that directly interface with these system input/output nodes must also be sufficiently protected to withstand the system-level high voltage transients. Failure to account for this protection early in a system design can lead to inadequate system protection, delayed product release, and reduced system performance. This article describes how to protect sensitive analog input and output nodes from these IEC standard transient levels.

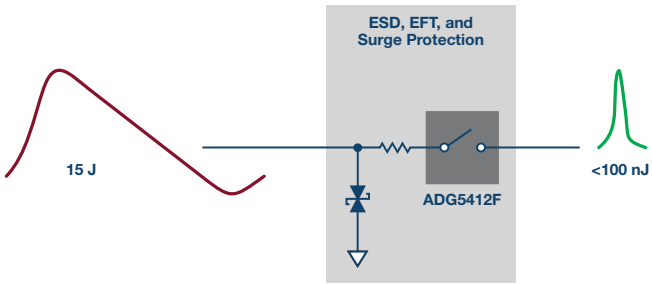

Figure 1. IEC system protection for precision analog inputs.

IEC 61000

IEC 61000 is the standard that covers EMC robustness at the system level. The three sections of the standard that deal with high voltage transients are IEC 61000-4-2, IEC 61000-4-4, and IEC 61000-4-5. These are the system-level standards for electrostatic discharge, electrical fast transients (EFT), and surge. These standards define the waveforms, test methods, and test levels for evaluating the immunity of electrical and electronic equipment when subjected to these transients.

The primary purpose of the IEC 61000-4-2 test is to determine the immunity of systems to external ESD events outside the system during its operation—for example, if a system input/output comes in contact with a charged human, cable, or tool. IEC 61000-4-2 specifies testing using two coupling methods: contact discharge and air gap discharge.

IEC 61000-4-4 EFT testing involves coupling a number of extremely fast transient impulses onto the signal lines to represent transient disturbances associated with external switching circuits that are capacitively coupled onto the signal lines. This testing reflects switch contact bounce or transients originating from the switching of inductive or capacitive loads, all of which are common in industrial environments.

Surge transients are caused by overvoltages from switching or lightning transients. Switching transients can result from power system switching, load changes in power distribution systems, or various system faults, such as short circuits and arcing faults to the grounding system of the installation. Lightning transients can be a result of high currents and voltages injected into the circuit from nearby lightning strikes.

Transient Voltage Suppressor

Basic parameters of a TVS:

A transient voltage suppressor (TVS) can be used to suppress voltage surges. They are used to clamp high voltage transients and shunt large currents away from sensitive circuitry. The basic parameters for a TVS are:

- Working peak reverse voltage: The voltage below which no significant conduction occurs
- Breakdown voltage: The voltage at which some specified conduction occurs
- Maximum clamping voltage: The maximum voltage across the device when conducting the maximum current specified

There are a number of factors that must be considered when using a TVS device on a system input or output. An ESD or EFT event will generate a very fast time (1 ns to 5 ns) transient waveform, resulting in an initial overshoot voltage on the system input before the TVS device clamps at its breakdown voltage. A surge event has a different transient waveform with a slow rise time (1.2 µs) and long duration (50 µs) pulse, and in this event the voltage will be initially clamped at the breakdown voltage, but it can continue to increase to the TVS maximum clamping voltage. In addition, the TVS must be higher than any tolerated dc overvoltage that could be caused by miswiring, loss of power, or user errors to protect the system against this dc overvoltage event. All three situations can cause a potentially damaging overvoltage on the input to the downstream circuitry.

Analog Input Protection Circuit

In order to fully protect a system input/output node, the system must be protected against dc overvoltages and high voltage transients. Using a precision, robust overvoltage protection (OVP) switch at the system input combined with the TVS can protect sensitive downstream circuitry (for example, analog-to-digital converters or amplifier inputs/outputs), as it can be used to block overvoltages and suppress residual currents that are not shunted to ground by the TVS.

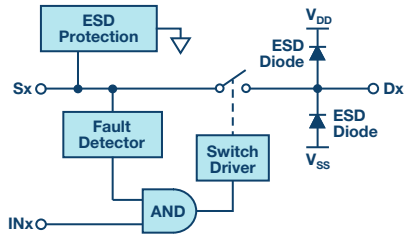

Figure 2. OVP switch functional block diagram.

Figure 2 shows the functional block diagram of a typical overvoltage protection switch; note that this switch does not have ESD protection diodes referenced to its supplies on its input node. It instead has an ESD protection cell that triggers above the device's maximum standoff voltage, which enables the device to stand off and block voltages beyond its supplies. As an analog system typically requires that only the outside facing pins of the switch need IEC protection, the ESD protection diodes are retained on the internal-facing pins (noted as switch output or drain side). These diodes benefit by serving as a secondary protection device. During a short duration, a high voltage transient with a fast rise time-like ESD or EFT, the transient voltage is clamped so the voltage will not reach downstream circuits. During a long duration, a high voltage transient with a slow rise time-like surge, the output voltage of the switch is clamped by the internal protection diodes before the overvoltage protection of the switch is activated and the switch opens to fully isolate the fault from the downstream circuitry.

Figure 3 shows the regions of operation for a system input that interfaces with the outside world. The leftmost region (in green) represents normal operation, where the input voltage is between the supply voltage ranges. The second region from the left (in blue) represents the range of possible persistent dc or long duration ac overvoltages presented to the input due to loss of power, miswiring, or short circuits. Also included in the diagram, on the far right hand side (in purple), is the trigger voltage for the internal ESD protection diodes of the overvoltage switch. The TVS breakdown voltage (in orange) must be selected to be less than the maximum standoff voltage of the overvoltage protection switch and also greater than any know possible persistent dc or long duration ac overvoltage, in order to avoid inadvertently triggering the TVS.

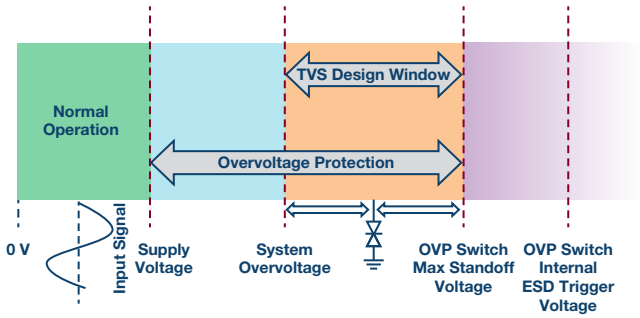

Figure 3. System operation regions.

The following protection circuit in Figure 4 can withstand up to 8 kV IEC ESD (contact discharge), 16 kV IEC ESD (air discharge), 4 kV EFT, and 4 kV surge. The ADG5412F (±55 V overvoltage protection and detection, quad SPST switch from Analog Devices) can withstand the overvoltages caused by ESD, EFT, and surge transients, while the overvoltage protection combined with the protection diodes on the drain protects and isolates downstream circuitry. Table 1 shows the levels of high voltage transients the ADG5412F can withstand various combinations of TVS breakdown voltages and resistors.

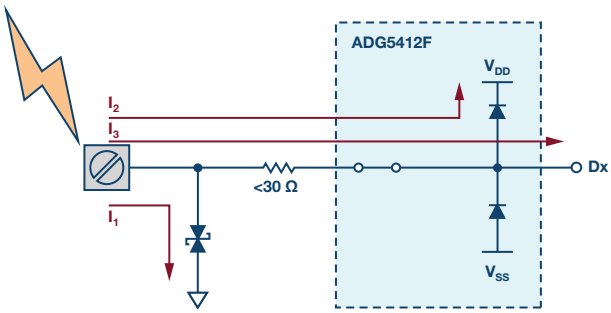

Figure 4. Protection circuit.

The protection network consists of a TVS and an optional low value resistor. The resistor is required to achieve the higher levels of ESD and EFT protection, as it prevents the internal ESD protection cell of the overvoltage switch from triggering before the TVS clamps the voltage on the input. Figure 4 also shows the various current paths during a high voltage transient

Table 1. Testing Results (IEC Air Was Not Tested With 0 Ω Resistor on 33 V TVS and 45 V TVS)

Protection	Protection IEC 61000-4-2 ESD Contact Discharge	IEC 61000-4-2 ESD Contact Discharge IEC 61000-4-2 ESD Air Discharge	IEC 61000-4-4 EFT	IEC 61000-4-4 EFT IEC 61000-4-5 Surge
33 V TVS and 0 Ω resistor	5 kV		3 kV	4 kV
33 V TVS and 10 Ω resistor	8 kV	16 kV	4 kV	4 kV
45 V TVS and 0 Ω resistor	4 kV		2 kV	4 kV
45 V TVS and 15 Ω resistor	8 kV	16 kV	4 kV	4 kV
54 V TVS and 30 Ω resistor	8 kV	16 kV	4 kV	4 kV

event. The majority of the current is shunted to ground through the TVS device (Path I1). Path I2 shows the current that is dissipated through the internal ESD diodes on the output of the ADG5412F, while the output voltage is clamped to 0.7 V above the supply voltage. Finally, the current in Path I3 is the residual current level that the downstream components must withstand. For more details on this protection circuit, please see the application note AN-1436 from Analog Devices.

IEC ESD Protection

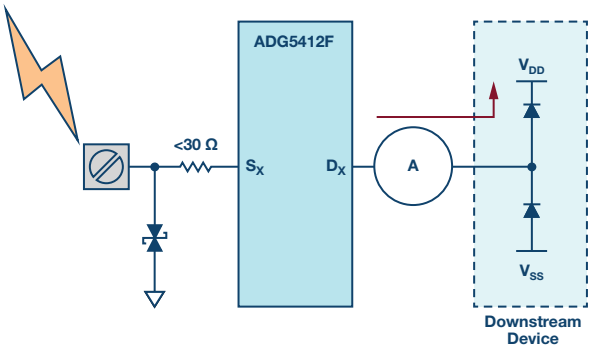

Figure 5. Test circuit

Figure 6 and Figure 7 show measurements taken during both an 8 kV contact discharge and a 16 kV air discharge IEC ESD event using the test circuit shown in Figure 5. As described previously, there is an initial overvoltage on the source pin before the TVS device clamps the voltage to approximately 54 V. The voltage at the drain of the switch during this overvoltage is clamped at 0.7 V above the supply. The drain current measurement shows the current flowing into the diodes of the downstream device. The peak current of the pulse is approximately 680 mA and the duration of the current is just approximately 60 ns. By comparison, a 1 kV HBM ESD strike that has a peak current of 660 mA has a duration of 500 ns. It is therefore reasonable to conclude that a downstream component with a HBM ESD rating of 1 kV should withstand both an 8 kV contact discharge and a 16 kV air discharge IEC ESD event using this protection circuit.

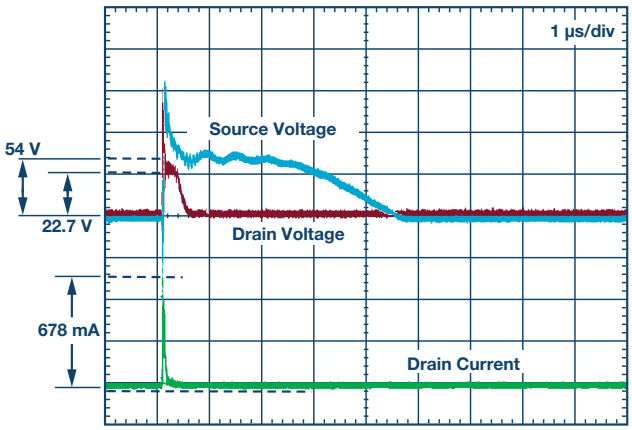

Figure 6. Drain voltage and output current at the drain during an 8 kV event.

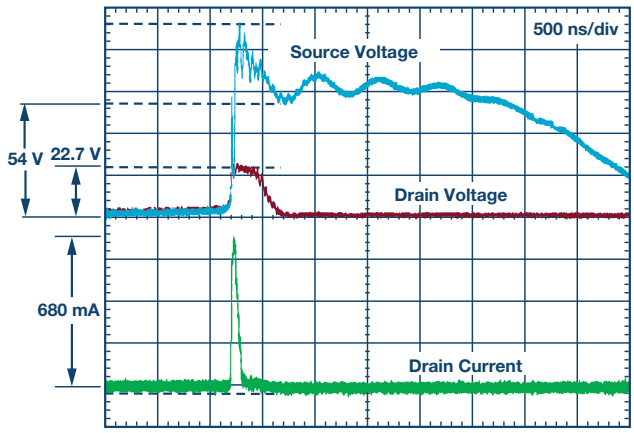

Figure 7. Drain voltage and output current at the drain during a 16 kV air discharge event.

EFT Protection

Figure 8 is a measurement taken during one pulse of a 4 kV EFT event. Similar to what happens during an ESD transient, there is an initial overvoltage on the source pin before the TVS device clamps the voltage to approximately 54 V. The voltage at the drain of the switch during this overvoltage is again clamped at 0.7 V above the supply. The peak current of the pulse flowing into the downstream device in this case is just 420 mA and the duration of the current is just approximately 90 ns. Comparing this again to an HBM ESD event, a 750 V HBM ESD strike has a peak current of 500 mA and has a duration of 500 ns. The energy is therefore transmitted to the pin of the downstream device during a 4 kV EFT event, which is less than that of a 750 V HBM ESD event.

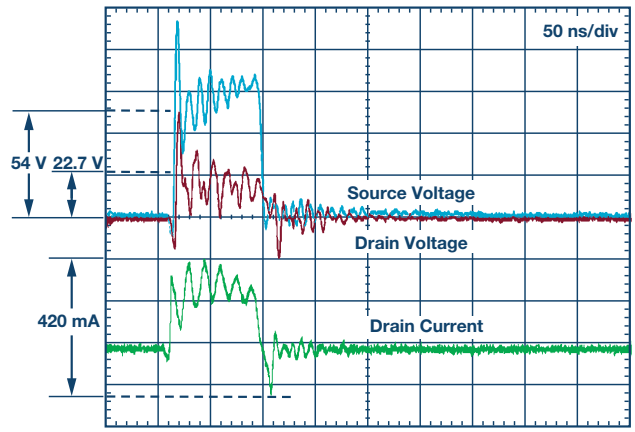

Figure 8. EFT current for a single pulse.

Surge Protection

This measurement in Figure 9 shows the result of a 4 kV surge transient applied to the input of the protection circuit. As mentioned previously, the voltage at the source can increase beyond the breakdown voltage of the TVS up to its maximum clamping voltage. The overvoltage protection

switch in this circuit has a reaction time of approximately 500 ns and the voltage on the drain of the device is clamped at 0.7 V above the supply during this first 500 ns time period. The peak current flowing to the downstream device is just 608 mA during this time period and after approximately 500 ns, the switch is seen to turn off and isolate the downstream circuitry from the fault. Again, this is less than the energy transmitted during a 1 kV HBM ESD event.

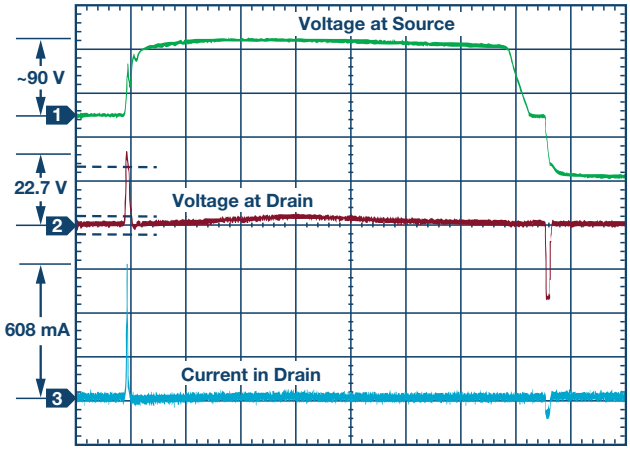

Figure 9. Operation of OVP during a surge event.

Conclusion

This article describes how to protect integrated circuit analog inputs and outputs against high voltage transients, as described by the standards IEC 61000-4-2, IEC 61000-4-4, and IEC 61000-4-5.

This information provides system designers with the knowledge required to design protection circuitry for system inputs and outputs while achieving the following benefits:

- Ease of protection design
- Faster time to market
- Higher protection circuit performance due to reduced number of discrete components required
- Reduced values of series resistance in the signal path
- Ease of TVS selection due to wide TVS design window
- System-level protection for the following standards
  - IEC 61000-4-2 16 kV air discharge
  - IEC 61000-4-2 8 kV contact discharge
  - IEC 61000-4-4 4 kV
  - IEC 61000-4-5 4 kV
- AC and persistent dc overvoltage protection up to ±55 V
- Power off protection up to ±55

Appendix

Analog Devices Overvoltage Protection and Detection Products: ±55 V OVP

Part Number	Configuration	HBM ESD Level (kV)	Specifications					Characterization Voltages (V_{NOM})				Packaging	
			R_{ON} Typ (Ω)	R_{ON} Flatness (Ω)	On Leakage Typ (nA)	QINJ Typ (pC)	BW (MHz)	Single		Dual			
								12	36	±15	±20	TSSOP	LFCSP
ADG5412F/ ADG5413F	SPST 4	5.5	10	0.6	0.3	680	270					EP	
ADG5412BF/ ADG5413BF	SPST 4	3	10	0.6	0.3	680	270						
ADG5436F	SPDT 2	6	10	0.6	0.3	654	108						
ADG5243F	SPDT 3	3.5	270	7	0.3	0.8	350						
ADG5404F	4:1/mux	5	10	0.6	0.3	680	108						
ADG5208F/ ADG5209F	8:1/diff 4:1/mux	3.5	250	6.5	0.3	0.4	190/290						
ADG5248F/ ADG5249F	8:1/diff 4:1/mux	3.5	250	6.5	0.3	0.8	190/320						
ADG5462F	Channel protector ×4	4	10	0.6	0.3	N/A	318						

David Forde [david.forde@analog.com] joined Analog Devices as a layout engineer in 2006 after graduating from Carlow Institute of Technology with a B.Sc. in integrated circuit design. In 2011, he graduated from the University of Limerick with an M.Eng. in VLSI systems and, in 2015, he joined the Instrumentation and Precision Technology Group as an applications engineer supporting the analog switch and multiplexer product portfolio.

David Forde

72 V Hybrid DC-to-DC Converter Reduces Intermediate Bus Converter Size by up to 50%

By **Bruce Haug**

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Background

Most intermediate bus converters (IBCs) provide isolation from input to output with the use of a bulky power transformer. They also normally require an inductor for output filtering. This type of converter is commonly used in datacom, telecom, and medical distributed power architectures. These IBCs are available from a wide variety of suppliers and are typically housed in industry-standard $^1/_{16}^{th}$, $^1/_8^{th}$, and $^1/_4^{th}$ brick footprints. A typical IBC has a nominal input voltage of 48 V or 54 V and produces a lower intermediate voltage between 5 V to 12 V with an output power level from several hundred watts to several kilowatts. The intermediate bus voltage is used as the input to point-of-load regulators that will power FPGAs, microprocessors, ASICs, I/Os, and other low voltage downstream devices.

However, in many new applications, such as a 48 V direct conversion application, isolation is not necessary in the IBC since the upstream 48 V or 54 V input is already isolated from the hazardous ac mains. In many applications, a hot swap front-end device is required to use a nonisolated IBC. As a result, nonisolated IBCs are being designed into many new applications, which significantly reduces the solution size and cost while also increasing the operating efficiency and providing design flexibility. A typical distributed power architecture is shown in Figure 1.

Now that nonisolated conversion is allowed in some distributed power architectures, one could consider using the single stage buck converter for this application. It would need to operate over an input voltage range from 36 V to 72 V and produce a 5 V to 12 V output voltage. The LTC3891 from Analog Devices can be used for this approach and provides an efficiency of about 97% when operating at a relatively low 150 kHz switching frequency. Operating the LTC3891 at higher frequencies results in lower efficiency due to the MOSFET switching losses that occur with the relatively high 48 V input voltage.

A New Approach

The new innovative approach to controllers combines a switched capacitor converter with a synchronous buck. The switched capacitor circuit reduces the input voltage by a factor of two and then feeds into the synchronous buck. This technique of reducing the input voltage in half and then bucking down to the desired output voltage results in higher efficiency or a much smaller solution size by operating at a much higher switching frequency. Other benefits include lower switching losses and reduced MOSFET voltage stress due the inherent soft switching characteristic of the switched capacitor front-end converter, resulting in lower EMI. Figure 2 shows how this combination has formed the hybrid step-down synchronous controller.

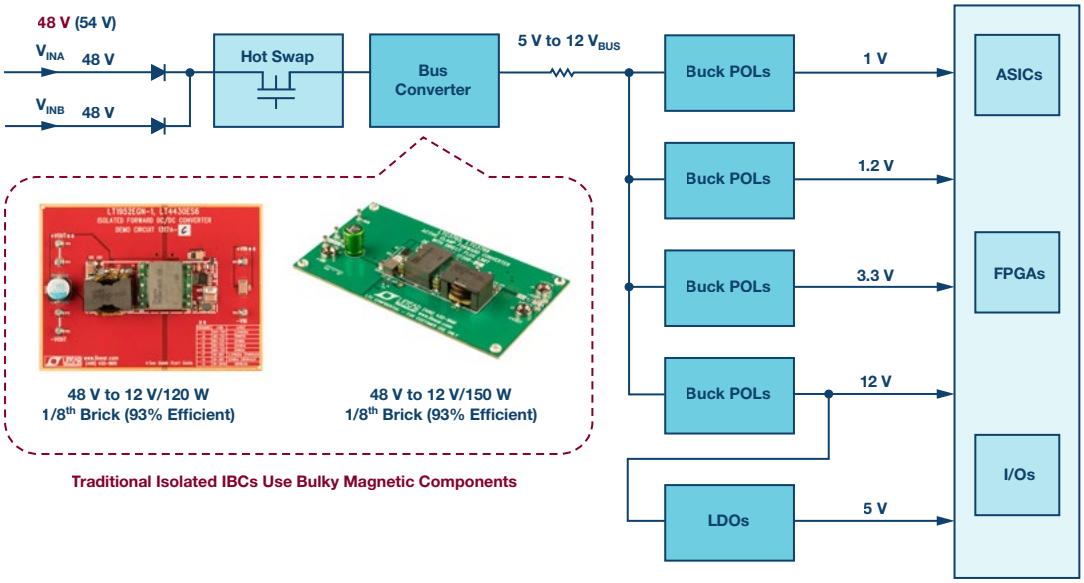

Figure 1. Typical distributed power architecture.

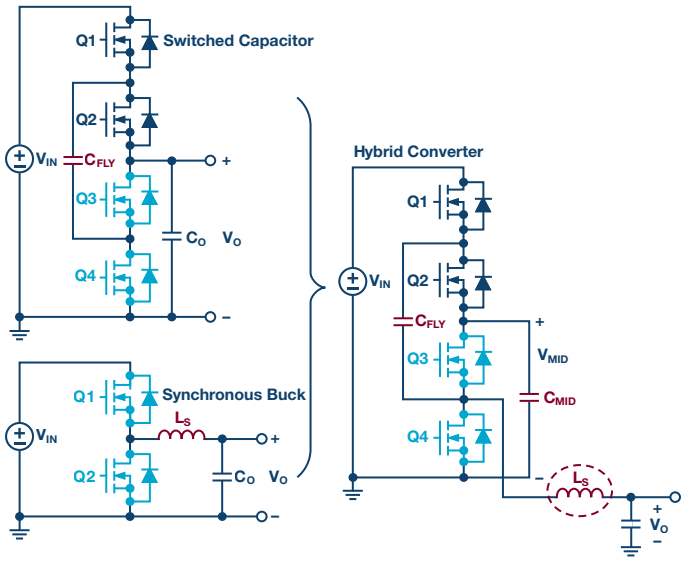

Figure 2. A switched capacitor plus a synchronous buck combine into an LTC7821 hybrid converter.

New High Efficiency Converter

The LTC7821 merges a switched capacitor circuit with a synchronous step-down converter, enabling up to a 50% reduction in dc-to-dc converter solution size compared to traditional buck converter alternatives. This improvement is enabled by a 3× higher switching frequency without compromising efficiency. Alternatively, when operating at the same frequency, an LTC7821-based solution can provide up to a 3% higher efficiency. Other benefits include low EMI emissions due to a soft-switched front end ideal for the next generation of nonisolated intermediate bus applications in power distribution, datacom, and telecom, as well as emerging 48 V automotive systems.

The LTC7821 operates over a 10 V to 72 V (80 V abs max) input voltage range and can produce output currents in multiple tens of amps, depending on the choice of external components. External MOSFETs switch at a fixed frequency, programmable from 200 kHz to 1.5 MHz. In a typical 48 V to 12 V/20 A application, an efficiency of 97% is attainable with the LTC7821 switching at 500 kHz. The same efficiency can only be achieved in a traditional synchronous step-down converter by switching at $^1/_{3^{rd}}$ the operating frequency, forcing the use of much larger magnetics and output filter components. The LTC7821's powerful 1 Ω N-channel MOSFET gate drivers maximize efficiency and can drive multiple MOSFETs in parallel for higher power applications. Due to its current-mode control architecture, multiple LTC7821s can be operated in a parallel, multiphase configuration with excellent current sharing and low output voltage ripple to enable much higher power applications without hot spots.

The LTC7821 implements many protection features for robust performance in a wide range of applications. An LTC7821-based design also eliminates the inrush current typically associated with switched capacitor circuits by prebalancing the capacitors on startup. The LTC7821 also monitors the system voltage, current, and temperature for faults and uses a sense resistor for overcurrent protection. It stops switching and pulls the FAULT

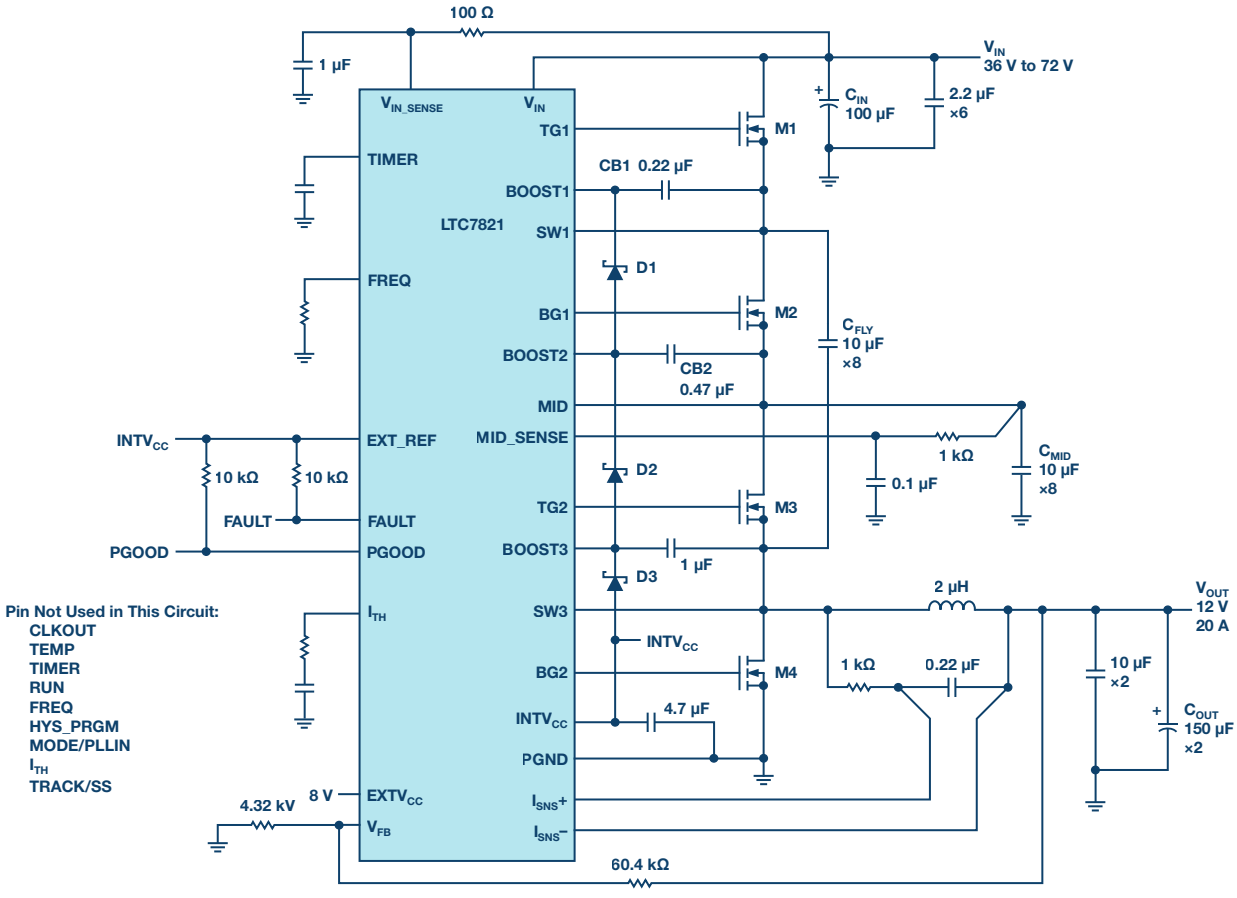

Figure 3. LTC7821 schematic showing 36 V_{IN} to 72 V_{IN}/12 V/20 A output.

pin low when a fault condition occurs. An onboard timer can be set for appropriate restart/retry times. Its $EXTV_{CC}$ pin permits the LTC7821 to be powered from the lower voltage output of the converter or other available sources up to 40 V, reducing power dissipation and improving efficiency. Additional features include ±1% output voltage accuracy over temperature, a clock output for multiphase operation, a power good output signal, short circuit protection, monotonic output voltage startup, optional external reference, undervoltage lockout, and internal charge balance circuitry. Figure 3 shows the schematic of the LTC7821 when converting a 36 V to 72 V input to a 12 V/20 A output.

The efficiency curves shown in Figure 4 represent a comparison of three different converter types for the application that converts a 48 V_{IN} to a 12 V_{OUT} at 20 A as follows:

- A single stage buck running at 125 kHz with a 6 V gate drive (blue curve)
- A single stage buck running at 200 kHz with a 9 V gate drive (red curve)
- The LTC7821 hybrid running at 500 kHz with a 6 V gate drive (green curve)

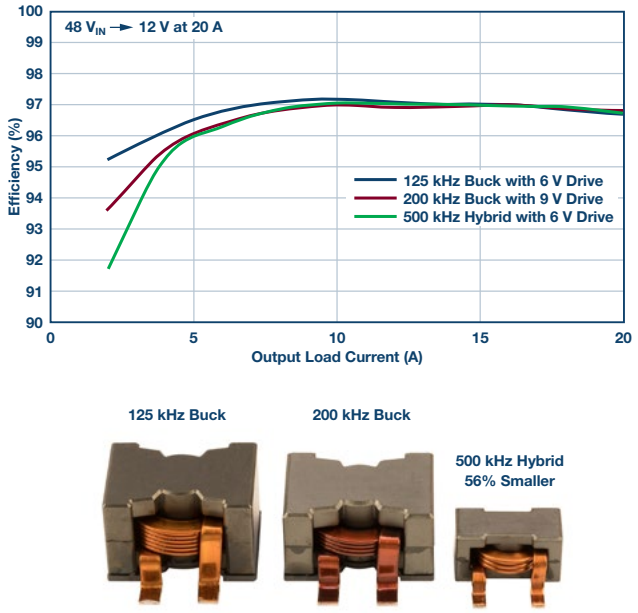

Figure 4. Efficiency comparison and transformer size reduction.

An LTC7821-based circuit running at up to 3× the operating frequency of the other converters has the same efficiency as the other solutions. This higher operating frequency results in a 56% reduction of the inductor size and up to a 50% reduction to the total solution size.

Capacitor Prebalancing

A switched capacitor converter usually has a very high inrush current when the input voltage is applied or when the converter is enabled, resulting in the possibility of supply damage. The LTC7821 has a proprietary scheme to precharge all switching capacitors before the converter PWM signal is enabled. Therefore, the inrush current during power up is minimized. In addition, the LTC7821 also has a programmable fault protect window to further ensure reliable operation of the power converter. These features result in the output voltage having a smooth soft start just like any other conventional current mode buck converter. See the LTC7821 data sheet for additional details.

Main Control Loop

Once the capacitor balancing phase is completed, normal operation begins. MOSFETs M1 and M3 are turned on when the clock sets the RS latch, and turned off when the main current comparator, ICMP, resets the RS latch. MOSFETs M2 and M4 are then turned on. The peak inductor current at the ICMP that resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The V_{FB} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8 V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After MOSFETs M1 and M3 have turned off, MOSFETs M2 and M4 are turned on until the beginning of the next cycle. During the switching of M1/M3 and M2/M4, capacitor C_{FLY} is alternately connected in series with or parallel to C_{MID}. The voltage at MID will be approximately at $V_{IN}/2$. So, this converter just operates like a conventional current-mode buck converter with a fast and accurate cycle-by-cycle current limit and option for current sharing.

Conclusion

The combination of a switched capacitor circuit to halve the input voltage followed by a synchronous step-down converter (hybrid converter) provides up to a 50% reduction in dc-to-dc converter solution size compared to traditional buck converter alternatives. This improvement is enabled by a 3× higher switching frequency without compromising efficiency. Alternatively, the converter can operate with 3% higher efficiency in a footprint comparable to existing solutions. This new hybrid converter architecture also provides other benefits that include soft switching for reduced EMI and MOSFET stress. Multiple converters can be easily paralleled with active accurate current sharing when high power is needed.

Bruce Haug [bruce.haug@analog.com] received his B.S.E.E. from San Jose State University in 1980. He joined Linear Technology (now a part of Analog Devices) as a product marketing engineer in April 2006. Bruce's past experience includes stints at Cherokee International, Digital Power, and Ford Aerospace. He is an avid sports participant.

Bruce Haug

Rarely Asked Questions—Issue 150 Dynamic Use of the Disable Pin on an Amplifier

By **Thomas Tzscheetzsch**

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Question:

Could I use the disable pin of an amplifier to save power without losing performance?

Answer:

Battery-operated applications are becoming popular in the IoT era. In this article, we will show that there does not have to be a trade-off between power saving and accuracy.

Some operational amplifiers have disable pins and when used correctly, they can yield up to 99% power savings without compromising accuracy. The disable pin is primarily used in static operation (standby mode). In this mode, all ICs are switched to a state of low power consumption, without the device being used for signal processing. This slashes the power consumption by several orders of magnitude.

If the operational amplifier is needed as a buffer amplifier for an ADC, as shown in Figure 1, it must be active to perform its function. However, the power consumption can still be kept low if the amplifier is switched to the power-down mode via the disable pin. In general, the power-down mode is used whenever the ADC does not have to read any new values into its *sample* and *hold* function block.

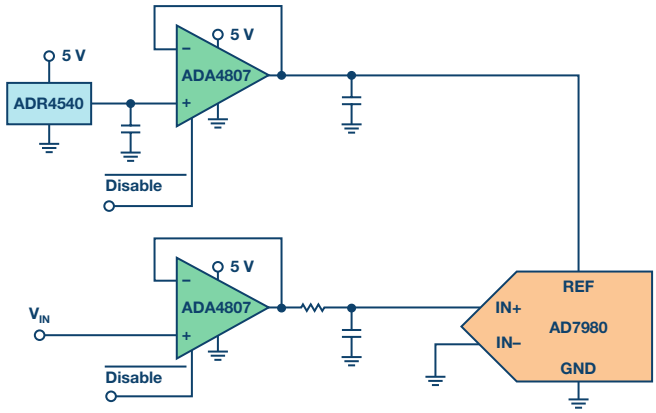

Figure 1. Typical schematic of an ADC input stage with ADC driver and reference buffer.

The easiest way to implement this is via the start command for conversion. In a standard ADC, the input (sample and hold) capacitor is first charged to the value to be measured. This is done until the signal is sent to the ADC for conversion. The input capacitor is then isolated and connected to the inputs on the converter stage, which is when conversion begins. Then it is completed and a *finished* signal is set, which is dependent on the converter type. Now comes the actual question: when does the operational amplifier have to be active? It must be active long enough in advance of the conversion start signal to ensure that the internal input capacitor has assumed the same value as the signal to be measured. The amount of time depends on such factors as the size of the input capacitor, the magnitude of the voltage to be measured, and the rate at which the operational amplifier can drive a capacitive load.

The data sheet for our ADC (AD7980) gives a value of 30 pF for the input capacitance in series with an impedance of 400 Ω. However, with the operational amplifier, it isn't that simple. A capacitive load of 15 pF is stated in the parameter table, but more is possible, as can be seen in the corresponding diagram (Figure 2). The low-pass filter with 2.7 nF and 20 Ω also needs to be considered.

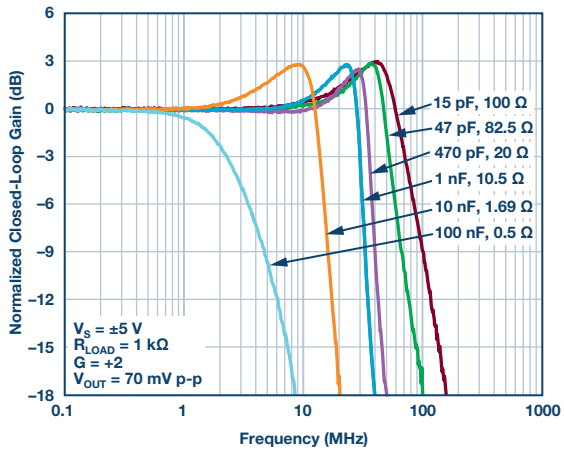

Figure 2. Frequency response of the ADA4807.

The diagram shows that the module can drive sufficiently high capacitive loads. After a disable, the amplifier needs about 500 ns to settle to the full output level, which in our case is a maximum of 5 V or 4.096 V.

To be on the safe side, we assume that the amplifier is switched on 750 ns before the start of conversion. The extrapolated data for 1 kSPS to 1 MSPS is compared.

The savings potential ranges from 99.83% (0.02 mW total consumption) at 1 kSPS to 92.41% (10.75 mW total consumption) at 1 MSPS. That's only the savings from the ADC driver; the reference buffer also has savings potential.

This example is intended to show what modern devices are capable of. At the minimum sampling time of 500 ns, the SINAD deviation was <0.5 dB. In the case of the driver, it is worthwhile to focus on faster derivatives and operate them dynamically. We have only considered the application as a buffer (gain = 1). For inverting or other amplifiers, the savings will be different depending on the conditions. Measurements should be carried out to check this.

Thomas Tzscheetzsch

Thomas Tzscheetzsch [thomas.tzscheetzsch@analog.com] joined Analog Devices in 2010, working as a senior field applications engineer. From 2010 to 2012, he covered the regional customer base in the middle of Germany and, since 2012, has been working in a key account team on a smaller customer base. After the reorganization in 2017, he's leading a team of FAEs in the IHC cluster in CE countries as FAE manager.

At the beginning of his career, he was working as an electronics engineer in a machine building company from 1992 to 1998, as head of the department. After his study of electrical engineering at the University of Applied Sciences in Göttingen, he worked at the Max Planck Institutes for solar system research as a hardware design engineer. From 2004 to 2010, he worked as an FAE in distribution and worked with Analog Devices' products.

Power Management for FPGAs

By **Frederik Dostal**

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There have been many technical discussions about designing a good power management solution for an FPGA application, as it is not a trivial task. One aspect of this task involves finding the right solution and selecting the most suitable power management product, while another is how to optimize the actual solution for use with FPGAs.

Finding the Right Power Supply Solution

Finding the best possible solution to power FPGAs is not simple. Many vendors market certain products as suitable to power FPGAs. What makes the selection of dc-to-dc converters specific to powering FPGAs? Not much. Generally, all power converters can be used to power FPGAs. Recommendations for certain products are usually based on the fact that many FPGA applications require multiple voltage rails, such as for the FPGA core, the I/Os, and possibly an additional rail for DDR memory termination. Often PMICs (power management integrated circuits), where multiple dc-to-dc converters are all integrated into one single regulator chip, are preferred.

One popular way to find a good solution for powering a specific FPGA is to use pre-existing power management reference designs, which many FPGA vendors offer. This is a good starting point for an optimized design. However, modifications of such designs are often necessary, since a system with an FPGA usually requires additional voltage rails and loads that also need to be powered. Additions to the reference design are also often necessary. Another thing to consider is that the input power of FPGAs is not fixed. The input voltage heavily depends on the actual logic levels and the design that the FPGA is implementing. After completing modification to the power management reference design, it will look different from the reference design's original suggestion. One can argue that the best solution is to not even bother with a power management reference design, but to enter the required voltage rails and currents straight into a power management selection and optimization tool such as LTpowerCAD® from Analog Devices.

Figure 1. LTpowerCAD tool to select the right dc-to-dc converters to power FPGAs.

LTpowerCAD can be used to come up with a power solution for individual voltage rails. It also offers a collection of reference designs, providing designers with a good starting point. LTpowerCAD can be downloaded for free from the Analog Devices website.

Once a power architecture and individual voltage converters have been selected, we need to choose suitable passive components and design the power supply. When doing this we need to keep the special load requirements of FPGAs in mind.

These are:

- Individual current requirements
- Voltage rail sequencing
- Monotonic rise of voltage rails
- Fast power transients
- Voltage accuracy

Individual Current Requirements

The actual current consumption of any FPGA depends heavily on the use case. Different clocking and different FPGA content requires different amounts of power. Because of this, the final power supply specification for a typical FPGA design is bound to change during the FPGA system design process. FPGA manufacturers supply power estimation tools that help to calculate the kind of power level that the solution will need. This information is quite useful to have before actual hardware is built. Still, the design of the FPGA needs to be final, or at least close to final, to get meaningful results with such power estimators.

Often, engineers design the power supply with the maximum FPGA current in mind. Then, if it turns out that the actual FPGA design requires less power, they scale down the power supply.

Voltage Rail Sequencing

Many FPGAs require different supply voltage rails to come up in a specific sequence. Often times the core voltage needs to be supplied before the I/O voltages come up. Otherwise some FPGAs will be damaged. To avoid this, the power supply needs to be sequenced in the correct order. Simple up-sequencing can easily be done by using enable pins on standard dc-to-dc converters. However, controlled down-sequencing is usually also required. It is difficult to achieve a good result when only enable pin sequencing is performed. A better solution is to use a PMIC with advanced integrated sequencing features, such as the ADP5014. The special circuit block that enables adjustable up and reverse order down-sequencing is indicated in red in Figure 2.

Figure 3 shows the sequencing done with this device. The time delay for up- and down-sequencing can be easily adjusted with delay (DL) pins on the ADP5014.

If individual power supplies are used, an additional sequencing chip can take care of the required on/off sequencing. One example is the LTC2924, which can control either the enable pins of dc-to-dc converters to turn on and off the power supplies or it can drive high-side N-channel MOSFETs to attach and detach an FPGA to a certain voltage rail.

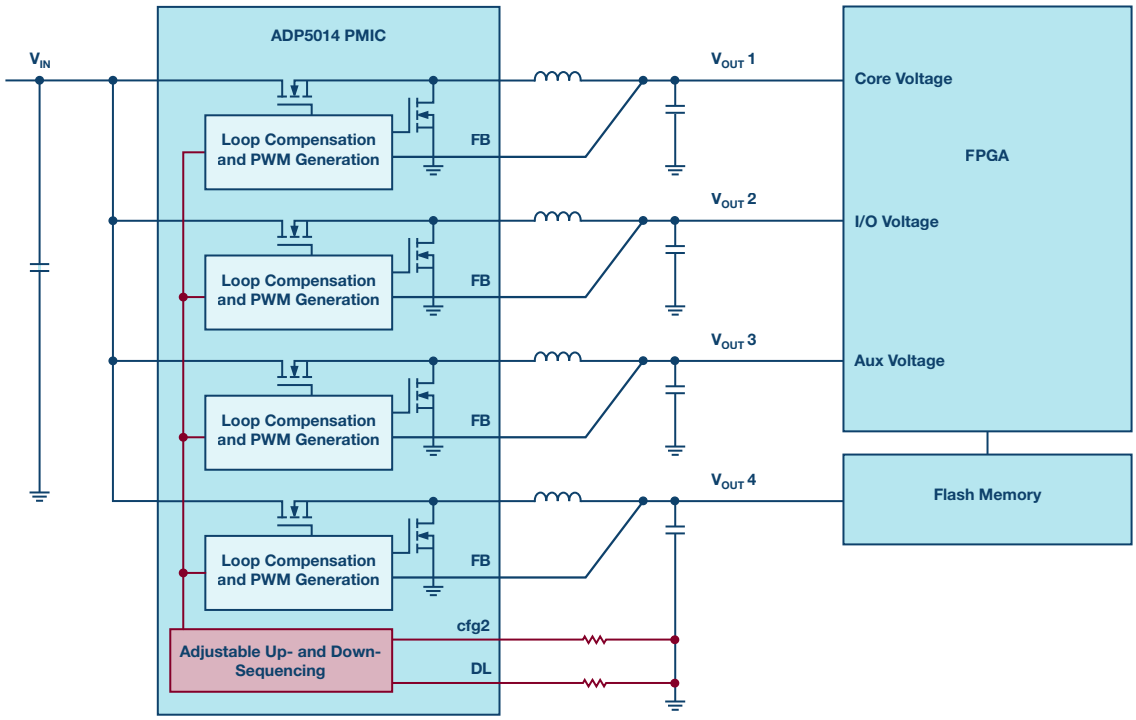

Figure 2. ADP5014 PMIC with integrated support for flexible up- and down-sequencing.

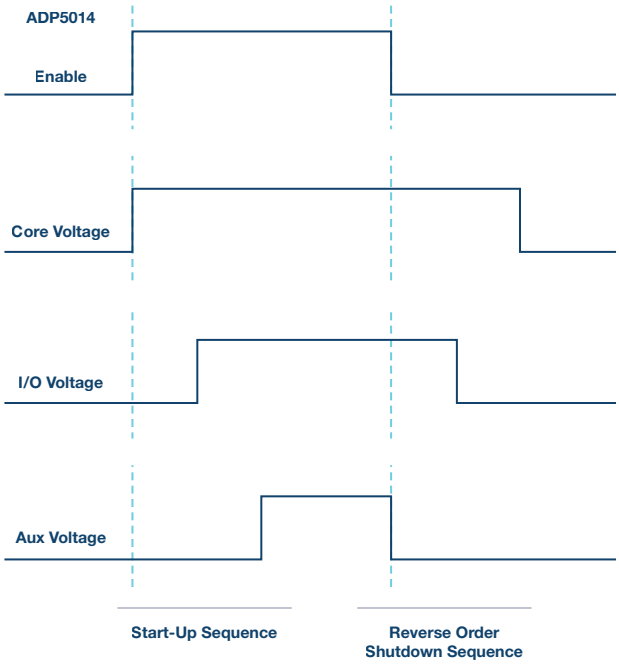

Figure 3. Start-up and shutdown sequencing of multiple FPGA supply voltages.

Monotonic Rise of Voltage Rails

Besides the voltage sequencing, a monotonic rise of the voltages during startup may also be necessary. This means that a voltage will only rise linearly, as shown by Voltage A in Figure 4. Voltage B in this plot shows an example of a voltage not rising monotonically. This can happen when the load starts pulling large currents at a certain voltage level during startup. One way to prevent this is to allow for a longer soft start of the power supply and to choose power converters that can quickly supply high amounts of current.

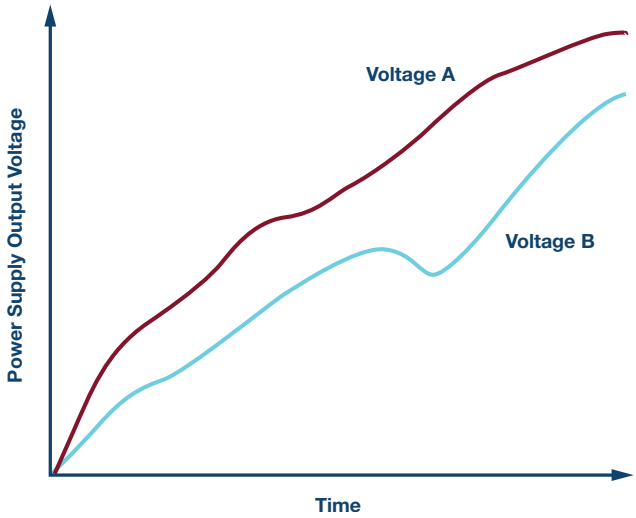

Figure 4. Voltage A rising monotonically, with Voltage B not rising monotonically.

Fast Power Transients

One other FPGA characteristic is that FPGAs very quickly start drawing high currents. They cause high load transients on the power supply. For this reason, many FPGAs require extensive input voltage decoupling. Ceramic capacitors are used very closely between the VCORE and the GND pins of the device. Values up to 1 mF are quite common. Such high capacitance helps to reduce the demand on the power supplies to deliver very high peak currents. However, many switching regulators and LDOs have a maximum output capacitance specified. The input capacitance requirement of the FPGA can exceed the maximum allowed output capacitance of the power supply.

Power supplies do not like huge output capacitors since, during startup, this capacitor bank looks like a short circuit on the output to the switching regulator. There is a solution for this problem. A long soft start time can allow for the voltage on the large capacitor bank to come up reliably without the power supply to go into short-circuit current limit mode.

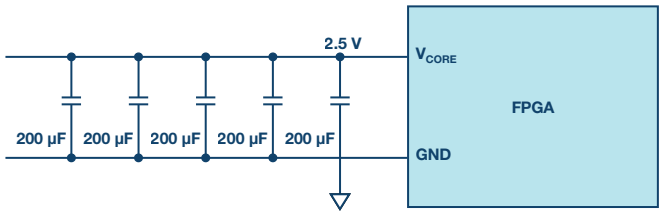

Figure 5. Input capacitor requirement of many FPGAs.

Another reason why some power converters do not like excessive output capacitance is that this capacitance value becomes part of the regulation loop. Converters with integrated loop compensation do not allow for excessive output capacitance to prevent loop instability of the regulator. Often there are ways to influence the control loop by using feedforward capacitance across the high-side feedback resistor, as shown in Figure 6.

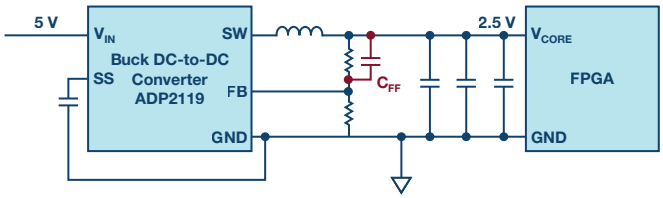

Figure 6. Feed forward capacitor to allow for control loop adjustment when no loop compensation pin is available.

For the load transient and start-up behavior of a power supply, the development tool chain including LTpowerCAD and especially LTspice is very helpful. One effect that lends itself well to modeling and simulation is the decoupling of the large input capacitors of the FPGA from the output capacitors of the power supply. Figure 6 shows this concept. While the POL (point-of-load) power supply tends to be located close to the load, often there is some PCB trace between the power supply and the FPGA input capacitor. When there are multiple FPGA input capacitors next to each other on the board, the ones that are furthest away from the power supply will have a smaller effect in the power supplies' transfer function, since there is some resistance

but also parasitic trace inductance between them. These parasitic board inductances can allow for the input capacitance of an FPGA to be larger than the maximum limit of output capacitance of the power supply, even though all the capacitors are connected to the same node on the board. In LTspice, parasitic trace inductances can be added to the schematic and such effects can be modeled. Simulation results are close to reality when adequate parasitic components are included in the circuit modeling.

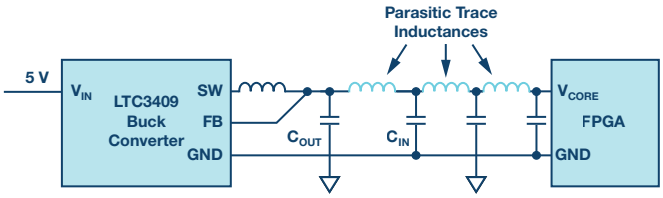

Figure 7. Parasitic decoupling between the power supply output capacitors and the FPGA input capacitors.

Voltage Accuracy

The voltage accuracy of an FPGA power supply usually needs to be quite high. A variation tolerance band of only 3% is quite common. For example, keeping a Stratix V core rail at 0.85 V within a 3% voltage accuracy window requires a complete tolerance band of only 25.5 mV. This small window includes voltage variation after load transients, as well as dc accuracy. Again, the available power supply tool chain including LTpowerCAD and LTspice is essential in the power design process for such strict requirements.

One last piece of advice is in regards to the selection of FPGA input capacitors. For them to quickly deliver large currents, ceramic capacitors are usually chosen. They work well for this purpose, but they need to be selected so that their true capacitance value does not drop with dc bias voltage. Some ceramic capacitors, especially the Y5U types, change their true capacitance value down to only 20% of the nominal face value when they are biased with a dc voltage close to their maximum rated dc voltage.

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Also by this Author:

Intermediate Voltage to Increase Power Conversion Efficiency

Volume 52, Number 1

A Robust Precision Data Acquisition and Control Platform for Extreme High Temperature Environments

By **Jeff Watson** and **Maithil Pachchigar**

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Introduction

The needs of multiple industries has led to the increased placement of high precision electronics closer to high temperature areas. There are several drivers for this trend, such as in energy exploration, where accessing hard-to-reach resources often requires equipment designed to operate at 175°C and higher. Due to size and power limitations, active cooling is not practical and convection of heat is very limited. In other systems, it is desirable to locate sensors and signal conditioning nodes close to areas of elevated temperature, such as engines, braking systems, or high power energy conversion electronics, in order to improve the overall system reliability or reduce costs. Aerospace, automotive, heavy industrial, and other end applications are all working to overcome this design challenge.[1]

Historically, it has been very challenging for engineers to design reliable, high performance electronics for these applications due to the lack of availability of components specified by their manufacturers for these operating conditions. Fortunately, in recent years there has been an increasing number of components, both ICs and passives, specified by their manufacturers for high temperature operation at 175°C and higher. In addition, recent reference designs have also focused on the performance of some of these components combined together in signal chain subsystems for precision data acquisition in order to enable system designers to more rapidly adopt the technology, such as CN-0365, and help them reduce design risk and time to market. However, until now there has been a gap for a fully featured, well characterized, and widely available platform for high temperature precision data acquisition.

In this article we introduce a new high temperature, precision data acquisition and processing platform that has been designed to operate at 200°C. This platform includes a high temperature circuit assembly with a data acquisition front end and microcontroller, optimized firmware, data capture and analysis software, source code, design files, a bill of materials, and test reports. This platform is suitable for reference design, rapid prototyping, and lab testing of high temperature instrumentation systems. The dimensions and construction of the circuit assembly have been designed to be compatible with oil and gas instrumentation form factors, although it can also be used as the basis for other high temperature applications.

Hardware Architecture Overview

Instrumentation used in oil and gas exploration, also known as downhole tools, is similar to many precision data acquisition and control platforms, but has some specialized performance and reliability requirements and is interesting to examine as a case study for this reference platform. In this application, signals from various sensors are sampled in order to collect information about the surrounding geologic formations. These sensors could take the form of electrodes, coils, piezoelectric, or other transducers. Accelerometers, magnetometers, and gyroscopes provide information about the inclination and rotation rate of the drill string. Some of these sensors are very low bandwidth, while others are capable of providing information in the audio frequency range and higher. Multiple acquisition channels are required and must maintain high precision at high temperatures—typically 175°C and higher. In addition, many of these instruments run on battery power or have limited power generation available and must therefore have low power consumption and multiple modes of operation for power optimization.

In addition to electronic systems requirements, downhole applications also have mechanical constraints that can dictate the electronic assembly form factor and also affect component packaging and selection. The latter will be discussed in more detail in later sections, but it is significant to note that circuit assemblies in this segment tend to have restrictions on the board width. Electronic assemblies must be placed within tube-shaped pressure vessels used in drilling operations, which leads to long and narrow aspect ratios. This form factor limits the size and density of components that can be populated and it also can restrict the partitioning of the component layout and signal routing, which can have a significant effect on performance with high precision electronics and thus require attention to layout and other packaging design details. Figure 2 shows a typical form factor, a circuit assembly mounted in a tubular pressure vessel (transparent, top), and a cross section of a tubular pressure vessel with board mounted (bottom).

The robust reference design platform presented in this article builds on the CN-0365 analog front-end reference design with the goal of providing a foundation for a high temperature, low power microcontroller-based precision data acquisition and control solution that meets the requirements for many downhole instrumentation and other high temperature electronics. Based upon the AD7981 analog-to-digital SAR converter, this reference

design demonstrates a fully featured system with two high speed simultaneously sampled channels along with eight additional multiplexed channels suitable for covering the acquisition requirements of a broad range of downhole tools (10 channels total). This analog front end is connected via SPI ports to the VA10800 ARM® Cortex®-M0 microcontroller from Alliances partners Vorago Technologies and Petromar Technologies. The design is the latest addition to the growing ecosystem of products and solutions for high temperature applications from ADI.

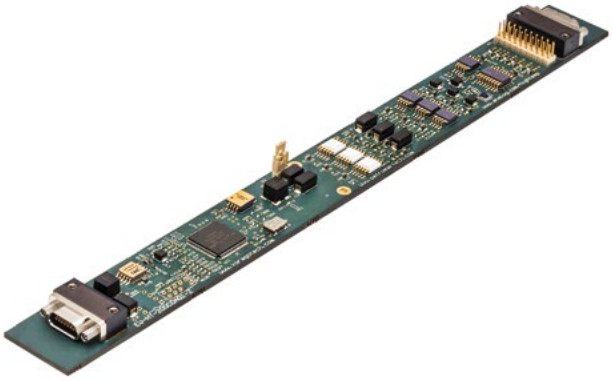

Figure 1. High temperature reference platform.

Once acquired, the data can be processed locally or transmitted via a UART or optional RS-485 communications interface. Other supporting components on the board, including memory, clock, power, and passives, are all rated for high temperature operation by their respective suppliers and verified to operate reliably at 200°C or higher. Figure 1 and 2 show the actual board and high level block diagram for this high temperature reference platform. The board rendering in Figure 2 is indicative of the downhole electronics board layout and form factor, approximately 11.4" long and 1.1" wide.

Figure 2. Downhole electronic assembly form factor.

The design of the precision data acquisition channel for this platform is covered extensively by the CN-0365 application note.[3] That design serves as the basis for the three ADC inputs on this platform, although some changes and optimizations were made, mostly in passive component selection, in order to address the form factor requirem ents of the board and extended reliable operation up to 200°C. The reference acquisition channel circuit is shown in Figure 4. There are two digital multiplexed channels that each contain a complete data acquisition channel, similar to CN-0365, that are capable of running at high sample rates. There is also an analog multiplexed channel that adds an ADG798 multiplexer in front of the inputs, which is optimized for lower throughput inputs. R1 and R3 provide a 1.25 V bias for the noninverting input of U1 and prevent it from floating to the rail of the analog input if left open, or if the multiplexer is deselected. R8 and R9 can be changed to increase the gain of U1. R4, R7, and C1 are the antialiasing filter, but they can be reconfigured as an attenuator or alternate filter configuration. R5, R6, and C4 form the RC filter between the ADC driver and ADC input that limits the amount of out-of-band noise arriving at the ADC input and attenuates the kickback voltage from the switched capacitors in the ADC's input.[4]

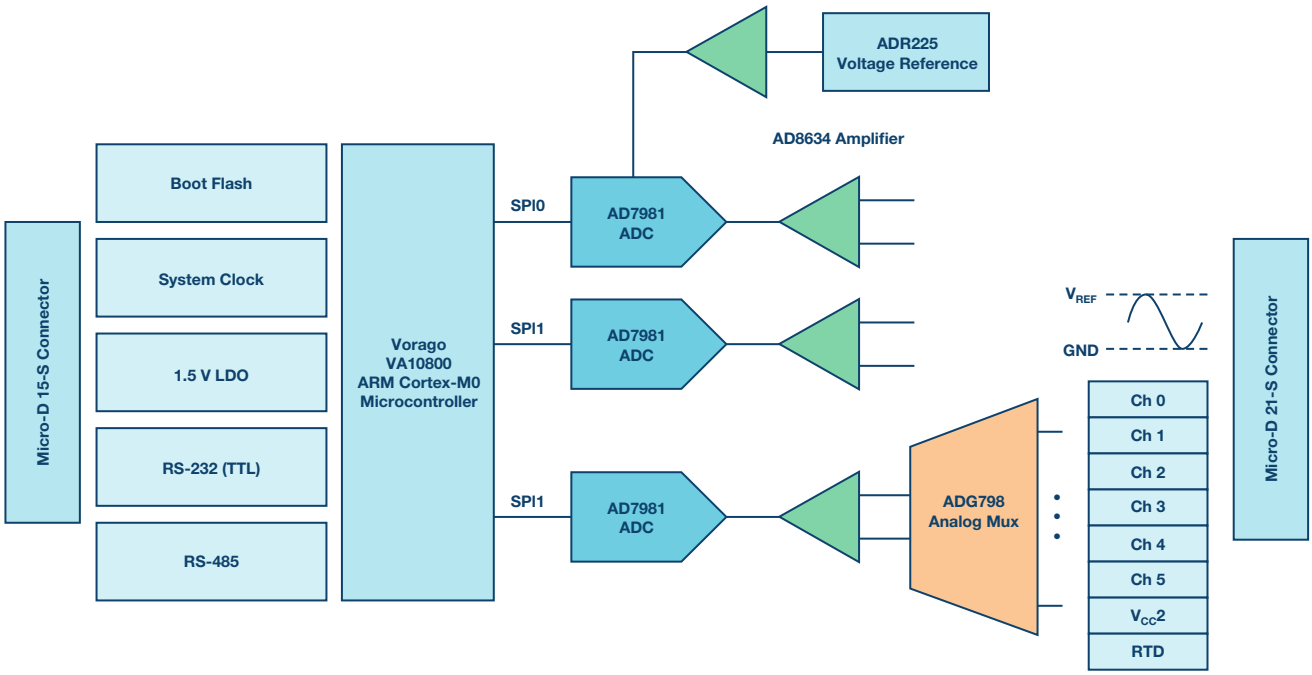

Figure 3. High temperature reference platform block diagram.

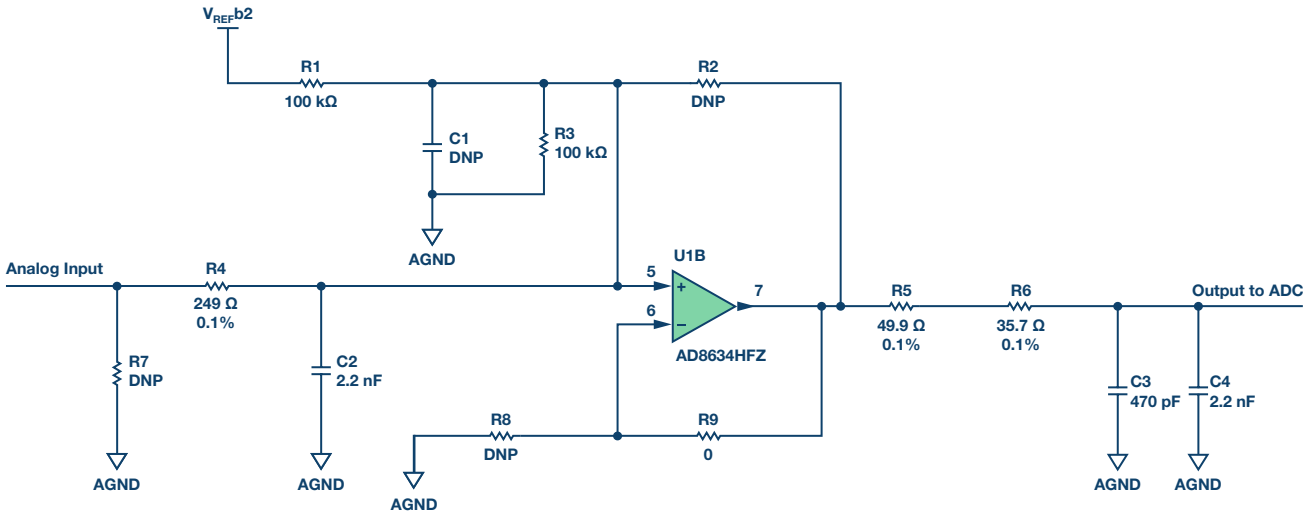

Figure 4. ADC driver configuration.

This platform was designed to take advantage of several key features of the AD7981 ADC. This 16-bit, 600 kSPS converter is capable of greater than 85 dB typical SINAD and ±0.6 LSB typical INL with a 2.5 V reference and no missing codes. Greater than 90 dB SINAD can be achieved with a 5 V reference, although that was not selected for this platform in order to maintain compatibility with lower voltage systems. Because the ADC core automatically powers down between conversion cycles, ADC power consumption automatically scales linearly with throughput. This allows power savings to be realized when using the converter at lower sampling rates.

Software Overview

Firmware

Firmware for the platform is built upon the FreeRTOS operating system and facilitates simple incorporation of tasks, such as data processing and other forms of communication. Code has been optimized to efficiently complete fast ADC conversions for nonmultiplexed channels 0 and 1, and down to 10 µs for the multiplexed channels 2 through 9. Conversion results can be processed locally, or streamed out of a UART channel at 2 Mbps. The conversion result buffer is 16 kB (8k samples), which can be shared among several channels or dedicated to a single channel. This firmware is provided in open source format to allow customization by the end user and can serve as the basis for end applications.

Data Capture and Analysis Software

Figure 5 shows the data capture and analysis software, which has been designed in .NET to interface with the circuit assembly through a USB-UART-TTL level translator. A well-defined protocol allows communication with the hardware including control and data streaming. Data can be captured in burst modes and also continuously. In addition, data analysis features are included to analyze and verify SNR, THD, and SINAD in the time and frequency domains (for example, FFT). Data can also be logged to files (for example, exported in Excel) for storage or processing in other applications. As with the firmware, the data capture software source code is freely available for customization by the end user.

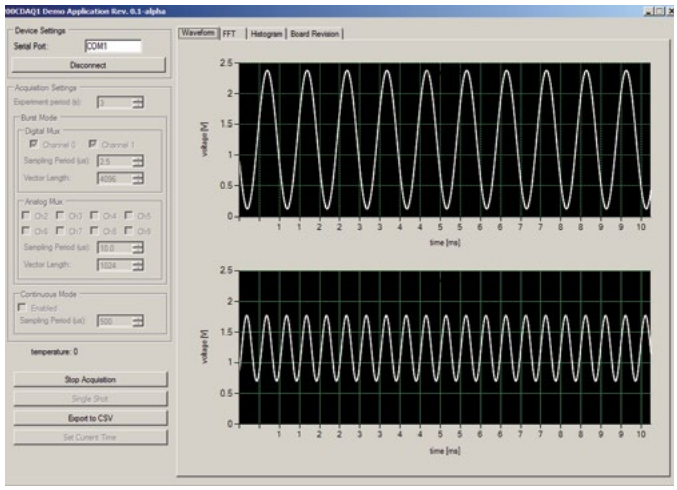

Figure 5. Data capture and analysis software.

High Temperature Construction

This reference platform was constructed using components and other materials that are suitable for 200°C operation. All components used on the assembly are rated for high temperature operation (unless otherwise noted) by the respective manufacturer and are readily available off the shelf from global distributors. The full BOM, PCB artwork, and assembly drawings are freely available as part of the reference design package.

Capacitors

C0G or NP0 dielectric capacitors are used for low value filtering and decoupling. These dielectrics have a very flat coefficient over temperature and are generally more tolerant to board flexing stresses.[5] Additionally, C0G or NP0 type capacitors are recommended for an RC filter that has high Q, low temperature coefficient, and stable electrical characteristics under varying voltages. Small footprint 0805 or less ceramics are used to minimize CTE mismatch between component and PCB. High temperature tantalum capacitors are chosen for bulk energy storage with trade-off considerations between footprint size and ESR.

Resistors

Thin film SMT resistors, automotive grade PATT series, are used for the majority of this design and are readily available in the marketplace. Some thick film SMT resistors are used for specific values and sizes as necessary in the design as well.

Connectors

The board is connectorized with a 200°C rated Micro-D, which is common in high reliability industries. To reduce signal crosstalk, provisions were made for the shell of the connector to be grounded to the PCB in the assembly. For applications where the highest signal integrity and lowest crosstalk are required, high temperature specialty connectors (or no connector) and coaxial or shielded balanced inputs should be utilized to minimize crosstalk.

PCB Design and Layout

The long and narrow PCB form factor was chosen for suitability in downhole applications where circuit boards have to conform to the constraints of a borehole and pressure housing. The circuit board material chosen is a high temperature halogen free polyimide. A 0.093" board thickness was specified for added rigidity and planarity over standard 0.062" thickness boards.

A nickel-gold surface finish is used, where nickel provides a barrier that resists intermetallic growth, and gold provides a good surface for solder joint bonding.

For the chosen 0.093" board thickness, a typical four layer stack-up will involve a ~13 mil copper layer separation with a large 60 mil internal core. At six layers, layer separation is typically 9.5 mil and 28 mil. For this reason, a six layer design was utilized and allows a ground plane next to each signal layer for better noise performance.

Power and digital communication signals feed into one connector and analog signals come in on the opposing connector. This provides good isolation and signal flow between digital and analog domains. The plane split is midboard, with power filtering provided near the split. The digital control lines that do cross the split plane are minimized, and series terminations are provided to minimize coupling of digital noise. The digital and analog ground planes are bonded at a single point with a copper net tie to provide a low impedance return path to the driving sources.

The multiplexer control signals run the length of the analog section but are routed to keep away from critical analog signal paths. In practice these multiplex control lines change synchronously with the acquisition measurement and crosstalk effects are thus minimized.

Solder

Sn95/Sb05 was chosen to provide a high enough melting point (>230°C) over the 200°C operational temperature and provide good workability and general assembly house availability.

Board Mounting

The post mounts provided on this board are for convenience only and are only useful for mounting in bench testing or lab situations. They are not suitable mounts for high shock and vibration environments. For use in high shock and vibration environments, the board can be prepared by first staking components to the board with epoxy. Susceptible items like the IDC headers can be encapsulated or removed from the assembly. Typical mounting for downhole or other harsh environment applications would involve a rail mount system that secures the perimeter of the board with flexible shock mount gaskets. Alternatively, the assembly can be fully encapsulated and potted inside mounting hardware that is then affixed to the chassis or enclosure.

More information on the appropriate parts can be found in the article "A Low Power Data Acquisition Solution for High Temperature Electronics Applications."[2]

Performance Test Results

Extensive testing was performed on several boards to assess typical performance over temperature, along with a 200 hour temperature soak at 200°C ambient to qualify the assembly process and board reliability.

The ac and dc signal chain performance is a key precision measurement metric of a SAR ADC-based precision data acquisition system. A ratiometric and robust platform achieves above –100 dB crosstalk and ±60 mV max offset drift at 200°C when running the ADC at 600 kSPS. For the ac test, a low distortion 1 kHz tone is used as the input signal and the board is powered with +5 V_{DC}/–2.5 V_{DC} analog supplies. An FFT of this tone acquired at 400 kSPS with spectrum analysis calculations are shown in Figure 6. Better than 84 dB SNR and –96 dB THD is obtained at 200°C. Figure 7 shows the SNR and SINAD and Figure 8 shows THD over temperature for the nonmultiplexed channels with the same input tone.

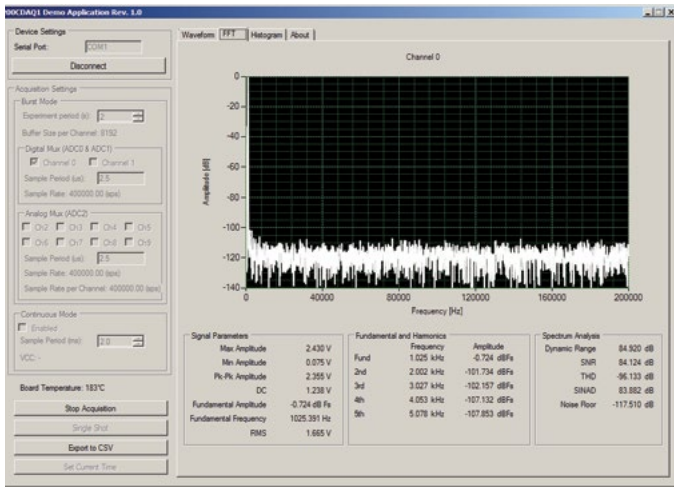

Figure 6. FFT and spectrum analysis at 200°C.

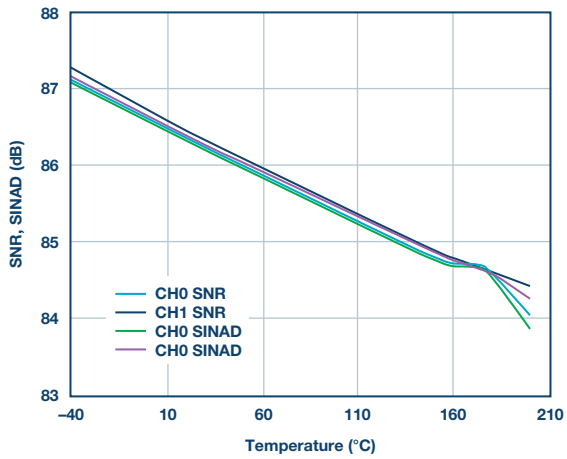

Figure 7. SNR and SINAD over temperature.

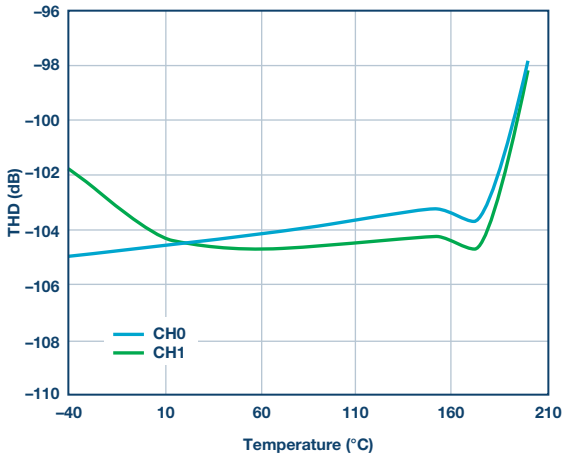

Figure 8. THD over temperature.

Current consumption on the analog and digital rails was measured over temperature as shown in Figure 9. Total power consumption at room temperature is 155 mW, increasing to 225 mW at 200°C. Power consumption on the 3.3 V rail is dominated from the microcontroller, which is running at full clock rate, and a precision oscillator. The converters were set to acquire a burst of 8192 samples every second.

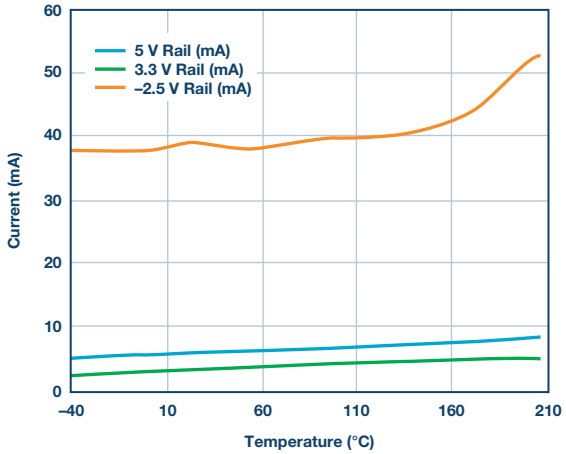

Figure 9. Current consumption for 2.5 V, 3 V, and 5 V rails

Test results of additional parameters can be found on the reference platform, which is qualified and characterized for 200°C operation.

Example Applications

In many applications in oil and gas exploration, aerospace, and heavy industrial, accelerometers are used both for orientation and vibration sensing. Accelerometers with analog outputs can give the highest degree of accuracy with flexibility to condition the sensor output as appropriate for the application.

The ADXL206 is a precision, low power, complete dual-axis iMEMS® accelerometer for use in high temperature environments. It provides ±5 *g* range and 0.5 Hz ≤ bandwidth ≤ 2.5 kHz. The output of the ADXL206 is centered about ½ V_{CC} and is ratiometric to V_{CC}. If the ADXL206 and the EV-HT-200CDAQ1 share V_{CC} (available on the connector), the V_{CC} reference available on channel S7 of the multiplexer can be used to zero dc offsets and power supply drift. An example circuit is shown in Figure 10. The 0 V to 5 V signal range of the ADXL206 must be scaled by ½ to fit within the 0 V to 2.5 V range of the precision data acquisition system. This is accomplished by first buffering the outputs and then using the attenuators inside the data acquisition system. C2 and C3 set the bandwidth of the ADXL206; the example in Figure 9 shows a bandwidth of 33 Hz. Low bandwidth applications can make use of the multiplexer inputs; for the highest bandwidth and accuracy, the two nonmultiplexed input channels can be used.

Summary

This article introduced a new, highly integrated robust, precision data acquisition reference platform, EV-HT-200CDAQ1, that is qualified and characterized for 200°C operation. This platform allows designers of high temperature electronics systems to use the latest state-of-the-art components for rapid prototyping and evaluation, minimizing development time and time to market. More information on the platform including full design package and software can be found here.

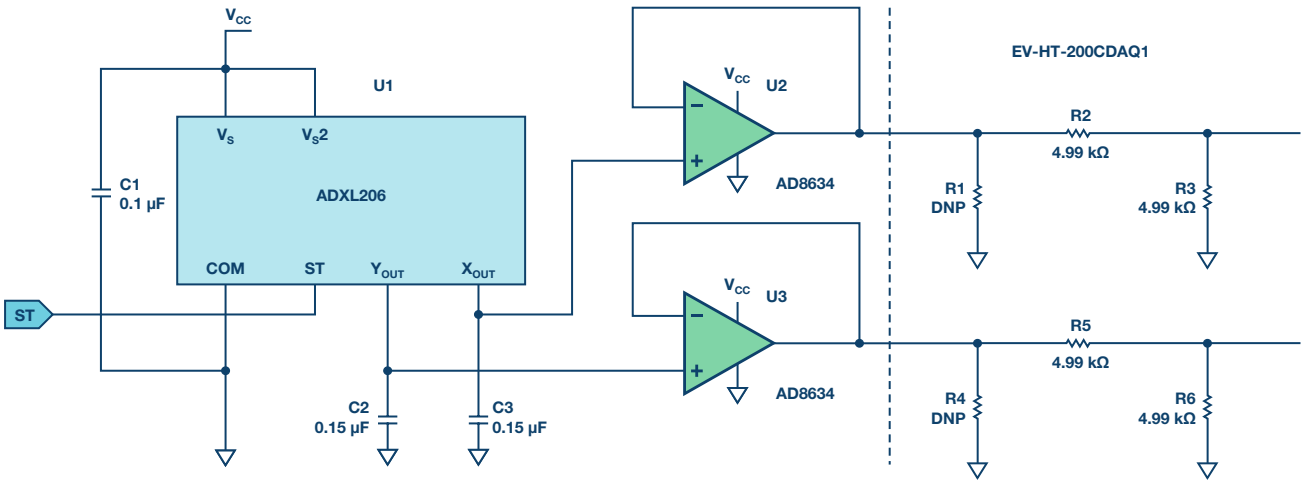

Figure 10. Interfacing high temperature accelerometer to EV-HT-200CDAQ1.

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A Low Power Data Acquisition Solution for High Temperature Electronics Applications

Volume 49, Number 3

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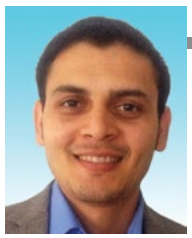

Maithil Pachchigar

Also by this Author:

Pin-Compatible, High Input Impedance ADC Family Enables Ease of Drive and Broadens ADC Driver Selection

Volume 51, Number 4

Vehicle Tracking Systems: Anytime, Anywhere, Anyhow

By **Steve Knoth**

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Background

A vehicle tracking system is ideal for monitoring either a single car or an entire fleet of vehicles. A tracking system consists of automatic tracking hardware and software for data collection (and data transmission if required). The global fleet management market size was valued at USD $8 billion in 2015 and is anticipated to exceed USD $22 billion by 2022, growing at a CAGR of over 20% from 2016 to 2023 (Source: Global Market Insights). The rising demand for commercial vehicles in regions such as Latin America, the Middle East, and Africa also represents a potential growth opportunity. In more developed regions such as Europe and North America, integration of Internet of Things (IoT) technology in vehicles is expected to boost the adoption rate of vehicle tracking systems, although the high cost of integration has slowed this progress. Further, the Asia Pacific vehicle tracking market size is anticipated to witness significant growth over the forecasted period, with Japan, India, and China being the primary driving countries. These emerging markets have high potential, primarily due to their many commercial vehicles.

Active vs. Passive Trackers

Active and passive trackers collect data in the same way and are equally accurate. The main difference between the two types involves time. Active trackers are also called *real-time* trackers, because they transmit data via satellite or a cellular network, which instantly indicates where the vehicle is located. In this way, a computer screen can display this movement in real-time. This makes active tracking the best choice for businesses interested in improving the efficiency of their deliveries and monitoring their employees driving in the field. An active tracker also has *geo-fence* capabilities (think of this feature like a *force field*), providing an alert when the vehicle enters or exits a predetermined location (Source: RMT Corporation). These kinds of systems can also help prevent theft and help recover stolen vehicles. Of course, active GPS tracking devices are more expensive than passive ones and require a monthly service fee.

Passive trackers, on the other hand, are less costly, are smaller, and are easier to conceal. Their downside is that they have limited data storage. They store the information on the device instead of transmitting the data to a remote location. The tracker must be removed from the vehicle and plugged into a computer to view any of its information. These systems are good for people tracking their mileage for work purposes, or for businesses interested in reducing the misuse of their vehicles. Also, they are often chosen for monitoring the actions of people as well (think of detective work). Passive trackers are a good choice if immediate feedback is not required and there is a plan to regularly check the device's data.

Both types of trackers are portable in nature and have a relatively small form factor. Therefore, battery power is required, as is backup capability to preserve data in case of power loss. Due to the higher automotive system voltages and currents required to charge the battery (typically a single-cell Li-ion cell), a switchmode charger is desirable for its higher charging efficiency when compared to a linear battery charging IC, as less heat in the form of power dissipation is generated. In general, embedded automotive applications have input voltages up to 30 V, with some even higher. In these GPS tracking systems, a charger with the typical 12 V to single-cell Li-ion battery (3.7 V typical) with added protection to much higher input voltages (in case of voltage transients from battery excursions), plus some sort of backup capability would be ideal.

Design Issues for Battery Charging ICs

Traditional linear topology battery chargers are often valued for their compact footprints, simplicity, and modest cost. However, drawbacks of traditional linear chargers have included limited input and battery voltage ranges, higher relative current consumption, excessive power dissipation (heat generation), limited charge termination algorithms, and lower relative efficiency. On the other hand, switchmode battery chargers are popular

choices due to their topology, flexibility, multichemistry charging, their high charging efficiencies that minimize heat to enable fast charge times, and their wide operating voltage ranges. Of course, trade-offs always exist. Some downsides of switching chargers include relatively high cost, more complicated inductor-based designs, potential noise generation, and larger footprint solutions. Modern lead acid, wireless power, energy harvesting, solar charging, remote sensor, and embedded automotive applications are predominantly powered by switchmode chargers for the positive reasons stated previously.

Traditionally, a tracker's backup power management system for batteries consisted of multiple ICs, a high voltage buck regulator, and a battery charger, plus all the discrete components; not exactly a compact solution. Hence, early tracking systems were not very compact in form factor. A typical application for a tracking system uses an automotive battery and a 1-cell Li-ion battery for storage and backup.

Why is it then that a more highly integrated power management solution is needed for tracking systems? Primarily, it is needed to reduce the size of the tracker itself; smaller is better in this market. Furthermore, there are requirements for safely charging the battery and protecting the IC against voltage transients, a need for system backup in case system power goes away or fails, and for powering the relatively lower rail voltages of the general packet radio service (GPRS) chipsets at ~4.45 V.

Power Backup Manager

An integrated power backup manager and charger solution, which solves the outlined objectives requires the following attributes:

- Synchronous buck topology for high efficiency
- Wide input voltage range to accommodate a variety of input power sources, plus protection against high voltage transients
- Proper battery charge voltage to support the GPRS chipset
- Simple and autonomous operation with onboard charge termination (no microcontroller needed)
- PowerPath control for seamless switchover between input power and backup power during a power fail event; it also needs to provide reverse blocking if a shorted input occurs
- Battery backup capability for system load power when the input is not present or fails
- Small and low profile solution footprints due to space constraints
- Advanced packaging for improved thermal performance and space efficiency

To address these specific needs, Analog Devices recently introduced the LTC4091—a complete, Li-ion battery backup management system for 3.45 V to 4.45 V supply rails that must be kept active during a long duration main power failure. The LTC4091 employs a 36 V monolithic buck converter with adaptive output control to provide power to the system load and enable high efficiency battery charging from the buck output. When external power is available, the device can provide up to 2.5 A of total output current and up to 1.5 A of charge current for a single-cell, 4.1 V or 4.2 V Li-Ion battery. If the primary input source fails and can no longer power the load, the LTC4091 provides up to 4 A to the system output load from the backup Li-ion battery via an internal diode, and relatively unlimited current if an external diode transistor is used. To protect sensitive downstream loads, the maximum output load voltage is 4.45 V. The device's PowerPath control provides a seamless switchover between input power and backup power during a power fail event and enables reverse blocking with a shorted input. Typical applications for the LTC4091 include fleet and asset tracking, automotive GPS data loggers and telematics systems, security systems, communications, and industrial backup systems.

The LTC4091 includes 60 V absolute maximum input overvoltage protection, making the IC immune to high input voltage transients. The LTC4091's battery charger provides two pin selectable charge voltages optimized for Li-ion battery backup applications: the standard 4.2 V and a 4.1 V option that trades off battery run time for increased charge/discharge cycle life. Other features include soft-start and frequency fold-back to control output current during startup and overload, as well as trickle charge, automatic recharge, low battery precharge, charge timer termination, thermal regulation, and a thermistor pin for temperature-qualified charging.

The LTC4091 is housed in a low profile (0.75 mm) 22-lead 3 mm × 6 mm DFN package with a backside metal pad for excellent thermal performance. The device operates from –40°C to +125°C. Figure 1 shows its typical application schematic.

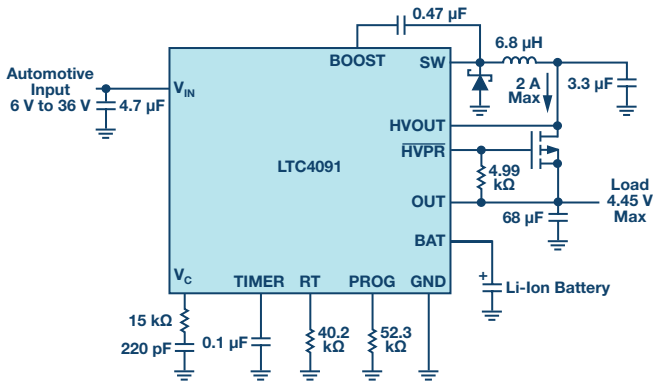


Figure 1. LTC4091 typical application schematic.

Thermal Regulation Protection

To prevent thermal damage to the IC or surrounding components, an internal thermal feedback loop automatically decreases the programmed charge current if the die temperature rises to approximately 105°C. Thermal regulation protects the LTC4091 from excessive temperature due to high power operation or high ambient thermal conditions, and allows the user to push the limits of the power handling capability with a given circuit board design without risk of damaging the LTC4091 or external components. The benefit of the thermal regulation loop is that charge current can be set according to actual conditions, rather than worst-case conditions with the assurance that the battery charger will automatically reduce the current in worst-case conditions.

Automotive Cold-Crank Ride Through

Automotive applications experience large dips in supply voltage, such as during a cold-crank event, which can cause the high voltage switching regulator to lose regulation, resulting in excessive V_C voltage and consequently excessive output overshoot when V_{IN} recovers. To prevent overshoot when recovering from a cold-crank event it is necessary to reset the LTC4091's soft-start circuit via the RUN/SS pin. Figure 2 below shows an example of a simple circuit that automatically detects a brown-out condition and resets the RUN/SS pin, re-engaging the soft-start feature and preventing damaging output overshoot.

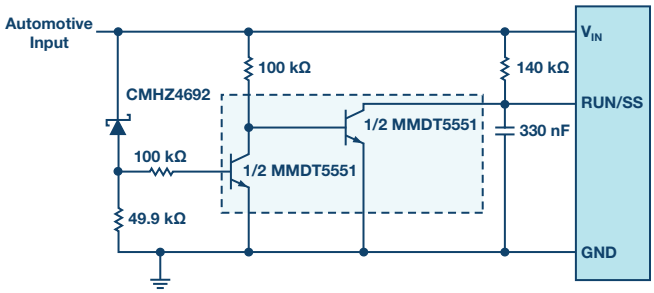
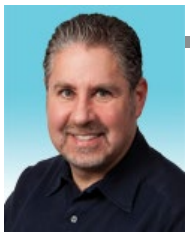


Figure 2. Cold-crank ride-through circuit.

Conclusion

The adoption rates of automotive and fleet vehicle tracking systems are on the rise. Modern tracker form factors have shrunk and features have grown to include active data transmission for real-time tracking. Furthermore, backup capability and lower voltages to power the system GPRS chipset are needed. Analog Devices' LTC4091 is a high voltage, high current buck battery charger and PowerPath backup manager with thermal regulation and other extensive protection that comprises a 1-chip, compact, powerful, and flexible solution for vehicle tracking applications, thus making a designer's task simpler and easier.



Steve Knoth

Steve Knoth [steve.knoth@analog.com] is a senior product marketing engineer in Analog Devices' Power by Linear Group. He is responsible for all power management integrated circuit (PMIC) products, low dropout regulators (LDOs), battery chargers, charge pumps, charge pump-based LED drivers, supercapacitor chargers, low voltage monolithic switching regulators, and ideal diode devices. Prior to joining Analog Devices (former Linear Technology) in 2004, Steve had held various marketing and product engineering positions since 1990 at Micro Power Systems, Analog Devices, and Micrel Semiconductor. He earned his bachelor's degree in electrical engineering in 1988 and a master's degree in physics in 1995, both from San Jose State University. Steve also received an M.B.A. in technology management from the University of Phoenix in 2000. In addition to enjoying time with his kids, Steve can be found tinkering with pinball/arcade games or muscle cars; and buying, selling, and collecting vintage toys and movie/sports/automotive memorabilia.

Rarely Asked Questions—Issue 151 High-Side Current Sensing

By **Aaron Schultz**

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Question:

Is placing a 100 Ω resistor in front of a MOSFET gate required for stability?

Answer:

Introduction

Ask any experienced electrical engineer—for example, Gureux, the professor in our story—about what to put in front of a MOSFET gate and you will probably hear "a resistor, approximately 100 Ω." Despite this certainty, one still wonders why and questions the utility and the resistance value. Because of that curiosity, we will examine these questions in the following example. Neubean, a young applications engineer, looks to test if it is actually necessary to place a 100 Ω resistor in front of a MOSFET gate for stabilization. Gureux, an applications engineer with 30 years of experience, monitors his experiments and gives his expert opinion along the way.

Introducing the HS Current Sense

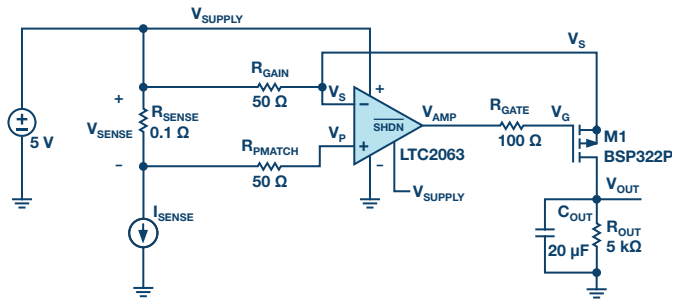

Figure 1. High-side current sense.

The circuit in Figure 1 shows a typical example of high-side current sense. Negative feedback tries to force the voltage V_{SENSE} upon gain resistor R_{GAIN}. The current through R_{GAIN} flows through P-channel MOSFET (PMOS) to resistor R_{OUT}, which develops a ground referenced output voltage. The overall gain is

$$V_{OUT} = I_{SENSE} \times R_{SENSE} \times \frac{R_{OUT}}{R_{GAIN}}$$

Optional capacitance C_{OUT} across the resistor R_{OUT} serves to filter the output voltage. Even if the drain current of the PMOS quickly follows the sensed current, the output voltage will exhibit a single-pole exponential trajectory.

The resistor R_{GATE} in the schematic separates the amplifier from the PMOS gate. What is the value? "100 Ω, of course!" the experienced fellow Gureux might say.

Trying Out Lots of Ω

We find our friend Neubean, a student of Gureux's, pondering this gate resistor. Neubean thinks that with enough capacitance from the gate to the source, or with enough gate resistance, he should be able to cause stability problems. Once it is clear that R_{GATE} and C_{GATE} interact detrimentally, then it will be possible to debunk the myth that 100 Ω, or in fact any gate resistance, is automatically appropriate.

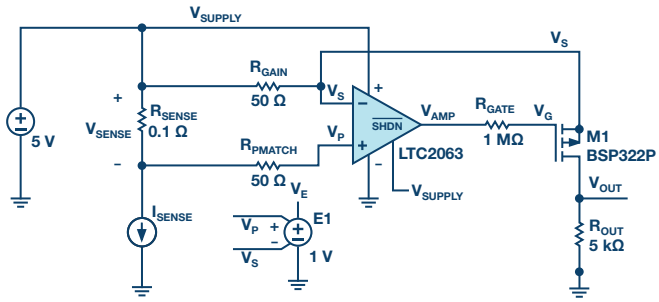

Figure 2. High-side current sense simulation.

Figure 2 shows an example of an LTspice simulation used to highlight the circuit behavior. Neubean runs simulations to show the stability problems that he believes will occur as R_{GATE} increases. After all, the pole from R_{GATE} and C_{GATE} ought to erode the phase margin associated with the open loop. Yet, to Neubean's amazement, no value of R_{GATE} shows any sort of problems in the time domain response.

Turns Out, the Circuit Is Not So Simple

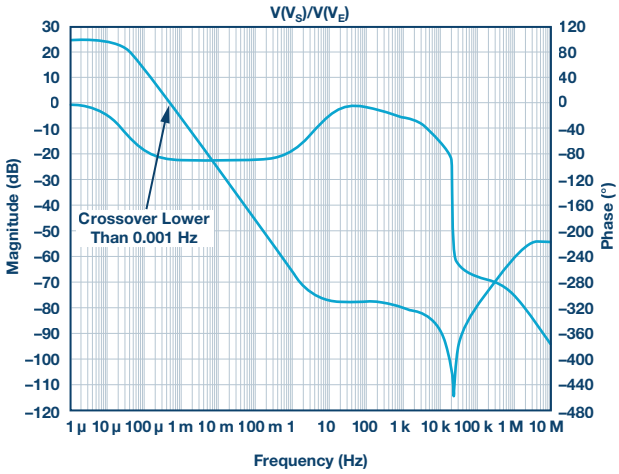

Figure 3. Frequency response from the error voltage to the source voltage.

In looking at the frequency response, Neubean realizes he needs to take care of identifying what the open loop response is. The forward path that forms the loop, when combining the unity negative feedback, starts from the difference and ends at the resulting negative input terminal. Neubean then simulates and plots $V_S/(V_P - V_S)$, or V_S/V_E. Figure 3 shows a plot's frequency domain plot for this open-loop response. In the Bode plot of Figure 3, there is very little dc gain and no evidence of phase margin problems at the crossover. In fact, the plot overall looks very strange as the crossover frequency is less than 0.001 Hz.

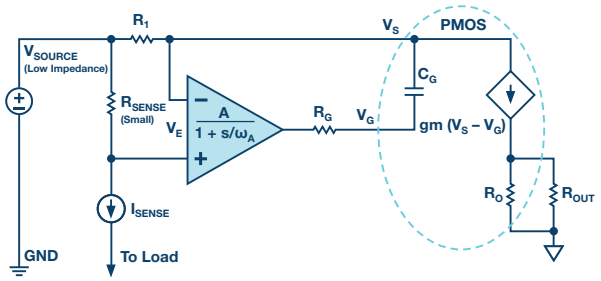

Figure 4. High-side sense circuit as a block diagram.

The decomposition of the circuit into a control system appears in Figure 4. The LTC2063, like almost all voltage feedback op amps, starts with high dc gain and a single pole. The op amp gains the error signal and drives the PMOS gate through the $R_{GATE} - C_{GATE}$ filter. The C_{GATE} and PMOS source connect together to the –IN input of the op amp. R_{GAIN} connects from that node to the low impedance source. Even in Figure 4, it might appear that the $R_{GATE} - C_{GATE}$ filter should cause stability problems, particularly if R_{GATE} is much larger than R_{GAIN}. After all, the C_{GATE} voltage, which directly affects the R_{GAIN} current in the system, lags op amp output changes.

Neubean offers one explanation to why perhaps R_{GATE} and C_{GATE} do not cause instability: "Well, the gate source is a fixed voltage, so then the $R_{GATE} - C_{GATE}$ circuit is irrelevant. All you need to do is adjust the gate and the source follows. It's a source follower."

His more experienced colleague Gureux says, "Actually, no. This is only valid when the PMOS operates normally as a gain block in the circuit."

Thus prompted, Neubean thinks about the math—what if we could directly model the response of the source of the PMOS to the gate of the PMOS? In other words, what is $V(V_S)/V(V_G)$? Neubean runs to the white board and writes the following equations.

$$\frac{V_S}{V_E} = \frac{A}{(1+\frac{s}{\omega_A})} \times \frac{gm \times R_1 + s \times R_1 \times C_G}{gm \times R_1 + s \times R_1 \times C_G + (1+\frac{s}{\omega_G})}$$

with

$$\omega_G = \frac{1}{R_G \times C_G}$$

op amp gain A, and op amp pole ωA.

$$\frac{V_S}{V_G} = \frac{gm + s \times C_G}{gm + s \times C_G + \frac{1}{R_1}}$$

Neubean immediately identifies the important term gm. What is gm? For a MOSFET,

$$gm = \sqrt{2 \times Kn \times Id}$$

Looking at the circuit back in Figure 1, a light bulb goes off in the Neubean's head. With zero current through R_{SENSE}, the current through the PMOS ought to be zero. With zero current, gm is zero, because the PMOS is effectively off, not being used, unbiased, and has no gain. When gm = 0, V_S/V_E is 0 at 0 Hz and V_S/V_G is 0 at 0 Hz, so there is no gain at all and the plots in Figure 3 may be valid after all.

Try to Go Unstable with the LTC2063

Armed with this revelation, Neubean quickly tries a few simulations with non-zero I_{SENSE}.

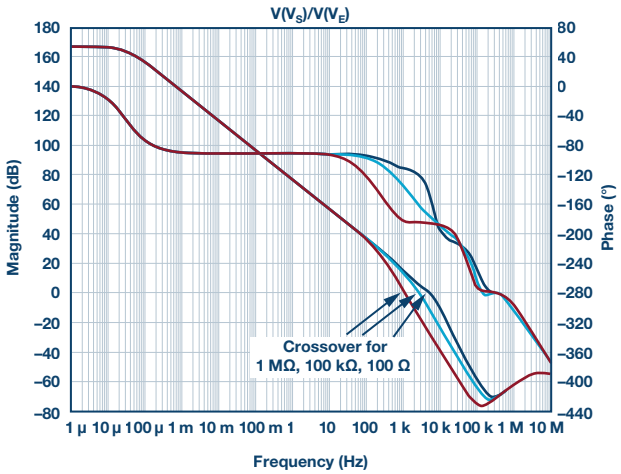

Figure 5. Frequency response from the error voltage to the source voltage, non-zero sense current.

Figure 5 shows what looks like a much more normal gain/phase plot of the response from V_E to V_S, crossing from >0 dB to <0 dB. Figure 5 should show about 2 kHz, with lots of PM at 100 Ω, a bit less PM at 100 kΩ, and even less with 1 MΩ, but not unstable.

Neubean goes to the lab and dials up a sense current with the high-side sense circuit LTC2063. He inserts a high R_{GATE} value, first 100 kΩ and then 1 MΩ, expecting to see unstable behavior or at least some kind of ringing. Unfortunately, he does not.

He tries to increase the drain current in the MOSFET first by using more I_{SENSE} and then by using a smaller R_{GAIN} resistance. Nothing works to destabilize the circuit.

He returns to the simulation and tries to fill a phase margin with non-zero I_{SENSE}. Even in simulation it seems difficult, if not impossible, to find instability or low phase margin.

Neubean finds Gureux and asks why he is failing to destabilize the circuit. Gureux advises him to do the numbers. Neubean is used to riddles from Gureux, so he examines what might be the actual pole associated with R_{GATE} and the total gate capacitance. With 100 Ω and 250 pF, the pole is at 6.4 MHz; with 100 kΩ, the pole is at 6.4 kHz; and with 1 MΩ, the pole is at 640 Hz. The LTC2063 gain bandwidth product (GBP) is 20 kHz. When the LTC2063 takes gain, the closed-loop crossover frequency can easily slide below any effect of the $R_{GATE} – C_{GATE}$ pole.

Yes, You Can Go Unstable

Realizing that the op amp dynamics need to continue up into the range of the $R_{GATE} – C_{GATE}$ pole, Neubean chooses a higher gain bandwidth product. The LTC6255 5 V op amp will directly fit into the circuit with a higher 6.5 MHz GBP.

Eagerly, Neubean tried a simulation with current, the LTC6255, 100 kΩ gate resistance, and with 300 mA sense current.

Neubean then proceeds to add R_{GATE} in simulation. With enough R_{GATE}, an extra pole can destabilize a circuit.

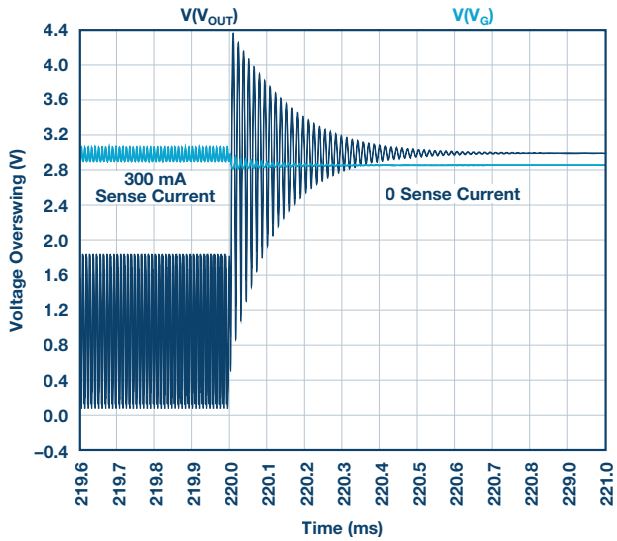

Figure 6. A time domain plot with ringing.

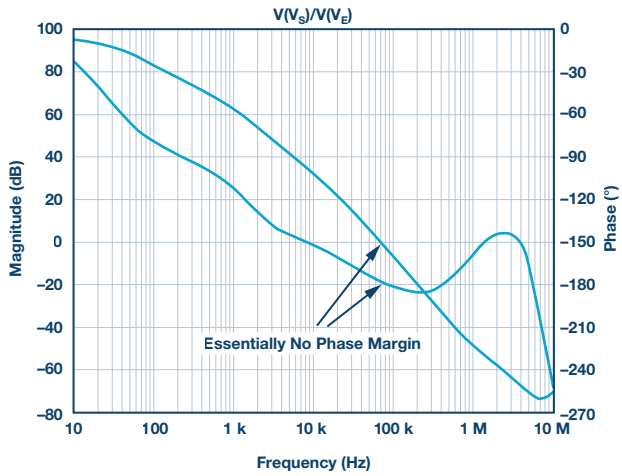

Figure 7. A normal Bode plot once we add current, V_E to V_S, with terrible phase margin.

Figure 6 and Figure 7 show simulation results with high R_{GATE} values. At a constant 300 mA sense current, this simulation shows instability.

Lab Results

Wanting to see if the circuit might act badly while sensing a non-zero current, Neubean tries the LTC6255 with a step changing load current and uses three different R_{GATE} values. I_{SENSE} transitions from a base of 60 mA to a higher value of 220 mA enabled by a momentary switch that brings in more parallel load resistance. There is no zero I_{SENSE} measurement, because it is already shown that the MOSFET gain is too low in that case.

Indeed, Figure 8 finally shows truly compromised stability with 100 kΩ and 1 MΩ resistors. Because the output voltage is heavily filtered, the gate voltage becomes the detector for ringing. Ringing denotes poor or negative phase margin, and ringing frequency indicates crossover frequency.

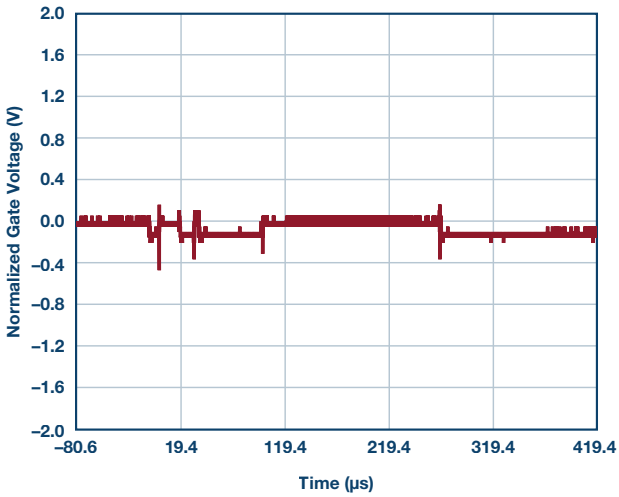

Figure 8. R_{GATE} = 100 Ω, current from low to high transient.

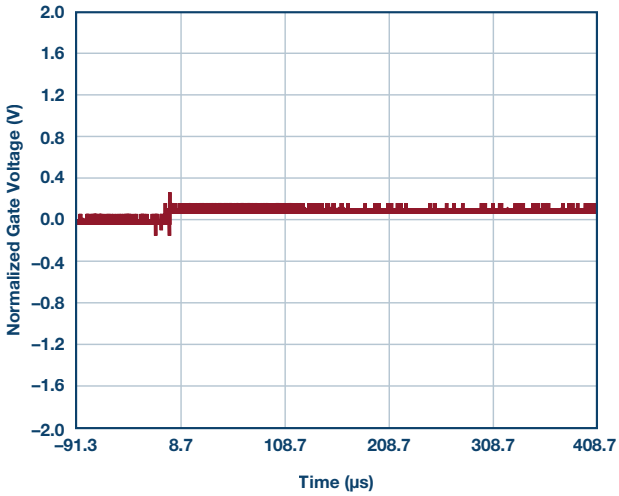

Figure 9. R_{GATE} = 100 Ω, current from high to low transient.

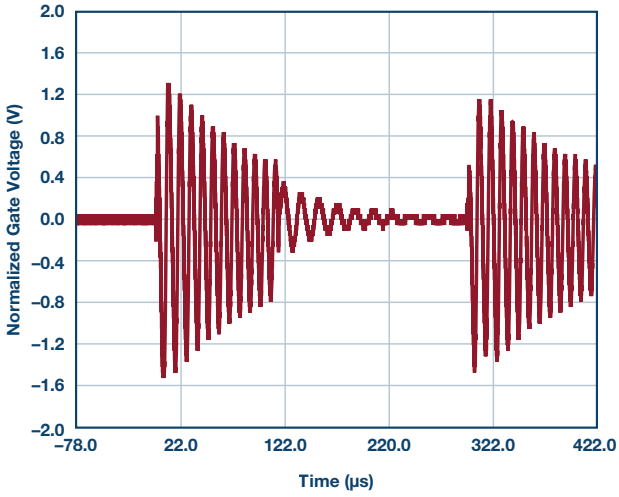

Figure 10. R_{GATE} = 100 kΩ, current from low to high transient.

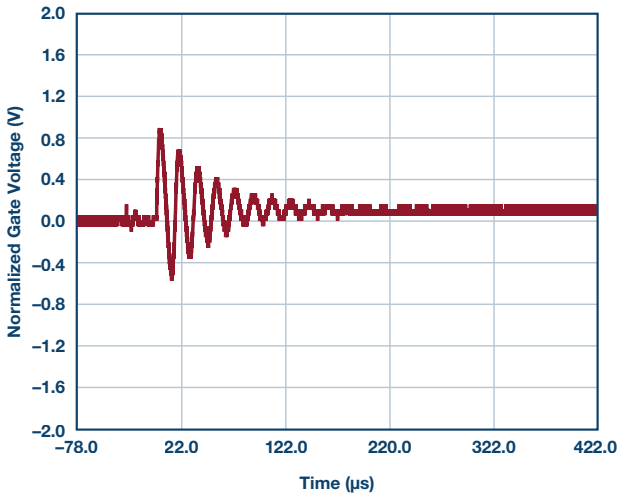

Figure 11. R_{GATE} = 100 kΩ, current from high to low transient.

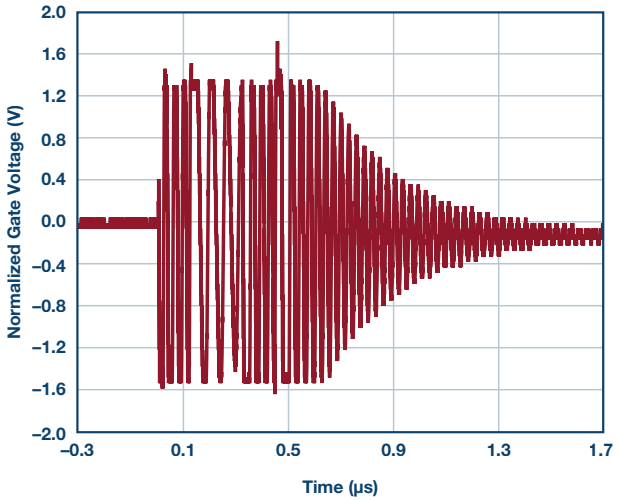

Figure 12. R_{GATE} = 1 MΩ, current from low to high transient.

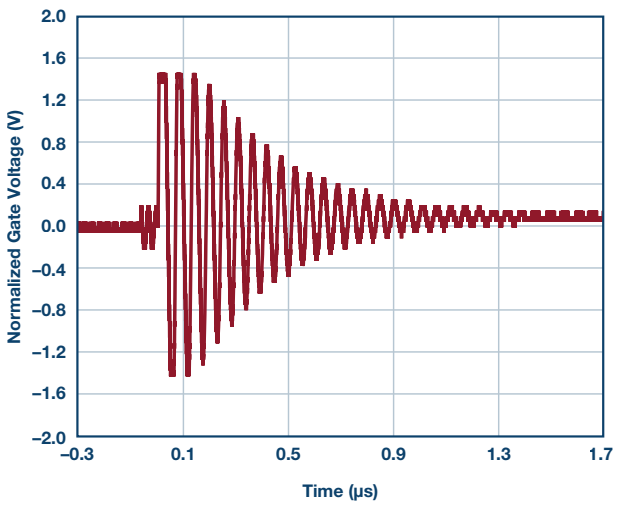

Figure 13. R_{GATE} = 1 MΩ, current from high to low transient.

A Moment to Brainstorm

Neubean realizes that he has seen many high-side integrated current sense circuits and, unfortunately, there is no chance for an engineer to decide on gate resistance, because everything is inside the part. Examples that came to his mind were AD8212, LTC6101, LTC6102, and LTC6104 high voltage, high-side current sense devices. In fact, the AD8212 uses a PNP transistor rather than a PMOS FET. He tells Gureux, "Eh, it doesn't really matter, because modern devices already solve this problem."

As though expecting this comment, almost cutting off Neubean before his last word, the professor responds: "Let's say you want a combination of extremely low supply current and zero-drift input offset, such as in a remotely located battery-powered instrument. You might want an LTC2063 or LTC2066 as the primary amplifier. Or, perhaps, you need to measure a low level current level perhaps through a 470 Ω shunt as accurately and noiselessly as possible; in that case you might want to use the ADA4528, which has rail-to-rail input capability. In these cases you will need to deal with the MOSFET drive circuitry."

And So …

Clearly, then, it is possible to destabilize the high-side current sense circuit by using too large of a gate resistor. Neubean relates this finding to his willing teacher Gureux. Gureux notes that R_{GATE} can in fact destabilize the circuit, but the initial inability to find this behavior drew from a wrongly formulated problem. There needed to be gain, which in this circuit required there to be non-zero signal being measured.

Gureux replies, "Sure, when a pole erodes the phase margin at a crossover, ringing happens. But your 1 MΩ of added gate resistance is absurd—even 100 kΩ is crazy. Remember, it is always good to try to limit the output current of an op amp in case it tries to swing a gate capacitance from one rail to another rail."

Neubean agrees. "So what value of resistance do I use?"

Gureux notes confidently, "100 Ω."

Aaron Schultz

Aaron Schultz [aaron.schultz@analog.com] is an applications engineering manager in the LPS business unit. His multiple system engineering roles in both design and applications have exposed him to topics ranging across battery management, photovoltaics, dimmable LED drive circuits, low voltage and high current dc-to-dc conversion, high speed fiber optic communication, advanced DDR3 memory R&D, custom tool development, validation, and basic analog circuits, while over half of his career has been spent in power conversion. He graduated from Carnegie Mellon University in 1993 and MIT in 1995. By night he plays jazz piano.

Notes

Notes

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