Analog Dialogue

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Your Engineering Resource for Innovative Design

Celebrating Fifty Years

- **Ray Stata Remembers:** A Note from Our First Editor
- **The Best of *Analog Dialogue*:** Highlights from Five Decades of Innovation
- **Six New Articles:** From Achieving Power Savings to Addressing Spur Issues, Space Constraints, and Noise

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ANALOG DEVICES

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In This Issue

Ray Stata Remembers

We are proud to celebrate the 50th anniversary of *Analog Dialogue* with the first edition published in 1967—just two years after the company was founded. *Analog Dialogue*, now the longest published corporate technical journal, has survived budget cuts and shifting priorities over many decades, because it is highly valued by our customers. In the past three months alone, nearly 240,000 *Analog Dialogue* site visitors have clicked to download the journal and its articles 90,000 times.

Written by Engineers for Engineers

Our customers are engineers. From the earliest days, our customers wanted more than innovative products, they wanted detailed technical information about how the products were designed, about the limitations of their performance, and about how to apply them. That was and continues to be the purpose of *Analog Dialogue*.

Analog Devices' business strategy was to continuously push the state of the art in product performance and capability. Customers looked to us to keep them informed about what was possible, not only through *Analog Dialogue,* but also through comprehensive data sheets, application notes, and tutorial handbooks. Consistently publishing high quality technical material takes a lot of hard work, resources, and discipline, but we do it because our technical community understands that this is an important part of the job and customers value this contribution as much as they value innovative products.

Responding, Adapting, and Growing for Five Decades

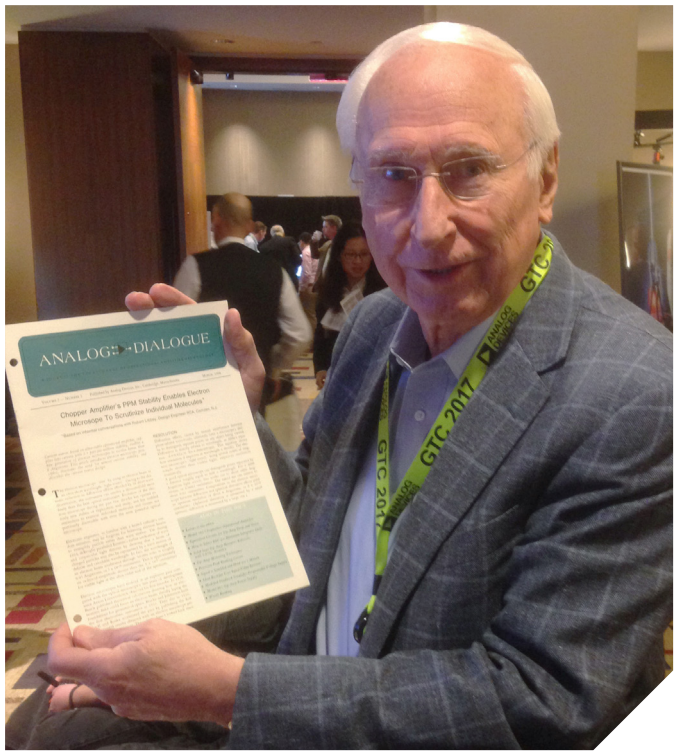
Few companies survive—let alone thrive—for 50 years, because they fail to sense and respond to change in the environment. Analog Devices reinvented itself three times over its 50-year history, as it shifted from module to IC technology; from low volume industrial and military markets to high volume communication and consumer markets; and from components to system-level ICs. The company continually expanded its product base from operational amplifiers to converters, RF, DSP, sensors, and power management to offer more complete solutions for both analog and digital signal processing products and systems.

The tagline and content of *Analog Dialogue* tracked the evolution of the company. The tagline for the premiere edition in 1967 read "A Journal for the Exchange of Operational Amplifier Technology," to reflect the initial focus on op amps.

But in 1969, the tagline was changed to "A Journal for the Exchange of Analog Circuit Technology," as the company diversified into converter products and other analog function circuits.

In 1971, *Analog Dialogue* was now "A Forum for the Exchange of Circuit Technology: Analog and Digital, Monolithic, and Discrete." ADI had entered the IC business and developed mixed analog and digital process technology for monolithic IC converters.

In 1979, the tagline was updated to "A Forum for the Exchange of Circuits and Systems for Measurement and Control," as for a brief time ADI experimented with more complete computerized systems for measurement and control.

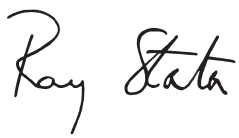


Ray Stata poses with an early edition of Analog Dialogue magazine.

In 1984, *Analog Dialogue* was described as "A Forum for the Exchange of Circuits, Systems, and Software for Real-World Signal Processing." The company had entered the DSP market, which broadened its vision to include both analog and digital signal processing and evolution toward more complete solutions, including software and algorithms.

Most recently, in 2016, the journal underwent a major redesign to reflect ADI's new Ahead of What's Possible brand and mission, and to become "Your Engineering Resource for Innovative Design." The way in which we support and collaborate with customers today involves consideration of not just hardware and signal processing capabilities, but also in how we combine these with deep domain expertise to deliver platforms, systems, and services. The new tagline recognizes *Analog Dialogue* as a tool for customers in their pursuit of innovation on many levels.

There are many factors that account for Analog Devices' long lived success, but no doubt our dedication to high quality technical communications as exemplified by *Analog Dialogue* has contributed much to our leadership, especially in the world of "analog devices." As our products grow ever more complex and specialized in their application, we continue to be committed to making your job easier through our technical publications such as *Analog Dialogue*.



Our First Editor

Ray Stata is Analog Devices Chairman of the Board. He cofounded the company in 1965. Shortly after starting the company, Ray established *Analog Dialogue* in 1967. Created as a resource for engineers, *Analog Dialogue* has provided product information, reflections on industry trends, and insights into both analog and digital circuit design. As *Analog Dialogue's* first editor, Ray set the vision and direction for the publication that continue to guide it more than half a century later.

Flexible ECG Front-End IC Serves Ultralow Power IoT Edge Node Signal Processing Designs

By **David Plourde**

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As system designers search for power efficient, signal conditioning components, they may find that there are very few ICs available under 100 µA supply current and even fewer that include a small package variant. With battery life and board space becoming critical specifications for the growing number of wireless sensor networks (WSNs), the lack of available options can be frustrating. In a search for a low power edge node IoT component, an analog front-end IC such as a heart rate monitor for wearable products may not even show up, or it may be quickly dismissed as too application specific. However, at 50 µA supply current and a tiny 2 mm × 1.7 mm WLCSP package, an ADI ECG front-end IC deserves a closer look. When designers dig deeper, they'll find that its flexible architecture is basically an instrumentation amplifier (IA) and a handful of op amps that can be configured to make some useful ultralow power signal processing circuits for more than just healthcare or fitness applications.

A simplified, single-lead electrocardiogram (ECG) front end is shown in Figure 1. It consists of an indirect current mode IA with a standalone transfer function of

$$IA_{OUT} = \left(1 + \frac{Rfb}{Rg}\right)(V_{IN}) + Ref$$

In the case of this front end, giving a fixed gain of 100. The reference of the IA is driven by the high-pass amplifier (HPA), which is configured as an integrator in feedback with its input tied to IA_{OUT} and crossover frequency set by an external capacitor and resistor. The HPA will force HPDRIVE to whatever voltage is needed to keep HPSENSE and therefore IA_{OUT} at the ref voltage. This circuit creates a first-order high-pass filter with cutoff frequency:

$$fc = \frac{100}{2\pi RC}$$

For diagnostic quality ECG, the cutoff frequency is typically set to 0.05 Hz, while 7 Hz may be suitable for fitness applications detecting heart rate only. The high-pass filter function solves the issue of rejecting the large dc half-cell potential (due to electrode/skin contact) and low frequency baseline wander associated with ECG measurements, while amplifying the higher frequency ECG signal (1 mV to 2 mV). The architecture enables a large gain since the rejection of the dc half-cell potential (up to 300 mV) occurs at the input of the IA. An added benefit is the rejection of the IA's offset and offset drift. Monitoring HPDRIVE with respect to ref will show an inverted version of the input offset being autocorrected.

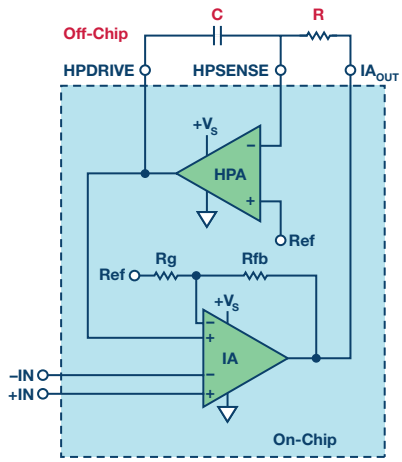


Figure 1. Simplified single-lead ECG front end.

While the design originally targeted ECG applications, any application that requires amplification of small, low frequency signals could benefit from its low power and small size—an electromagnetic water flow sensor, for example. If dc measurements are required, then a simple modification to the circuit is all that is needed. Figure 2 shows a dc-coupled IA with a fixed gain of 100. This is done by removing the R and C from Figure 1 and shorting HPSENSE to HPDRIVE, making the HPA a unity-gain buffer. This will still force the IA reference to the reference voltage. In this case, IA offset voltages should be considered.

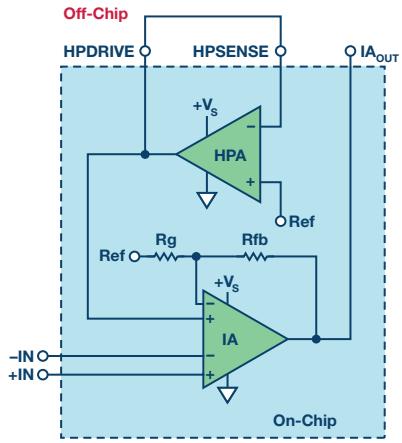


Figure 2. DC-coupled IA with fixed gain of 100.

If a gain of 100 is too high or the bandwidth of 1 kHz is too low, the circuit could be modified, as shown in Figure 3. The HPA is now configured as an inverting amplifier with a gain of –R2/R1and input fed back from IA_{OUT}. The new transfer function can be simplified as follows:

$$IA_{OUT} = \frac{V_{IN}}{\left(\frac{1}{100} + \frac{R2}{R1}\right)} + Ref$$

By configuring the HPA as an attenuator (R2 < R1), gains of less than 100 can be achieved. Due to the 300 mV differential input limit and stability of the circuit, it is not recommended to go below a gain of 10. Table 1 shows some gain configurations to consider.

Table 1. DC-Coupled IA with Different Gain and Bandwidth Configurations

R2	R1	Gain	Bandwidth
Short	Open	100	1.2 kHz
10 kΩ	1 MΩ	50	2.4 kHz
40 kΩ	1 MΩ	20	6.5 kHz
90 kΩ	1 MΩ	10	15.2 kHz

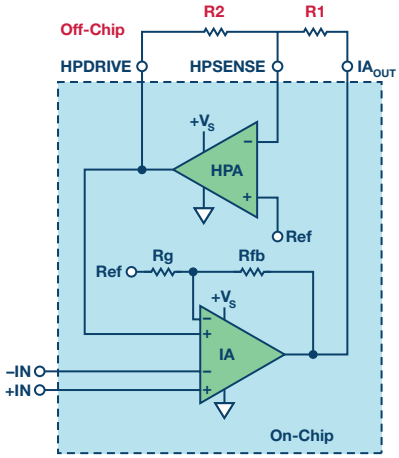


Figure 3. DC-coupled IA with adjustable gain and bandwidth.

If dc precision remains important, then leaving the IA in a gain of 100 and modifying the circuit per Figure 4 provides a means of compensating offsets of the IA and any attached sensors. The adjusted transfer function is shown below:

$$IA_{OUT} = 100\left(V_{IN} - \left(\frac{R2}{R1}\right)V_{TUNE}\right) + Ref$$

V_{TUNE} is the source voltage used to correct for offset voltages and could be provided by a filtered PWM signal from a microcontroller or driven directly from a low power DAC. The HPA remains configured as an inverting amplifier with gain of –R2/R1 and can be used to further adjust the range and resolution of the offset correction. Breaking down V_{IN} to components and plugging into above equation gives target transfer function:

$$V_{IN} = V_{SIGNAL} + V_{OS}$$

$$V_{OS} = \left(\frac{R2}{R1}\right)V_{TUNE}$$

$$IA_{OUT} = (100)\ V_{SIGNAL} + Ref$$

The total offset can be compensated by attaching a sensor without V_{SIGNAL} applied. Just measure IA_{OUT} with respect to reference and adjust (R2/R1) V_{TUNE} until the voltage is close enough to zero.

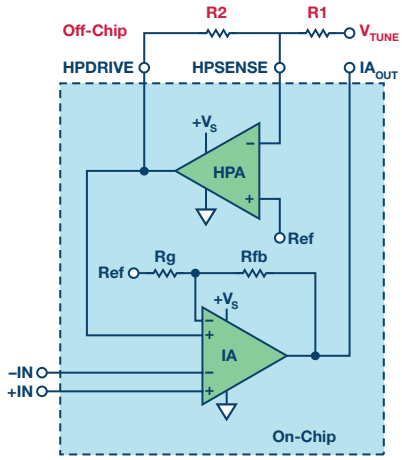


Figure 4. DC-coupled IA with offset compensation.

Before utilizing the above mentioned circuit configurations for low power IoT designs, the rest of the AD8233 ECG front-end solution should be understood. The circuit is detailed in Figure 5. The first op amp, A1, is fully uncommitted and typically used for additional gain and/or filtering after the IA stage. It could be similarly advantageous for other sensor applications. Amplifier A2 is typically used as the right leg drive in ECG solutions. A buffered version of the IA's input common mode appears at the inverting input of A2 where:

$$V_{CM} \sim \frac{+IN + -IN}{2}$$

The amplifier would normally be configured as an integrator with a capacitor placed between RLDFB and RLD, while RLD drives a third electrode, improving the overall system common-mode rejection ratio (CMRR). Unless a useful circuit can be built from this amplifier, it is better to power down the amplifier by tying $\overline{\text{RLDSDN}}$ digital input to ground, and leaving the RLD and RLDFB pins floating.

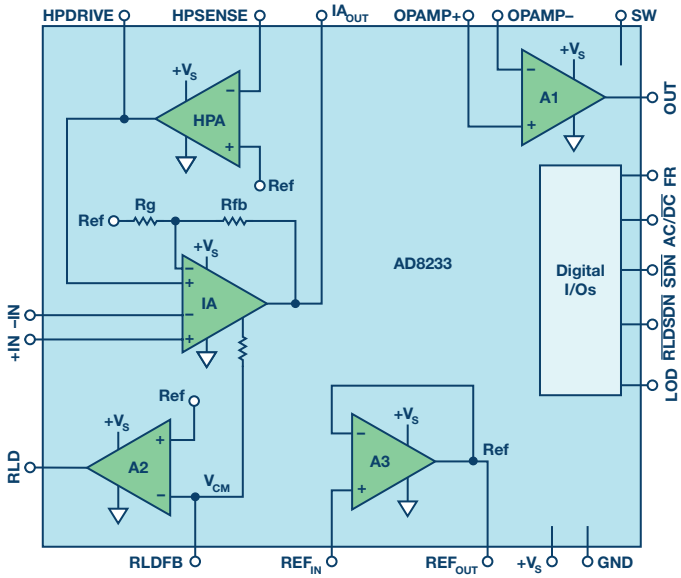


Figure 5. Complete ECG and low power signal conditioning front end.

The third op amp, A3, is an integrated reference buffer that drives the reference voltage both on-chip and off-chip at REF_{OUT}. Usually, REF_{IN} is set to +Vs/2, where the single-supply +Vs can range from 1.7 V to 3.5 V. An easy low power solution is to tie two 10 MΩ resistors as a voltage divider from +Vs to GND, as shown in Figure 6. A capacitor is added between REFIN and GND to help with any noise pickup. Alternatively, REF_{IN} could be driven from an ADC reference or used to level shift the IA output.

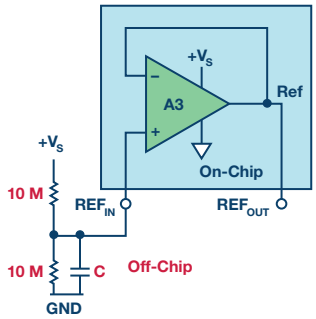


Figure 6. Low power reference.

The digital input FR enables the fast restore function, which is beneficial when using the ac-coupled circuit in Figure 1. It will take some time to charge the external capacitor during startup or in the event of a dc step at the input. When this happens, the IA will rail until the integrator has settled. The automatic fast restore detects this event and switches a smaller resistor in parallel with the external resistor for a fixed amount of time, greatly speeding up the settling time. The SW pin is used to quickly settle a second external high-pass filter if needed.

The AC/DC digital input determines the method for lead off detection used in ECG applications, but could also be utilized as a wire break detection for other sensors at the input. If configured correctly, the digital output LOD would indicate when one of the IA inputs becomes disconnected from the sensor.

In addition to its small size and low active power dissipation, the AD8233 incorporates a shutdown (SDN) pin that drops the total supply current to less than 1 µA. This is convenient when taking infrequent sensor measurements, which greatly increases overall battery life. The wire break detection will remain functional even in shutdown mode.

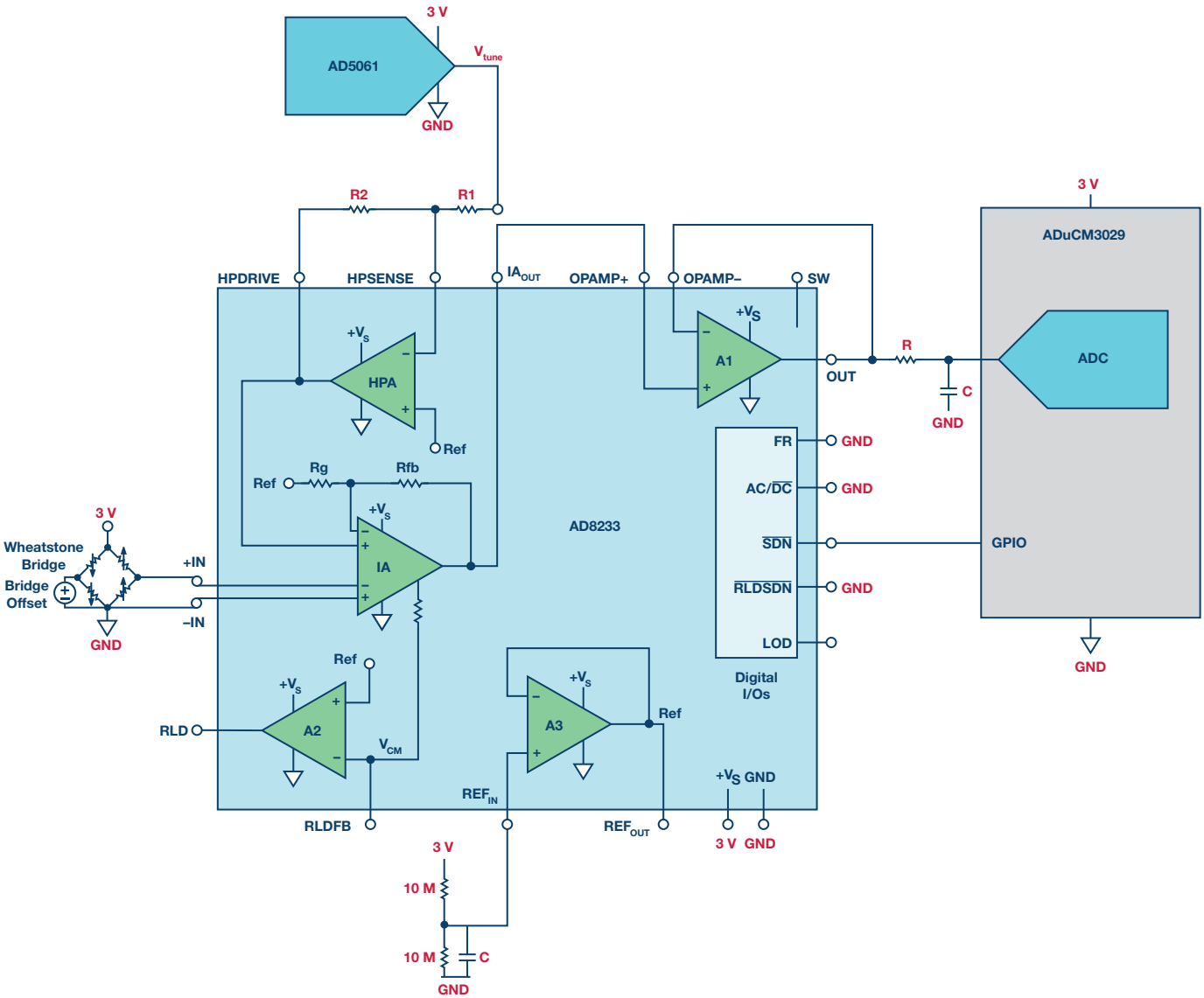


Figure 7. Low power pressure sensor circuit.

Now that the complete AD8233 chip is better understood, let's take a look a couple of different sensor application ideas. Table 2 provides a getting started guide for building non-ECG circuits.

Table 2. AD8233 Starting Guide for Non-ECG Applications

Pins	Action
$+V_S$ to GND	Battery or regulated voltage (1.7 V to 3.5 V)
REF_{IN}	Set to $+V_S/2$—Figure 6
+IN, –IN	Connect sensor (nominal $V_{cm} = +V_S/2$)
HPSENSE, HPDRIVE, IA_{OUT}	Reference figures 1 to 4
RLD, RLDFB, SW, LOD	Float
FR, AC/$\overline{DC}$, $\overline{RLSDN}$	Tie to GND
$\overline{SDN}$	Tie to +Vs (active), tie to GND (shutdown)
OPAMP+, OPAMP–, OUT	Flexible use (additional gain/filtering after IA)
REF_{OUT}	External reference for A1 and ADC or microcontroller

IoT Edge Node Applications for the AD8233

A great example of where the fixed gain of 100 and offset correction in Figure 4 could be suitable is a pressure sensor application based on a Wheatstone bridge. The bridge naturally sets the input common mode to +Vs/2. Depending on measurement range and current required, the bridge could be driven by REF_{OUT} or the uncommitted op amp, such that the bridge supply current is disabled in shutdown. Figure 7 shows an example circuit. The AD5601 DAC is a good choice for correcting the bridge and IA offset, due to its low power (60 µA at 3 V), shutdown pin, and small SC70 package. The op amp (A1) is left as a placeholder buffer with option to set additional gain or filtering of noise and 60 Hz. The output amplifier drives an on-board ADC of the ultralow power ARM® Cortex®-M3 (ADuCM3029) that also comes in a space saving WLCSP package. A GPIO from the ADuCM3029 can control the shutdown pin of the AD8233.

Another application that could take advantage of the circuit in Figure 4, is making a temperature measurement with a thermocouple. A K-type thermocouple is fairly linear over a wide temperature range with a Seebeck coefficient of about 41 µV/°C at room temperature (25°C). Assuming the reference or cold junction was compensated for, the output of the IA would be a gained up version of the measurement junction ~4.1 mV/°C (for more accurate results, use a NIST lookup table). The output of a thermocouple is the difference between the measurement junction and the reference junction, so an equivalent reference junction drift must be added to cancel it.

To start the process, determine the expected reference junction temperature range by using the NIST table to determine the expected drift. For example:

$$0°C \text{ to } 50°C: \frac{2.023\ mV - 0\ mV}{50°C} = 40.46\ \mu V/°C$$

$$25°C \text{ to } 100°C: \frac{4.096\ mV - 1\ mV}{75°C} = 41.28\ \mu V/°C$$

By placing an accurate temperature sensor at the reference junction, the results can be fed back into V_{TUNE} and adjusted by –R2/R1 to get the correct drift. Note that the drift of temperature sensor should be negative or the IA inputs swapped in order to get a positive drift at the IA output. To separate offset and drift correction, the circuit could be split into a summing node where the offset is fixed at V_{TUNE2} via –R2/R3. See the updated transfer function:

$$IA_{OUT} = 100\left(V_{IN} - \left(\frac{R2}{R1}\right)V_{TUNE} - \left(\frac{R2}{R3}\right)V_{TUNE2}\right) + Ref$$

$$V_{IN} = V_{MEAS_{TC}} - V_{REF_{TC}} + V_{OS_{IA}}$$

The modified circuit is shown in Figure 8. Note that the input common mode is set to $+V_S/2$ by 10 MΩ pull-up on +IN and 10 MΩ pull-down on –IN. This configuration would enable use of lead off detection of the AD8233 by pulling +IN to +Vs in the event of a wire break. This could be monitored at the LOD pin. The AD8233 also has an integrated RFI filter to assist with any high frequency pickup from the thermocouple. Placing additional resistance in series with the inputs can reduce the cutoff frequency.

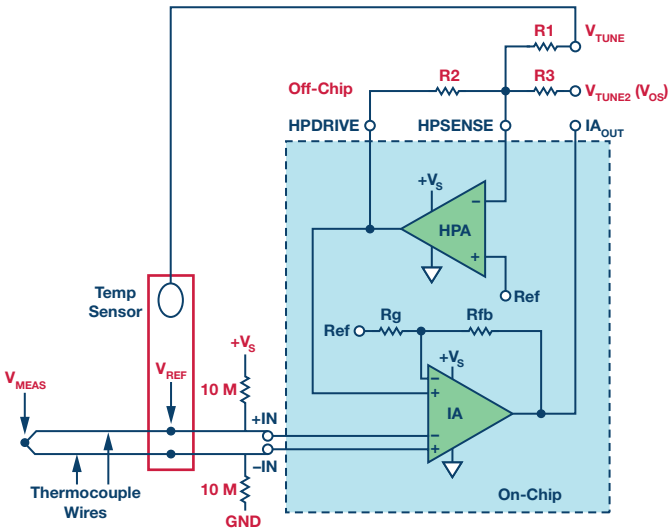


Figure 8. Thermocouple circuit with reference junction compensation and wire break detection.

Conclusion

Breaking down the AD8233 proved it to be more than an ECG front end. Its unique mix of active low power (50 µA), tiny 2 mm × 1.7 mm WLCSP package, shutdown pin, and flexible architecture enables smaller, lighter designs with extended battery life. So the next time you are searching for components for your IoT, WSN, or any other low power design acronym, take a look at the AD8233 and see what circuits you can come up with. Your battery's life may depend on it.

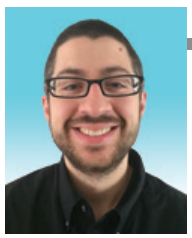
References

Castro, Gustavo and Scott Hunt. "How to Stay Out of Deep Water when Designing with Bridge Sensors." *Analog Dialogue*, Volume 48, 2014.

Duff, Matthew and Joseph Towey. "Two Ways to Measure Temperature Using Thermocouples Feature Simplicity, Accuracy, and Flexibility." *Analog Dialogue*, Volume 44, 2010.

ITS-90 Table for Type K Thermocouple.

David Plourde [david.plourde@analog.com] is an analog IC design engineer in Analog Devices' Linear and Precision Technology Group in Wilmington, MA. His interests include low power design and system-level solutions, primarily for healthcare applications. David received his B.S. and M.S. degrees from Worcester Polytechnic Institute. He joined Analog Devices in 2006 as a product/test engineer.



David Plourde

Analyzing and Solving Fixed Frequency Spur Issues in High Precision ADC Signal Chains

By **Steven Xie**

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Introduction

Current high resolution SAR ADCs and Σ-Δ ADCs provide high resolution and low noise, but system designers can have difficulty achieving the rated data sheet SNR performance. It can be even harder to achieve the optimum SFDR—that is, a clear noise floor without spurs in their system signal chain. Spurs can be introduced by improper circuitry surrounding the ADC or can be the result of external interference that occurs in a harsh operating environment.

This article will introduce approaches for determining the root causes of spur issues in high resolution, precision ADC applications and present solutions to solve them. These techniques and methods will help improve end-system EMC capability and reliability.

This article will cover five different application cases of specific design solutions for reducing spurs:

- Spur issues caused by dc-to-dc power supply radiation from the controller board.
- Spur issues caused by ac-to-dc adaptor noise through the external reference.
- Spur issues caused by analog input cable.
- Spur issues caused by interference coupled on the analog input cable.
- Spur issues caused by room lighting.

Spurs and SFDR

As is known, spurious-free dynamic range (SFDR) represents the smallest power signal that can be distinguished from a large interfering signal. For current high resolution, precision ADCs, the SFDR is typically dominated by the dynamic range between a fundamental frequency and the second or third harmonic of the fundamental frequency of interest. However, there are spurs that can occur and limit the performance due to other aspects of the system.

The spurs can be categorized as input frequency dependent spurs and fixed frequency spurs. The input frequency dependent spurs are related to harmonic or nonlinearity performance. This article will focus on the fixed frequency spurs that are caused by power supplies, external references, digital interfacing, external interference, and more. Based on the application, these types of spurs can either be reduced or avoided entirely to help achieve maximum signal chain performance.

Spur Issues Caused by On-Board DC-to-DC Power Supply Noise

Typically, LDOs are the suggested solution for generating low noise power supply rails for precision ADCs in precision measurement systems because of the dc-to-dc switching regulator's higher ripple noise. The fixed frequency or pulse-width modulated switching regulators provide switching ripple that is usually at a fixed frequency ranging from tens of kHz to a couple of MHz. The noise at the fixed frequency can feed into the ADC conversion codes via the ADC's PSRR mechanism.

Some designers may use dc-to-dc switching regulators for precision ADC applications due to limited budget or board space. They have to limit the ripple noise or use ADCs with high PSRR to make sure that the ripple noise is below the ADC noise floor in order to achieve signal chain performance. Otherwise, there could be spurs at the switching frequency in the ADC's output spectrum, which may degrade signal chain dynamic range.

The AD7616 is a 16-bit DAS that supports dual-simultaneous sampling of 16 channels for power line monitoring. It has a very high PSRR and will do a good job of rejecting/attenuating the switching ripple. For example, a dc-to-dc switching power supply with 100 mV p-p ripple noise at 100 kHz is used for AD7616, a V_{CC} 5 V with ±10 V input range.

The digital code noise caused by the ripple noise is:

$$\frac{100\ \text{mV p–p}}{10^{\frac{88\ \text{dB}}{20}}} = 3.98\ \mu\text{V}\ \textit{or}\ 0.013\ \text{LSB}$$

This level of ripple showing up in the ADC output is extremely low for a 16-bit converter. High PSRR performance in ADCs makes it possible to use switching regulators in precision measurement systems.

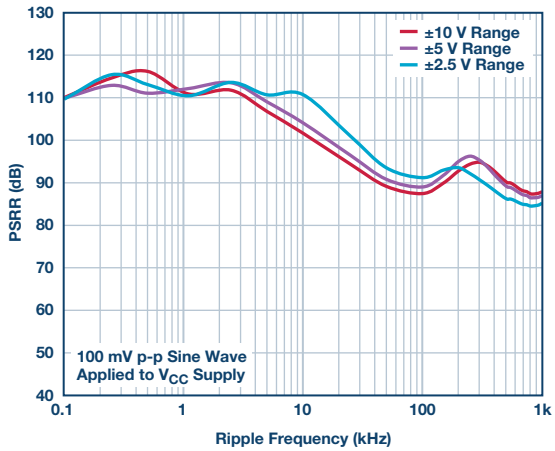

Figure 1. AD7616 PSRR vs. ripple frequency.

Spur Issues Caused by DC-to-DC Power Supply Radiation

Using a high PSRR ADC does not ensure that switching regulators will not cause problems in precision measurement systems. The ripple noise from switching regulators could feed into the ADC's digital codes through other ways.

The AD4003 is a low noise, low power, high speed 18-bit, 2 MSPS precision successive approximation register (SAR) ADC. During EVAL-AD4003FMCZ evaluation board ac performance testing, a spur at a level of about –115 dBFS was found at around 277.5 kHz; the spur and its second harmonic appeared as shown in Figure 2.

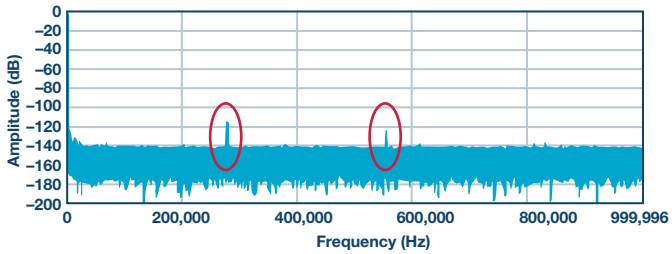

Figure 2. Spur issue as seen on an EVAL-AD4003FMCZ eval board.

First, it was confirmed that the AD4003 power supplies were not causing the spurs.

Then, tests were performed to determine if the spurs were coming from the analog input.

- The spurs decreased when the differential analog input conditioning circuitry was removed.
- The spurs decreased when a narrow bandwidth RC filter (such as 1 kΩ, 10 nF) was inserted at the front end of AD4003 buffer amplifier, ADA4807-1.

These results show that the noise causing the spurs may pass through the conditioning circuitry and into the AD4003's analog inputs. Next, the sensor output was disconnected and the conditioning circuitry removed, leaving only the $V_{REF}/2$ CM voltage input at the noninverting input of the ADA4807-1. However, the spurs remained and at a similar level.

It was then suspected that the interference source was located around the EVAL-AD4003FMCZ signal chain. To prove this, a copper foil shield was placed at various locations on the EVAL-AD4003FMCZ board and the controller SDP-H1 board. It was determined that when the copper foil shield was placed over the dc-to-dc power supplies on the SDP-H1 board, as shown in Figure 3, the spurs would disappear. The spur frequency of 277.5 kHz matches the programmed switching frequency of the ADP2323 regulator. Figure 4 shows the 3.3 V VADJ_FMC switching frequency power as captured by the EVAL-AD7616SDZ GUI FFT.

Figure 3. VADJ_FMC inductor L5 covered by copper foil shield.

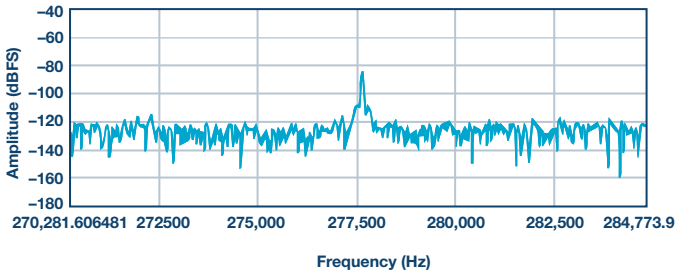

Figure 4. VADJ_FMC 3.3 V switching ripple captured by EVAL-AD7616SDZ GUI FFT.

The conclusion was reached that the dc-to-dc switching frequency interference was being emitted by the 8.2 µH inductor, L5. The interference was being injected into the signal chain at the input of buffer amplifier ADA4807-1, where it then went into the AD4003 ADC's analog input.

Possible solutions to this spur issue caused by dc-to-dc power converter are:

- Use a low-pass filter at the front end of the AD4003 ADC to attenuate the coupled dc-to-dc switching frequency interference to a level that meets the design target (that is, spur buried in noise floor) if the application bandwidth allows it.
- Use the new SDP-H1 board (BOM Rev 1.4), which uses a shielded inductor for L5. The radiated interference power is reduced, so the spurs captured in AD4003 ADC's spectrum are much lower.
- The VADJ_FMC voltage level can be programmed by the EEPROM on the EVAL-AD4003FMCZ board. It was found that using a lower voltage level, such as 2.5 V for VADJ_FMC, caused the spurs to disappear also.

Spur Issues Caused by AC-to-DC Adaptor Noise Coupling Through the External Reference

ADCs quantize an analog signal into a digital code as referred to the ADC's dc reference voltage level. Therefore, the noise on the dc reference input will directly feed into the ADC's output digital codes.

The AD7175-2 is a low noise, fast settling, multiplexed, 2-/4-channel (fully/pseudo differential) Σ-Δ ADC for low bandwidth inputs. During the EVAL-AD7175SDZ evaluation board's signal chain test, a cluster of spurs around 60 kHz was captured, as shown in Figure 5.

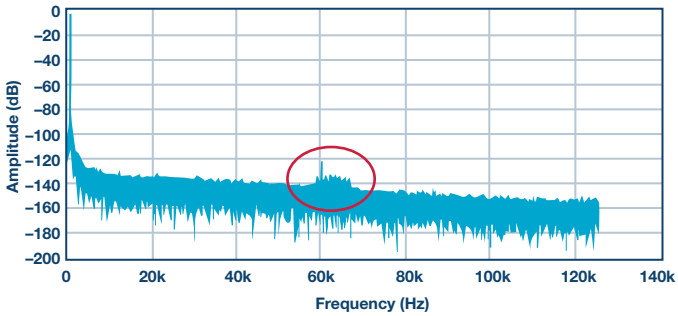

Figure 5. Spur issue as seen on EVAL-AD7175-2SDZ eval board.

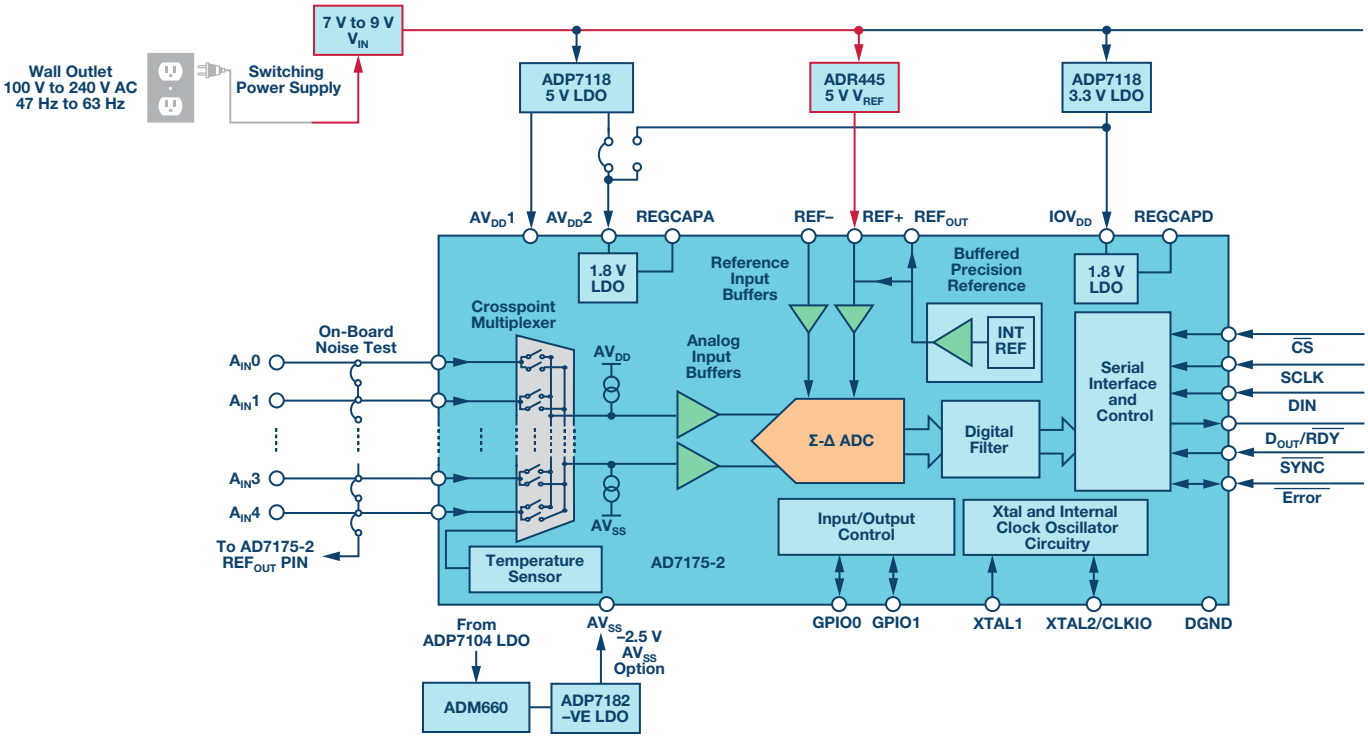

Figure 6. Spur issue seen on EVAL-AD7175-2SDZ eval board.

The AD7175-2 ADC's power supplies and analog conditioning circuitries were evaluated and found to be good. However, as shown in Figure 6, the AD7175-2's 5 V reference input is generated by the ADR445 reference that is supplied by a 9 V dc from an ac-to-dc adaptor that is external to the evaluation board. Next, a bench 9 V dc power module was substituted for the adaptor. As a result, the cluster of spurs disappeared, leaving only a narrow spur at 60 kHz.

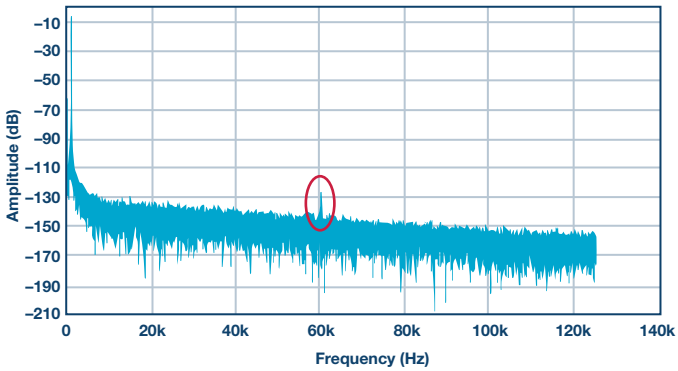

Figure 7. The cluster of spurs removed on EVAL-AD7175-2SDZ eval board.

The 9 V output ac-to-dc adaptor was tested with the EVAL-AD7616SDZ GUI FFT while supplying the EVAL-AD7175-2SDZ board with 320 mA of current output. The switching frequency power at the ADR445 reference's power pin is about –70 dBFS with an AD7616 ±10 V input range, which means 6.325 mV p-p or –64 dBFS at an AD7175-2 ±5 V input range.

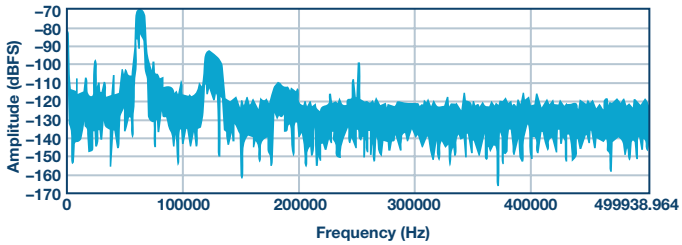

Figure 8. 3.3 V VADJ_FMC switching ripple captured by EVAL-AD7616SDZ GUI FFT.

$$20\ \text{V} \times 10^{\frac{-70\ \text{dB}}{20}} = 6.325\ \text{mV p-p}$$

$$20 \times \log\left(\frac{6.325\ \text{mV p-p}}{10\ \text{V}}\right) = -64\ \text{dBFS}$$

This power switching ripple noise feeds into the AD7175-2 ADC and shows up in the digital codes with some attenuation as stated below:

- The ADR445 reference's data sheet specifies a PSRR of 49 dB at 60 kHz.
- The ADR445 reference's output impedance is about 4.2 Ω at 60 kHz. It combines with the 4.8 µF reservoir caps, giving a further 18 dB of attention.
- Additionally, the AD7175-2 ADC's digital filter sinc5 + sinc1 adds about –3 dB of attenuation at 60 kHz, when ODR is 256 kSPS.

This calculated –134 dBFS level is very close to the level of the captured –130 dBFS cluster of spurs (not including the highest narrow spur) shown in Figure 5. This verifies that the cluster of spurs is caused by the ac-to-dc adaptor's switching ripple feeding through the external reference ADR445. The remaining narrow spur will be resolved in the subsequent section.

$$-64\ \text{dBFS} - 49\ \text{dB} - 18\ \text{dB} - 3\ \text{dB} = -134\ \text{dBFS}$$

Spur Issues Caused by Interference Injected into the Signal Chain

In the hardware system, there is generally a long signal chain from the input sensor to the input of the precision converters. This signal chain includes connecting cables, connectors, routing wires, scaling and conditioning circuitries, ADC drivers, and more. There is a high potential for external interference to inject into the analog input signal chain and cause ADC spurs.

Spur Issues Caused By Power Cable Interference into the Signal Chain

During the investigation of the remaining narrow spur on the EVAL-AD7175-2SDZ evaluation board's spectral output, it was noticed that there was a digital oscilloscope operating on the test bench. As shown in Figure 9, the scope's 220 V ac power supply cable (the black one) was overlapping the EVAL-AD7175-2SDZ EVB's analog input cable (the gray one). When the oscilloscope was turned off or its power cable was physically moved away from the analog input cable, the narrow spur at 60 kHz disappeared, as shown in Figure 10.

In the system cabinet, care should be taken in routing the cables from the sensor to the DAQ board. It is a good practice to keep the low level sensitive analog signals separated from the high current power lines.

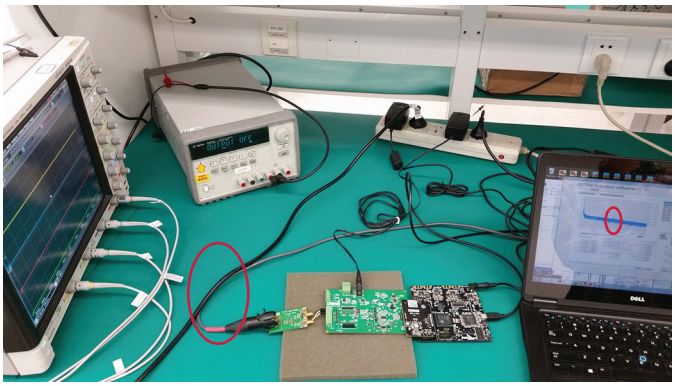

Figure 9. Spur caused by oscilloscope power supply cable.

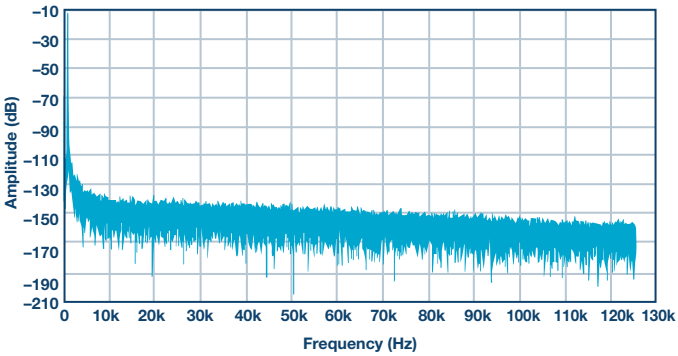

Figure 10. All spurs removed on EVAL-AD7175-2SDZ eval board.

Spur Issues Caused by Lamp Radiation

A spur appeared on the FFT spectrum while testing the EVAL-AD7960FMCZ evaluation board. As shown in Figure 11, the spur level was about –130 dB at 40 kHz.

The 40 kHz seemed to be unrelated to any of the signal frequencies that appear on the EVAL-AD7960FMCZ board and its controller board, SDP-H1. The next approach to finding the source of the spur was to clear the test bench in case there was something generating external interference. When the fluorescent light on the bench rack was turned off, the spur disappeared. Furthermore, it was found that as the EVAL-AD7960FMCZ board was put closer to the light, the 40 kHz spur would get higher. An additional RC filter (such as 1 kΩ, 10 nF) was placed at the front of the buffer amplifier ADA4899-1 and the spur decreased about 10 dB. That meant that the fluorescent light was radiating disturbance into the signal chain path at the front of the noninverting input of the buffer amplifier.

For systems that operate in a lighted environment, installing a shielding case over the front-end circuitry can help protect it from radiating interference and optimize signal chain performance.

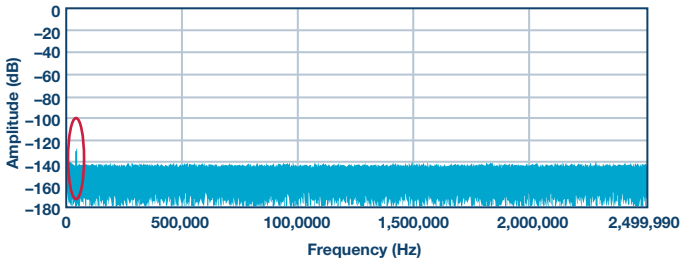

Figure 11. Spurs on EVAL-AD7960FMCZ by flourescent lighting radiation.

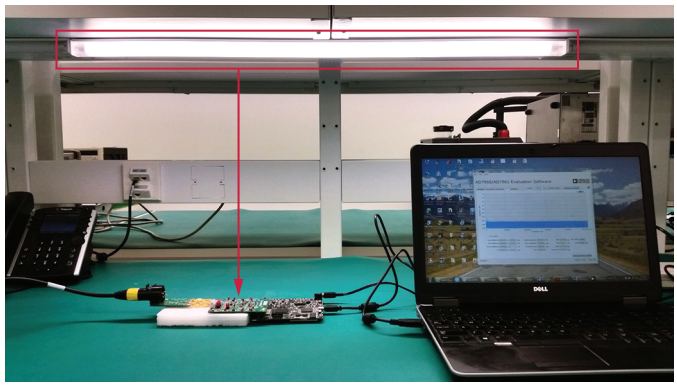

Figure 12. Fluorescent lighting in proximity to the EVAL-AD7960FMCZ board.

Spur Issues Caused by a Long Analog Input Cable

During the evaluation of the EVAL-AD4003FMCZ board, an AP SY2712 signal generator was used to drive a low noise and low THD sine wave to the analog inputs through an XLR microphone cable (about 2 meters long). In this setup, a spur was apparent at a level of about –125 dB at 700 kHz, as shown in Figure 13.

In the investigation of the spur, three ways to solve it were found:

- Bypass the two meter long XLR microphone cable and short the AP balanced output XLR male connector to the interposer XLR female connector.
- Set the signal source SY2712's output impedance from Z-Out = 40 Ω to Z-Out = 600 Ω.
- The spur becomes smaller when a narrow bandwidth RC filter (such as 1 kΩ, 10 nF) is inserted in the signal chain at the front end of the AD4003's buffer amplifier, the ADA4807-1.

Finally, the conclusion was reached that the mismatch in the signal source's output impedance, and the long XLR cable, caused the high frequency spur at 700 kHz.

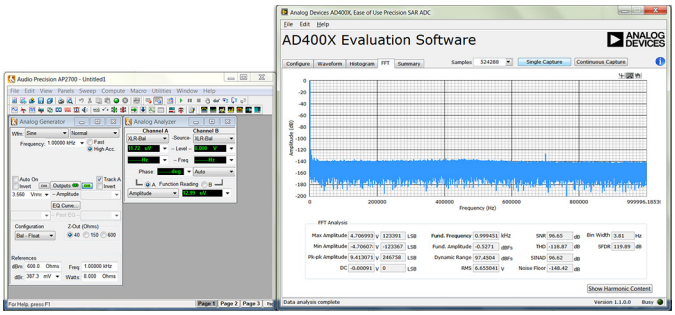

Figure 13. Spur on EVAL-AD4003FMCZ eval board caused by XLR cable.

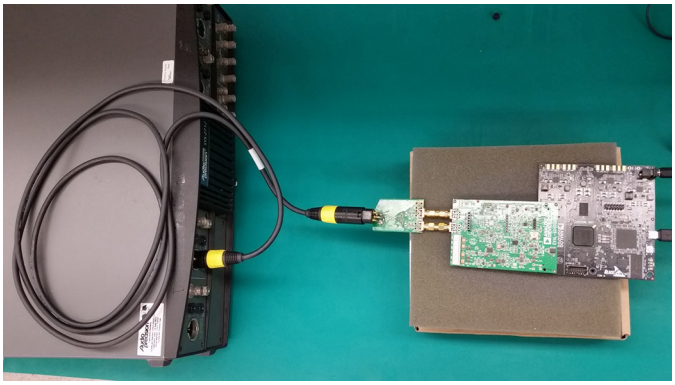

Figure 14. AP driving the EVAL-AD4003FMCZ board through a long XLR cable.

Conclusion

This article discusses approaches for determining the root causes of spur issues in high resolution, precision ADC circuits, in system applications. It introduces specific design solutions to eliminate or reduce spurs in five different application cases. The article also discusses spur calculation methods to help estimate the spur power level as a design target for specific applications.

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AD7175-2 Evaluation Kits. Analog Devices, Inc.

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Acknowledgements

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Volume 50, Number 2

Rarely Asked Questions—140 Presto! Multiply Your ADC's Virtual Channel Count with DDC Magic

By **Umesh Jayamohan**

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Question:

I bought a dual-channel ADC and configured the digital downconverters. Now I am being told I have four converters! Is there a 2-for-1 data converter sale I wasn't aware of?

Answer:

Ever since the advent of the very first monolithic, silicon-based analog-to-digital converters (ADCs), the ADC has been keeping pace with the rapid advancements in silicon processing technology. Over the years, the silicon processing technology has advanced enough that it is now possible to economically design ADCs with a lot more powerful digital processing. Earlier generation ADC designs used very little digital circuitry outside of error correction and digital drivers. The new family of GSPS (gigasample per second) converters (also known as RF sampling ADCs) are enabled using sophisticated 65 nm CMOS technology and can pack a lot more digital processing power to enhance the ADC's performance.

With high sample rates (in the GSPS realm) also come a huge payload of data (bits per second). Take the AD9680, which is a dual 14-bit, 1.25 GSPS/1 GSPS/820 MSPS/500 MSPS, JESD204B analog-to-digital converter as an example. At the maximum sample rate of 1.25 GSPS, the ADC streams

$$14\ bits \times 2\ converter\ channels \times 1.25\ \text{Gbps} = 35\ \text{Gbps}$$

This amount of data will require an enormous number of LVDS routing lanes to extract the digital data. In order to facilitate the implementation of this large throughput, the JESD204B standard was adopted. The JESD204B is a high speed, data transmission protocol that employs 8b/10b encoding and scrambling among other features aimed at providing adequate signal integrity. With the JESD204B standard, the total throughput now becomes

$$16\ bits \times 2\ converter\ channels \times \left(\frac{10}{8}\right) \times 1.25\ \text{Gbps} = 50\ \text{Gbps}$$

Using the JESD204B standard, the data throughput can be split across four high speed serial lanes at 12.5 Gpbs on each lane. Compare this to an LVDS interface where, at a line rate cap of about 1 Gbps/lane, the chip would need more than 28 pairs!

A quick inspection of the AD9680 data sheet reveals that there is quite the alphabet soup as far as setting up the link goes. Whereas earlier generation LVDS ADCs were easier to implement, the newer generation JESD204B ADCs are a bit more complicated. They become even more complicated when you take into account the internal digital downconverter (DDC) setups. However, the ADC setup is primarily determined by three letters in that alphabet soup:

L = number of lanes per JESD204B link

M = number of converters per JESD204B link

F = number of octets per frame of data in the JESD204B link

Take for example the AD9250, which is a dual 14-bit, 250 MSPS JESD204B analog-to-digital converter. Figure 1 shows the block diagram representation of the AD9250 in its default setup.

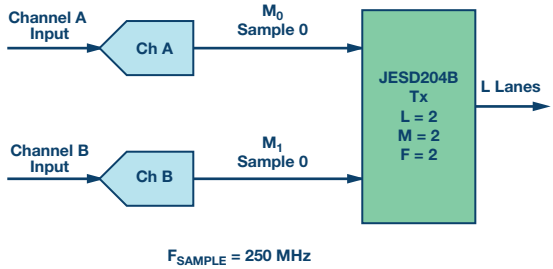

Figure 1. Setting up the AD9250.

In this setup the JESD204B link (JESD204B transmitter) is pretty straightforward, as there are no additional digital processing done in the AD9250. To the JESD204B link, Channel A becomes Converter 0 (M_0), whereas Channel B becomes Converter 1 (M_1), which means the value of M becomes 2. The total line rate for this setup is

(continued on Page 20)

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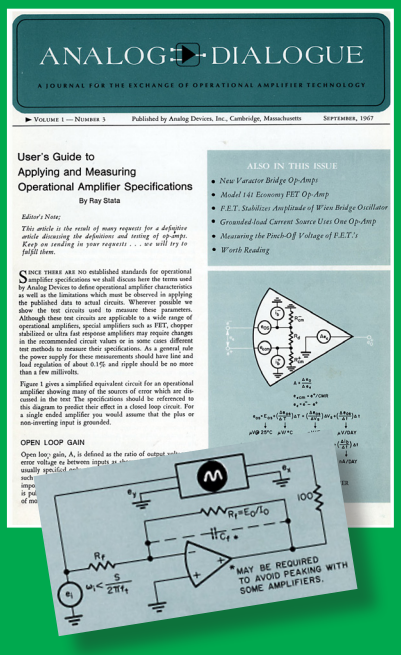
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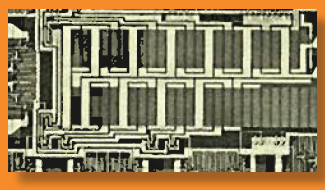
Jim Cecil *and* ***Jerry Whitmore***



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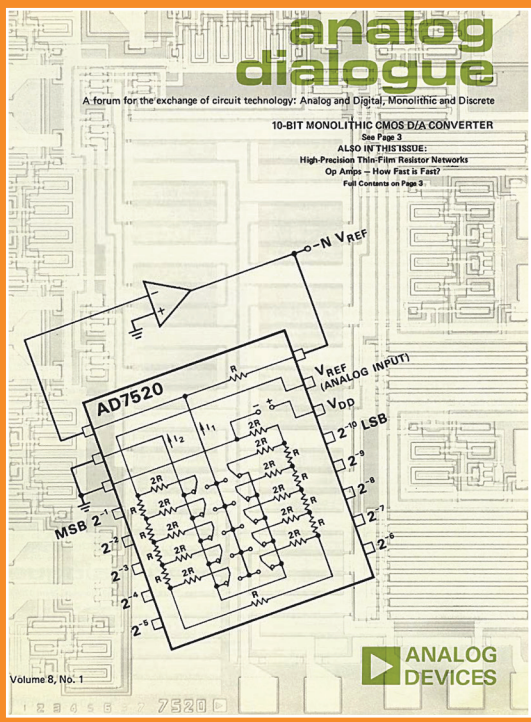
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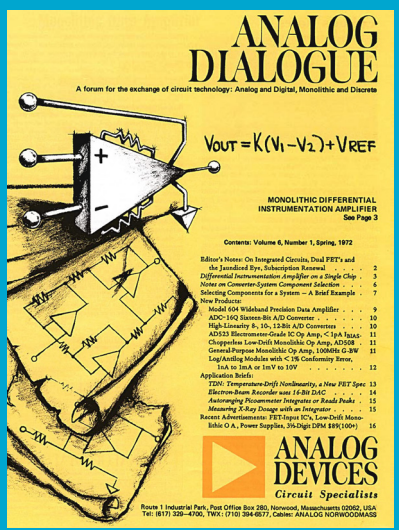
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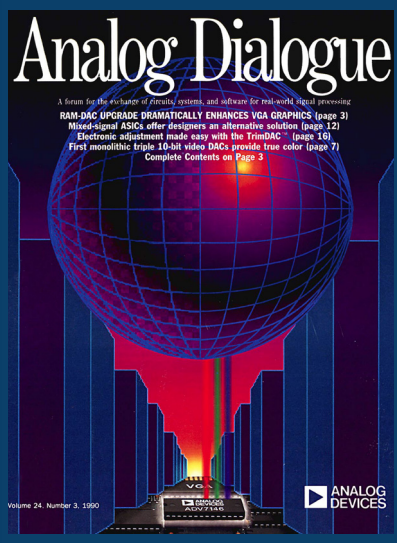

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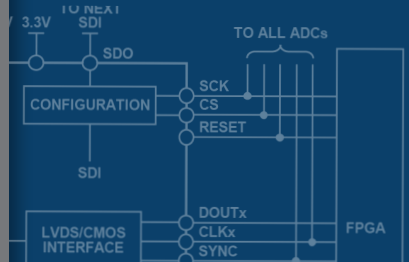

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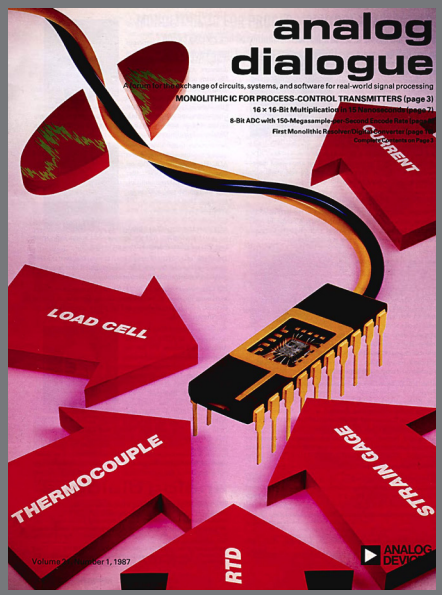

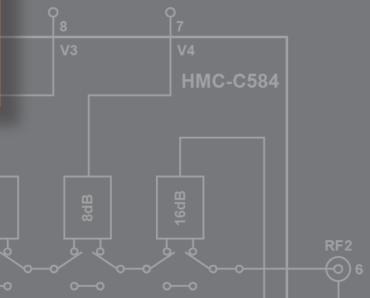

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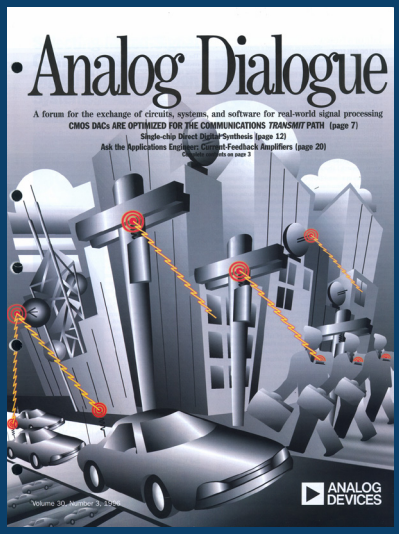

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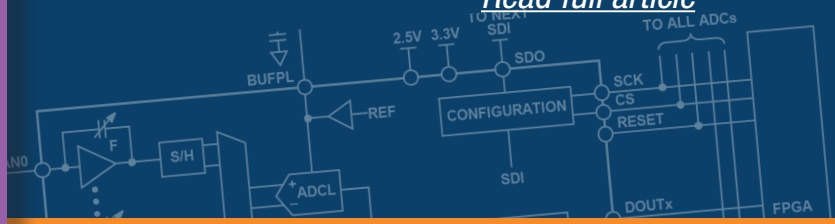

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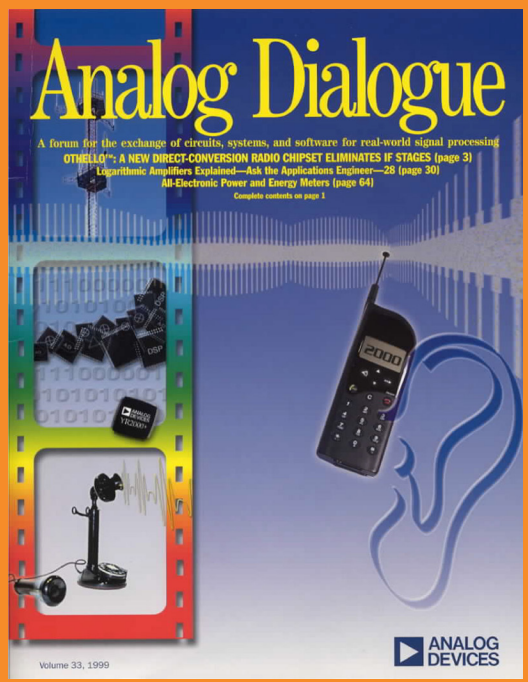

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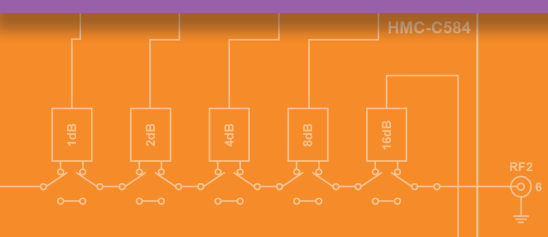

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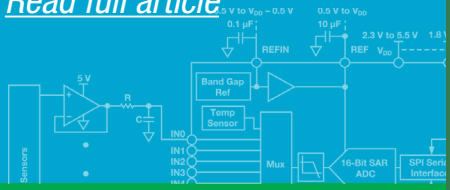

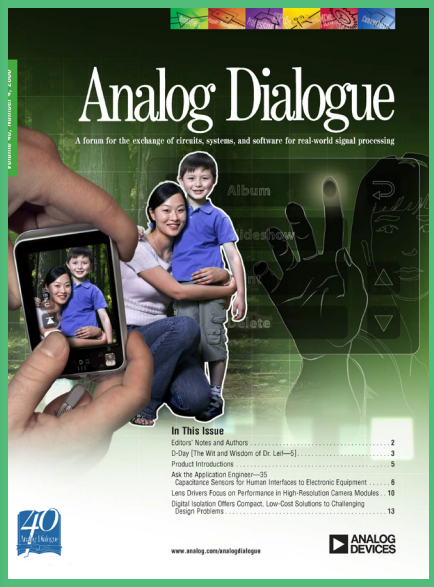

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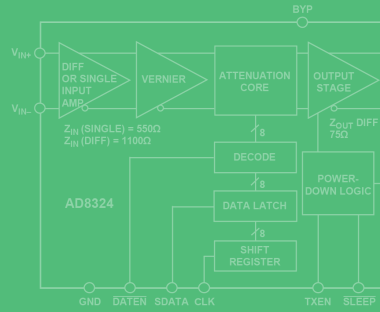

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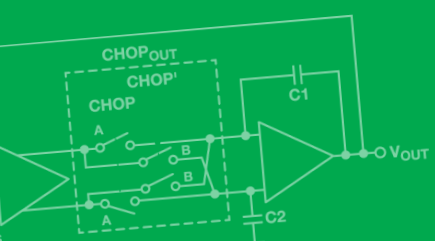

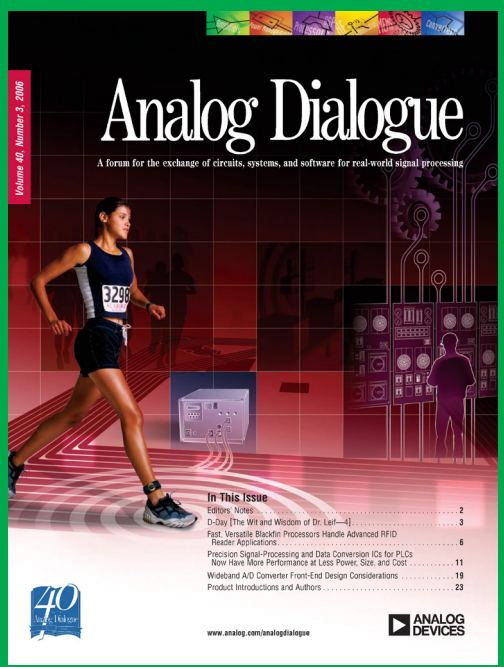

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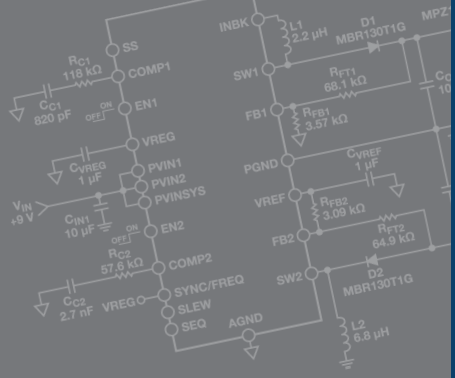

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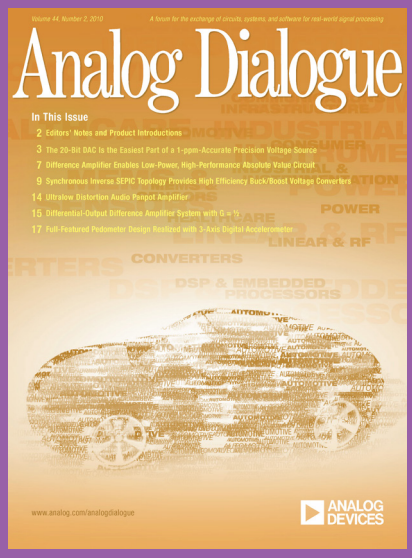

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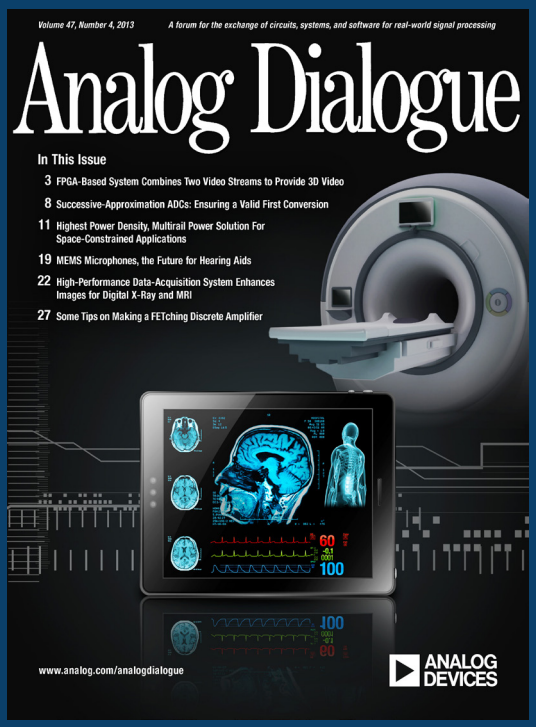

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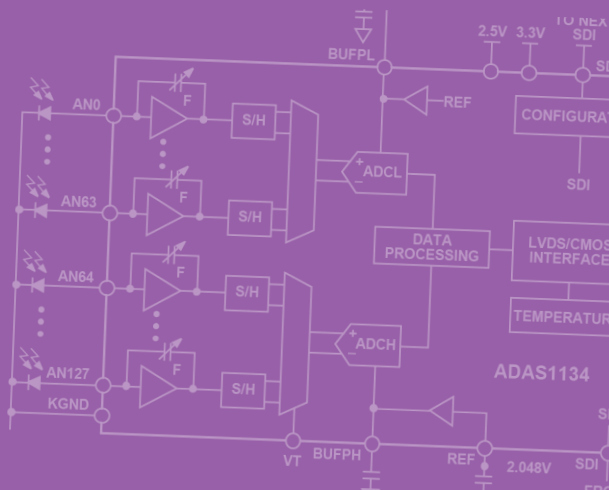

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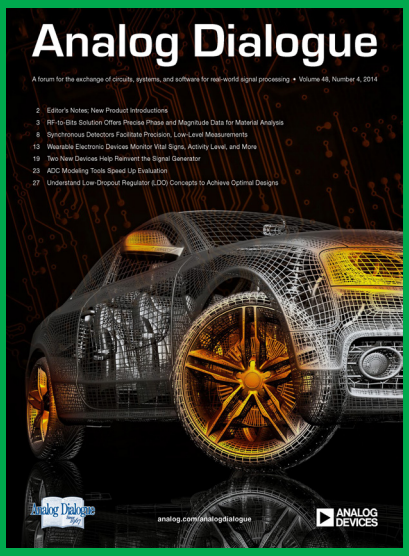

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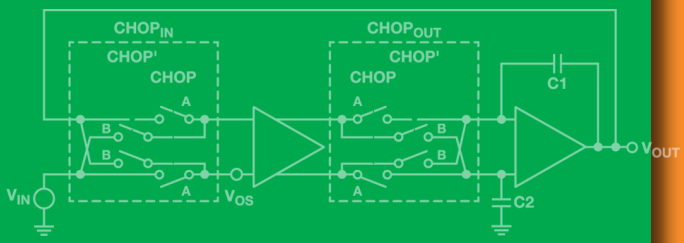

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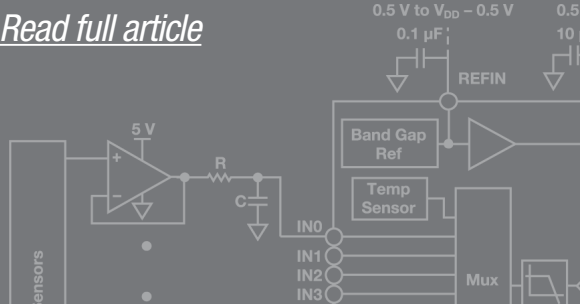

(continued from Page 13)

$$Line\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times F_{OUT}}{L} =$$

$$\frac{2 \times 16 \times 1.25 \times 250\ M}{2} = 5\ \text{Gbps/}lane$$

Compare this to the AD9680 sampling at 1 GSPS—but in this case, two digital downconverters are used in a complex (I/Q) setup. Figure 2 shows the AD9680 where the digital downconverters are used to decimate the data sampled at 1 GSPS by four. This results in an output sample rate (F_{OUT}) of 250 MSPS.

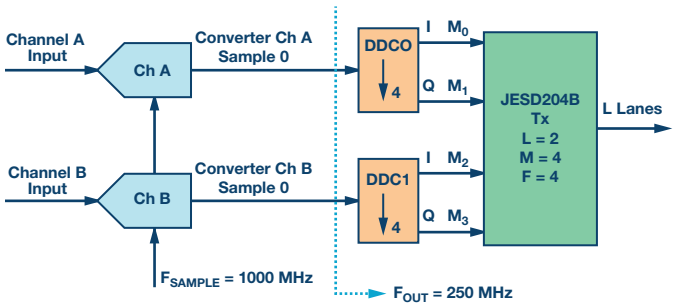

Figure 2. Setting up the AD9860-1000 with two DDCs set to decimate by 4.

It is clear from Figure 2 that the AD9680 can effectively reduce the sample rate using the internal on-chip digital downconverters. Since each of the DDCs outputs a 16-bit stream, the actual (physical) converter bit streams are now decoupled from the "M" parameter of the JESD204B alphabet soup. Per the standard, M is the number of converters per link.

In the modified scenario, M now becomes a parameter called a virtual converter. Even though the AD9680 physically only has two ADC channels (A and B), with the DDCs in complex output mode enabled, there are now four different (16-bit) data streams to the JESD204B interface. To the JESD204B interface, this looks like there are now four (virtual) converters sending bit streams. Hence, the M = 4 or converter multiplying act. The output line rate in this case becomes

$$Line\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times F_{OUT}}{L} =$$

$$\frac{4 \times 16 \times 1.25 \times 250\ M}{2} = 10\ \text{Gbps/}lane$$

The flexibility of the AD9680's JESD204B interface becomes apparent here, as there are now two options available depending on what the line rate acceptability of the receive logic (ASIC or FPGA). Table 1 shows the available options for the JESD204B interface in the AD9680 setup shown in Figure 2.

Table 1. Configuration Options for the AD9680 ADC's JESD204B Output Interface

# Virtual Converters M	# Lanes Per Link L	# Octets Per Frame F	Line Rate (Gbps/Lane)
4	4	2	5
	2	4	10

For a dual-channel ADC like the AD9680 that has four DDCs, Table 2 shows the virtual converter mapping that is available for various configurations.

Table 2. Configuration Options for the AD9680 ADC's JESD204B Output Interface

Number of Virtual Converters Supported	Chip Operating Mode	Chip Q Ignore	Virtual Converter Mapping							
			0	1	2	3	4	5	6	7
1 to 2	Full Bandwidth Mode	Real or Complex	ADC A Samples	ADC B Samples	Unused	Unused	Unused	Unused	Unused	Unused
1	One DDC Mode	Real (I Only)	DDC 0 I Samples	Unused	Unused	Unused	Unused	Unused	Unused	Unused
2	One DDC Mode	Complex (I/Q)	DDC 0 I Samples	DDC 0 Q Samples	Unused	Unused	Unused	Unused	Unused	Unused
2	Two DDC Mode	Real (I Only)	DDC 0 I Samples	DDC 1 I Samples	Unused	Unused	Unused	Unused	Unused	Unused
4	Two DDC Mode	Complex (I/Q)	DDC 0 I Samples	DDC 0 Q Samples	DDC 1 I Samples	DDC 1 Q Samples	Unused	Unused	Unused	Unused
4	Four DDC Mode	Real (I Only)	DDC 0 I Samples	DDC 1 I Samples	DDC 2 I Samples	DDC 3 I Samples	Unused	Unused	Unused	Unused
8	Four DDC Mode	Complex (I/Q)	DDC 0 I Samples	DDC 0 Q Samples	DDC 1 I Samples	DDC 1 Q Samples	DDC 2 I Samples	DDC 2 Q Samples	DDC 3 I Samples	DDC 3 Q Samples

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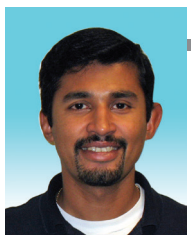

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Because Mr. Ohm Said So ...

Volume 50, Number 4

Precision SPI Switch Configuration Increases Channel Density

By **Stephen Nugent**

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Abstract

When designing a system that requires high channel density such as in test instrumentation, there is typically a necessity to include a large number of switches on the board. When using switches controlled by a parallel interface, a large percentage of board space is taken up by the logic lines necessary to control the switches, as well as the serial-to-parallel converters needed to generate the GPIO control signals. This article discusses the new generation of ADI SPI controlled switches that address this design challenge, their architecture, and the channel density increase they offer vs. parallel controlled switches. ADI's innovative copackaging process enables a new SPI-to-parallel converter die to be combined with existing high performance analog switch die. This allows space saving to be offered without compromise to the precision switch performance.

Maximizing channel count in test equipment is of the utmost importance, as this allows more devices to be tested in parallel, which, in turn, cuts testing time and cost for the end customer. Switches are a key element in allowing channel increases, as they enable the tester to share its resources to support multiple DUTs. But more parallel controlled switches means more control lines, resulting in increased board space consumed. This severely restricts the channel density that can be realized.

Using SPI controlled switches in this situation offers significant benefits in terms of solution size and channel count. The SPI switches can be placed in a daisy-chain formation that massively reduces the number of digital lines needed as compared to a traditional solution.

This article details the problems encountered when trying to maximize channel count, discusses the traditional method used to control a group of switches and the associated drawbacks, presents the solution offered by SPI controlled analog switches, and finally introduces the best-in-class performance, SPI controlled ADI precision switches.

Common Issues When Maximizing Channel Count

When developing a module where the main aim is to maximize channel count, board space becomes a commodity. Switches are key to increasing channel count in a system but as the number of switches increase, board space is reduced not only by the switches themselves, but by the logic lines and associated devices needed to generate these logic lines. Ultimately the channel count that can be realized suffers because of the associated items needed to control the switch itself.

Traditional Parallel Switch Solution

The most common solution to increasing channel density is to use switches that are controlled by parallel logic signals. This requires a large amount of GPIO signals that a standard microcontroller would not be able to supply. A solution to generating the GPIO signals is using serial-to-parallel converters. These devices output parallel signals and are configured by serial protocols such as I^2C and SPI.

Figure 1 is a layout, showing eight ADG1412 quad, single-pole, single-throw (SPST) switches in a 4 × 8 cross point configuration on a 6-layer board. The switches are controlled by two serial-to-parallel converters with the serial lines coming from a controller board. Each converter supplies 16 GPIO lines each that are distributed between the eight switches. The layout shows the footprints of the devices, supply decoupling capacitors, and the digital control signals in gray. The size of 4 × 8 matrix solution using the parallel controlled switches is 35.6 mm × 19 mm, which occupies an area of 676.4 mm.^{2}

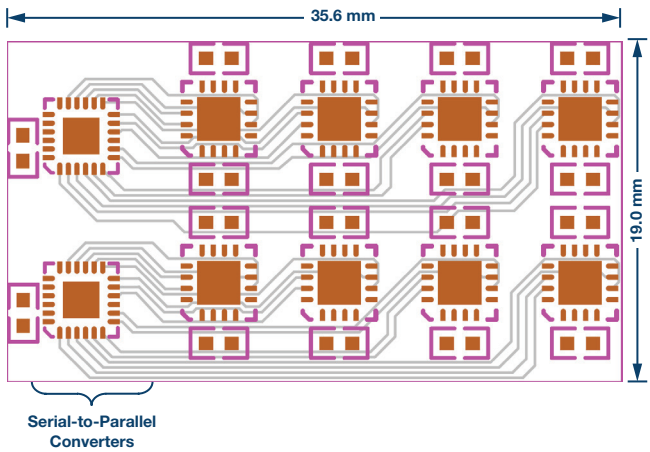

Figure 1. Parallel controlled switch 4 × 8 matrix layout.

As is evident from Figure 1, a large percentage of the solution area is taken up by the serial-to-parallel converters and the digital control lines, rather than the switches themselves. This inefficient use of board space is not ideal and will vastly reduce the number of switches in the module, which, in turn, has a detrimental effect on the channel count of the system.

SPI Switch Solution

Figure 2 shows a 4 × 8 cross point configuration with eight quad SPST switches on a 6-layer board. However, this time the switches are SPI controlled ADGS1412 devices. As before, the device footprints, supply decoupling capacitors, and SDO pull-up resistors are shown.

The solution shows the devices configured in a daisy-chain formation. All devices share the same chip select and serial clock digital lines from an SPI interface, while the first device in the chain receives the serial data. This data is then passed through all devices in the chain like a shift register. The size of this example solution is 30 mm × 18 mm, which is an area of 540 mm.^{2}

The use of the SPI interface in a daisy-chain format vastly reduces the board space occupied by the serial-to-parallel converter and the digital lines. So much so that an overall board area reduction of 20% is realized with the same switch configuration. This enables a large increase in channel density. The system platform is also simplified. When the switch count increases on a board, the space area savings ramps up along with that—leading to >50% space saving on boards containing hundreds of switches.

This demonstrates the ability to fit more switches into a smaller area, which, in turn, would allow for the large channel count on a fixed area board compared to the traditional serial-to-parallel converter solution.

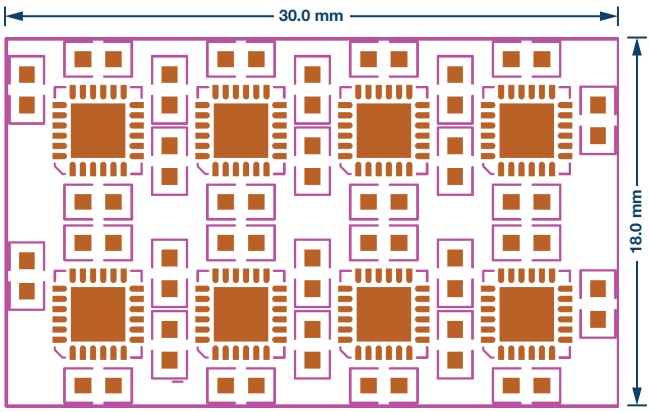

Figure 2. Daisy-chain switch, 4 × 8 matrix layout.

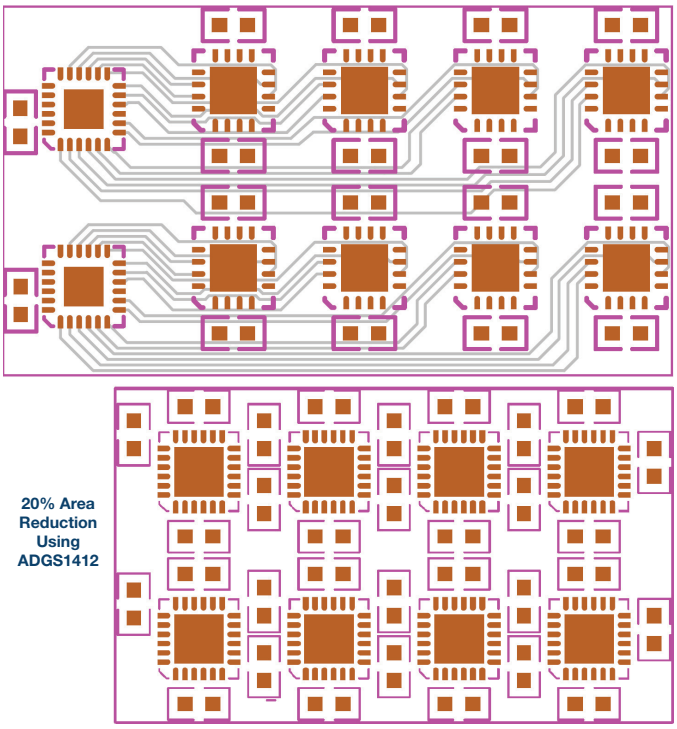

Figure 3. Area comparison of SPI switch and parallel switch solutions.

ADI SPI Switch Features

ADI's new SPI switch portfolio can be used to achieve increased channel density, as shown in the previous example. An innovative stacked dual-die solution (Figure 4) enables ADI's current industry-leading precision switches to be configured with an industry standard, SPI mode 0 interface. This means that the space saving can be achieved without having an adverse effect on the performance of the system. The following is a summary of the key functionality of the new ADI SPI switch.

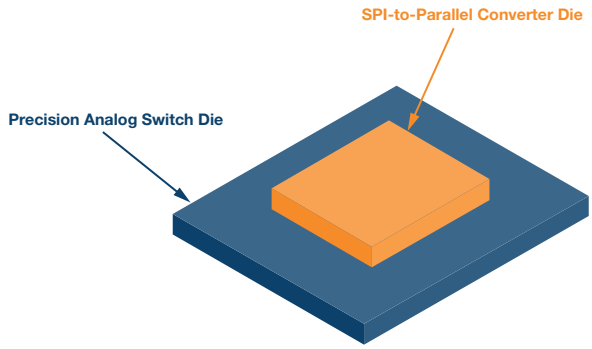

Figure 4. ADI's innovative stacked dual-die solution.

Daisy-Chain Mode

As outlined before, the ADI SPI switches are able to operate in daisy-chain mode. The connection of ADGS1412 devices in a daisy-chain is illustrated in Figure 5. All devices share $\overline{CS}$ and SCLK digital lines, whereas the SDO of a device forms a connection to the SDI of the next device. One single 16-bit SPI frame is used to command all the devices in the chain to enter daisy-chain mode. In daisy-chain mode, SDO is an 8-cycle delayed version of SDI, so the desired switch configuration can be passed from one device to the next device in the chain.

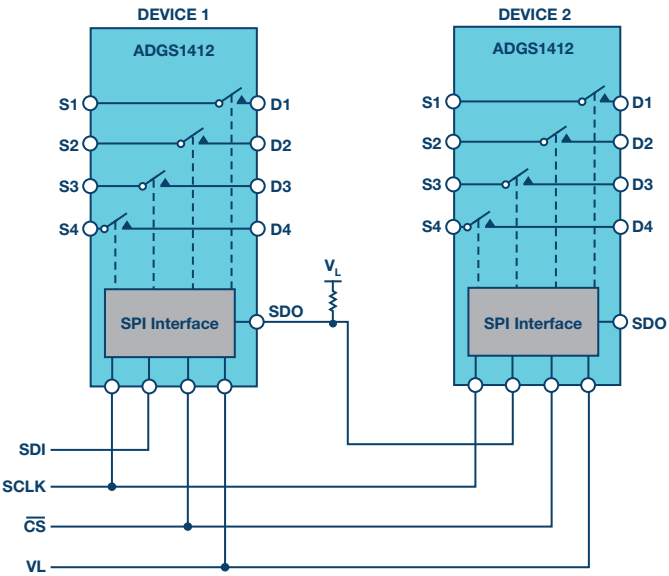

Figure 5. Two switches in a daisy-chain configuration.

Error Detection Function

When the device is in address mode or burst mode, protocol and communication errors on the SPI interface are detectable. There are three error detection methods, which are incorrect SCLK count, invalid read and write address, and CRC error detection up to 3 bits. These error detection function ensure a robust digital interface even in the harshest of environments.

ADI SPI Switch Family

The ADGS1412 is the first release in a family of SPI switches that are being developed by Analog Devices. Thanks to the innovative dual-die solution developed by ADI, the ADGS1412, has the same best-in-class, low R_{ON} performance as the parallel controlled ADG1412 while offering the benefits that a serial interface brings.

The portfolio will be built on ADI's high performance switches, offering SPI controlled versions of the industry-leading switches already available. Table 1 shows the current and planned products in the new ADI SPI switch family. The part number represents which analog switch die is copackaged with the SPI-to-parallel converter with an additional S to show that this is the SPI controlled version. These products will be released throughout 2017.

Table 1. Planned Device-Optimized Products in the New SDI SPI

Part Number	Configuration	Device Optimization
ADGS1412	4 × SPST	R_{ON} optimized
ADGS5412	4 × SPST	Low R_{ON}, latch-up immune
ADGS1212	4 × SPST	Charge injection and C_{ON} optimized
ADGS1612	4 × SPST	R_{ON} optimized, medium voltage
ADGS5414	8 × SPST	Low R_{ON}, latch-up immune

Summary

Using SPI controlled switches in a high channel density application has many advantages over the use of parallel controlled switches. It enables the reduction of board space used per switch, which, in turn, increases the density of switches that can be realized. This is due to the reduction of digital control lines needed and the removal of the devices required to provide these control lines.

Analog Devices has a new innovative precision SPI switch solution that enables the increase of channel density. This is facilitated by the daisy-chain mode that is available on these devices. The same industry-leading switch performance seen in Analog Devices' current switch offerings is maintained due to the dual-die solution used. The ADGS1412 is the first release in a family of new SPI controlled switches with a complete portfolio coming in 2017 and 2018.

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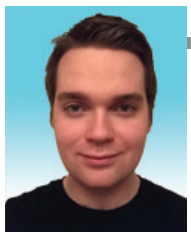

Stephen Nugent

Understanding and Eliminating 1/f Noise

By **Robert Kiely**

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Introduction

This article explains what 1/f noise is and how to reduce or eliminate it in precision measurement applications. 1/f noise cannot be filtered out and can be a limit to achieving the best performance in precision measurement applications.

What Is 1/f Noise?

1/f noise is low frequency noise for which the noise power is inversely proportional to the frequency. 1/f noise has been observed not only in electronics but also in music, biology, and even economics.[1] The sources of 1/f noise are still widely debated and much research is still being done in this area.[2]

Looking at the voltage noise spectral density of the ADA4622-2 op amp shown in Figure 1, we can see that there are two distinct regions visible in the graph. On the left of Figure 1 we can see the 1/f noise region and on the right of Figure 1 we can see the broadband noise region. The crossover point between the 1/f noise and the broadband noise is called the 1/f corner.

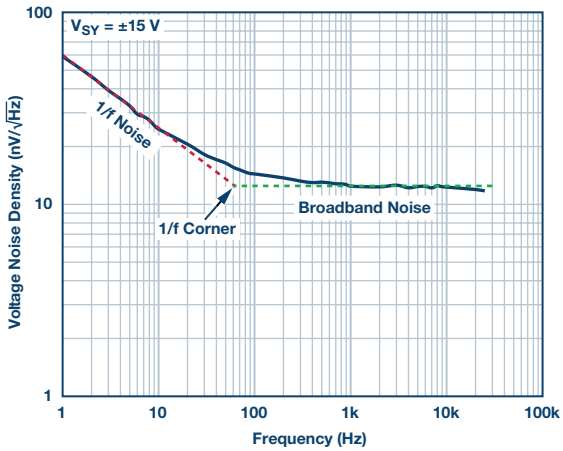

Figure 1. ADA4622-2 voltage noise spectral density.

How Do We Measure and Specify 1/f Noise?

After comparing the noise density graphs of a number of op amps, it becomes apparent that the 1/f corner can vary for each product. To easily compare components, we need to use the same bandwidth when measuring the noise of each component. For low frequency voltage noise, the standard specification is 0.1 Hz to 10 Hz peak-to-peak noise. For op amps, the 0.1 Hz to 10 Hz noise can be measured using the circuit shown in Figure 2.

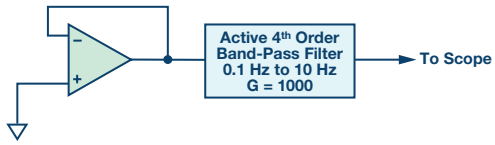

Figure 2. Low frequency noise measurement.

The op amp is put in a unity-gain feedback configuration with the noninverting input grounded. The op amp is powered from a split supply to allow for the input and the output to be at the ground.

The active filter block limits the bandwidth of the noise that is measured while simultaneously providing a gain of 1000 to the noise from the op amp. This ensures that the noise from the device under test is the dominant source of noise. The offset of the op amp is not important, as the input to the filter is ac-coupled.

The output of the filter is connected to an oscilloscope and the peak-to-peak voltage is measured for 10 seconds to ensure we capture the full 0.1 Hz to 10 Hz bandwidth (1/10 seconds = 0.1 Hz). The results shown on the scope are then divided by the gain of 1000 to calculate the 0.1 Hz to 10 Hz noise. Figure 3 shows the 0.1 Hz to 10 Hz noise for the ADA4622-2. The ADA4622-2 has a very low, 0.1 Hz to 10 Hz noise of just 0.75 µV p-p typical.

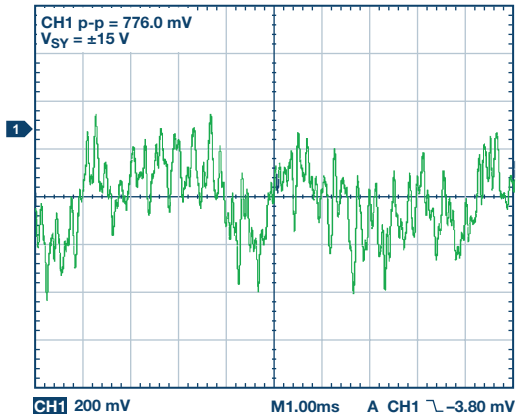

Figure 3. 0.1 Hz to 10 Hz noise, V_{SY} = ±15 V, G = 1000.

What Impact Does 1/f Noise Have in My Circuit?

The total noise in a system is the combined 1/f noise and broadband noise from each component in the system. Passive components have 1/f noise and current noise also has a 1/f noise component. However, for low resistances the 1/f noise and current noise are usually too small to be considered. This article will focus on voltage noise only.

To calculate the total system noise we calculate the 1/f noise and the broadband noise, and then combine them. If we use the 0.1 Hz to 10 Hz noise specification to calculate the 1/f noise, then we are assuming that the 1/f corner is below 10 Hz. If the 1/f corner is above 10 Hz, then we can estimate the 1/f noise using the following formula[3]:

$$\frac{1}{f}\ Noise_{rms} = en_{1Hz}\left(\sqrt{\ln\left(\frac{f_h}{f_l}\right)}\right)$$

where:

e_{n1Hz} is the noise density at 1 Hz,

f_h is the 1/f noise corner frequency,

f_l is 1/aperture time.

For example, if we want to estimate the 1/f noise for the ADA4622-2, then f_h is about 60 Hz. We set f_l to be equal to 1/aperture time. Aperture time is the total measurement time. If we set the aperture time or measurement time to be 10 seconds, then f_l is 0.1 Hz. The noise density at 1 Hz, e_{n1Hz}, is approximately 55 nV$\sqrt{\text{Hz}}$. This gives us a result of 139 nV_{rms} between 0.1 Hz and 60 Hz. To convert this to peak-to-peak we should multiply by 6.6, which will give us approximately 0.92 µV p-p.[4] This is about 23% higher than the 0.1 Hz to 10 Hz specification.

The broadband noise can be calculated using the following formula:

$$Noise_{rms} = e_n\ \left(\sqrt{\text{NEBW}}\right)$$

where:

e_n is the noise density at 1 kHz,

NEBW is the noise equivalent bandwidth.

The noise equivalent bandwidth takes into account the additional noise beyond the filter cutoff frequency due to the gradual roll-off of the filter. The noise equivalent bandwidth is dependent on the number of poles in the filter and the filter type. For a simple one pole, low-pass Butterworth filter, the NEBW is 1.57 × filter cutoff.

The wideband rms noise for the ADA4622-2 is just 12 nv$\sqrt{\text{Hz}}$ at 1 kHz. Using a simple RC filter on the output with a cutoff frequency of 1 kHz, the wideband rms noise is approximately 475.5 nV_{rms} and can be calculated as follows:

$$WB\ Noise_{rms} = 12\ nV\ \left(\sqrt{1\ \text{kHz} \times 1.57}\right)$$

Note that a simple low-pass RC filter has the same transfer function as a single-pole, low-pass Butterworth filter.

To get the total noise we must add the 1/f noise and the broadband noise together. To do this we can use the root sum square method as the noise sources are uncorrelated.

$$Total\ Noise_{rms} = \sqrt{\left(\frac{1}{f}Noise_{rms}\right)^2 + \left(WB\ Noise_{rms}\right)^2}$$

Using this equation we can calculate the ADA4622-2 total rms noise with a simple 1 kHz, low-pass RC filter on the output to be 495.4 nV_{rms}. This is just over 4% higher noise than the broadband noise alone. It's clear from this example that 1/f noise affects systems that measure from dc up to very low bandwidth only. Once you go beyond the 1/f corner by about a decade or more, the contribution of the 1/f noise to the total noise becomes almost too small to worry about.

Since noise adds together as a root sum square, we can decide to ignore the smaller noise source if it is below about 1/5th of the larger noise source, since below a ratio of 1/5th the noise contribution is about a 1% increase in the total noise.[5]

How Do We Remove or Mitigate 1/f Noise?

Chopper stabilization, or chopping, is a technique to reduce amplifier offset voltage. However, since 1/f noise is near dc low frequency noise, it is also effectively reduced by this technique. Chopper stabilization works by alternating or chopping the input signals at the input stage and then chopping the signals again at the output stage. This is the equivalent to modulation using a square wave.

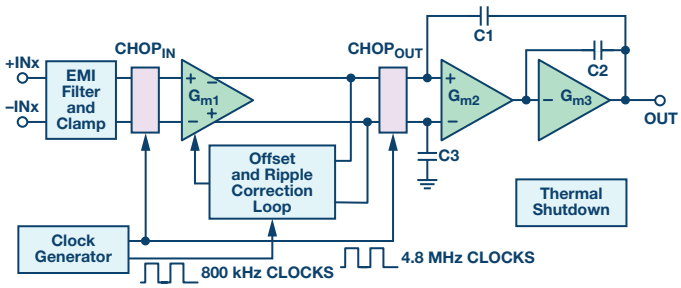

Figure 4. ADA4522 architecture block diagram.

Referring to the ADA4522 architecture block diagram shown in Figure 4, the input signal is modulated to the chopping frequency at the $CHOP_{IN}$ stage. At the $CHOP_{OUT}$ stage, the input signal is synchronously demodulated back to its original frequency and simultaneously the offset and 1/f noise of the amplifier input stage are modulated to the chopping frequency. In addition to reducing the initial offset voltage, the change in offset vs. common-mode voltage is reduced, which results in very good dc linearity and a high common-mode rejection ratio (CMRR). Chopping also reduces the offset voltage drift vs. temperature. For this reason, amplifiers that use chopping are often referred to as zero-drift amplifiers. One key thing to note is that zero-drift amplifiers only remove the 1/f noise of the amplifier. Any 1/f noise from other sources, such as the sensor, will pass through unaffected.

The trade-off for using chopping is that it introduces switching artifacts into the output and increases the input bias current. Glitches and ripple are visible on the output of the amplifier when viewed on an oscilloscope and noise spikes are visible in the noise spectral density when viewed using a spectrum analyzer. The newest zero-drift amplifiers from Analog Devices—such as the ADA4522 55 V zero-drift amplifier family—use a patented offset and ripple correction loop circuit to minimize switching artifacts.[6]

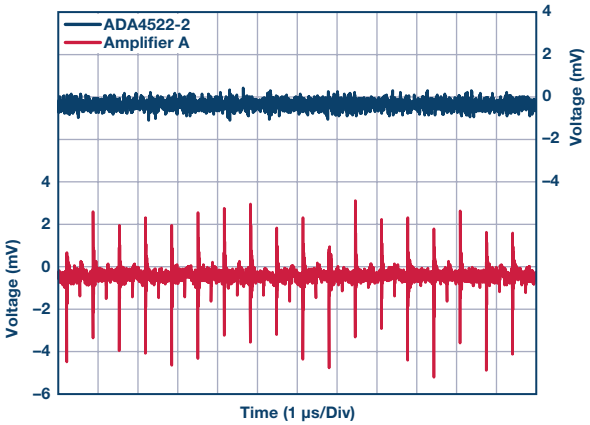

Figure 5. Output voltage noise in the time domain.[6]

Chopping can also be applied to instrumentation amplifiers and ADCs. Products such as the AD8237 true rail-to-rail, zero-drift instrumentation amplifier, the new AD7124-4 low noise and low power, 24-bit Σ-Δ ADC, and the recently released AD7177-2 ultralow noise, 32-bit Σ-Δ ADC, use chopping to eliminate 1/f noise and minimize drift vs. temperature.

One disadvantage to using square wave modulation is that square waves contain many harmonics. Noise at each harmonic will be demodulated back to dc. If sine wave modulation is used instead, then this approach is much less susceptible to noise and can recover very small signals in the presence of large noise or interference. This is the approach used by lock-in amplifiers.[7]

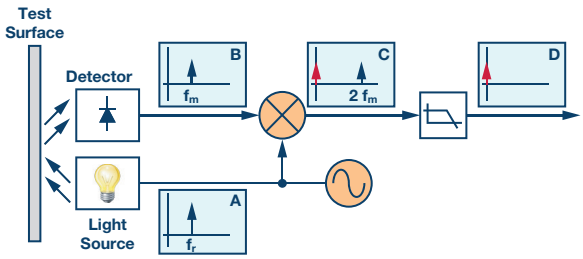

Figure 6. Measuring surface contamination with a lock-in amplifier.[7]

In the example shown in Figure 6, the sensor output is modulated by using a sine wave to control a light source. A photodetector circuit is used to detect the signal. Once the signal passes through the signal conditioning stage it can be demodulated. The same sine wave is used to modulate and demodulate the signal. The demodulation returns the sensor output to dc, but also shifts the 1/f noise of the signal conditioning stage to the modulation frequency. The demodulation can be done in either the analog or digital domain after ADC conversion. A very narrow low-pass filter—for example, 0.01 Hz—is used to reject the noise above dc and we are left with only the original sensor output with extremely low noise. This relies on the sensor output being at exactly dc, so the precision and fidelity of the sine wave is important. This approach eliminates the 1/f noise of the signal conditioning circuitry, but does not eliminate the 1/f noise of the sensor.

If a sensor requires an excitation signal, then it is possible to eliminate the 1/f noise from the sensor using ac excitation. AC excitation works by alternating the sensor excitation source to produce a square wave output from the sensor and then subtracting the output from each phase of the excitation. This approach not only allows us to eliminate the 1/f noise of the sensor, but also eliminates offset drift in the sensor and eliminates unwanted parasitic thermocouple effects.[8]

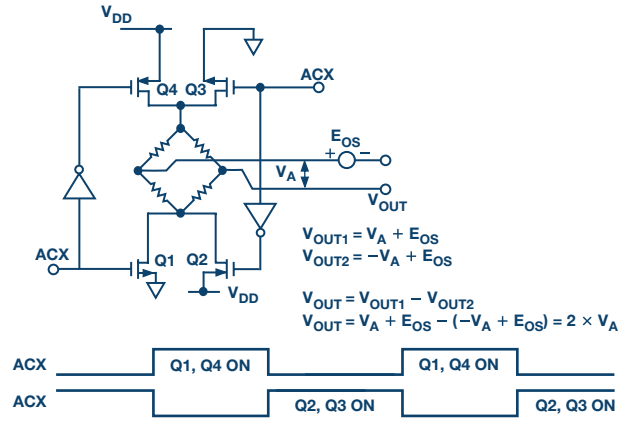

Figure 7. AC excitation of a bridge sensor.[8]

AC excitation can be done using discrete switches and controlling them with a microcontroller. The AD7195 low noise, low drift, 24-bit Σ-Δ ADC with internal PGA included drivers to implement ac excitation of the sensor. The ADC manages the ac excitation transparently by synchronizing the sensor excitation with the ADC conversions, making ac excitation easier to use.

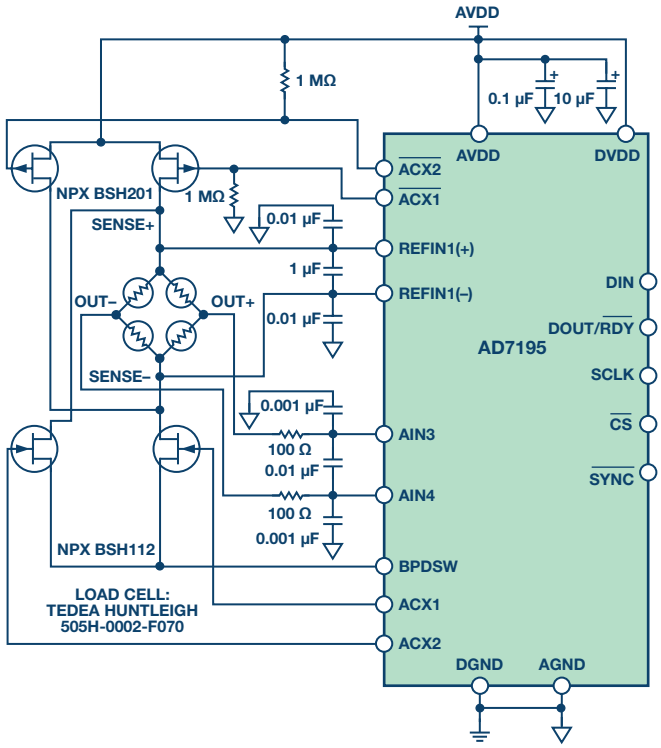

Figure 8.CN-0155—Precision weigh scale design using a 24-bit Σ-Δ ADC with internal PGA and ac excitation.

Implementation

When using zero-drift amplifiers and zero-drift ADCs, it is very important to be aware of the chopping frequency of each component and the potential for intermodulation distortion (IMD) to occur. When two signals are combined, the resulting waveform will contain the original two signals, as well as the sum and difference of these two signals.

For example, if we consider a simple circuit using the ADA4522-2 zero-drift amplifier and the AD7177-2 Σ-Δ ADC, the chopping frequencies of each part will mix and create sum and difference signals. The ADA4522-2 has a switching frequency of 800 kHz, while the AD7177-2 has a switching frequency of 250 kHz. The mixing of these two switching frequencies will cause additional switching artifacts at 550 kHz and 1050 kHz. In this case, the AD7177-2 maximum corner frequency of the digital filter, 2.6 kHz, is much lower than the lowest artifact and will remove all of these IMD artifacts. However, if two identical zero-drift amplifiers are used in series, the IMD created will be the difference in the internal clock frequency of the parts. This difference could be small, and therefore, the IMD would appear at much closer to dc and be more likely to fall inside the bandwidth of interest.

In any case it is important to consider IMD when designing a system that uses zero-drift or chopped parts. It should be noted that most zero-drift amplifiers have much lower switching frequencies than the ADA4522-2. In fact, the high switching frequency is a key benefit to using the ADA4522 family when designing precision signal chains.

Conclusion

1/f noise can limit performance in any precision dc signal chain. However, it can be removed by using techniques such as chopping and ac excitation. There are some trade-offs to using these techniques, but modern amplifiers and Σ-Δ converters have addressed these issues, making zero-drift products easier to use across a broader range of end applications.

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Robert Kiely

Rarely Asked Questions—Issue 141 Sometimes, a Signal Needs to Ride the Rails

By **Daniel Burton**

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Question:

I'm designing a signal conditioning block for a precision sensor analog front end. Should I use an op amp with rail-to-rail input?

Answer:

Possibly—it depends on if the output signal from the sensor forces the op amp to a voltage near the supply rails. For example, if we were to monitor a load current of 0 mA to 500 mA through a precision 10 Ω shunt resistor, the maximum output would be 5 V. If the amplifier supply voltage was 5 V, you would need to choose an amplifier with a rail-to-rail input voltage range.

The classic input stage of many op amps is a transistor differential pair. In order for the op amp to amplify the common-mode voltage (V_{CM}) signal at the input, it must have sufficient voltage headroom between the V_{CM} and the supply voltages. If V_{CM} gets close enough to either supply rail so that the input pair runs out of headroom, the input offset voltage, as well as other key parameters, will be degraded, resulting in a loss of accuracy, as seen in Figure 1. It is these headroom requirements that define the op amp's specified input voltage range (IVR). Some of the industry's highest precision amplifiers, like the ADA4610, have this classic input structure. As long as the input voltage stays away from the rails, it has excellent precision.

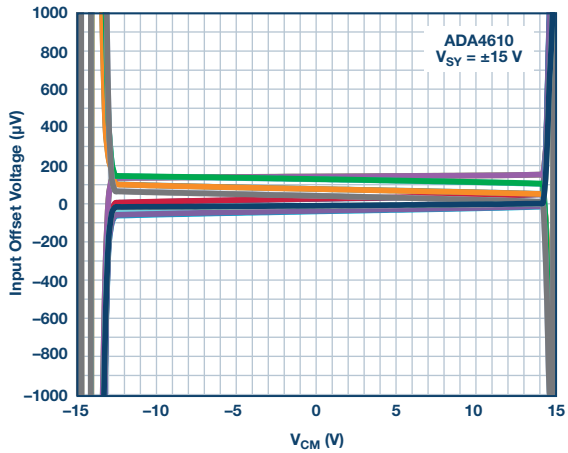

Figure 1. ADA4610 Typical input offset voltage vs. common-mode voltage.

If the sensor's output signal does not include the V+ rail, but does range all the way down to the negative rail, it requires an amplifier that can accept a V_{CM} that also goes to V–. This type of op amp is called single supply because, by tying the V– to ground, only one voltage source is required. Single-supply op amps use a special circuit topology that allows amplification of the signal even when it is near the V– rail.

Similarly, some applications require an op amp that maintains accuracy when the input ranges all the way from V– to V+. This is called a rail-to-rail input (RRI) op amp. These op amps typically combine two differential pairs—one for each rail. The ADA4661 is a classic example of an RRI op amp. As seen in Figure 2, it has excellent accuracy across the whole range of the supply voltages.

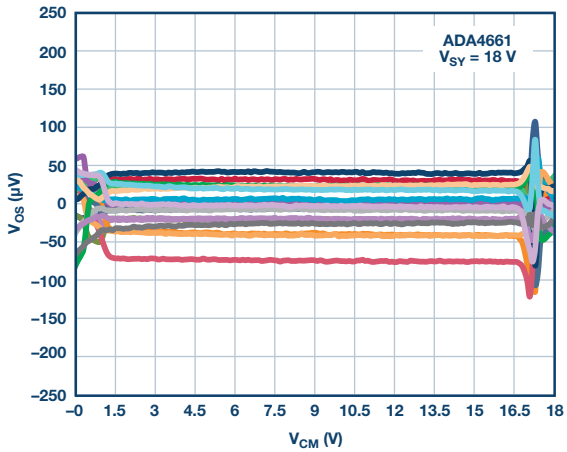

Figure 2. ADA4661: rail-to-rail op amp, typical input offset voltage vs. common-mode voltage.

There are trade-offs when the input is comprised of two different pairs to create a rail-to-rail input. As V_{CM} transitions from one pair to the other, a small crossover distortion is reflected in the offset voltage. In the ADA4661, you can see the distortion amplitude is about 50 µV and occurs about 2 V below the V+ rail. Although this may not be significant in some systems, we may need to avoid this distortion in others. One solution is to design the system so that the input voltage stays below the crossover voltage. In Figure 2, that would still give over 16 V of IVR. Applications with a low supply voltage (say 5 V) create a challenge since we can't afford to give up enough IVR (say 2 V) without significantly reducing the voltage range of the input signal. In that application, we'll need a different type of input stage.

The ADA4500 eliminates crossover, and therefore crossover distortion, by using a single input pair, combined with a charge pump that provides a higher internal voltage so that the pair has sufficient supply voltage, even when the op amp filter is at the rails. With this structure the sensor can drive the op amp's input voltage over the full supply range with no crossover distortion, as shown in Figure 3. While doing so, it delivers a guaranteed 95 dB of common-mode rejection and input offset voltage of 120 µV at 25°C for superior accuracy, even when the input signal has to ride the rails.

For a detailed discussion of op amp input structures and trade-offs, see Mini Tutorial MT-035 "Op Amp Inputs, Outputs, Single-Supply, and Rail-to-Rail Issues" as well as the other references listed below.

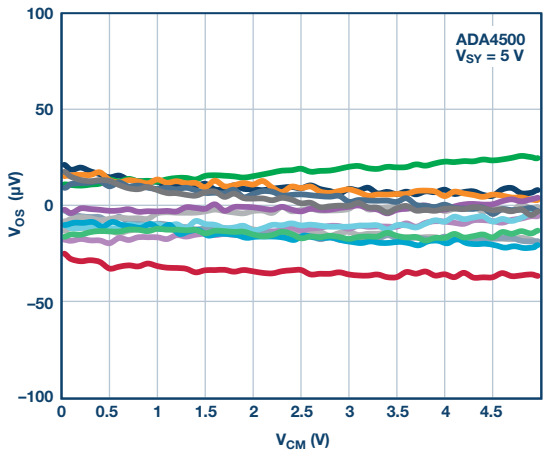

Figure 3. The ADA4500 rail-to-rail op amp eliminates distortion across its full supply range.

Table 1. Selection of Precision Op Amps from Classic Rail-to-Rail (All Values Are in V)

Precision Op Amp	Headroom from V+	Headroom from V–	Supply Range	Input Structure
ADA4610	2.5	2.5	10 to 36	Classic differential pair
ADA4522	1.5	0	4.5 to 55	Single supply
ADA4622	1	–0.2	10 to 30	Single supply
ADA4084	0	0	3 to 30	Rail-to-rail
ADA4661	0	0	3 to 18	Rail-to-rail
ADA4505	0	0	1.8 to 5	Zero crossover distortion
ADA4500	0	0	2.7 to 5.5	Zero crossover distortion

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Volume 50, Number 3

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Bernhard became editor of *Analog Dialogue* in March 2017, when the preceding editor, Jim Surber, decided to retire. Bernhard has been with Analog Devices for over 25 years, starting at the ADI Munich office in Germany.

Bernhard has worked in various engineering roles including sales, field applications, and product engineering, as well as in technical support and marketing roles.

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