Analog Dialogue

Volume 50, Number 4, 2016

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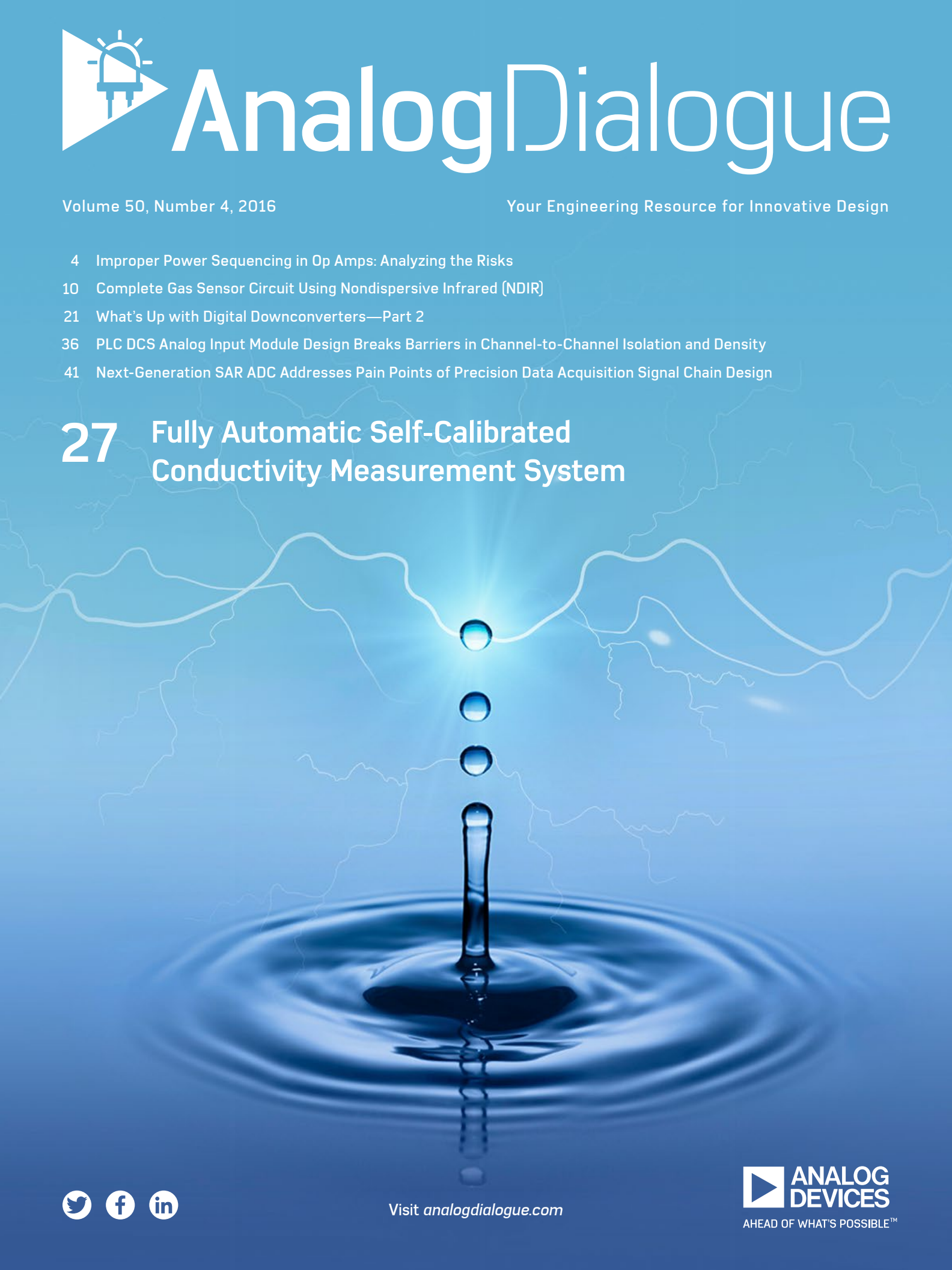

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In This Issue

Jim Surber, Editor

Jim became editor of *Analog Dialogue* in May of 2015, when the preceding editor, Scott Wayne, decided to retire. Jim has been with Analog Devices for 40+ years, starting with a company called Computer Labs, a maker of high speed data converters, which was acquired by ADI in 1978.

Jim has worked in production test, applications engineering, product line marketing, and, most recently, marketing communications. He enjoys writing and has published several technical articles in various magazines down through the years. Residing in Greensboro, North Carolina, Jim enjoys spending time with his family on frequent mountain outings.

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AnalogDialogue

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Improper Power Sequencing in Op Amps: Analyzing the Risks

By **David Guo**

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Introduction

In systems with multiple supply voltages, operational amplifier power supplies must be established simultaneously with or before any input signals are applied. If this doesn't happen, overvoltage and latch-up conditions can occur.

However, this can sometimes be a difficult requirement to meet in real-world applications. This article takes a look at the activity of op amps in different power sequence situations (see Table 2), analyzes possible issues, and presents some suggestions.

Power Sequencing Issues Can Vary

There are a number of different scenarios where power sequencing issues may arise. For example, in one customer application, an AD8616 can be configured as a buffer, the input is 0 V before power supplies are established (Figure 1), and the negative supply is powered on before the positive supply (negative power is present and positive power is absent).

Table 1 shows the results of all AD8616 pins in such conditions. Before V+ is applied, the voltage at the V+ pin and OUT pins is negative. This may not damage the op amp, but if these signals are connected to terminals on other chips that haven't been fully powered (for example, assuming the ADC uses the same V+, and its power pin normally tolerates only –0.3 V minimum voltage), the chips may suffer damage. A similar issue will happen if V+ is powered up before V–.

Table 2 highlights some possible situations in power sequencing.

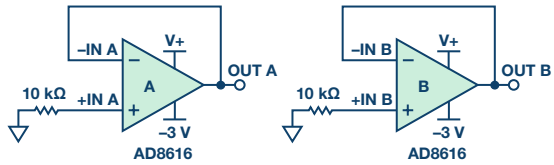

Figure 1. AD8616 test circuit with –3 V V– applied and V+ absent.

Table 1. AD8616 Pins' Voltage with –3 V V– Applied and V+ Absent

Pin1: OUTA	Pin2: –INA	Pin3: +INA	Pin4: V–	Pin5: +INB	Pin6: –INB	Pin7: OUTB	Pin8: V+
–1.627	–1.627	–0.959	–3.000	–0.959	–1.627	–1.627	–1.627

Table 2. Possible Situations in Power Sequencing

	IN	V+	V–	Amplifier Power with Load	Amplifier Out with Load
Case 1	Floating Floating	Present Absent	Absent Present	No No	No No
Case 2	0 V 0 V	Present Absent	Absent Present	No No	No No
Case 3	Positive or negative Positive or negative	Present Absent	Absent Present	No No	No No
Case 4	Positive or negative Positive or negative Positive or negative Positive or negative	Present Present Absent Absent	Absent Absent Present Present	Yes No Yes No	No Yes No Yes

Electrostatic Discharge (ESD) Diodes Within Op Amps

Electrostatic discharge can also result in an overvoltage event. Most op amps have an internal ESD diode to prevent electrostatic ESD events. ESD diodes can provide a key to analyzing activity when either V+ or V– is absent. Figure 2 is a simplified block diagram of the ADA4077/ADA4177. Table 3 shows the ADA4077-2/ADA4177-2's typical drop voltage of internal ESD diodes and back-to-back diodes. Notice that back-to-back diodes are placed between the two input terminals of the op amps to clamp the maximum differential input signal.

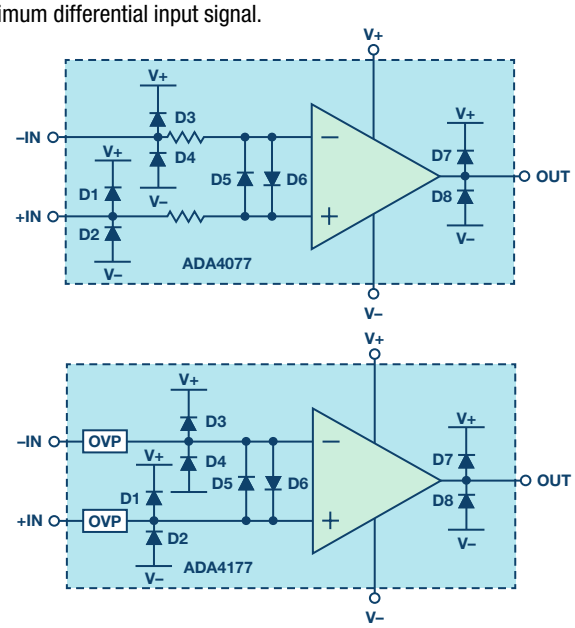

Figure 2. ADA4077/ADA4177 simplified block diagram.

Table 3. Internal Diode of an Op Amp

	ADA4077	ADA4177
D1	0.838	Unknown
D2	0.845	Unknown
D3	0.837	Unknown
D4	0.844	Unknown
D5	Unknown	Unknown
D6	Unknown	Unknown
D7	0.841	0.849
D8	0.842	0.849

Also note that when DMM is used to measure D5/D6 of the ADA4077-2, it shows no diode between the two input terminals. In fact, there are two series of resistors before the back-to-back diodes to limit input current smaller than ±10 mA. The internal resistors and back-to-back diodes limit the differential input voltage to ±Vs to prevent a base-emitter junction breakdown.

For the ADA4177, OVP cells are integrated for robustness. They are placed before the ESD diodes and back-to-back diodes, so it's hard to measure these diodes by DMM. The output ESD diodes of ADA4177 can be measured.

Evaluation Setup

Figure 3 is used to measure the activity of the op amp. Channel A and Channel B are each configured as a buffer, and the Channel B noninverting input is connected to the GND by a 100 kΩ resistor. By making V+ absent (V– present) or V+ present (V– absent), the input and power-related variables can be measured by the ampere and voltage meters. By analyzing these variables, we can determine the current flow path.

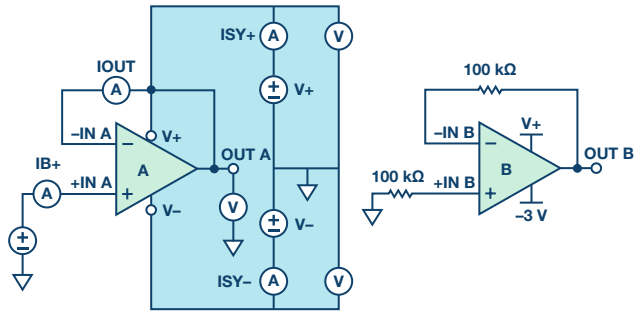

Figure 3. Setup for power sequencing test.

Case 1: Input Is Floating

Table 4 shows the results of a floating input and one absent supply. When V– is present and V+ is absent, there is a negative voltage at the V+ pin. When V+ is present and V– is absent, there is a positive voltage at the V– pin.

Testing the ADA4077-2 and ADA4177-2 reveals similar results. No large currents are observed at the input pins and power pins, and the op amp with floating input remains safe when a power rail is absent.

Case 2: Input Is Grounded

Table 5 shows the results when the input is grounded. Note for IB+, a negative value means the current flow out of the +IN terminal. For IOUT, a negative value means the current flow out of the –IN terminal.

Table 4. ADA4077-2/ADA4177-2 Results with Floating Input

	Condition	V+	V–	ISY+ (mA)	ISY– (mA)	IB+ (mA)	IOUT (mA)	IN (V)	OUT (V)
ADA4077-2	All power	15	–15	1.02	1.01	–0.00005	0.00007	0.001	–0.008
	V+ absent	–13.1	–15	0	0.12	–0.00001	0.001	–13.73	–14.42
	V– absent	15	13.06	0.15	0	–0.00001	0.001	12.93	13.62
ADA4177-2	All power	15	–15	0.98	0.96	–0.00001	0.00002	0	0.001
	V+ absent	–14.26	–15	0	0.14	–0.00002	0.00137	–13.77	–13.78
	V– absent	15	12.96	0.14	0	–0.00001	–0.00039	12.26	12.31

Table 5. ADA4077-2/ADA4177-2 Results with Grounded Input

	Condition	V+	V–	ISY+ (mA)	ISY– (mA)	IB+ (mA)	IOUT (mA)	IN (V)	OUT (V)
ADA4077-2	All power	15	–15	1.01	1	–0.00005	0.00001	0	–0.019
	V+ absent	–0.846	–15	0	2.30	2.300	–1.60	–0.017	–2.68
	V– absent	15	0.847	1.78	0	–1.758	1.064	0.012	2.116
ADA4177-2	All power	15	–15	0.98	0.96	–0.00001	0.00002	0	0
	V+ absent	–11.99	–15	0	9.3	9.300	–0.200	–0.068	–11.98
	V– absent	15	1.848	1.84	0	–1.823	0.067	0.013	1.851

Taking ADA4077-2 with V+ absent as an example, V+ is clamped to the VIN voltage by an ESD diode.

- VIN is connected to V+ via an ESD clamp diode, so when VIN is 0 V, V+ is –0.846 V.
- Current flow path loop: as per the red path shown in Figure 4, 0.7 mA current flows from GND (+IN) to V+. 1.6 mA current flows from GND (+IN) through an internal resistor, D5 and the feedback path between –IN and OUT, then the current flows into the output terminal. Finally the two currents (0.7 mA and 1.6 mA) combine to flow to –15 V, and the combined current flows back to GND (+IN).

Results are similar between the ADA4177-2 and ADA4077-2. Note that within the ADA4177-2, D1 is implemented by an emitter base of a lateral PNP transistor. The transistor routes the overvoltage current away from the V+ to the V–. The ADA4177 circuit in Figure 4 shows 9.1 mA current flow from V+ back to V–, and combined with 0.2 mA current in the feedback path, results in a 9.3 mA current flow to –15 V, then the current flows back to GND.

No large currents are observed at the input pins and power pins for either the ADA4077-2 or the ADA4177-2 (Table 5). These op amps can withstand any order of PU sequencings in a gain of 1 with +IN grounded.

Case 3: With Input

A positive or negative signal (+10 V or –10 V) is applied to the +IN terminal when one power is absent. Table 6 shows no large current, so these op amps can withstand any order of PU sequencings in a gain of 1 with +IN grounded for a short duration.

The current flow path analysis is similar with Case 2 (0 V input), refer to Figure 5.

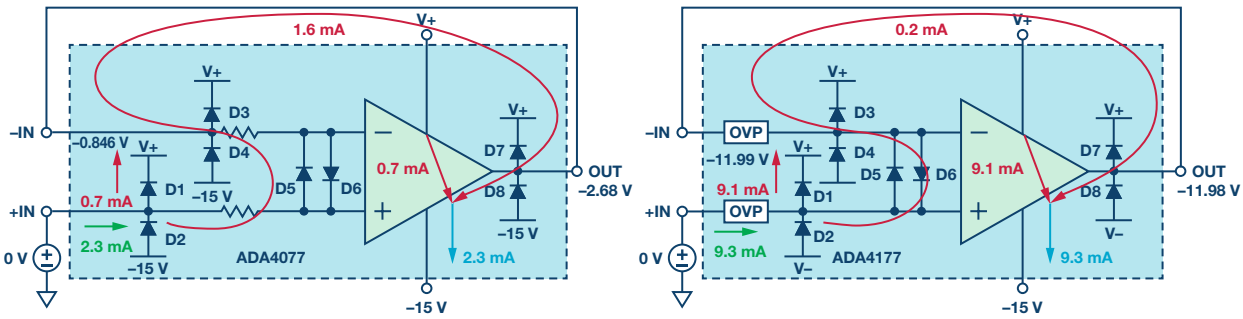

Figure 4. ADA4077/ADA4177 current path when V+ is absent (input grounded).

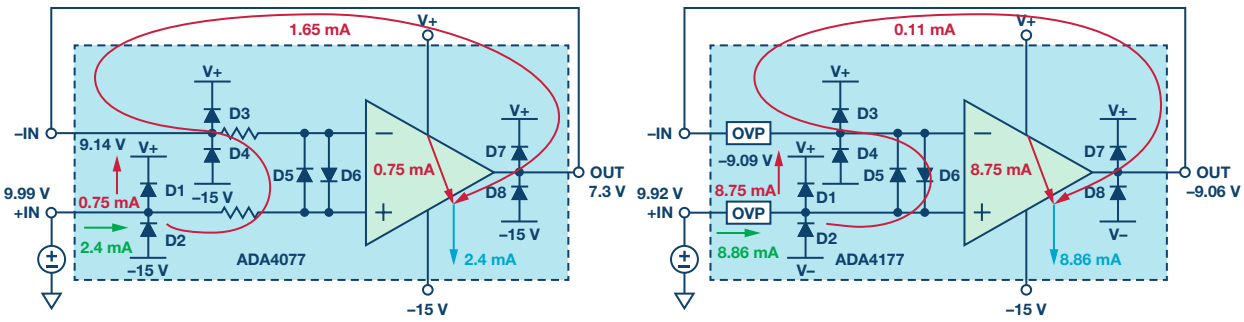

Figure 5. ADA4077/ADA4177 current path when V+ is absent (10 V input).

Table 6

	Condition	V+	V–	ISY+ (mA)	ISY– (mA)	IB+ (mA)	IOUT (mA)	IN (V)	OUT (V)
ADA4077-2	All power	15	–15	1.03	1.01	0.00098	–0.00003	10	9.97
	V+ absent and positive input	9.14	–15	0	2.4	2.396	–1.653	9.99	7.3
	V+ absent and negative input	–10.83	–15	0	2.41	2.308	–1.651	–10.02	–12.66
	V– absent and positive input	15	10.83	1.81	0	–1.689	1.055	10.02	12.09
	V– absent and negative input	15	–9.15	1.77	0	–1.759	1.031	–9.99	–7.88
ADA4177-2	All power	15	–15	1.02	1	–0.00099	–0.00009	9.99	9.97
	V+ absent and positive input	–9.09	–15	0	8.86	8.866	–0.113	9.92	–9.06
	V+ absent and negative input	–12.33	–15	0	4.31	4.18	–0.039	–10.02	–12.32
	V– absent and positive input	15	11.42	1.33	0	–1.2	0.056	9.99	11.43
	V– absent and negative input	15	–8.33	1.51	0	–1.492	0.062	–9.97	–8.32

Case 4: With Input and with Load at Power/Output

In a real application, the op amp circuit may work with another circuit. For example, the op amp's output may drive a load, or the op amp's power supply may also power other circuits. This can cause a problem.

In this test, a 47 Ω resistor is connected between the output and GND or the absent power pins and GND. Table 7 shows the test results for the ADA4077. Large currents are highlighted in red. Three possible situations can pose risks, assuming V+ is absent:

- Situation 1: When the input is 10 V and the load of OUT is 47 Ω, the output is 1.373 V. When there is a 23 mA current flow out of the op amp's output pin (refer to Figure 6) the current path is:
  - Input signal source supply 30.2 mA current
  - 24 mA current flow through D1 to V+, and 6.2 mA current flow through D5 and feedback path to OUT
  - 24 mA current from V+ is divided to 1 mA (to V–) and 23 mA (to OUT)
  - 29.2 mA current flows through 47 Ω load to GND

The current needs to be limited. By adding a 1 kΩ resistor at +IN, the input current is decreased to 6.8 mA.

- Situation 2: When the input is 10 V and the load of V+ is 47 Ω, 170 mA current flows into the ADA4077-2 and flows out of V+ pin to a 47 Ω power load. 170 mA current will burn the internal diode and damage the chip. By adding a 1 kΩ resistor at +IN, the input current is decreased to 8.9 mA. Figure 7 shows the current flow path.

Table 7. ADA4077 with Load at Output Pin or Absent Power Pin

ADA4077-2	Condition	IN (V)	V+	V–	ISY+ (mA)	ISY– (mA)	IB+ (mA)	IOUT (mA)	OUT (V)
V+ absent	Vo or V+ no load/positive input	9.99	9.14	–15	0	2.4	2.396	–1.653	7.3
	Vo 47 Ω to GND	9.98	8.77	–15	0	1.00	30.22	–6.174	1.373
	Vo 47 Ω to GND and 1 kΩ	9.98	2.389	–15	0	0.76	6.828	–2.104	0.284
	V+ 47 Ω to GND	9.59	8.01	–15	170	5.05	175	–5.0	6.06
	V+ 47 Ω to GND and 1 kΩ	9.94	0.295	–15	6.27	2.69	8.96	–2.69	–1.876
	Vo or V+ no load/negative input	–10.02	–10.83	–15	0	2.41	2.308	–1.651	–12.66
	Vo 47 Ω to GND	–9.97	–3.226	–15	0	48.6	–4.65	4.885	–2.501
	Vo 47 Ω to GND and 1 kΩ	–10.02	–10.83	–15	0	14.30	2.284	–1.629	–0.563

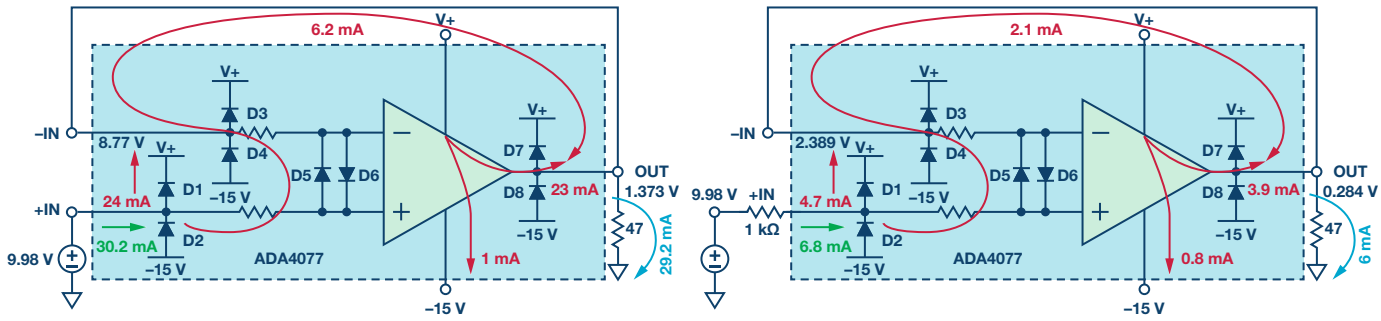

Figure 6. ADA4077 current path when V+ is absent (10 V input and 47 Ω output load).

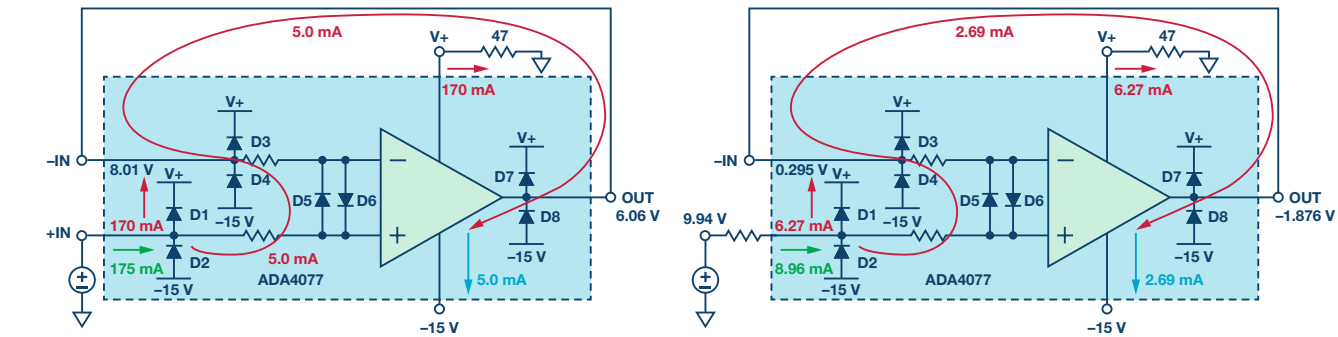

Figure 7. ADA4077 current path when V+ is absent (10 V input and 47 Ω power load).

- Situation 3: When input is negative (–10 V) and the load of OUT is 47 Ω (refer to Figure 8), there is a 48 mA current that flows through the chip. This will generate a 48 mA × (–2.5 V + 15 V) = 0.6 W power dissipation. Considering the ADA4077-2's 158° C/W ΘJA , the junction temperature is 94.8° higher than the ambient temperature. If there are two channels or there is a heavier load, the junction temperature may be higher than 150°, and the chip may be damaged.
- Instead of adding a current-limiting resistor at the input, the resistor should be added at the output.
- When V+ is present and V– is absent, the same phenomena will happen. By adding external resistors to limit the current, the circuit can be more robust.

For ADA4177-2, only Situation 3 applies. When there is a large negative input and a heavy load at the output at the same time and when V+ is absent and there is 53 mA current flow through the chip, the power dissipation may be increased and the junction temperature is increased (refer to Figure 9). By adding a 1 kΩ resistor at the output, the risk can be avoided.

Of the two op amps, the ADA4177-2 is more robust than the ADA4077-2. It is a preferred choice for applications that require both precision and robustness.

Other Op Amp Activity in Power Sequencing

Among op amps, there are varying implementations of diodes, resistors, and OVP cells. Some op amps have no internal OVP cells, some have no back-to-back diodes. A different implementation will produce different results if one power supply is absent. In addition, different op amp designs can produce different results.

For example, the ADA4084-2 has no internal current-limiting resistor or OVP cells, and it has ESD diodes connected to the power supply and back-to-back diodes. Table 9 and Figure 10 show the results when V+ is absent and there is 10 V input. The ADA4084's activity and current path are similar to those of the ADA4077-2 and ADA4177-2 (discussed previously in Case 3). However, because the ADA4084 has no internal resistor or OVP cell to limit the current, 60 mA current will flow into the chip, which may cause damage.

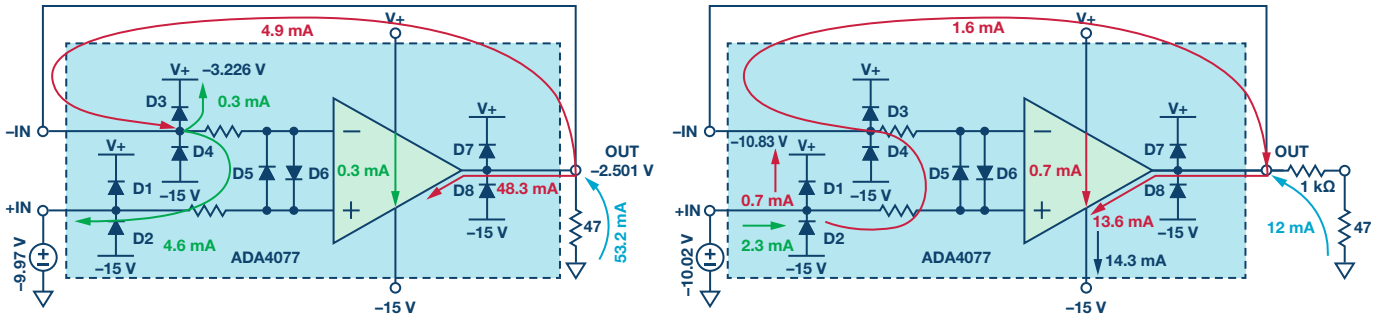

Figure 8. ADA4077 current path when V+ is absent (–10 V input and 47 Ω output load).

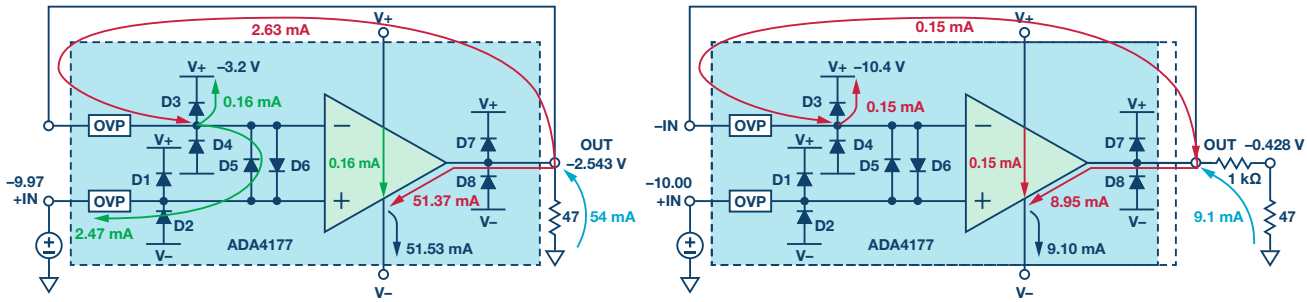

Figure 9. ADA4177 current path when V+ is absent (–10 V input and 47 Ω output load).

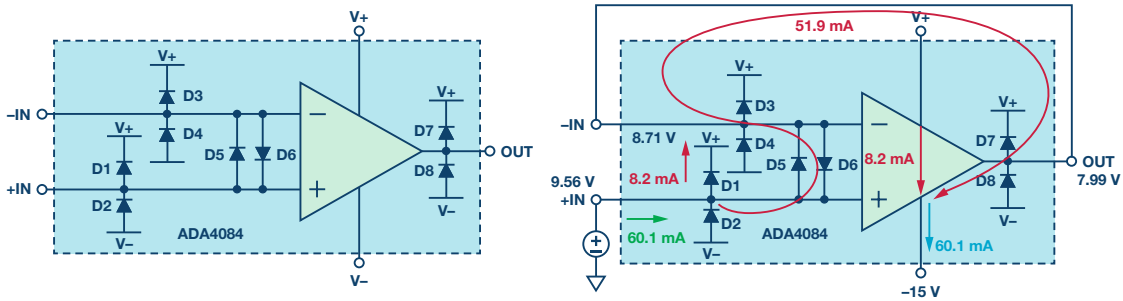

Figure 10. ADA4084 current path when V+ is absent (10 V input).

Table 8. ADA4177 with Load at Output Pin or Absent Power Pin

ADA4177-2	Condition	IN (V)	V+	V–	ISY+ (mA)	ISY– (mA)	IB+ (mA)	IOUT (mA)	OUT (V)
V+ absent	Vo or V+ is floating and negative input	–10.02	–12.33	– 15	0	4.31	4.18	–0.039	–12.32
	Vo 47 Ω to GND	–9.97	–3.218	– 15	0	51.53	–2.473	2.632	–2.543
	Vo 47 Ω to GND and 1 kΩ	–10	–10.4	– 15	0	9.10	–0.003	0.147	–0.428

Table 9

ADA4084-2	Condition	V+	V–	I+ (mA)	I– (mA)	IB+ (mA)	IOUT (mA)	IN (V)	OUT (V)
	All power	15	–15	1.38	1.37	–0.001	–0.0001	10	9.98
	V+ absent and positive input	8.71	–15	0	60.1	60.102	–51.89	9.56	7.99

In system applications, different op amps, different topology (such as noninverting amplification, inverting amplification, and difference amplification), different load, and external connections can be implemented. If one power supply is absent, the risks need to be evaluated. This article can provide guidance on setting up the evaluation circuit (Figure 2), how to analyze the current path, and evaluate the potential risks.

Summary

To avoid overvoltage or latch-up situations, operational amplifier power supplies must be established simultaneously. General guidelines are:

- During the Power On sequence, turn on the supply first, then apply a signal at the input
- During the Power Off, turn off the input signal first, then turn off the power supply

In real-world applications, these guidelines may be difficult to adhere to. This can cause problems, especially when there is an input signal, and designers need to properly evaluate the risk. An effective solution is try to limit the input current of the op amp so it is within the specifications in the data sheet. Adding a current-limiting resistor at the input and output can help in applications where power can't be supplied at the same time.

We tested three ADI op amps in a power supply absent application (ADA4084-2, ADA4077-2, and ADA4177-2). When integrated with internal resistors, the ADA4077-2 proved to be very robust. The ADA4177, when integrated with an OVP circuit, delivered the best robustness. In applications where the power may be absent, and external current-limiting resistors can't be added, the ADA4177 is recommended to avoid degrading the precision.

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ADA4177 data sheet. Analog Devices, Inc.

Arkin, Michael and Eric Modica. "Robust Amplifiers Provide Integrated Overvoltage Protection." *Analog Dialogue*, Volume 46, Number 1, 2012.

Blanchard, Paul and Brian Pelletier. "Using ESD Diodes as Voltage Clamps." *Analog Dialogue*, Volume 49, Number 10, 2015.

For more information on the ADA4177 and ADA4077, see the product pages and data sheets here: ADA4177 and ADA4077.

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David Guo

Also by this Author:

Low Power, Unity-Gain Difference Amplifier Implements Low Cost Current Source

Volume 45, Number 2

Complete Gas Sensor Circuit Using Nondispersive Infrared (NDIR)

By **Robert Lee** and **Walt Kester**

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Introduction

Nondispersive infrared (NDIR) spectroscopy is often used to detect gas and measure the concentration of carbon oxides (for example, carbon monoxide and carbon dioxide). An infrared beam passes through the sampling chamber, and each gas component in the sample absorbs some particular frequency of infrared. By measuring the amount of absorbed infrared at the appropriate frequency, the concentration of the gas component can be determined. The technique is said to be nondispersive because the wavelength that passes through the sampling chamber is not prefiltered and instead the optical filter is in front of the detector to eliminate all light except the wavelength, which the selected gas molecules can absorb.

The circuit shown in Figure 1 is a complete thermopile-based gas sensor using the NDIR principle. This circuit is optimized for CO2 sensing, but can also accurately measure the concentration of a large number of gases by using thermopiles with different optical filters.

The printed circuit board (PCB) is designed in an Arduino shield form factor and interfaces to the EVAL-ADICUP360 Arduino-compatible platform board. The signal conditioning is implemented with the AD8629 and the ADA4528-1 low noise amplifiers and the ADuCM360 precision analog microcontroller, which contains programmable gain amplifiers, dual, 24-bit, Σ-Δ analog-to-digital converters (ADCs), and an ARM® Cortex®-M3 processor.

The thermopile sensor is composed of a large number of thermocouples connected usually in series or, less commonly, in parallel. The output voltage of the series connected thermocouples depends on the temperature difference between the thermocouple junctions and the reference junctions. This principle is called the Seebeck effect after its discoverer, Thomas Johann Seebeck.

The circuit uses the AD8629 op amp to amplify the thermopile sensor output signals. The relatively small output voltage of the thermopile (from hundreds of microvolts to several millivolts) requires high gain with very low offset and drift to avoid dc errors. The high impedance (typically 84 kΩ) of the thermopile requires low input bias current to minimize errors, and the AD8629 bias current is only 30 pA typical. The very low drift with time and temperature eliminates additional errors once the temperature measurement has been calibrated. A pulsed light source synchronized with the ADC sampling rate minimizes the errors caused by low frequency drift and flicker noise.

The AD8629 only has 22 nV/√Hz voltage noise spectral density at 1 kHz, which is less than the thermopile voltage noise density of 37 nV/√Hz.

The AD8629 also has a very low current noise spectral density of 5 fA/√Hz typical at 10 Hz. This current noise flows through the 84 kΩ thermopile and only contributes 420 pV/√Hz at 10 Hz.

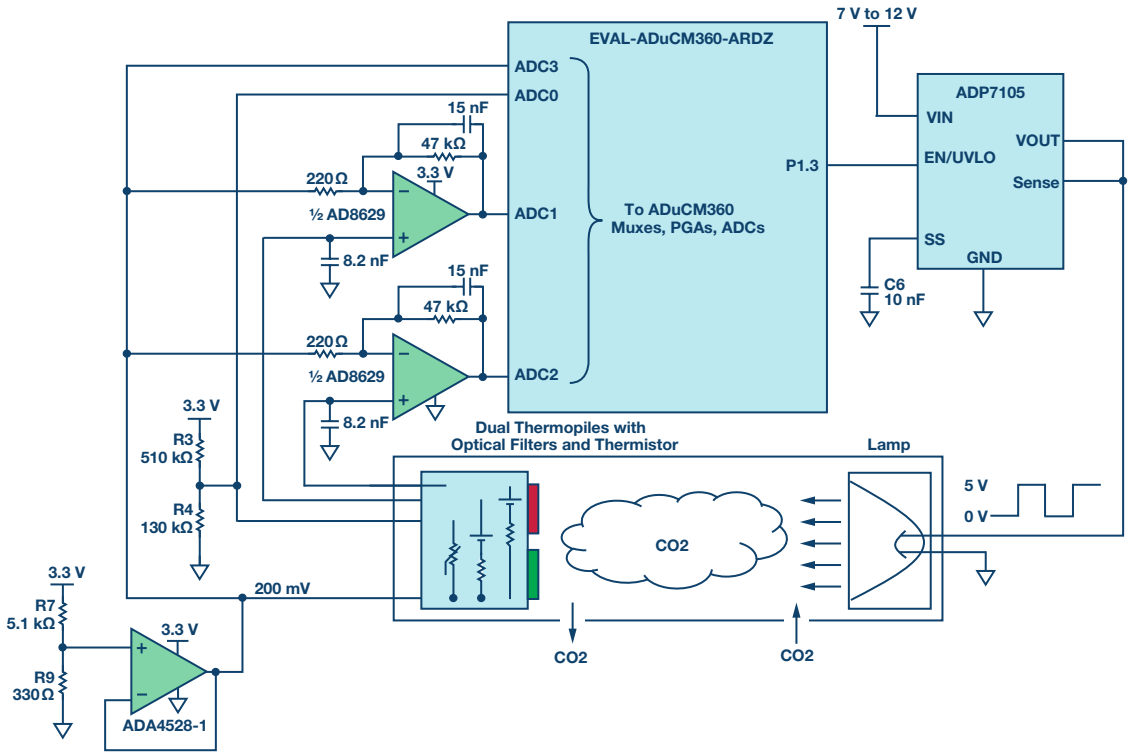

Figure 1. NDIR gas sensing circuit (simplified schematic: all connections and decoupling not shown) circuit description.

With the 200 mV common-mode voltage buffered by low noise amplifier ADA4528-1, the NTC and thermopile signal output meets the requirements of the ADuCM360 buffered mode input—AGND + 0.1 V to approximately AVDD – 0.1 V for ADuCM360 ADC buffered mode input. The CN-0338 Arduino shield board can be compatible with other types of Arduino-compatible platform board with single-input ADCs only.

The circuit chopping frequency can be 0.1 Hz to 5 Hz, selected by software. The ADP7105 low dropout regulator generates a stable 5 V output voltage to drive the lamp, and is turned on and off by the ADuCM360. The soft start feature of the ADP7105 eliminates the in-rush current when cold starting the lamp.

The ADuCM360 includes dual, 24-bit, Σ-Δ ADCs for simultaneous sampling of a dual element thermopile at programmable rates of 3.5 Hz to 3.906 kHz. The data rate in the NDIR system is limited from 3.5 Hz to 483 Hz for best noise performance.

Thermopile Detector Theory of Operation

To understand the thermopile, it is useful to review the basic theory of thermocouples.

If two dissimilar metals are joined at any temperature above absolute zero, there is a potential difference between them (their thermoelectric EMF or contact potential), which is a function of the temperature of the junction (see the thermoelectric EMF circuit in Figure 2).

If the two wires are joined at two places, two junctions are formed (see the thermocouple connected to load in Figure 2). If the two junctions are at different temperatures, there is a net EMF in the circuit, and a current flows determined by the EMF and the total resistance in the circuit (see Figure 2). If one of the wires is broken, the voltage across the break is equal to the net thermoelectric EMF of the circuit, and if this voltage is measured, it can be used to calculate the temperature difference between the two junctions (see the thermocouple voltage measurement in Figure 2). Remember that a thermocouple measures the temperature difference between two junctions, not the absolute temperature at one junction. The temperature at the measuring junction can be measured only if the temperature of the other junction (often called the reference junction or the cold junction) is known.

However, it is not so easy to measure the voltage generated by a thermocouple. Suppose that a voltmeter is attached to the first thermocouple measurement circuit (see the practical thermocouple voltage measurement showing cold junction in Figure 2). The wires attached to the voltmeter form further thermocouples where they are attached. If both these additional junctions are at the same temperature (it does not matter what temperature), the law of intermediate metals states that they make no net contribution to the total EMF of the system. If they are at different temperatures, they introduce errors. Because every pair of dissimilar metals in contact generates a thermoelectric EMF—including copper/solder, kovar/copper (kovar is the alloy used for IC lead frames), and aluminum/kovar (at the bond inside the IC)—the problem is even more complex in practical circuits, and it is necessary to take extreme care to ensure that all the junction pairs in the circuitry around a thermocouple, except for the measurement and reference junctions themselves, are at the same temperature.

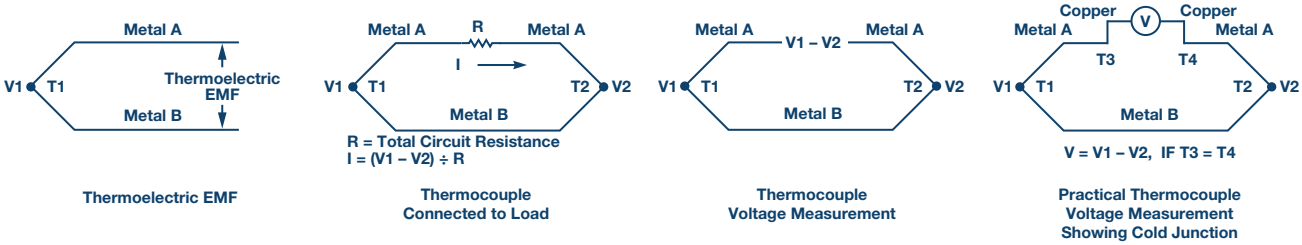

Figure 2. Thermocouple principles.

A thermopile consists of a series connection of a large number of thermocouples, as shown in Figure 3. Compared to a single thermocouple, the thermopile generates much higher thermoelectric voltage.

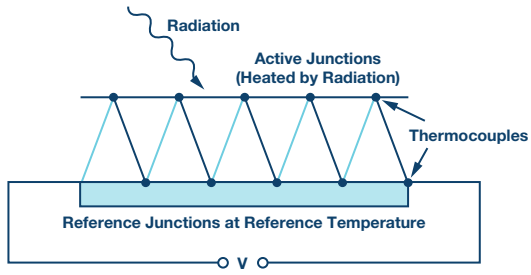

Figure 3. Thermopile constructed of multiple thermocouples.

In the NDIR application, pulsed and filtered IR light is applied to the series connected active junctions; the junctions are therefore heated, which in turn generates a small thermoelectric voltage. The temperature of the reference junction is measured with a thermistor.

Many gases have permanently or nonpermanently separated centers of positive and negative charge. The gases are able to absorb specific frequencies in the infrared spectrum, which can be used for gas analysis. When infrared radiation is incident on the gas, the energy states of atoms vibrating in the molecules change in discrete steps when the wavelength of the infrared matches the molecules' natural frequencies or resonances.

For a majority of IR gas sensing applications, the identities of the target gases are known; therefore, there is little need for gas spectrometry. However, the application must deal with a certain amount of cross sensitivity between different gases if their absorption lines overlap.

Carbon dioxide has a very strong absorption band between 4200 nm and 4320 nm, as shown in Figure 4.

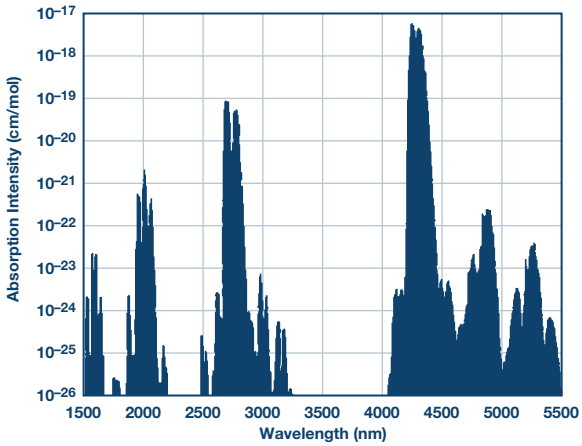

Figure 4. Absorption spectrum of carbon dioxide (CO2).

The available output range of IR sources and the absorption spectrum of water also govern the choice of the sensing wavelengths. Water shows strong absorptions below 3000 nm and also between 4500 nm and

8000 nm. Any attempt to sense gas spectral lines in these regions is subject to strong interference if moisture (high humidity) is present with the target gas. Figure 5 shows the absorption spectrum of carbon dioxide overlaid with the absorption spectrum of water. (All absorption data was taken from the HITRAN database).

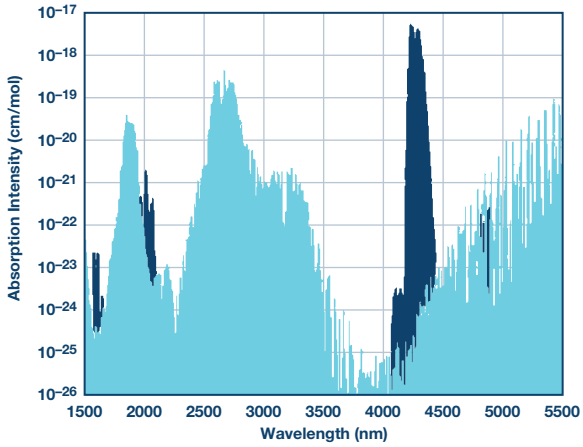

Figure 5. Absorption spectrum of carbon dioxide overlaid with water.

If IR light is applied to a dual thermopile detector fitted with a pair of optical filters so that one filter is centered on 4260 nm and the other on 3910 nm, the concentration of carbon dioxide can be measured from the ratios of the two thermopile voltages. The optical filter that resides within the absorption channel serves as the detection channel and the optical filter that resides outside the absorption spectrum serves as the reference channel. Measuring errors caused by dust or diminishing radiation intensity are removed by the use of the reference channel. It is important to note that there are no gas absorption lines at 3910 nm, making this the ideal location for the reference channel.

Thermopiles used in NDIR sensing have relatively high internal resistance and 50 Hz/60 Hz power-line noise can couple into the signal path. The thermopile can have source impedances of about 100 kΩ causing the thermal noise to dominate the system. For example, the thermopile detector chosen in the Figure 1 system has a voltage noise density of 37 nV/√Hz. By maximizing the amount of signal coming from the detector and using less gain in the circuit, it is possible to ensure the best performance of the gas measuring system.

The best way to maximize the signal from the thermopile detector is to use a sample chamber with high reflective properties, which ensures that the detector absorbs the radiation emitted from the source and not the chamber itself. Using a reflective chamber to reduce the amount of radiation absorbed by the chamber can also reduce the amount of power consumed by the system because a less powerful radiation source can be used.

Beer-Lambert Law for NDIR Gas Absorption

The infrared intensity on the active detector decreases according to the exponential relationship called the Beer-Lambert Law:

$$I = I_0 e^{-klx}$$

where:
I is the intensity in target gas.
I_0 is the intensity in zero gas.
k is the absorption coefficient for the specific gas and filter combination.
l is the equivalent optical path length between the lamp and detectors.
x is the concentration of the gas.

For the active detector output, there is a corresponding output voltage change, $V_0 - V$:

$$FA = \frac{(V_0 - V)}{V_0} = \frac{(I_0 - I)}{I_0} = 1 - \frac{I}{I_0}$$

where:
FA is the fractional absorbance.
V_0 is the output in zero gas.
V is the output in target gas.

Rearranging and combining the previous two equations gives:

$$FA = 1 - e^{-klx}$$

If k and l are held constant, FA can be plotted against x as shown in Figure 6 (where kl = 115, 50, 25, 10, and 4.5). The value of FA increases with c, but eventually saturates at high gas concentrations.

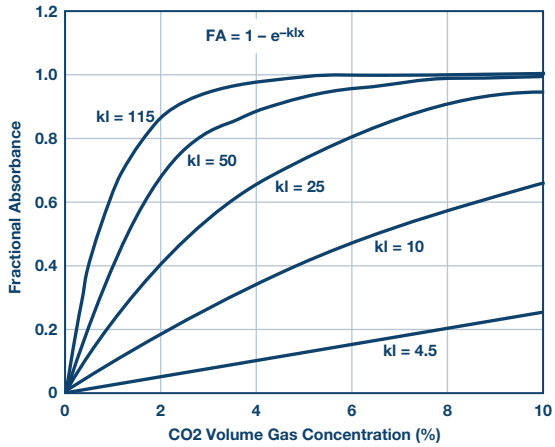

Figure 6. Typical fractional absorbance for kl = 4.5, 10, 25, 50, 115.

This relationship implies that for any fixed setup, the ability to resolve a change in gas level is better at low concentrations than at high concentrations. However, k and l can be adjusted to provide the optimum absorbance for the required range of gas concentration. This means that long optical paths are more suited for low gas concentrations, and short optical paths are more suited for high gas concentrations.

The following describes a two-point calibration procedure necessary to determine the kl constant using the ideal Beer-Lambert equation. If b = kl, then:

$$FA = 1 - \left(\frac{I}{I_0}\right)$$

$$FA = 1 - e^{-bx}$$

The first part of the calibration requires applying low concentration CO2 gas (or pure nitrogen, which is 0% concentration of CO2 gas) to the sensor assembly:

- ACT_{LOW} is the peak-to-peak output of the active detector in low concentration gas.
- REF_{LOW} is the peak-to-peak output of the reference detector in low concentration gas.
- T_{LOW} is the temperature of the low concentration gas.

The second part of the calibration requires applying CO2 gas of a known concentration (x_{CAL}) to the assembly. Usually, the x_{CAL} concentration level is chosen to be the maximum value of the concentration range (for example, 0.5% vol. for the industrial air quality range).

- ACT_{CAL} is the peak-to-peak output of the active detector in the calibration gas of concentration x_{CAL}.
- REF_{CAL} is the peak-to-peak output of the reference detector in the calibration gas of concentration x_{CAL}.

The following two simultaneous equations in two unknowns (I_0 and b) can then be written:

$$I_{LOW} = I_0 e^{-b(x_{LOW})}$$
$$I_{CAL} = I_0 e^{-b(x_{LOW})}$$

Solving the two equations for I_0 and b:

$$I_0 = ZERO = \frac{ACT_{LOW}}{REF_{LOW}} \times \left(\frac{ACT_{LOW}}{REF_{LOW}} \times \frac{REF_{CAL}}{ACT_{CAL}} \right)^{\frac{x_{LOW}}{x_{CAL} - x_{LOW}}}$$

$$b = \left[\frac{\ln\left(\frac{ACT_{LOW}}{REF_{LOW}} \times \frac{REF_{CAL}}{ACT_{CAL}} \right)}{x_{CAL} - x_{LOW}} \right]$$

Then, for a gas of unknown concentration (x), where:

ACT is the peak-to-peak output of the active detector in unknown gas.

REF is the peak-to-peak output of the reference detector in unknown gas.

T is the temperature of the unknown gas in K.

$$FA = 1 - \left(\frac{I}{I_0} \right) = 1 - \frac{ACT}{REF \times ZERO}$$

$$x = \frac{T}{T_{LOW}} \left[\frac{\ln(1 - FA)}{-b} \right]$$

$$x = \frac{T}{T_{LOW}} \left[\frac{\ln\left(\frac{ACT}{REF \times ZERO} \right)}{-b} \right]$$

The T/T_{LOW} factor compensates for the change in concentration with temperature due to the ideal gas law.

Modified Beer-Lambert Law

Practical considerations in the NDIR implementation require modifications to the Beer-Lambert Law, as follows, to obtain accurate readings:

$$FA = SPAN(1 - e^{-bx^c})$$

The SPAN factor is introduced because not all the IR radiation that impinges upon the active thermopile is absorbed by the gas, even at high concentrations. SPAN is less than 1 because of the optical filter bandwidth and the fine structure of the absorption spectra.

Variations in the optical path length and light scattering require the addition of a power term, c, for accurately fitting the equation to the actual absorption data.

The value of the b and SPAN constants also depend upon the range of concentration measured. The typical concentration ranges are as follows:

- Industrial air quality (IAQ): 0 to 0.5% vol. (5000 ppm). Note that CO2 concentration in ambient air is approximately 0.04% vol., or 400 ppm.
- Safety: 0 to 5% vol.
- Combustion: 0 to 20% vol.
- Process control: 0 to 100% vol.

The exact values of b and c for a particular system are usually determined by taking a number of data points for FA vs. the concentration, x, and then using a curve fitting program.

For a given system where the b and c constants have been determined, the value of ZERO and SPAN can be calculated using the two-point calibration method.

The first step in the procedure it to apply a low gas concentration of x_{LOW} and record the following:

- ACT_{LOW}: the peak-to-peak output of the active detector in low concentration gas.
- REF_{LOW}: the peak-to-peak output of the reference detector in low concentration gas.
- T_{LOW}: the temperature of the low concentration gas in K.

The second part of the calibration requires applying CO2 gas of a known concentration (x_{CAL}) to the assembly. Usually, the x_{CAL} concentration level is chosen to be the maximum value of the concentration range (for example, 0.5% vol. for the industrial air quality range). Record the following:

- ACT_{CAL}: the peak-to-peak output of active detector in the calibration gas of concentration x_{CAL}.
- REF_{CAL}: the peak-to-peak output of the reference detector in the calibration gas of concentration x_{CAL}.

The following two simultaneous equations in two unknowns (I_0 and SPAN) can then be written:

$$1 - \frac{I_{LOW}}{I_0} = SPAN\left(1 - e^{-b(x_{LOW}{}^c)}\right)$$
$$1 - \frac{I_{CAL}}{I_0} = SPAN\left(1 - e^{-b(x_{CAL}{}^c)}\right)$$

Solving the two equations for ZERO and SPAN yields:

$$I_0 = ZERO = \frac{ACT_{LOW}\left(e^{-b(x_{CAL}{}^c)} - 1\right)REF_{CAL} + ACT_{CAL}\left(1 - e^{-b(x_{LOW}{}^c)}\right)REF_{LOW}}{\left(e^{-b(x_{CAL}{}^c)} - e^{-b(x_{LOW}{}^c)}\right) \times REF_{CAL} \times REF_{LOW}}$$

$$SPAN = \frac{ACT_{CAL} \times REF_{LOW} - ACT_{LOW} \times REF_{CAL}}{ACT_{LOW}\left(e^{-b(x_{CAL}{}^c)} - 1\right)REF_{CAL} + ACT_{CAL}\left(1 - e^{-b(x_{LOW}{}^c)}\right)REF_{LOW}}$$

Then, for a gas of unknown concentration (x), where:

ACT is the peak-to-peak output of the active detector in unknown gas.

REF is the peak-to-peak output of the reference detector in unknown gas.

T is the temperature of the unknown gas in K.

$$FA = SPAN(1 - e^{-bx^c})$$

$$FA = 1 - \frac{ACT}{REF \times ZERO}$$

$$x = \frac{T}{T_{LOW}}\left[\frac{\ln\left(1 - \frac{FA}{SPAN}\right)}{-b}\right]^{\frac{1}{c}}$$

This equation assumes that $T_{LOW} = T_{CAL}$.

Effects of Ambient Temperature

The thermopile detector senses temperature by absorbing radiation, but it also responds to ambient temperature changes that can give rise to spurious and misleading signals. For this reason, many thermopiles have thermistors integrated into the package.

The radiation absorption is related to the number of target molecules in the chamber, not the absolute percentage of target gas. Therefore the absorption is described by the ideal gas law at standard atmosphere pressure.

It is necessary to record the temperature data in both the calibration state and the measurement state:

$$x_T = \frac{T}{T_{LOW}}x$$

where:
x is the concentration of gas without temperature compensation.
T_{LOW} is the temperature in K at low and high gas concentration.
T is the temperature in K at sampling.
x_T is the gas concentration at temperature T.

In addition to the ideal gas law variation of concentration with temperature, SPAN and FA vary slightly with temperature and may require correction for extremely high accuracy concentration measurements.

This article does not deal with SPAN and FA temperature correction; however, details can be found in Application Note 1, Application Note 2, Application Note 3, Application Note 4, and Application Note 5 from SGX Sensortech, and the AAN-201, AAN-202, AAN-203, AAN-204, and AAN-205 application notes from Alphasense Limited.

Thermopile Driver

The HTS-E21-F3.91/F4.26 thermopile (Heimann Sensor, GmbH) has an 84 kΩ internal resistance in each channel. The equivalent circuit of the driver for one of the thermopile channels is shown in Figure 7. The internal 84 kΩ thermopile resistance and the external 8.2 nF capacitor form an RC low-pass noise filter with a –3 dB cutoff frequency:

$$f_{-3dB} = \frac{1}{2 \times \pi \times 84\ k\Omega \times 8.2\ nF} \approx 231\ Hz$$

Changing C11 and C15 for various thermopiles also changes the noise performance and the response time.

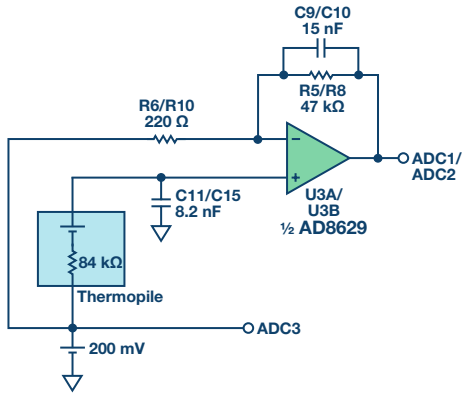

Figure 7. Thermopile driver equivalent circuit, G = 214.6.

The step function setting time of the 84 kΩ/8.2 nF filter to 22 bits is approximately

$$\tau = 84\ k\Omega \times 8.2\ nF \times \ln 2^{22} \approx 10.5\ ms$$

The AD8629 noninverting amplifier is set to a gain of 214.6 and the –3 dB cutoff frequency:

$$f_{-3dB} \approx \frac{1}{2 \times \pi \times 47\ k\Omega \times 15\ nF} \approx 225.75\ Hz$$

The settling time to 22 bits is approximately

$$\tau = 47\ k\Omega \times 15\ nF \times \ln 2^{22} \approx 10.75\ ms$$

The maximum NDIR chop frequency is 5 Hz, and the minimum half cycle pulse width is therefore 100 ms. The settling time to 22 bits is approximately 0.1 × the minimum chop pulse width.

The AD8629 has a 0.1 Hz to 10 Hz input voltage noise of 0.5 µV p-p. Ignoring the sensor voltage noise and the AD8629 current noise, a 1 mV p-p signal output from the thermopile yields a signal-to-noise ratio (SNR) of:

$$SNR = 20\ log\ \frac{1\ mV}{0.5\ \mu V} \approx 66\ dB$$

One of the thermopiles is connected as the pseudo differential input to the ADuCM360 ADC1/ADC3 pair, and the second is connected to the ADC2/ADC3 pair. The ADC3 input is connected to a common-mode voltage of 200 mV, driven by the ADA4528-1 low noise amplifier. The ADA4528-1 input 0.1 Hz to 10 Hz voltage noise is 99 nV p-p. The 200 mV common-mode voltage is required to keep the ADC input pins greater than 0.1 V.

The gain of the AD8629 stage is 214.6, and the gain of the internal PGA of ADuCM360 is automatically set by software from 1 to 128 to ensure the input signal matches the full-scale span of the ADC input, ±1.2 V. The peak-to-peak signal from the thermopile can range from a few hundred µV to several mV. For instance, if the full-scale thermopile signal is 1 mV p-p, a PGA gain of 4 produces an 860 mV p-p into the ADC.

Thermopiles with different sensitivities may require a different gain in the AD8629 stage. Interfacing the CN-0338 Arduino shield board with other Arduino-compatible platforms may require higher gains if the platform uses an ADC without an internal PGA.

The easiest way to change the AD8629 gain is to change R6 and R10, which does not affect the dominant pole frequency set by R5/R8 and C9/C10.

The thermopile output data processing algorithm can be selected in software. The user can select between peak-to-peak and averaging algorithms

Further details regarding the acquisition of the signals, lamp pulse timing, along with the processing algorithms for temperature compensation are included in the CN-0338 source code found in the CN-0338 Design Support Package and in the CN-0338 User Guide.

NTC Thermistor Driver

The characteristics of the integrated NTC temperature sensor in the thermopile are as follows:

$R_{TH} = 100\ k\Omega$
$\beta = 3940$

The Thevenin equivalent circuit for the thermistor driver is shown in Figure 8. The R3 and R4 divider resistors provide a 670.3 mV voltage source in series with the 103.6 kΩ. The driving voltage is 670.3 mV – 200 mV = 470.3 mV.

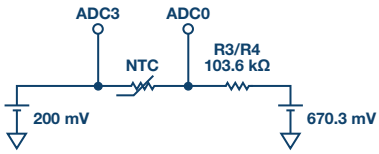

Figure 8. NTC thermistor driver equivalent circuit.

When R_{TH} = 100 kΩ at 25°C, the voltage across the thermistor is 231 mV, and the PGA gain is therefore set at 4 when making the measurement.

The flexible input multiplexer and dual ADCs in the ADuCM360 allow simultaneous sampling of both the thermopile signals and the temperature sensor signal to compensate for drift.

IR Light Source Driver

The filament light source selected is the International Light Technologies MR3-1089, with a polished aluminum reflector that requires a drive voltage of 5.0 V at 150 mA for maximum infrared emission and the best system performance. Heat from the lamp keeps the temperature of the optical reflector higher than ambient, which is helpful in preventing condensation in humid environments.

Filament lamps have a low resistance when cold (turned off), which can result in a current surge at the instant of turn-on. A regulator with a soft start function is useful in addressing this problem.

The ADP7105 low dropout voltage regulator has a programmable enable pin that can be used with a general-purpose input/output pin of the ADuCM360 to enable/disable the lamp voltage. A soft start capacitor, C6, of 10 nF provides a soft start time of 12.2 ms, which is approximately 0.125× the minimum chop step time of 100 ms.

The lamp on-current (~150 mA) is large, therefore careful circuit design and layout is required to prevent the lamp switching pulses from coupling into the small thermopile output voltages.

Take care to ensure the lamp return path does not flow through the sensitive thermopile detector ground return path. The lamp current must not use the same return path as the processor—otherwise it may cause voltage offset errors. It is strongly recommended that a separate voltage regulator be used for the lamp drive and the signal conditioning portion of the system.

The ADP7105 lamp driver is supplied directly from the external power supply connected to the EVAL-ADICUP360 board.

Software Considerations

Synchronized Chopping and Sampling

To measure the gas concentration, the peak-to-peak signal value in both the reference and active channel must be sampled. The ADuCM360 includes two 24-bit, Σ-Δ ADCs, and the ADCs operate in continuous sampling mode. Programmable gain amplifiers with gain options of 1, 2, 4, 8, 16, 32, 64, and 128 drive the ADCs.

The default chopping frequency is set to 0.25 Hz, and the default sampling rate is set to 10 Hz. However, the chopping frequency can be set in the software from 0.1 Hz to 5 Hz, and the ADC sampling rate from 3.5 Hz to 483 Hz. The software ensures that the sampling rate is at least 30 times the chopping frequency.

For the default chopping frequency of 0.25 Hz, the thermopile data is taken at a 10 Hz rate during the last 1.5 sec of the 2 sec half cycle to ensure that the signal has settled. The data during the first 500 ms is ignored (blanking time). The blanking time can also be set in the software for both edges. Note that the NTC thermistor data is taken during the blanking time.

Calibration Procedure: Ideal Beer-Lambert Equation

Because of differences in the characteristics of lamps and thermopiles, the circuit must be calibrated initially and also after changing either the thermopile or the lamp.

It is recommended that the entire assembly be placed in a closed chamber where gas of a known CO2 concentration can be injected until all existing gas in the chamber is flushed out. After stabilizing for a few minutes, the measurements can then be made.

The calibration method and algorithms are shown in the following steps for the ideal Beer-Lambert equation:

1. Input the following command: **sbllcalibrate** (standard Beer-Lambert calibration).
2. Inject low concentration, x_{LOW}, or zero gas (nitrogen), and stabilize the chamber.
3. Input the CO2 concentration into the terminal.
4. The system measures ACT_{LOW}, the peak-to-peak output of the active detector in low concentration gas.
5. The system measures REF_{LOW}, the peak-to-peak output of the reference detector in low concentration gas.
6. The system measures temperature of low gas, T_{LOW}.
7. Inject high concentration CO2, of concentration x_{CAL}, into the chamber.
8. Input the CO2 concentration into the terminal.
9. The system measures ACT_{CAL}, REF_{CAL}, and the calibration temperature, T_{CAL}.
10. The system calculates ZERO and b:

$$ZERO = \frac{ACT_{LOW}}{REF_{LOW}} \times \left(\frac{ACT_{LOW}}{REF_{LOW}} \times \frac{REF_{CAL}}{ACT_{CAL}} \right)^{\frac{x_{LOW}}{x_{CAL} - x_{LOW}}}$$

$$b = \left[\frac{ln\left(\frac{ACT_{LOW}}{REF_{LOW}} \times \frac{REF_{CAL}}{ACT_{CAL}} \right)}{x_{CAL} - x_{LOW}} \right]$$

To measure an unknown concentration of CO2 gas using the ideal Beer-Lambert equation, do the following:

1. Apply the unknown concentration of gas to the chamber and stabilize.
2. Measure ACT, the peak-to-peak output of the active detector.
3. Measure REF, the peak-to-peak output of the reference detector.
4. Measure the temperature, T, in Kelvin.
5. Use the ZERO value from the calibration.
6. Use the b value from the calibration.
7. Calculate the fractional absorbance:

$$FA = 1 - \frac{ACT}{REF \times ZERO}$$

Calculate the concentration and apply the ideal gas law temperature compensation:

$$x = \frac{T}{T_{LOW}} \left[\frac{\ln\left(\frac{ACT}{REF \times ZERO} \right)}{-b} \right]$$

This procedure assumes that $T_{LOW} = T_{CAL}$.

Note that the CN-0338 software will automatically perform Steps 2 through 7.

Calibration Procedure: Modified Beer-Lambert Equation

If the constants b and c are known from measurements, use the following procedure.

1. Input the following command: **mbllcalibrate** (modified Beer-Lambert calibration).
2. Input the b and c constants.
3. Inject low concentration CO2 gas, x_{LOW} (nitrogen), and stabilize the chamber.
4. Input the CO2 concentration into the terminal.
5. The system measures ACT_{LOW}, the peak-to-peak output of the active detector in low gas.
6. The system measures REF_{LOW}, the peak-to-peak output of the reference detector in low gas.
7. The system measures the temperature, T_{LOW}.
8. Inject high concentration CO2, of concentration x_{CAL}, into the chamber.
9. Input the CO2 concentration into the terminal.
10. The system measures ACT_{CAL}, REF_{CAL}, and the calibration temperature, T_{CAL}.
11. The system calculates ZERO and SPAN:

$$ZERO = \frac{ACT_{LOW}\left(e^{-b(x_{CAL}c)} - 1\right)REF_{CAL} + ACT_{CAL}\left(1 - e^{-b(x_{LOW}c)}\right)REF_{LOW}}{\left(e^{-b(x_{CAL}c)} - e^{-b(x_{LOW}c)}\right) \times REF_{CAL} \times REF_{LOW}}$$

$$SPAN = \frac{ACT_{CAL} \times REF_{LOW} - ACT_{LOW} \times REF_{CAL}}{ACT_{LOW}\left(e^{-b(x_{CAL}c)} - 1\right)REF_{CAL} + ACT_{CAL}\left(1 - e^{-b(x_{LOW}c)}\right)REF_{LOW}}$$

To measure an unknown concentration of CO2 gas using the modified Beer-Lambert equation, do the following:

1. Apply the unknown concentration of gas to the chamber and stabilize.
2. Measure ACT, the peak-to-peak output of the active detector.
3. Measure REF, the peak-to-peak output of the reference detector.
4. Measure the temperature, T, in kelvin.
5. Use the ZERO and SPAN values from calibration.
6. Use the values of b and c that were previously determined.
7. Calculate fractional absorbance:

$$FA = 1 - \frac{ACT}{REF \times ZERO}$$

Calculate the concentration and apply the ideal gas law temperature compensation:

$$x = \frac{T}{T_{LOW}} \left[\frac{\ln\left(1 - \frac{FA}{SPAN}\right)}{-b} \right]^{\frac{1}{c}}$$

This procedure assumes that $T_{LOW} = T_{CAL}$.

NTC Thermistor Algorithm and Calculations

The NTC thermistor equivalent circuit is shown in Figure 9.

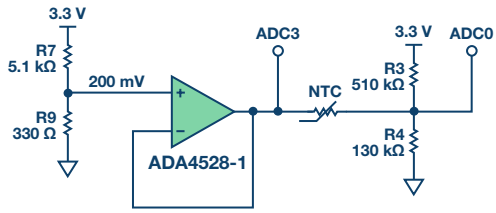

Figure 9. NTC thermistor circuit.

The voltage across the thermistor is:

$$V_{NTC} = \frac{(R4 \times R7 - R3 \times R9) \times R_{NTC} \times VCC}{(R7 + R9)\,[R4 \times R_{NTC} + R3\,(R4 + R_{NTC})]}$$

where:
VCC is 3.3 V.
R_{NTC} is thermistor resistance.

The NTC thermistor resistance can be expressed as:

$$\frac{1}{T} = \frac{1}{T_0} + \frac{1}{\beta} \times \ln \frac{R_{NTC}}{R_{TH}}$$

where:
R_{TH} is the thermistor resistance at temperature T_0.
β is a parameter given in the NTC thermistor data sheet.
R_{NTC} is the the thermistor resistance at temperature T.

Combining the two equations yields:

$$T = \frac{T_0 \times \beta}{\beta + T_0 \times \ln\left[\frac{R3 \times R4 \times (R7 + R9) \times V_{NTC}}{(R4 \times R7 - R3 \times R9) \times R_{TH} \times VCC - (R3 + R4) \times (R7 + R9) \times R_{TH} \times V_{NTC}}\right]}$$

During each lamp chopping time interval, the ADC is switched to NTC sampling, as shown in Figure 10.

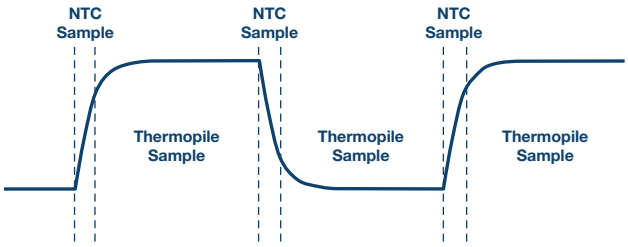

Figure 10. Timing of NTC and thermopile sampling and lamp chopping.

User Interactive Interface

The EVAL-ADICUP360 platform board connects to a PC via the USB port. The board appears as a virtual COM device. Any type of serial port terminal can be used to interact with the EVAL-ADICUP360 board for development and debugging. Further details regarding the operation of the software are included in the CN-0338 Circuit Note.

Figure 11 shows the fractional absorbance (FA) as a function of CO2 concentration for a typical EVAL-CN0338-ARDZ board.

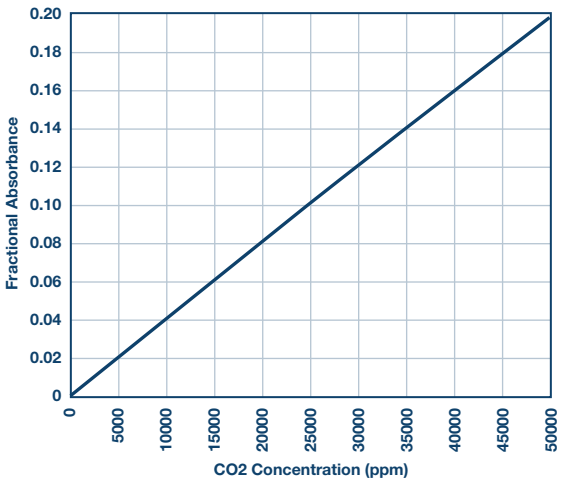

Figure 11. Fractional absorbance vs. CO2 concentration for the typical EVAL-CN0338-ARDZ board.

A complete design support package for the EVAL-CN0338-ARDZ board including layouts, bill of materials, schematics, and source code can be found at www.analog.com/CN0338-DesignSupport.

A functional diagram of the test setup is shown in Figure 12 and a photograph of the EVAL-CN0338-ARDZ Arduino shield board and the EVAL-ADICUP360 Arduino-compatible platform board is shown in Figure 13.

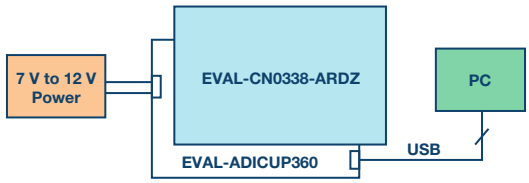

Figure 12. Test setup functional block diagram.

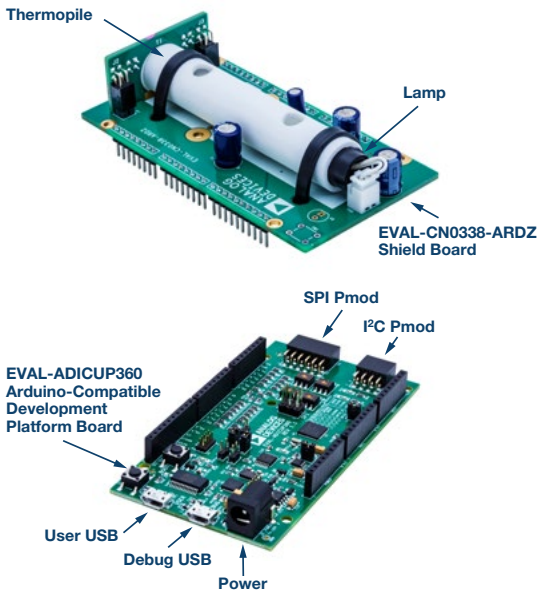

Figure 13. EVAL-CN0338-ARDZ board and EVAL-ADICUP360 board photos.

Summary

The analog electronics needed to implement the NDIR measurement require precision low noise amplification and high resolution analog-to-digital conversion. The circuit described in this article is a highly integrated solution that utilizes the ADuCM360 precision analog microcontroller to perform the precision PGA function, the precision Σ-Δ ADC conversion, and the digital control and processing.

The Arduino shield-compatibility allows for rapid prototyping of NDIR designs with the ability to tailor the software to the specific application requirements.

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MT-037 Tutorial, *Op Amp Input Offset Voltage*. Analog Devices, Inc., 2009.

MT-101 Tutorial, *Decoupling Techniques*. Analog Devices, Inc., 2009.

Data Sheets and Evaluation Boards

ADP7105 data sheet.

ADuCM360 data sheet.

EVAL-CN0338-ARDZ Arduino Shield Board.

EVAL-ADICUP360 Arduino-Compatible Platform Board.

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Walt Kester

Rarely Asked Questions—Issue 134 Because Mr. Ohm Said So ...

By **Umesh Jayahoman**

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Question:

In my system the SPI interface for the ADC is returning 0xFF for every read. What could be wrong?

Answer:

The new generation of GSPS (gigasample per second) ADCs (analog-to-digital converters) offer industry-leading performance and reliability in the systems implementation. However, if the SPI interface reads back 0xFF for every read, well, that is certainly a nonstarter. This could very well mean something inside the ADC is not up to snuff. Let us find out what it could be.

The latest generation of GSPS ADCs, like the AD9680 for example, is designed on a deep submicron 65 nm CMOS process. In order to hit the required ac performance specifications, the design had to accommodate multiple voltage domains (1.25 V, 2.5 V, 3.3 V). Usually, any silicon device with these multiple voltage domains will need some sort of power supply sequencing. However, the designers at Analog Devices built in some supervisory circuits to make the AD9680 easier for customers to implement in their systems by eliminating the need for any power supply sequencing.

The AD9680 has an internal power-on reset (POR) nanny circuit that manages all the power rails. Until this POR circuit is satisfied with the power rail levels, the device will be in reset mode. In reset mode, if SPIVDD is at 1.8 V, 2.5 V, or 3.3 V, the ADC will send 0xFF through the SPI port for every read. Looks like we are getting somewhere. This is where your best friend is the old reliable digital multimeter (DMM).

Using the DMM, the first place to check would be the supply voltages at the various pins of the AD9680. Chances are one of them is out of range as far as the POR circuit is concerned. Now here is where things could get tricky. Take a look at Figure 1, which shows the block diagram schematic of the AD9680-1250 being clocked at 1.25 GHz. Everything here looks normal to someone taking a first look at the schematic. The decoupling capacitors are not shown here, as neither are other supply domains. The focus is on the 1.25 V domain as this is the smallest supply voltage.

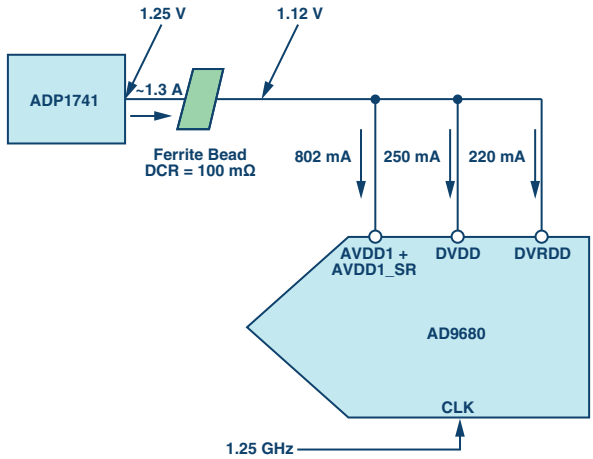

Figure 1. Powering the 1.25 V domains on the AD9680 using the ADP1741 LDO.

The ADP1741 should have enough room to supply all the domains connected to 1.25 V. However, the culprit here is not the LDO, nor the ADC, but the unsuspecting ferrite bead. Usually, ferrite beads are used in power networks to filter the power going to a certain device. One parameter of the ferrite bead that is often overlooked is the DCR (dc resistance). So why do we have to worry about the DCR? Because a certain gentleman by the name of Georg Simon Ohm said so.

Ohm's law states that the current through a conductor between two points is directly proportional to the potential difference across the two points. So, the ADP1741 LDO output might measure 1.25 V, which sounds OK. However, if you measure the voltage at the ADC pins, or on the other side of the ferrite bead, the DMM reads 1.12 V (assuming nominal currents). This is the real reason why the ADC SPI was reading 0xFF. The nanny obviously was not happy with the voltages inside the AD9680.

So what is the remedy? There are some options:

1. Choose to not use the ferrite bead. This may or may not make the design more susceptible to noise.

2. Adjust the LDO output voltage up to account for the IR drop across the ferrite bead. However, this could potentially expose the AD9680 to excessive voltages when an adequate amount of current isn't being pulled.

3. Choose another ferrite bead that has the same impedance and current carrying capacity, but lower DCR (less than 50 mΩ).

4. Split the voltage outputs to the respective domains (AVDD1, AVDD1_SR, DVDD, DRVDD) and use a ferrite bead with lower DCR to ensure proper operating voltage.

Figure 2 shows Options 2 and 4, discussed above. Option 4 offers the best compromise. However, this does add to the bill of material (BOM) cost, which must be taken into consideration. Option 4 also provides more noise immunity by providing some filtering between the AVDD, DVDD, and DRVDD domains.

So the next time you plug in an ADC, clock it, and find that it doesn't work and the SPI is returning 0xFF for every read cycle, you might have Mr. Ohm to thank. In this case, the venerable DMM becomes your tool of choice, not an oscilloscope or your friendly applications engineer. A ferrite bead certainly can offer good noise immunity to your system. However, if not chosen correctly, and if Ohm's law is not heeded, this small component can cause some serious issues in realizing an ADC's true performance in the system.

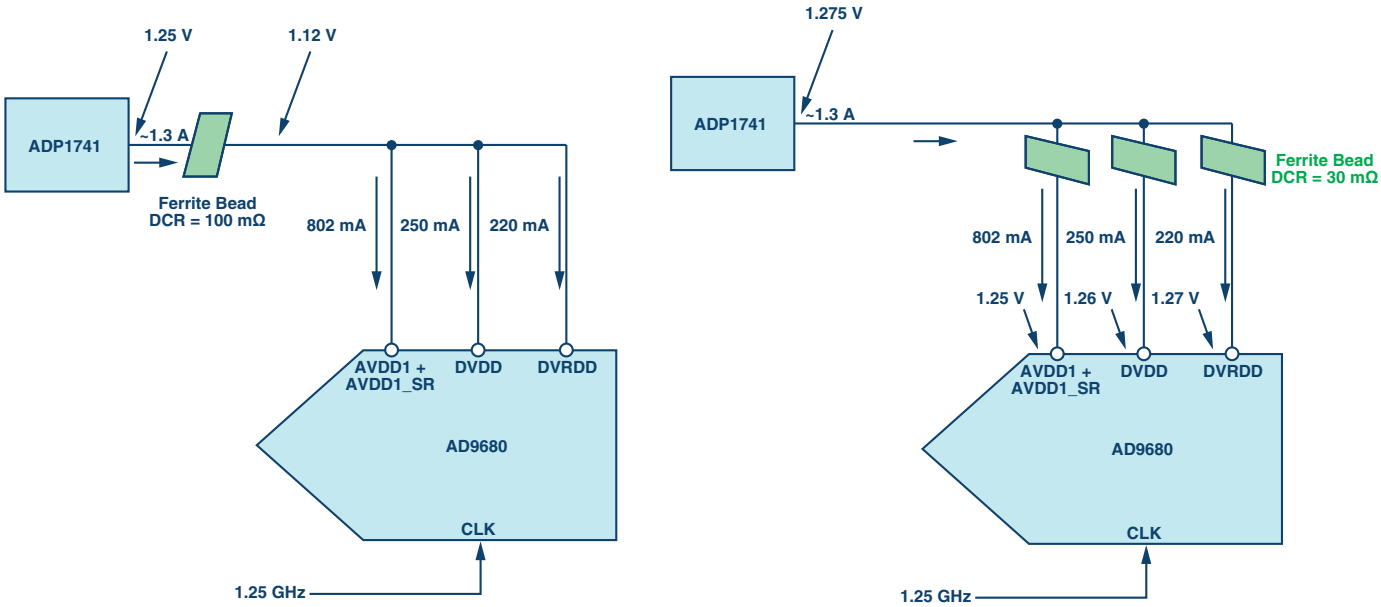

Figure 2: Different options of choosing and using a ferrite bead to power the AD9680.

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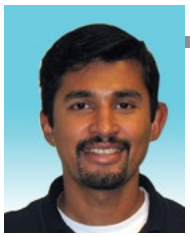

Umesh Jayahoman

Also by this Author:

Rarely Asked Questions—

Issue 129, May 2016
Who Ate My dBs?

What's Up with Digital Downconverters—Part 2

By **Jonathan Harris**

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In the first part of this article, What's Up with Digital Downconverters—Part 1, we looked at the industry push for sampling higher frequencies in higher frequency RF bands and how digital downconverters (DDCs) can enable this type of radio architecture. Several technical aspects were discussed relating to the DDC that resides in the AD9680 family of products. One such aspect was that higher input sampling bandwidths allow for radio architectures that can directly sample at higher RF frequencies and convert the input signals directly to baseband. The DDC enables an RF sampling ADC to digitize such signals without the expense of a large amount of data throughput. The tuning and decimation filtering that resides in the DDC can be utilized to tune the input band and filter undesired frequencies. In this installment we will take a closer look at the decimation filtering and apply it to the example that was discussed in Part 1. In addition we will take a look at Virtual Eval, which incorporates the ADIsimADC engine into a new and revamped software simulation tool. Virtual Eval will be used to demonstrate how closely the simulated result matches the measured data from the example.

In Part 1, we looked at an example where we used the NCO and decimation filtering in the DDC to see the effects of frequency folding and translating in the DDC. Now we will take a closer look at the decimation filtering and how ADC aliasing influences the effective response of the decimation filtering. Once again we will look to the AD9680 as an example. The decimation filter responses are normalized so that the response can be seen and understood and can be applied to each speed grade. The decimation filter responses simply scale with the sample rate. In the filter response plots included here the specific insertion loss vs. frequency is not given exactly but is figuratively shown to illustrate the approximate response of the filter. These examples are intended to give a high level understanding of decimation filter responses in order to understand approximately where the filter pass band and stop band reside.

Recall that the AD9680 has four DDCs that consist of an NCO, up to four cascaded half-band (HB) filters (which will also be referred to as decimation filters), an optional 6 dB gain block, and an optional complex to real conversion block as illustrated in Figure 1. As we discussed in Part 1, the signal first passes through the NCO, which shifts the input tones in frequency, then passes through the decimation, optionally through the gain block, and optionally through the complex to real conversion.

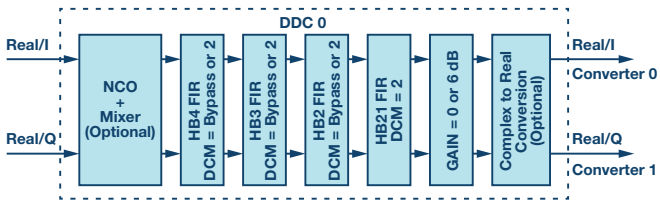


Figure 1. DDC signal processing blocks in the AD9680.

We will begin by looking at the DDC decimation filters when the complex to real conversion block is enabled in the AD9680. This means the DDC will be configured to accept a real input and have a real output. In the AD9680, the complex to real conversion automatically shifts the input frequencies up in frequency by an amount equal to $f_S/4$. Figure 2 shows the low-pass response of the HB1 filter. This is the response of HB1 showing the real and complex domain response. In order to understand the real operation of the filter it is important to first see the basic filter response in the real and complex domains so that the low-pass response can be seen. The HB1 filter has a pass band of 38.5% of the real Nyquist zone. It also has a stop band that is 38.5% of the real Nyquist zone with the transition band making up the remaining 23%. Likewise in the complex domain, the pass band and stop band each make up 38.5% (77% total) of the complex Nyquist zone with the transition band making up the remaining 23%. As Figure 2 illustrates, the filter is a mirror image between the real and complex domains.

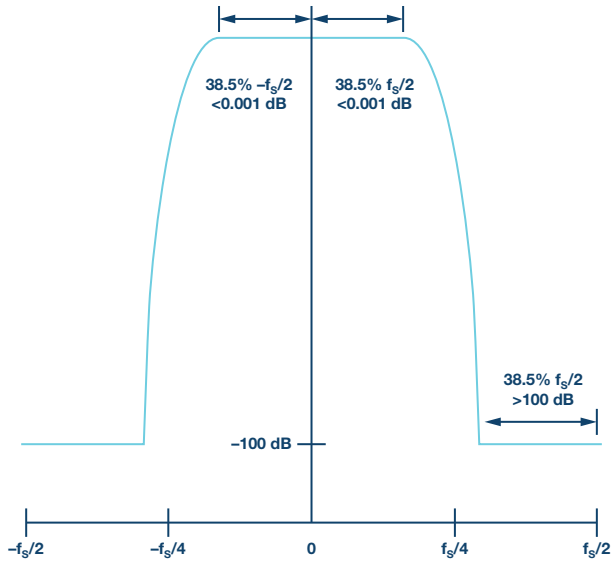


Figure 2. HB1 filter response—real and complex domain response.

Now we can observe what happens when we place the DDC into real mode by enabling the complex to real conversion block. Enabling the complex to real conversion results in a shift of $f_S/4$ in the frequency domain. This is illustrated in Figure 3, which shows the frequency shift and the resulting filter response. Notice the solid lines and the dotted lines of the filter response. The solid line and shaded area indicates this is the new filter response after the $f_S/4$ frequency shift (the resulting filter response cannot cross the Nyquist boundary). The dotted lines are given for illustration to show the filter response that would exist if not for running into the Nyquist boundary.

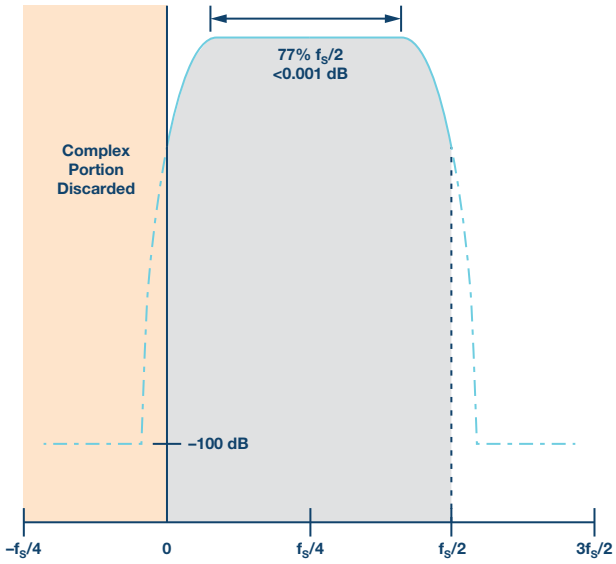


Figure 3. HB1 filter response—real DDC mode (complex to real conversion enabled).

Notice that the HB1 filter bandwidth remains unchanged between Figures 2 and 3. The difference between the two is the $f_S/4$ frequency shift and the resultant center frequency within the first Nyquist zone. Notice however that in Figure 2 we have 38.5% of Nyquist for the real portion of the signal and 38.5% of Nyquist for the complex portion of the signal. In Figure 3 with the complex to real conversion block enabled there is 77% of Nyquist for the real signal and the complex domain has been discarded. The filter response remains unchanged apart from the $f_S/4$ frequency shift. Also, notice as a product of this conversion the decimation rate is now equal to one. The effective sample rate is still f_S but instead of the entire Nyquist zone there is only 77% of available bandwidth in the Nyquist zone. This means that with the HB1 filter and the complex to real conversion block enabled the decimation rate equals one (see the AD9680 data sheet for more information).

Next we will look at the filter responses of different decimation rates (that is, enabling multiple half-band filters) and how aliasing of the ADC input frequencies impacts the effective decimation filter responses. The actual frequency response of HB1 is given by the solid blue line in Figure 4. The dashed line represents the effective aliased response of HB1 due to the aliasing effects of the ADC. Due to the fact that frequencies input into 2nd, 3rd, 4th, etc. Nyquist zones alias into the 1st Nyquist zone of the ADC, the HB1 filter response is effectively aliased into these Nyquist zones. For example, a signal residing at $3f_S/4$ will alias into the first Nyquist zone at $f_S/4$. It is important to understand that the HB1 filter response resides only in the first Nyquist zone and that it is the aliasing of the ADC that results in the effective response of the HB1 filter appearing to be aliased into the other Nyquist zones.

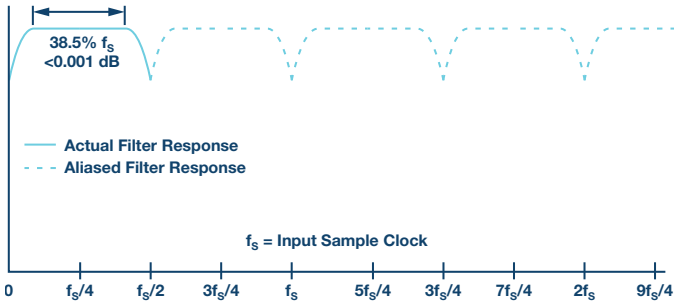


Figure 4. HB1 effective filter response due to ADC aliasing.

Now let's look at the case where we enable HB1 + HB2. This results in a decimation ratio of two. Once again, the actual frequency response of the HB1 + HB2 filters is given by the solid blue line. The center frequency of the filter pass band is still $f_S/4$. Enabling both HB1 + HB2 filters results in an available bandwidth of 38.5% of the Nyquist zone. Once again, notice the aliasing effects of the ADC and its impact on the combination of HB1 + HB2 filters. A signal that appears at $7f_S/8$ will alias into the first Nyquist zone at $f_S/8$. Likewise a signal at $5f_S/8$ will alias into the first Nyquist zone at $3f_S/8$. These examples with the complex to real conversion block enabled can easily be extended from HB1 + HB2 to include one or both of the HB3 and HB4 filters. Note that the HB1 filter is nonbypassable when the DDC is enabled while HB2, HB3, and HB4 filters can optionally be enabled.

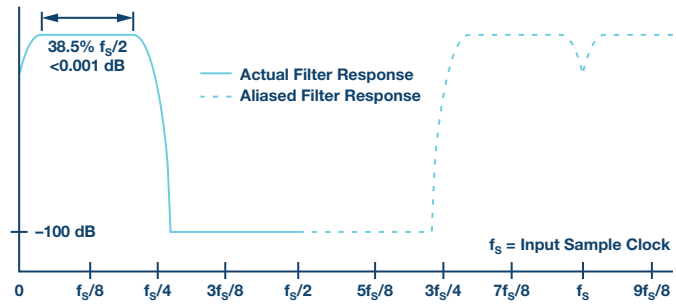


Figure 5. HB1 + HB2 effective filter response due to ADC aliasing (decimation rate = 2).

Now that the real mode operation with the decimation filters enabled has been discussed, the complex mode of operation with the DDC can now be examined. The AD9680 will continue to be used as an example. Similar to the real mode operation of the DDC, the normalized decimation filter responses will be presented. Once again, the example filter response plots included here do not show the specific insertion loss vs. frequency, but instead they figuratively show the approximate response of the filter. This is done to give a high level understanding of how the filter responses are affected by the ADC aliasing.

With the DDC in complex mode it is configured to have a complex output that consists of real and complex frequency domains commonly referred to as I and Q. Recall from Figure 2 that the HB1 filter has a low-pass response with a pass band of 38.5% of the real Nyquist zone. It also has a stop band that is 38.5% of the real Nyquist zone with transition band making up the remaining 23%. Likewise, in the complex domain, the pass band and stop band each make up 38.5% (77% total) of the complex Nyquist zone with the transition band making up the remaining 23%.

When operating the DDC in complex output mode with the HB1 filter enabled the decimation ratio is equal to two and the output sample rate is half of the input sample clock. Extending the plot from Figure 2 to show the effects of the aliasing of the ADC we have what is shown in Figure 6. The solid blue line represents the actual filter response while the dotted blue line represents the effective aliased response of the filter due to the aliasing effects of the ADC. An input signal at $7f_S/8$ will alias into the first Nyquist zone at $f_S/8$, placing it in the pass band of the HB1 filter. The complex image of this same signal resides at $-7f_S/8$ and will alias in the complex domain to $-f_S/8$, placing it in the pass band of the HB1 filter in the complex domain.

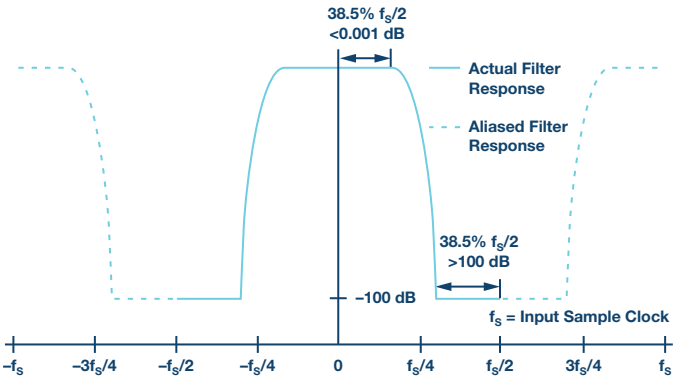


Figure 6. HB1 effective filter response due to ADC aliasing (decimation rate = 2)—complex.

Moving on, we will look at the case where HB1 + HB2 are enabled, which is shown in Figure 7. This results in a decimation ratio of four for each I and Q output. Once again, the actual frequency response of the HB1 + HB2 filters is given by the solid blue line. Enabling both HB1 + HB2 filters results in an available bandwidth of 38.5% of the decimated Nyquist zone in each of the real and complex domains (38.5% of $f_S/4$, where f_S is the input sample clock). Notice the aliasing effects of the ADC and its impact on the combination of HB1 + HB2 filters. A signal that appears at $15f_S/16$ will alias into the first Nyquist zone at $f_S/16$. This signal has a complex image at $-15f_S/16$ in the complex domain and will alias into the first Nyquist zone in the complex domain at $-f_S/16$. Once again these examples can be extended to the cases where HB3 and HB4 are enabled. These are not shown in this article but can be extrapolated easily based on the response of HB1 + HB2 shown in Figure 7.

Some questions that come to mind when looking at all of these decimation filter responses may be: "Why do we decimate?" and "What advantage does it offer?" Different applications have different requirements that can benefit from decimation of the ADC output data. One motivation is to gain signal-to-noise ratio (SNR) over a narrow band of frequency that resides in an RF frequency band. Another reason is less bandwidth to process, which results in lower output lane rates across the JESD204B interface. This can allow the use of a lower cost FPGA. By using all four decimation filters, the DDC can realize processing gain and improve the SNR by up to 10 dB. In Table 1 we can see the available bandwidth, decimation ratio, output sample rate, and the ideal SNR improvement offered by the different decimation filter selections when operating the DDC in real and complex modes.

This discussion of the DDC operation has given a good insight into both the real and complex modes of operation of the decimation filters in the AD9680. There are several advantages that are offered by utilizing the decimation filtering. The DDC can operate in real or complex mode and allow the user to use different receiver topologies depending on the needs of the particular application. This can now be put together with what was discussed in Part 1 and help to look at a real example with the AD9680. This example will put measured data together with simulated data from Virtual Eval so that the results can be compared.

Table 1. DDC Filter Characteristics for AD9680

Decimation Filter Selection	Complex Output		Real Output		Alias Protected Bandwidth	Ideal SNR Improvement
	Decimation Ratio	Output Sample Rate	Decimation Ratio	Output Sample Rate		
HB1	2	$0.5 \times f_S$	1	f_S	$0.385 \times f_S$	1
HB1 + HB2	4	$0.25 \times f_S$	2	$0.5 \times f_S$	$0.1925 \times f_S$	4
HB1 + HB2 + HB3	8	$0.125 \times f_S$	4	$0.25 \times f_S$	$0.09625 \times f_S$	7
HB1 + HB2 + HB3 + HB4	16	$0.0625 \times f_S$	8	$0.125 \times f_S$	$0.048125 \times f_S$	10

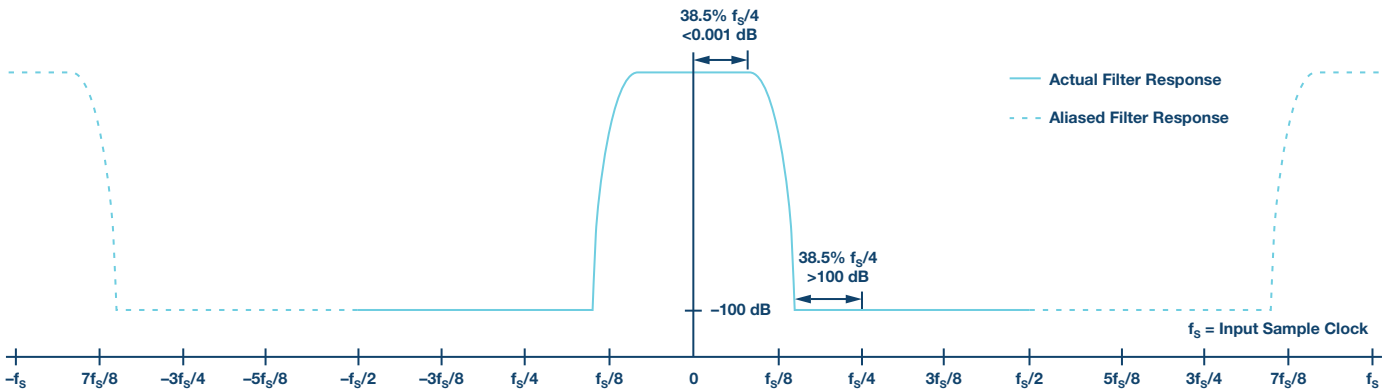


Figure 7. HB1 + HB2 effective filter response due to ADC aliasing (decimation rate = 4)—complex.

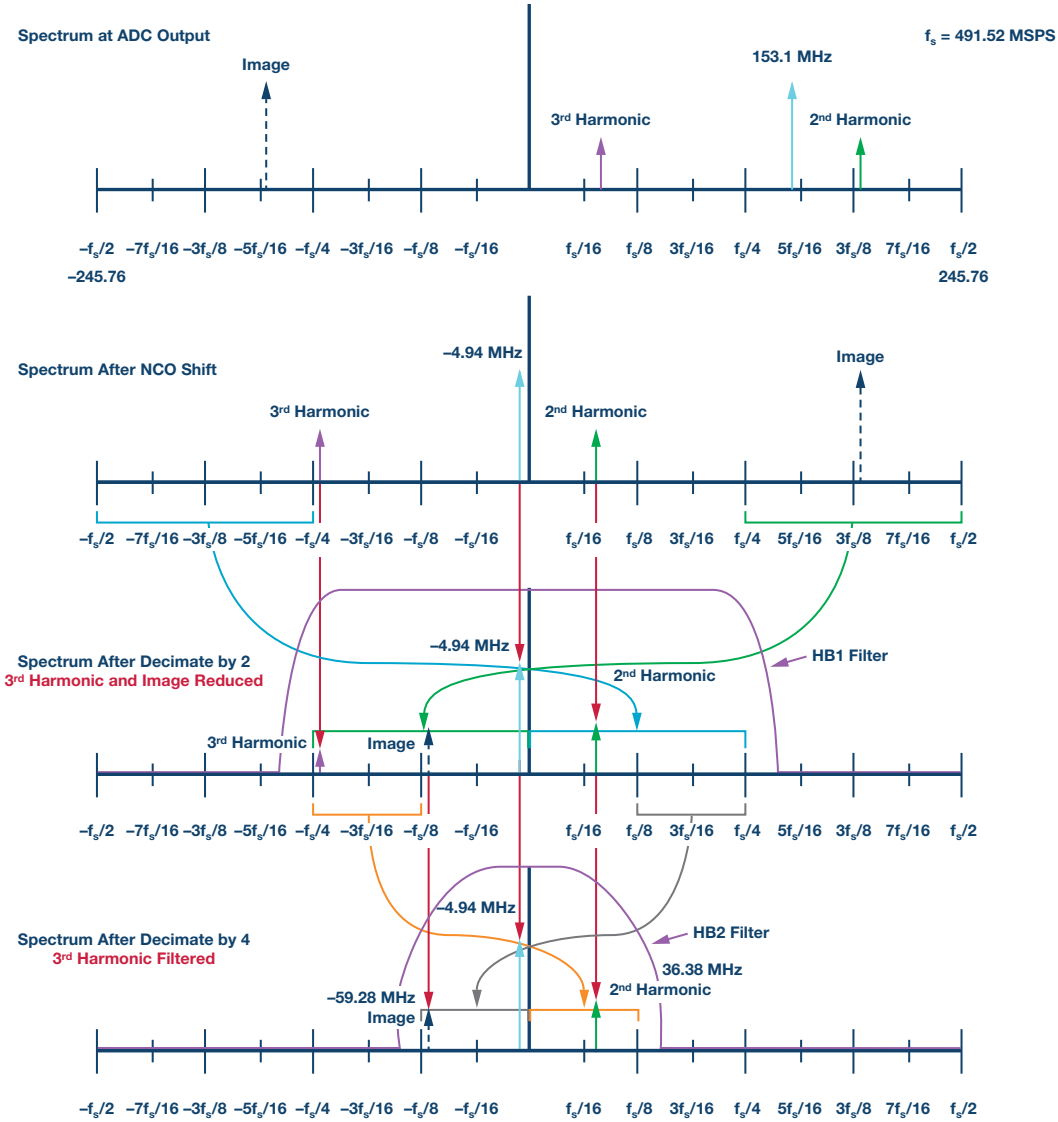


Figure 8. Signals as they pass through the DDC signal processing block—decimation filtering shown.

In this example the same conditions as were used in Part 1 will be used. The input sample rate is 491.52 MSPS and the input frequency is 150.1 MHz. The NCO frequency is 155 MHz and the decimation rate is set to four (due to the NCO resolution, the actual NCO frequency is 154.94 MHz). This results in an output sample rate of 122.88 MSPS. Since the DDC is performing complex mixing the complex frequency domain is included in the analysis. Note that the decimation filter responses have been added and are shown in dark purple in Figure 8.

Spectrum After the NCO Shift:

1. The fundamental frequency shifts from +150.1 MHz down to –4.94 MHz.
2. The image of the fundamental shifts from –150.1 MHz and wraps around to +186.48 MHz.
3. The 2nd harmonic shifts from 191.32 MHz down to 36.38 MHz.
4. The 3rd harmonic shifts from +41.22 MHz down to –113.72 MHz.

Spectrum After Decimate by 2:

1. The fundamental frequency stays at –4.94 MHz.
2. The image of the fundamental translates down to –59.28 MHz and is attenuated by the HB1 decimation filter.
3. The 2nd harmonic stays at 36.38 MHz.
4. The 3rd harmonic is attenuated by the HB1 decimation filter.

Spectrum After Decimate by 4:

1. The fundamental stays at –4.94 MHz.
2. The image of the fundamental stays at –59.28 MHz and is attenuated by the HB2 decimation filter.
3. The 2nd harmonic stays at –36.38 MHz and is attenuated by the HB2 decimation filter.
4. The 3rd harmonic is filtered and virtually eliminated by the HB2 decimation filter.

The actual measurement on the AD9680-500 is shown in Figure 9. The fundamental frequency is at –4.94 MHz. The image of the fundamental resides at –59.28 MHz with an amplitude of –67.112 dBFS, which means that the image has been attenuated by approximately 66 dB. The 2nd harmonic resides at 36.38 MHz and has been attenuated by approximately 10 dB to 15 dB. The 3rd harmonic has been filtered sufficiently so that it does not rise above the noise floor in the measurement.

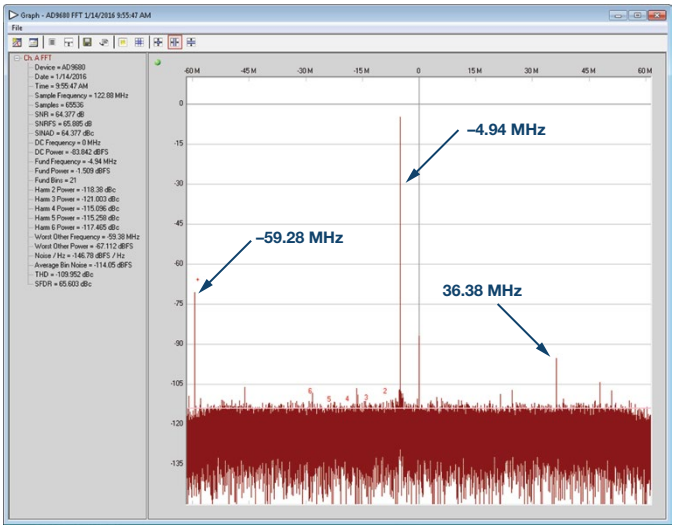


Figure 9. FFT complex output of signal after DDC with NCO = 155 MHz and decimate by 4.

Now Virtual Eval can be used to see how the simulated results compare to the measured results. To begin, open the tool from the website and select an ADC to simulate (see Figure 10). The Virtual Eval tool is on the Analog Devices website at Virtual Eval. The AD9680 model that resides in Virtual Eval incorporates a new feature being developed that allows the user to simulate different speed grades of ADCs. This feature is key to the example since the example utilizes the AD9680-500. Once Virtual Eval loads, the first prompt is to select a product category and a product. Notice that Virtual Eval not only covers high speed ADCs but also has product categories for precision ADCs, high speed DACs, and integrated/special purpose converters.

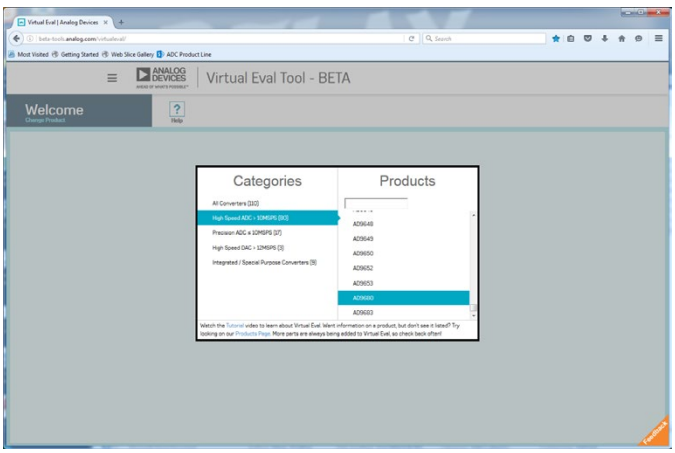


Figure 10. Product category and product selection in Virtual Eval.

Select the AD9680 from the product selection. This will open up the main page for the simulation of the AD9680. The Virtual Eval model for the AD9680 also includes a block diagram that gives details on the internal configuration of the ADC analog and digital features. This block diagram is the same as the one given in the data sheet for the AD9680. From this page select the desired speed grade from the drop-down menu on the left side of the page. For the example here, select the **500 MHz** speed grade as shown in Figure 11.

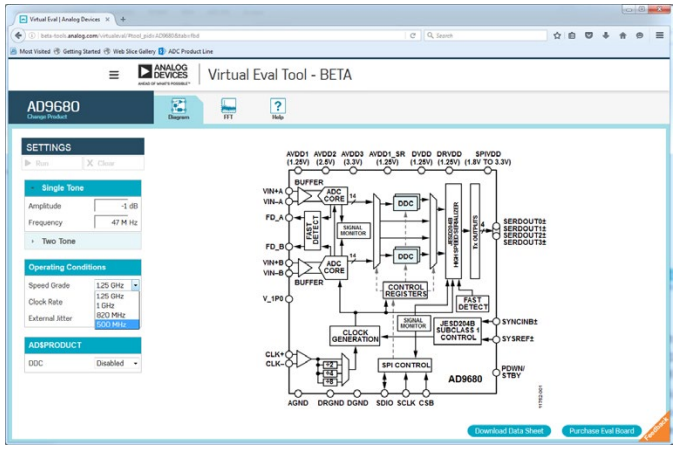


Figure 11. AD9680 speed grade selection and block diagram in Virtual Eval.

Next, the input conditions must be set in order to perform the FFT simulation (see Figure 12). Recall the test conditions for the example include a clock rate of 491.52 MHz and an input frequency of 150 MHz. The DDC is enabled with the NCO frequency set to **155 MHz**, the ADC input is set to **Real**, the complex to real conversion (C2R) is **Disabled**, the DDC decimation rate is set to **Four**, and the 6 dB gain in the DDC is **Enabled**. This means the DDC is set up for a real input signal and a complex output signal with a decimation ratio of four. The 6 dB gain in the DDC is enabled in order to compensate for the 6 dB loss due to the mixing process in the DDC. Virtual Eval will show only noise or distortion results at a time, so two plots are included where one shows the noise results (Figure 12) and the other shows the distortion results (Figure 13).

Figure 12. AD9680 FFT simulation in Virtual Eval—noise results.

Figure 13. AD9680 FFT simulation in Virtual Eval—distortion results.

There are many performance parameters that are denoted in Virtual Eval. The tool gives the harmonic locations as well as the location of the fundamental image, which can be very handy when frequency planning. This can help make frequency planning a bit easier by allowing the user to see if the fundamental image or any harmonic tones show up in the desired output spectrum. The simulation in Virtual Eval gives an SNR value of 71.953 dBFS and an SFDR of 69.165 dBc. Consider for a moment, however, that the fundamental image would not typically be in the output spectrum and if we remove that spur, then the SFDR is 89.978 dB (which is 88.978 dBc when referred to the –1 dBFS input power).

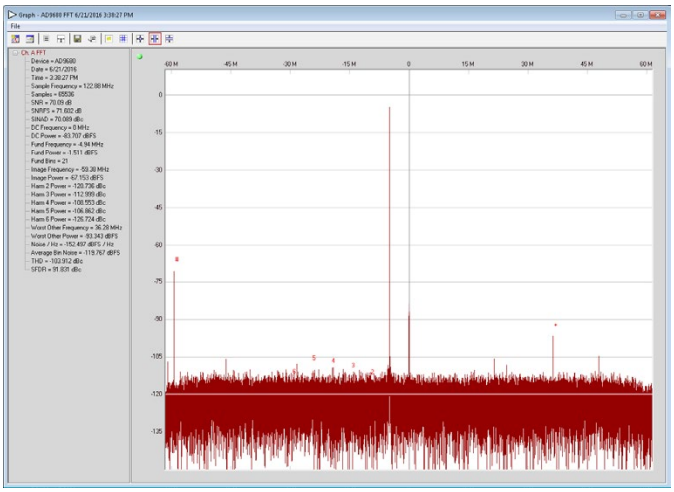
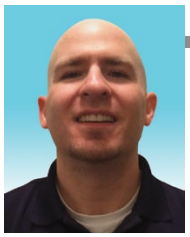


Figure 14. AD9680 FFT measurement result.

The Virtual Eval simulator does not include the fundamental image when it calculates the SNR. Make sure to adjust the settings in VisualAnalog™ to ignore the fundamental image in the measurement to achieve the correct SNR. The idea is to frequency plan where the fundamental image is not in the desired band. The measured result for the SNR is 71.602 dBFS, which is quite close to the simulated result of 71.953 dBFS in Virtual Eval. Likewise, the measured SFDR is 91.831 dBc, which is very close to the simulated result of 88.978 dBc.

Virtual Eval does an incredible job at accurately predicting the behavior of hardware. Device behavior can be predicted from the comfort of a nice chair with a good hot cup of coffee or tea. Particularly in the case of an ADC with DDCs such as the AD9680, Virtual Eval is able to simulate the ADC performance including images and harmonics well enough that the user can frequency plan and keep these undesired signals out of band where possible. As carrier aggregation and direct RF sampling continue to increase in popularity, having a tool in the tool box like Virtual Eval is quite handy. The ability to accurately predict ADC performance and frequency plan aids system designers to properly frequency plan a design in applications such as communication systems, as well as military/aerospace radar systems and many other types of applications. I would encourage you to take advantage of the digital signal processing features in the latest generation ADCs from Analog Devices. I would also recommend using Virtual Eval to help plan out your next design and have an idea ahead of time of the expected performance.

Jonathan Harris



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Fully Automatic Self-Calibrated Conductivity Measurement System

By **Robert Lee** and **Walt Kester**

Introduction

The increasing importance of monitoring water quality has led to the development of a number of related sensors and signal conditioning circuits. Water quality is measured in terms of bacteria count, pH level, chemical content, turbidity, and conductivity. All aqueous solutions conduct electricity to some degree. Adding electrolytes such as salts, acids, or bases to pure water increases the conductivity and decreases resistivity. This article focuses on conductivity measurements.

Pure water does not contain significant amounts of electrolytes and conducts only a small amount of electric current when a sample is subjected to an applied voltage—its conductivity is therefore low. On the other hand, a large quantity of electrolytes in the sample causes more current to be conducted—its conductivity is higher.

It is more common to think in terms of resistance rather than conductance, but the two are reciprocals. The resistivity, ρ, of a material or liquid is defined as the resistance of a cube of the material with perfectly conductive contacts on opposite faces. The resistance, R, for other shapes, can be calculated by

$$R = \rho L/A \qquad (1)$$

where:
L is the distance between the contacts.
A is the area of the contacts.

Resistivity is measured in units of Ω cm. A 1 Ω cm material has a resistance of 1 Ω when contacted on opposite faces of a 1 cm × 1 cm × 1 cm cube.

Conductance is simply the reciprocal of resistance, and conductivity is the reciprocal of resistivity. The unit of measurement of conductance is siemens (S), and the unit of measurement of conductivity is S/cm, mS/cm, or µS/cm.

For the purposes of this article, Y is the general symbol for conductivity measured in S/cm, mS/cm, or µS/cm. However, in many cases, the distance term is dropped for convenience, and the conductivity is simply expressed as S, mS, or µS.

Measuring Conductivity Using Conductivity Cells

A conductivity system measures conductivity by means of electronics connected to a sensor, called a conductivity cell, immersed in a solution, as shown in Figure 1.

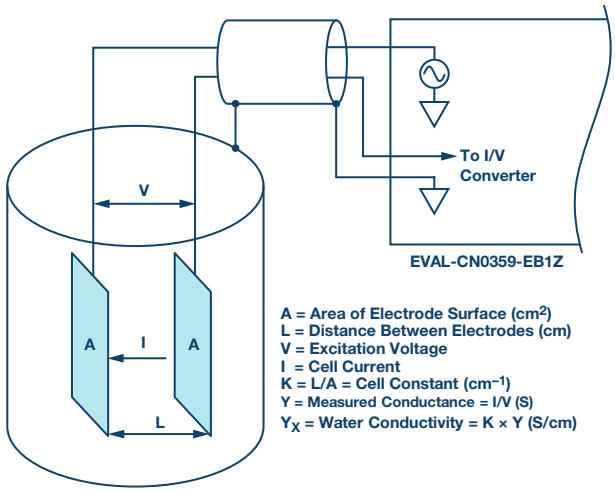


Figure 1. Interface between conductivity cell and electronics (EVAL-CN0359-EB1Z).

The electronic circuitry impresses an alternating voltage on the sensor and measures the size of the resulting current, which is related to the conductivity. Because conductivity has a large temperature coefficient (up to 4%/°C), an integral temperature sensor is incorporated into the circuitry to adjust the reading to a standard temperature, usually 25°C (77°F). When measuring solutions, the temperature coefficient of the conductivity of the water itself must be considered. To compensate accurately for the temperature, a second temperature sensor and compensation network must be used.

The contacting type sensor typically consists of two electrodes that are insulated from one another. The electrodes, typically Type 316 stainless steel, titanium palladium alloy, or graphite, are specifically sized and spaced to provide a known cell constant. Theoretically, a cell constant of 1.0/cm describes two electrodes, each sized 1 cm^2 in area, and spaced 1 cm apart. Cell constants must be matched to the measurement system for a given range of operation. For instance, if a sensor with a cell constant of 1.0/cm is used in pure water with a conductivity of 1 µS/cm, the cell has a resistance of 1 MΩ. Conversely, the same cell in seawater has a resistance of 30 Ω. Because the resistance ratio is so large, it is difficult for ordinary instruments to accurately measure such extremes with only one cell constant.

When measuring the 1 µS/cm solution, the cell is configured with large area electrodes spaced a small distance apart. For example, a cell with a cell constant of 0.01/cm results in a measured cell resistance of approximately 10 kΩ rather than 1 MΩ. It is easier to accurately measure 10 kΩ than 1 MΩ; therefore, the measuring instrument can operate over the same range of cell resistance for both ultrapure water and high conductivity seawater by using cells with different cell constants.

The cell constant, K, is defined as the ratio of the distance between the electrodes, L, to the area of the electrodes, A:

$$K = L/A \quad (2)$$

The instrumentation then measures the cell conductance, Y:

$$Y = I/V \quad (3)$$

The conductivity of the liquid, Y_X, is then calculated:

$$YX = K \times Y \quad (4)$$

There are two types of conductivity cells: those with two electrodes and those with four electrodes, as shown in Figure 2. The electrodes are often referred to as poles.

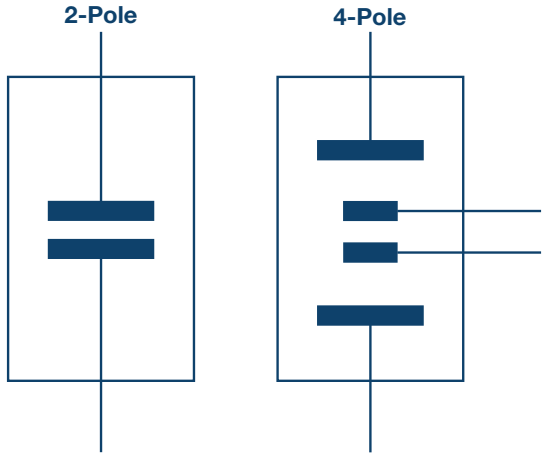


Figure 2. 2-pole and 4-pole conductivity cells.

The 2-pole sensor is more suitable for low conductivity measurements, such as purified water, and various biological and pharmaceutical liquids. The 4-pole sensor is more suitable for high conductivity measurements, such as waste water and seawater analysis.

The cell constants for 2-pole cells range from approximately 0.1/cm to 1/cm, and the cell constants for 4-pole cells range from 1/cm to 10/cm.

The 4-pole cell eliminates the errors introduced by polarization of the electrodes and field effects that can interfere with the measurement.

The actual configuration of the electrodes can be that of parallel rings, coaxial conductors, or others, rather than the simple parallel plates shown in Figure 2.

Regardless of the type of cell, it is important not to apply a dc voltage to any electrode because ions in the liquid will accumulate on the electrode surface, thereby causing polarization, measurement errors, and damage to the electrode.

Take special care with sensors that have shields, as in the case of coaxial sensors. The shield must be connected to the same potential as the metal container holding the liquid. If the container is grounded, the shield must be connected to the circuit board ground.

The final precaution is not to exceed the rated excitation voltage or current for the cell. The following circuit allows programmable excitation voltages from 100 mV to 10 V, and the R23 (1 kΩ) series resistor limits the maximum cell current to 10 mA.

Circuit Description

The circuit shown in Figure 3 is a completely self-contained, microprocessor controlled, highly accurate conductivity measurement system that is ideal for measuring the ionic content of liquids, water quality analysis, industrial quality control, and chemical analysis.

A carefully selected combination of precision signal conditioning components yields an accuracy of better than 0.3% over a conductivity range of 0.1 µS to 10 S (10 MΩ to 0.1 Ω) with no calibration requirements.

Automatic detection is provided for either 100 Ω or 1000 Ω platinum (Pt) resistance temperature devices (RTDs), allowing the conductivity measurement to be referenced to room temperature.

The system accommodates 2- or 4-wire conductivity cells, and 2-, 3-, or 4-wire RTDs for added accuracy and flexibility.

The circuit generates a precise ac excitation voltage with minimum dc offset to avoid a damaging polarization voltage on the conductivity electrodes. The amplitude and frequency of the ac excitation is user-programmable.

An innovative synchronous sampling technique converts the peak-to-peak amplitude of the excitation voltage and current to a dc value for accuracy and ease in processing using the dual, 24-bit, Σ-Δ ADC contained within the precision analog microcontroller.

The intuitive user interface is an LCD display and an encoder push button. The circuit can communicate with a PC using an RS-485 interface if desired, and it operates on a single 4 V to 7 V supply.

The excitation square wave for the conductivity cell is generated by switching the ADG1419 between the +VEXC and –VEXC voltages using the PWM output of the ADuCM360 microcontroller. It is important that the square wave has a precise 50% duty cycle and a very low dc offset. Even small dc offsets can damage the cell over a period of time.

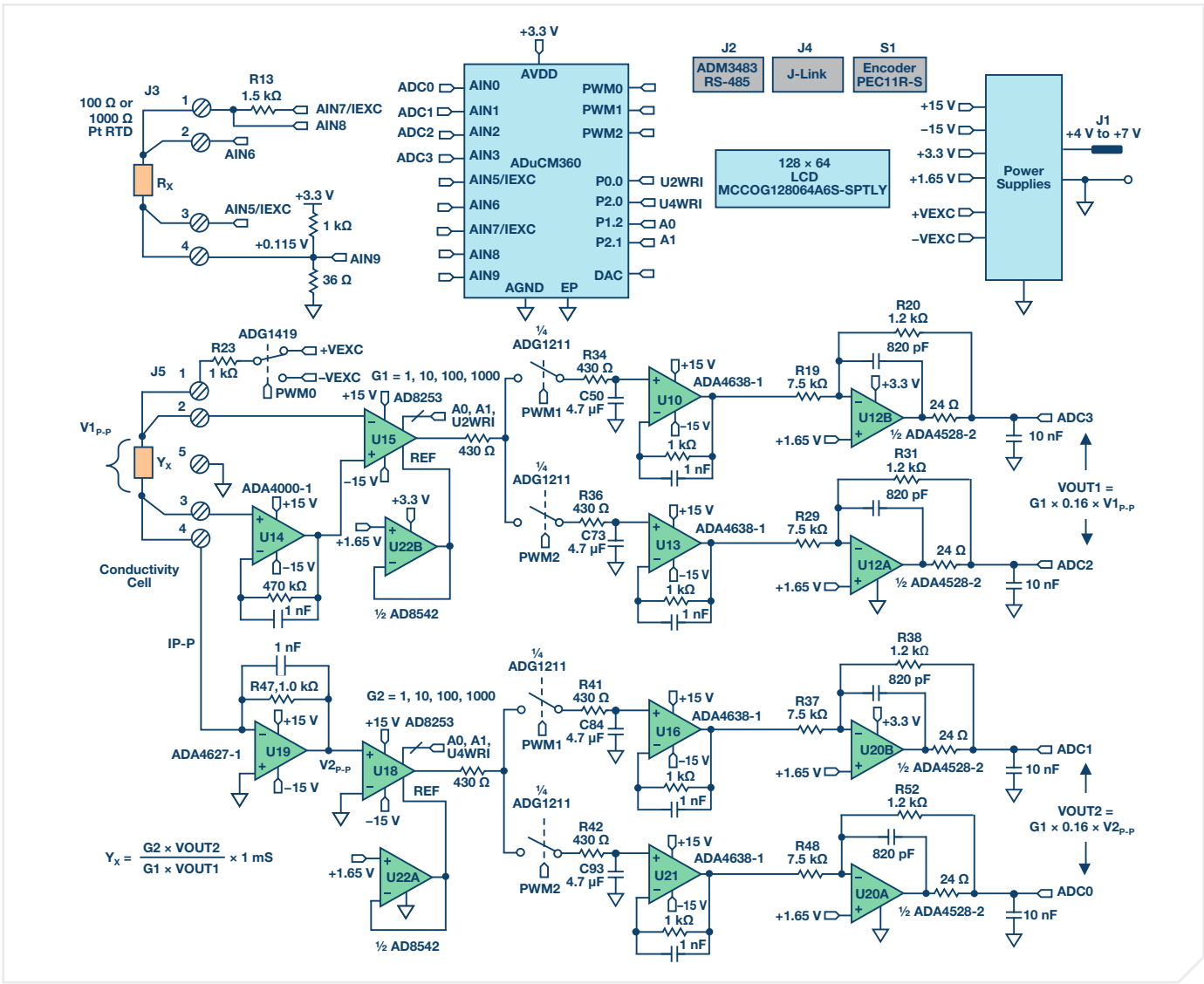


Figure 3. High performance conductivity measurement system (simplified schematic: all connections and decoupling not shown).

The +VEXC and –VEXC voltages are generated by the ADA4077-2 op amps (U9A and U9B), and their amplitudes are controlled by the DAC output of the ADuCM360, as shown in Figure 4.

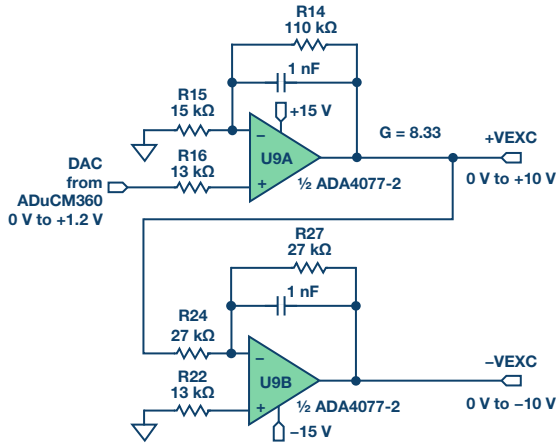


Figure 4. Excitation voltage sources.

The ADA4077-2 has a typical offset voltage of 15 µV (A grade), a 0.4 nA bias current, a 0.1 nA offset current, and an output current of up to ±10 mA, with a dropout voltage of less than 1.2 V. The U9A op amp has a closed-loop gain of 8.33 and converts the ADuCM360 internal DAC output (0 V to 1.2 V) to the +VEXC voltage of 0 V to 10 V. The U9B op amp inverts the +VEXC and generates the –VEXC voltage. R22 is chosen such that R22 = R24||R27 to achieve first-order bias current cancellation. The error due to the 15 µV offset voltage of U9A is approximately (2 × 15 µV) ÷ 10 V = 3 ppm. The primary error introduced by the inverting stage is therefore the error in the resistor matching between R24 and R27.

The ADG1419 is a 2.1 Ω, on-resistance SPDT analog switch with an on-resistance flatness of 50 mΩ over a ±10 V range, making it ideal for generating a symmetrical square wave from the ±VEXC voltages. The symmetry error introduced by the ADG1419 is typically 50 mΩ ÷ 1 kΩ = 50 ppm. Resistor R23 limits the maximum current through the sensor to 10 V/1 kΩ = 10 mA.

The voltage applied to the cell, V1, is measured with the AD8253 instrumentation amplifier (U15). The positive input to U15 is buffered by the ADA4000-1 (U14). The ADA4000-1 is chosen because of its low bias current of 5 pA to minimize the error in measuring low currents associated with low conductivities. The negative input of the AD8253 does not require buffering.

The offset voltages of U14 and U15 are removed by the synchronous sampling stage and do not affect the measurement accuracy.

U15 and U18 are AD8253 10 MHz, 20 V/µs, programmable gain (G = 1, 10, 100, 1000) instrumentation amplifiers with gain error of less than 0.04%. The AD8253 has a slew rate of 20 V/µs and a settling time of 1.8 µs to 0.001% for G = 1000. Its common-mode rejection is typically 120 dB.

The U19 (ADA4627-1) stage is a precision current to voltage converter that converts the current through the sensor to voltage. The ADA4627-1 has an offset voltage of 120 µV (typical, A grade), a bias current of 1 pA (typical), a slew rate of 40 V/µs, and a 550 ns settling time to 0.01%. The low bias current and offset voltage make it ideal for this stage. The symmetry error produced by the 120 µV offset error is only 120 µV/10 V = 12 ppm.

The U22A and U22B (AD8542) buffers supply the 1.65 V reference to the U18 and U15 instrumentation amplifiers, respectively.

The following is a description of the remainder of the signal path in the voltage channel (U17A, U17B, U10, U13, U12A, and U12B). The operation of the current channel (U17C, U17D, U16, U21, U20A, and U20B) is identical.

The ADuCM360 generates the PWM0 square wave switching signal for the ADG1419 switch as well as PWM1 and PWM2 synchronizing signals for the synchronous sampling stages. The cell voltage and the three timing waveforms are shown in Figure 5.

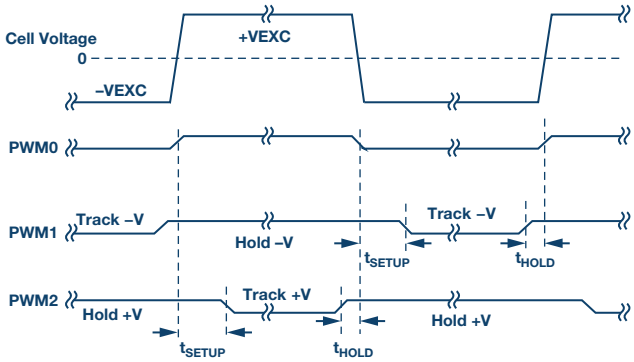


Figure 5. Cell voltage and track-and-hold timing signals.

The output of the AD8253 in amp (U15) drives two parallel track-and-hold circuits composed of ADG1211 switches (U17A/U17B), series resistors (R34/R36), hold capacitors (C50/C73), and unity-gain buffers (U10/U13).

The ADG1211 is a low charge injection, quad SPST analog switch, operating on a ±15 V power supply with up to ±10 V input signals. The maximum charge injection due to switching is 4 pC, which produces a voltage error of only 4 pC ÷ 4.7 µF = 0.9 µV.

The PWM1 signal causes the U10 track-and-hold buffer to track the negative cycle of the sensor voltage and then hold it until the next track cycle. The output of the U10 track-and-hold buffer is therefore a dc level corresponding to the negative amplitude of the sensor voltage square wave.

Similarly, the PWM2 signal causes the U13 track-and-hold buffer to track the positive cycle of the sensor voltage and then hold it until the next track cycle. The output of the U13 track-and-hold buffer is therefore a dc level corresponding to the positive amplitude of the sensor voltage square wave.

The bias current of the track-and-hold buffers (ADA4638-1) is 45 pA typical, and the leakage current of the ADG1211 switch is 20 pA typical. Therefore, the worst-case leakage current on the 4.7 µF hold capacitors is 65 pA. For a 100 Hz excitation frequency, the period is 10 ms. The drop voltage over one-half the period (5 ms) due to the 65 pA leakage current is (65 pA × 5 ms) ÷ 4.7 µF = 0.07 µV.

The offset voltage of the ADA4638-1 zero-drift amplifier is only 0.5 µV typical and contributes negligible error.

The final stages in the signal chain before the ADC are the ADA4528-2 inverting attenuators (U12A and U12B) that have a gain of −0.16 and a common-mode output voltage of +1.65 V. The ADA4528-2 has an offset voltage of 0.3 µV typical and therefore contributes negligible error.

The attenuator stage reduces the ±10 V maximum signal to ±1.6 V with a common-mode voltage of 1.65 V. This range is compatible with the input range of the ADuCM360 ADC input, which is 0 V to 3.3 V (1.65 V ± 1.65 V) for an AVDD supply of 3.3 V.

The attenuator stages also provide noise filtering and have a −3 dB frequency of approximately 198 kHz.

The differential output of the voltage channel, VOUT1, is applied to the AIN2 and AIN3 inputs of the ADuCM360. The differential output of the current channel, VOUT2, is applied to the AIN0 and AIN1 inputs of the ADuCM360.

The equations for the two outputs are given by

$$VOUT1 = G1 \times 0.16 \times V1_{P\text{-}P} \quad (5)$$

$$VOUT2 = G2 \times 0.16 \times V2_{P\text{-}P} \quad (6)$$

The cell current is given by

$$I_{P\text{-}P} = V1_{P\text{-}P} \times YX \quad (7)$$

The $V2_{P\text{-}P}$ voltage is given by

$$V2_{P\text{-}P} = I_{P\text{-}P} \times R47 \quad (8)$$

Solving Equation 8 for $I_{P\text{-}P}$ and substituting into Equation 7 yields the following for Y_X:

$$Y_X = \frac{V2_{P\text{-}P}}{V1_{P\text{-}P} \times R47} \quad (9)$$

Solving Equation 5 and Equation 6 for $V1_{P\text{-}P}$ and $V2_{P\text{-}P}$ and substituting into Equation 9 yields the following:

$$Y_X = \frac{G2 \times VOUT2}{G1 \times VOUT1 \times R47} \quad (10)$$

$$Y_X = \frac{G2 \times VOUT2}{G1 \times VOUT1} \times 1\,\text{mS} \quad (11)$$

Equation 11 shows that the conductivity measurement depends on G1, G2, and R47, and the ratio of VOUT2 to VOUT1. Therefore, a precision reference is not required for the ADCs within the ADuCM360.

The AD8253 gain error (G1 and G2) is 0.04% maximum, and R47 is chosen to be a 0.1% tolerance resistor.

From this point, the resistors in the VOUT1 and VOUT2 signal chain determine the overall system accuracy.

The software sets the gain of each AD8253 as follows:

- If the ADC code is over 94% of full scale, the gain of the AD8253 is reduced by a factor of 10 on the next sample.
- If the ADC code is less than 8.8% of full scale, the gain of the AD8253 is increased by a factor of 10 on the next sample.

System Accuracy Measurements

The following four resistors affect the accuracy in the VOUT1 voltage channel: R19, R20, R29, and R31.

The following five resistors affect the accuracy in the VOUT2 current channel: R47, R37, R38, R48, and R52.

Assuming that all nine resistors are 0.1% tolerance, and including the 0.04% gain error of the AD8253, a worst-case error analysis yields approximately 0.6%. The analysis is included in the CN-0359 Design Support Package.

In practice, the resistors are more likely to combine in an RSS manner, and the RSS error due to the resistor tolerances in the positive or negative signal chain is $\sqrt{5} \times 0.1\% = 0.22\%$.

Accuracy measurements were taken using precision resistors from 1 Ω to 1 MΩ (1 S to 1 µS) to simulate the conductivity cell. Figure 6 shows the results, and the maximum error is less than 0.1%.

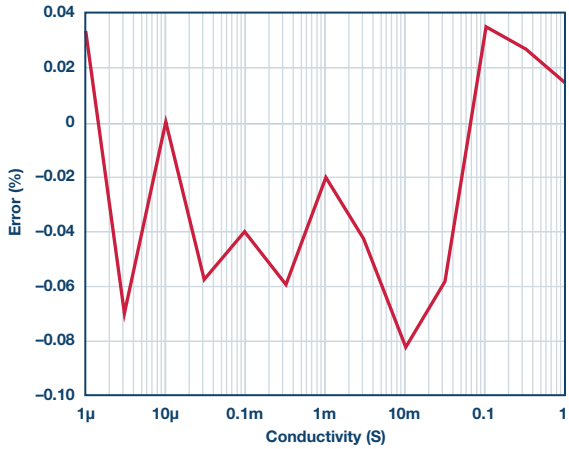


Figure 6. System error (%) vs. conductivity of 1 µS to 1 S.

RTD Measurement

Conductivity measuring system accuracy is only as good as its temperature compensation. Because common solution temperature coefficients vary in the order of 1%/°C to 3%/°C or more, measuring instruments with adjustable temperature compensation must be used. Solution temperature coefficients are somewhat nonlinear and usually vary with the actual conductivity as well. Therefore, calibration at the actual measuring temperature yields the best accuracy.

The ADuCM360 contains two matched, software configurable, excitation current sources. They are individually configurable to provide a current output of 10 µA to 1 mA, and matching is better than 0.5%. The current sources allow the ADuCM360 to easily perform 2-wire, 3-wire, or 4-wire measurements for either Pt100 or Pt1000 RTDs. The software also automatically detects if the RTD is Pt100 or Pt1000.

The following discussion shows simplified schematics of how the different RTD configurations operate. All mode switching is accomplished in the software, and there is no need to change the external jumper settings.

Figure 7 shows the configuration for 4-wire RTDs.

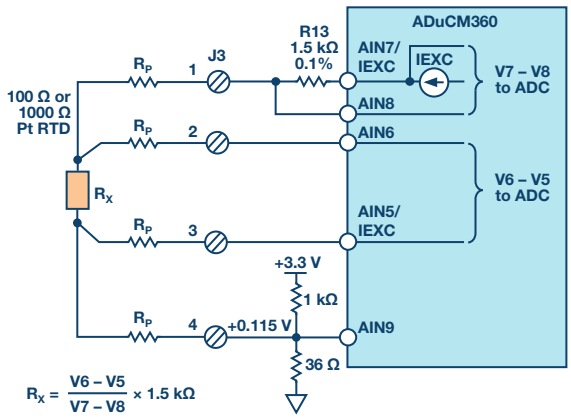


Figure 7. Configuration for 4-wire RTD connection.

The parasitic resistance in each of the leads to the remote RTD is shown as R_P. The excitation current (IEXC) passes through a precision 1.5 kΩ resistor and the RTD. The on-chip ADC measures the voltage across the RTD (V6 – V5) and uses the voltage across R13 (V7 – V8) as a reference.

It is important that the R13 resistor and the IEXC excitation current value be chosen such that the ADuCM360 maximum input voltage at AIN7 does not exceed AVDD – 1.1 V; otherwise, the IEXC current source does not function properly.

The RTD voltage is accurately measured using the two sense leads that connect to AIN6 and AIN5. The input impedance is approximately 2 MΩ (unbuffered mode, PGA gain = 1), and the current flowing through the sense lead resistance produces minimum error. The ADC then measures the RTD voltage (V6 – V5).

The RTD resistance is then calculated as:

$$R_X = \frac{V6 - V5}{V7 - V8} \times 1.5\ \text{k}\Omega \qquad (12)$$

The measurement is ratiometric and does not depend on an accurate external reference voltage, only the tolerance of the 1.5 kΩ resistor. In addition, the 4-wire configuration eliminates the error associated with the lead resistances.

The ADuCM360 has a buffered or unbuffered input option. If the internal buffer is activated, the input voltage must be greater than 100 mV. The 1 kΩ/36 Ω resistor divider provides a 115 mV bias voltage to the RTD that allows buffered operation. In the unbuffered mode, Terminal 4 of J3 can be grounded and connected to a grounded shield for noise reduction.

The 3-wire connection is another popular RTD configuration that eliminates lead resistance errors, as shown in Figure 8.

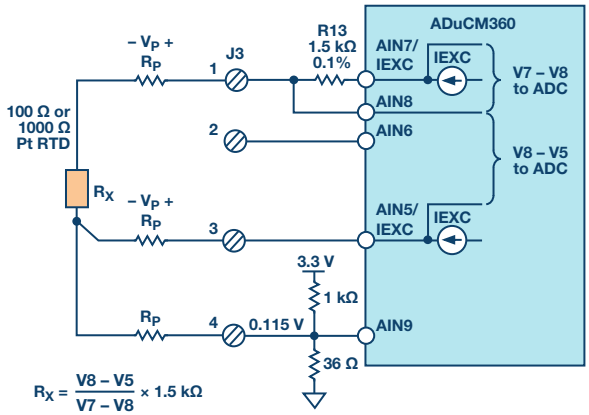


Figure 8. Configuration for 3-wire RTD connection.

The second matched IEXC current source (AIN5/IEXC) develops a voltage across the lead resistance in series with Terminal 3 that cancels the voltage dropped across the lead resistance in series with Terminal 1. The measured V8 – V5 voltage is therefore free of lead resistance error.

Figure 9 shows the 2-wire RTD configuration where there is no compensation for lead resistance.

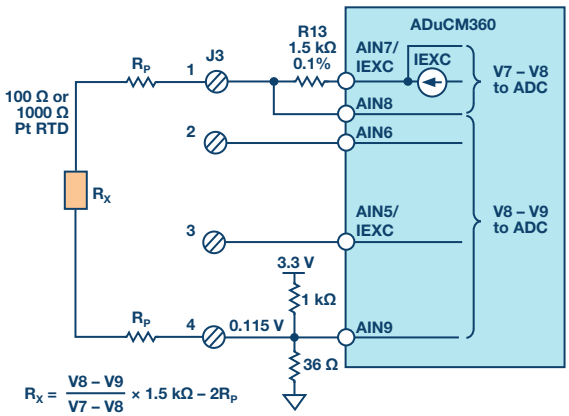


Figure 9. Configuration for 2-wire RTD connection.

The 2-wire configuration is the lowest cost circuit and is suitable for less critical applications, short RTD connections, and higher resistance RTDs such as Pt1000.

Power Supply Circuits

To simplify system requirements, all the required voltages (±15 V and +3.3 V) are generated from a single 4 V to 7 V supply, as shown in Figure 10.

The ADP2300 buck regulator generates the 3.3 V supply for the board. The design is based on the downloadable ADP230x Buck Regulator Design Tool.

The ADP1613 boost regulator generates a regulated +15 V supply and an unregulated −15 V supply. The −15 V supply is generated with a charge pump. The design is based on the ADP161x Boost Regulator Design Tool.

Details regarding the selection and design of power supplies are available at *www.analog.com/ADIsimPower*.

Use proper layout and grounding techniques to prevent the switching regulator noise from coupling into the analog circuits. See the *Linear Circuit Design Handbook*, the *Data Conversion Handbook*, the MT-031 Tutorial, and the MT-101 Tutorial for further details.

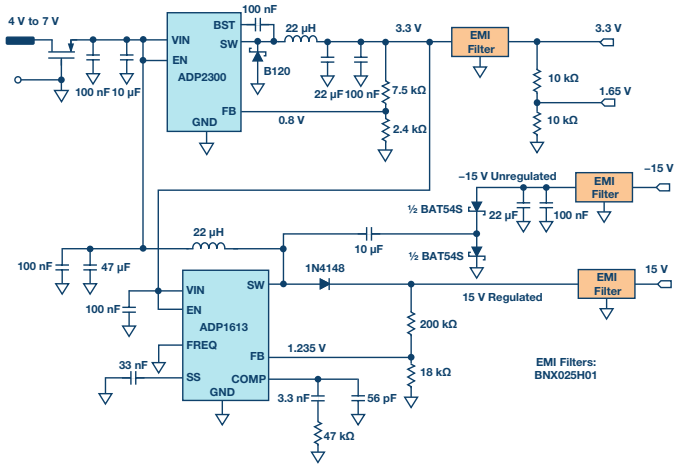


Figure 10. Power supply circuits.

Figure 11 shows the LCD backlight driver circuit.

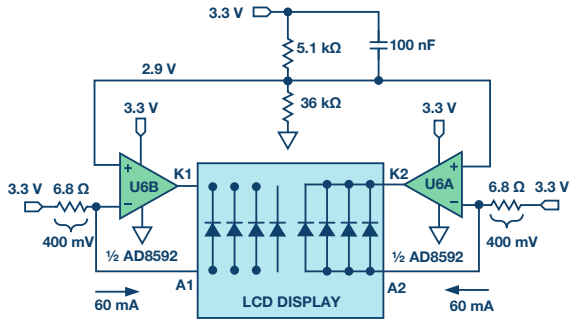


Figure 11. LCD backlight drivers.

Each half of the AD8592 op amp acts as a 60 mA current source to supply the LCD backlight currents. The AD8592 can source and sink up to 250 mA, and the 100 nF capacitor ensures a soft startup.

Hardware, Software, and User Interface

The complete circuit including software is available as the CN-0359 Circuits from the Lab Reference Design. The circuit board, EVAL-CN0359-EB1Z, comes preloaded with the code required to make the conductivity measurements. The actual code can be found in the CN-0359 Design Support Package, in the CN0359-SourceCode.zip file.

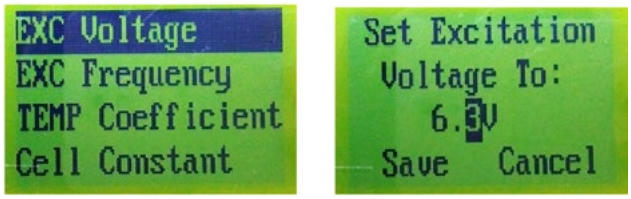
The user interface is intuitive and easy to use. All user inputs are from a dual function push button/rotary encoder knob. The encoder knob can be turned clockwise or counterclockwise (no mechanical stop), and can also be used as a push button.

Figure 12 is a photo of the EVAL-CN0359-EB1Z board that shows the LCD display and the position of the encoder knob.

Figure 12. Photo of an EVAL-CN0359-EB1Z board showing the home screen in measurement mode.

After connecting, the conductivity cell and the RTD the board is powered up. The LCD screen appears as shown in Figure 12.

The encoder knob is used to input the excitation voltage, excitation frequency, temperature coefficient of the conductivity cell, the cell constant, setup time, hold time, RS-485 baud rate and address, LCD contrast, and so forth. Figure 13 shows some of the LCD display screens.



Setting Screen | Setting Excitation Voltage

Figure 13. LCD display screens.

The EVAL-CN0359-EB1Z is designed to be powered with the EVAL-CFTL-6V-PWRZ 6 V power supply. The EVAL-CN0359-EB1Z requires only the power supply and the external conductivity cell and RTD for operation.

The EVAL-CN0359-EB1Z also has an RS-485 connector, J2, that allows an external PC to interface with the board. Connector J4 is a JTAG/SWD interface for programming and debugging the ADuCM360.

Figure 14 is a typical PC connection diagram showing an RS-485 to USB adapter.

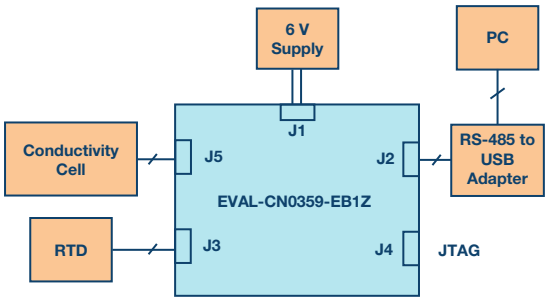


Figure 14. Test setup functional diagram.

Summary

The circuit described in this article is based on the Analog Devices CN-0359 reference design. Complete documentation including circuit note, detailed schematic, bill of material, layout, Gerber files, and source code is available at *http://www.analog.com/CN0359-DesignSupport*.

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Data Sheets

AD8253 data sheet.
AD8542 data sheet.
AD8592 data sheet.
ADA4000-1 data sheet.
ADA4077-2 data sheet.
ADA4528-2 data sheet.
ADA4627-1 data sheet.
ADA4638-1 data sheet.
ADG1211 data sheet.
ADG1419 data sheet.
ADM3075 data sheet.
ADP2300 data sheet.
ADP1613 data sheet.
ADuCM360 data sheet.

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Also by this Author:

Complete Gas Sensor Circuit Using Nondispersive Infrared (NDIR)

Volume 50, Number 4

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Walt Kester

Also by this Author:

Complete Gas Sensor Circuit Using Nondispersive Infrared (NDIR)

Volume 50, Number 4

Rarely Asked Questions—Issue 135 Amplifier R_F: Think Before You Choose!

By **Tina Collins**

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Question:

I'm selecting an op amp for my precision signal path. Isn't faster always better?

Answer:

When selecting the feedback resistor (R_F) for single-ended voltage feedback and a fully differential amplifier, consideration needs to be given to the system requirements. There are trade-offs in the selection of R_F, which include power dissipation, bandwidth, and stability. If speed is critical, as discussed in RAQ Issue 122, "The Truth About Voltage Feedback Resistors," the recommended data sheet R_F value is advised. If power dissipation is critical, and the system requires a higher gain, a larger R_F can be the right choice.

The choices for R_F increase as gain increases. The destabilizing effect between the internal capacitance of the amplifier and the feedback resistor is reduced with larger gains. As gain increases, the amplifier is less sensitive to gain peaking.

The example of Figure 1 shows the lab results of the normalized frequency response for the ADA4807-1, low noise, rail-to-rail input and output, voltage feedback amplifier in a noninverting configuration with an R_F of 10 kΩ for gains of 11 V/V, 21 V/V, and 31 V/V.

The degree of peaking in the small signal frequency response indicates instability. Increasing the gain from 11 V/V to 31 V/V results in less than 1 dB of peaking. This would imply that the amplifier has sufficient phase margin with an R_F of 10 kΩ and is stable at high gains.

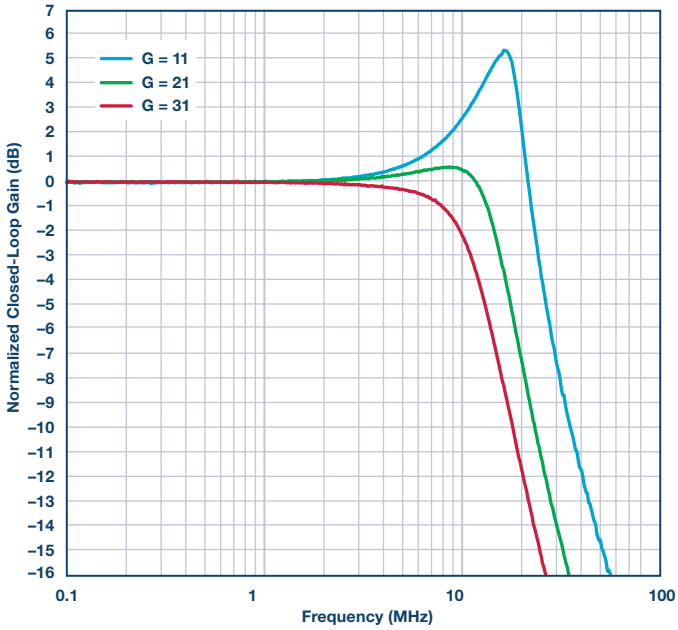

Figure 1. Lab results for different gains with R_F = 10 kΩ. V_S = ±5 V, R_{LOAD} = 1 kΩ for gains 11 V/V, 21 V/V, and 31 V/V.

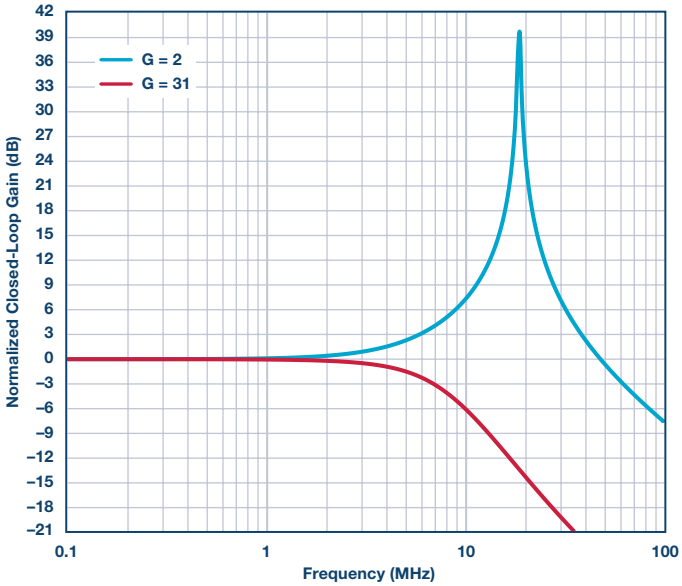

Figure 2. Simulation results using the ADA4807 SPICE model. R_F = 10 kΩ, V_S = ±5 V, R_{LOAD} = 1 kΩ for gain = 2, and 31 V/V.

Validating a circuit in the lab is not a mandatory step for verifying potential instabilities. Figure 2 shows the simulation results using the SPICE model with gain of 2 V/V and 31 V/V. The instability with using a large gain resistor such as 10 kΩ in a gain of 2 V/V is shown in comparison with the same R_F in a gain of 31 V/V. Figure 3 shows results for gains 11 V/V, 21 V/V, and 31 V/V in the time domain.

There are system trade-offs in the selection of R_F. To achieve full performance from a system, the appropriate R_F choice will depend on the system requirements with respect to stability, bandwidth, and power.

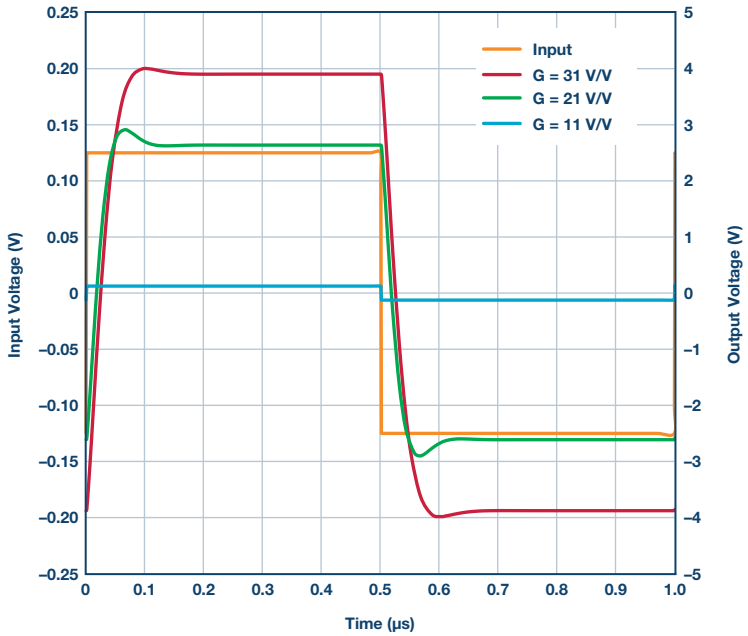

Figure 3. Pulse response simulation results using the ADA4807 SPICE model. V_S = ±5 V, R_F = 10 kΩ; G = 11 V/V, 21 V/V, and 31 V/V and R_{LOAD} = 1 kΩ.

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PLC DCS Analog Input Module Design Breaks Barriers in Channel-to-Channel Isolation and High Density

By **Van Yang**, **Songtao Mu**, and **Derrick Hartmann**

Introduction

In high end factory automation applications such as gas and oil plants and power plants, the requirements of low EMI, small size, high reliability, and low cost are especially challenging for channel-to-channel isolated designs. For this reason, the standard module implementation has a channel density that is typically limited to only four or eight channels, with only hundreds of volts of channel-to-channel isolation.

This article will briefly discuss isolation in the process control analog input module and the traditional approaches to achieving this. It then outlines an alternative high density, easy to design, channel-to-channel isolation analog input module architecture. Test results are included that show that the 16-channel, 2.5 kV rms channel-to-channel isolation demo module easily passes the EN55022, Class B isolation standard.

Isolation in the Process Control Analog Input Module

Galvanic isolation is the principle of physically and electrically separating two circuits, so that there is no direct conduction path but data and power can still be exchanged. This is typically achieved using transformers, optocouplers, or capacitors. Isolation is used to protect circuitry and human beings, break ground loops, and improve common-mode voltage and noise rejection performance.

Typically process control inputs are either group isolated or channel-to-channel isolated (see Figure 1). For group isolation, a number of input channels are grouped together to share a single isolation barrier, including power isolation and signal isolation. This saves cost over channel-to-channel isolation, but it limits the common-mode voltage difference between channels in the group, meaning they should all be placed in the same zone. Channel-to-channel isolation, as in the right of Figure 1, is always favorable for its improved robustness. That said, it comes at a much higher cost per-channel, so this trade-off must be carefully assessed by plant builders.

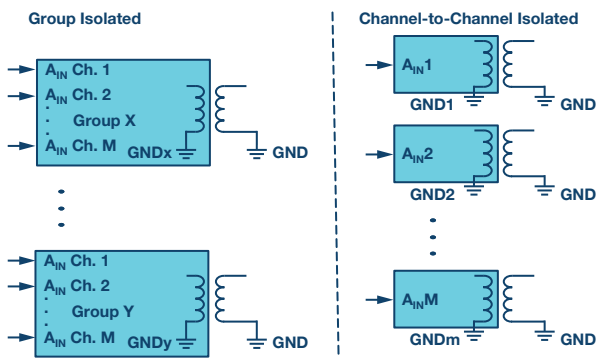

Figure 1. Group isolation and channel-to-channel isolation.

With a channel-to-channel isolation design, every channel needs dedicated power isolation and signal isolation. The isolation is one of the key limitations for input module channel density, EMI, cost, and reliability. In modern designs, a digital isolator is used per channel for data isolation. A typical digital isolator, such as the ADuM141E, would have four isolated data channels in a 16-lead SOIC (6.2 mm × 10 mm) package. Power isolation is still required per channel, though, so let's discuss three traditional approaches to power isolation: multitaps transformer, push-pull design, and isolated dc-to-dc modules.

Figure 2 shows a flyback isolation dc-to-dc architecture with a multitap transformer. A flyback converter drives the transformer to generate multiple outputs on the taps. It's a mature power architecture but has six major disadvantages for process control applications, which are:

1. It needs a customized transformer with multitaps and a shield to control EMI. This is hard to achieve in a small form factor with sufficient reliability.
2. Only one channel could be used for a feedback control loop, meaning that the other channels are more loosely regulated. This needs to be carefully evaluated to ensure reliable operation.
3. Channel density is limited by specific transformer placement. For the power coming from each tap output, the transformer is placed as the center of the analog input module with each input channel laid out in fanout sectors around the transformer, limiting the analog input module card channels to four or eight.
4. Interference from one channel can be coupled into other channels through the coupling capacitors between the taps of the transformer.
5. The isolation voltage level. Multitap transformers can only achieve hundreds of volts of channel-to-channel isolation unless special insulation materials or designs are incorporated, which significantly increases the transformer cost.
6. The high cost of achieving UL/CSA certification for the customized transformer.

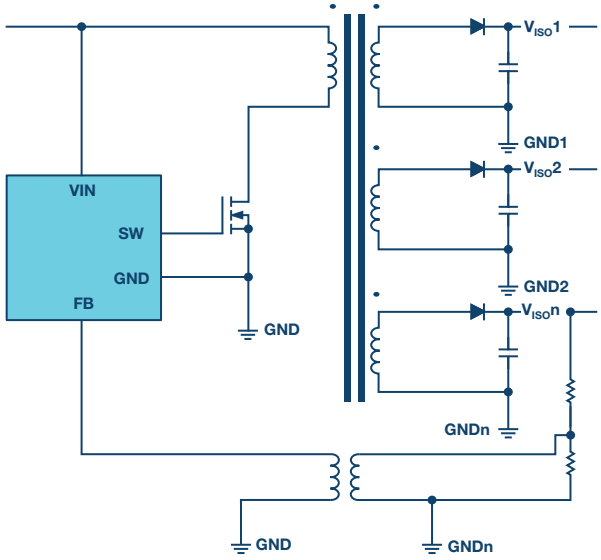

Figure 2. Multitap transformer power isolation design.

Another approach is to use a separate transformer per channel and use a push-pull approach to isolating each channel. In this approach, no feedback is used. Instead, a well-regulated supply (for example, 7 V) is used to drive each of the transformers, which is then further regulated on the secondary side using an LDO. This approach is feasible as the current draw on the secondary side is relatively low, which makes adequate regulation possible.

Some of the drawbacks of this approach are the requirement for preregulation as well as additional components per channel. The transformer selected must meet the isolation rating required. The preregulation, as well as a transformer, switches, and an LDO per channel take up board space and add cost. There is also a significant evaluation effort required to ensure that the regulation is sufficient under all conditions.

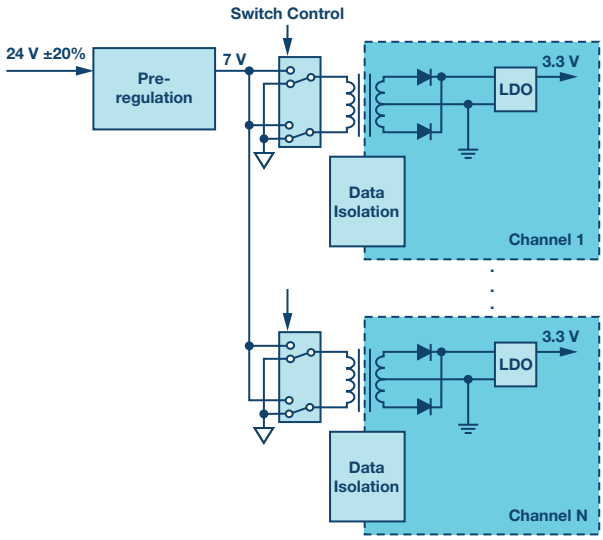

Figure 3. Push-pull isolation design.

Using surface-mount isolated dc-to-dc modules certified by UL/CSA make the isolated power design much easier and can improve channel density while increasing isolation voltage to thousands of volts. That said, the cost is relatively high and typically these can only pass the EN55022 Class A. These modules may also have conducted electromagnetic interference issues as most of the modules PWM frequency are below 1 MHz to minimize the electromagnetic radiation interference. Also, the majority of the process control analog input modules consume less than 10 mA current, far less than most of the isolated power modules in the market.

All three traditional approaches discussed struggle to meet the required isolation performance and cost. These approaches also still require separate data isolators per channel, adding additional space and cost. What if the power isolation could be included as part of the data isolator? It can, and it is.

ADI *i*Coupler® techology and *iso*Power® technology are widely used in the industrial and automotive market and these two technologies can be integrated into a single package. Taking the ADuM5411 as an example, per the block diagram shown in Figure 4, this device includes complete power isolation and four channels of data isolation in a 7.8 mm × 8.2 mm, 24-lead TSSOP package. It offers up to 150 mW output, enough for analog input signal conditioning and digitizing and passes the 2500 V rms UL1577 isolation standard. What's more, the CMTI (common-mode transient immunity) is greater than 75 kV/µs, making it ideal for harsh industrial environments, such as power plants, where high transient voltages and currents exist.

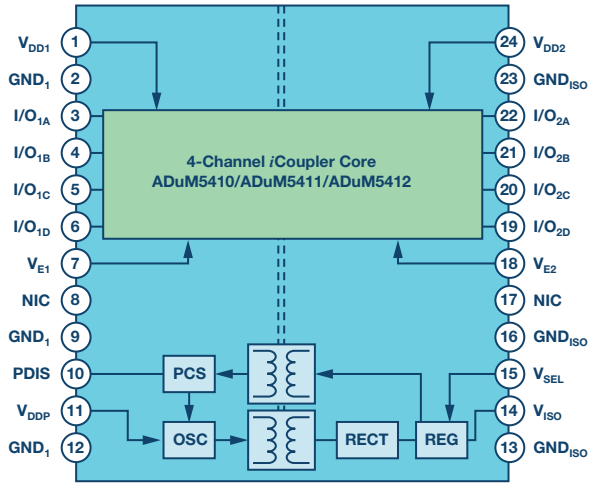

Figure 4. ADuM5411 block diagram.

Due to the high integration of both data and power isolation, the analog input module design is greatly simplified and higher channel densities are possible. It enables the possibility of providing 16 or more channels in the same space as eight channels using older isolation methods.

A 16-channel, channel-to-channel isolation temperature input module was designed and tested using this isolation approach (see Figure 5). The ADuM5411 devices in the module provide isolated power and data to each of the 16 temperature input channels. The thermocouple and/or RTD measurements are performed by highly integrated temperature front-end ICs (AD7124, or AD7792) providing additional space saving over more discrete designs. The ADP2441 converts the 24 V backplane supply to 3.3 V to power the MCU, touchscreen, and the ADuM5411. Each input channel requires an area of only 63.5 mm × 17.9 mm.

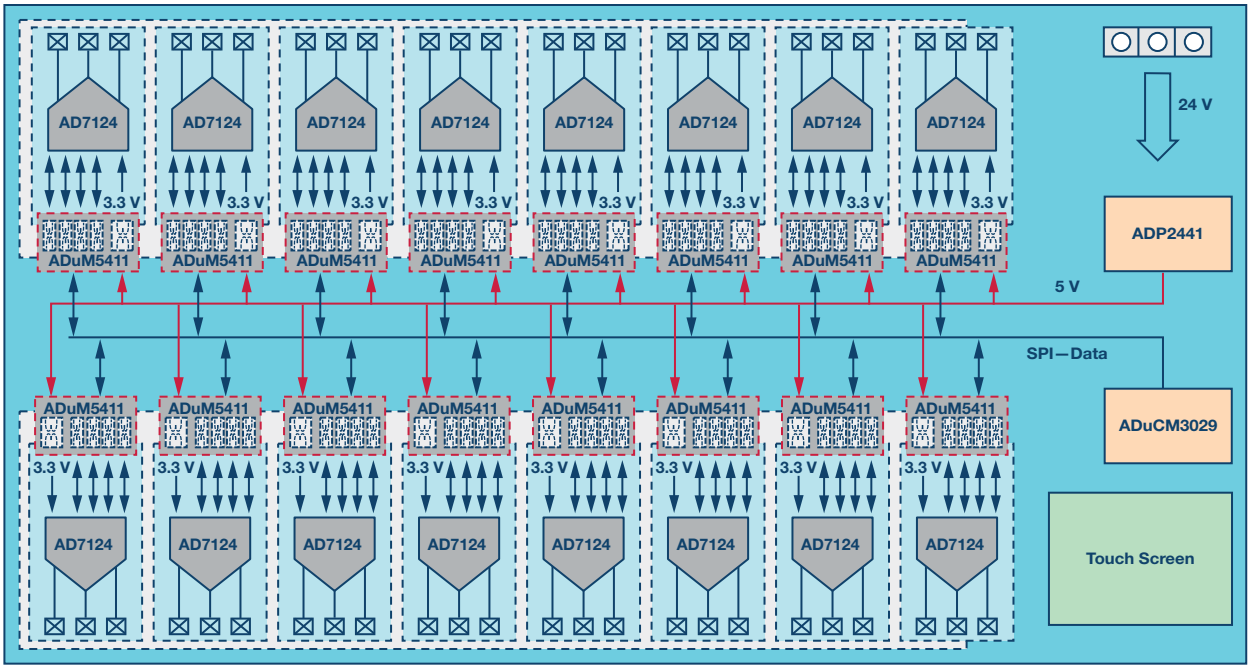

Figure 5. 16-channel temperature channel-to-channel isolation input module block diagram.

Layout Design for ADuM5411

The ADuM5411 uses a switching frequency of 125 MHz. Due to the high number of channels, special care was taken to ensure the board would pass the electromagnetic radiation interference test per EN55022 to Class B.

To minimize the radiated emission, the principles used were to minimize the power draw and minimize the current loop return path. The power was minimized by using low power integrated temperature front-end ICs. This means less power will be drawn across the isolation barrier, meaning there will also be less energy radiated. The AD7124 only draws 0.9 mA when fully active. To minimize the current return loop, both ferrite beads as well as a small amount of stitching capacitance were used.

Ferrite beads are a useful method to control the radiating signal at its source by presenting a much higher impedance than a PCB trace. Referring to Figure 6, ferrite beads were placed in series with the ADuM5411's pins. The frequency response of the ferrite beads is a very important consideration. The ferrite bead used is BLM15HD182SN1, which provides greater than 2 kΩ—between 100 MHz and 1 GHz frequency range. The ferrite beads should be placed as close to the ADuM5411's pad as possible. E9 on the VISO path and E10 on the GNDISO path are the most critical ferrite beads.

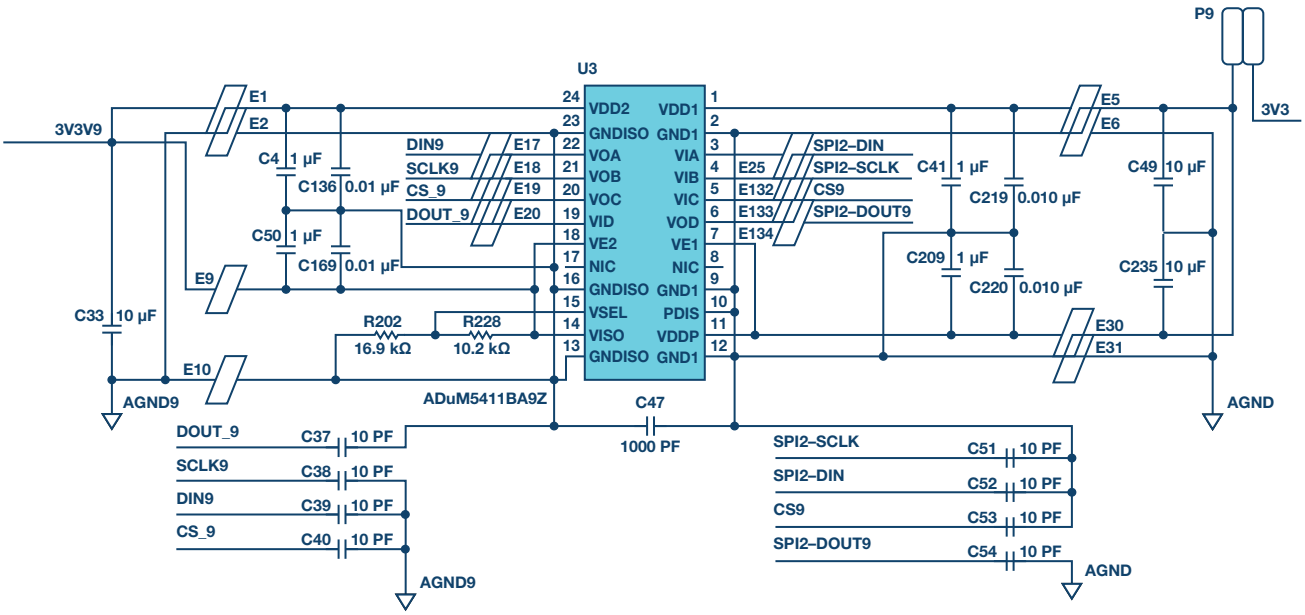

Figure 6. ADuM5411 schematic.

Capacitance can also be used to provide a low impedance return path, thus reducing emissions. One method to do this is to use a surface-mounted safety rated capacitor crossing the barrier, guaranteed to meet standards for creepage, clearance, and withstand voltage. These capacitors are available from suppliers like Murata or Vishay. This method is only effective up to around 200 MHz, though, due to the inductance introduced by mounting the capacitor. For this reason, a more effective technique is to build a stitching capacitance internal to the PCB under the ADuM5411. This could be a floating stitching capacitor or an overlapping stitching capacitor, as shown in Figure 7.

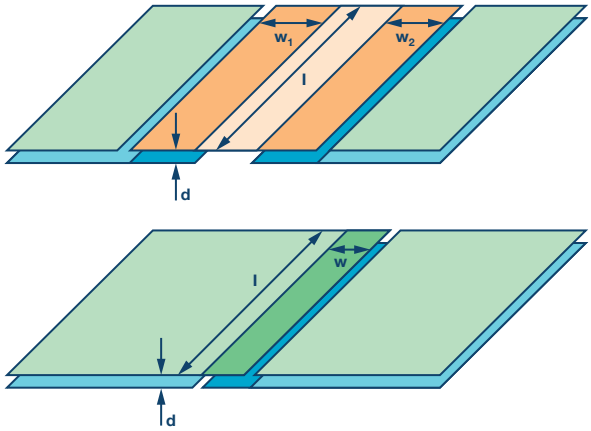

Figure 7. Floating stitching capacitor and overlapping stitching capacitor.

For the floating stitching capacitor, two serial capacitors are built in, C1 and C2. The total capacitance is calculated by Equation 1.

$$C = \frac{C1 \times C2}{C1 + C2},\ C1 = \frac{lw_1\varepsilon}{d},\ C2 = \frac{lw_2\varepsilon}{d}$$

where:
ε is the permittivity of the PCB insulation material, 4.5 for FR4 material.

For the overlapping stitching capacitor, the capacitance is calculated by Equation 2.

$$C1 = \frac{lw\varepsilon}{d},\ \varepsilon$$

where:
ε is the permittivity of the PCB insulation material, 4×10^{-1} 1 F/m for FR4 material.

With the same material, area, and distance, the total capacitance value of floating stitching is half that of the overlapping stitching, but the thickness of the insulation material is doubled. Reinforced insulation, per IEC60950 2.10.6.4, requires 0.4 mm (15.74 mils) minimum insulation material thickness in the interior layers, but basic insulation has no such requirement. As the ADuM5411 only provides 2.5 kV rms basic isolation, an overlapping stitching capacitor was chosen to maximize the capacitance. The thickness of the interior layers has also been controlled to 5 mils for the same reason.

The 16-channel, channel-to-channel temperature input module PCB uses a 6-layer board. To maintain mechanical and EMI performance, the top and bottom layers were controlled to 20 mils and interior layers to 5 mils, as per Figure 8.

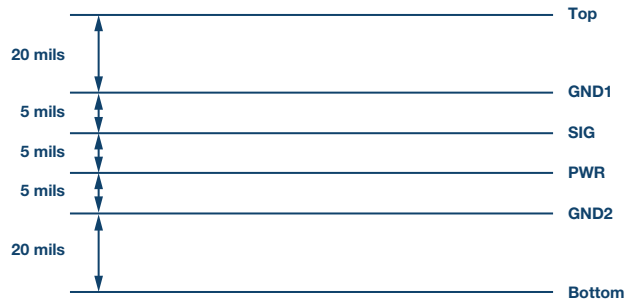

Figure 8. Six-layer PCB stack assignment.

As per Figure 9, the overlap stitching capacitors' planes are built in the GND1, SIG, PWR, and GND2. The planes on GND1 and PWR are connected to the ADuM5411's secondary side and the planes in the SIG and GND2 are connected to ADuM5411's primary side. This means three parallel stitching capacitors are formed between GND1 and SIG, SIG and PWR, PWR and GND2. The width of the overlap area is 4.5 mm, and the length is 17 mm, meaning the total stitching capacitance is 72 pF.

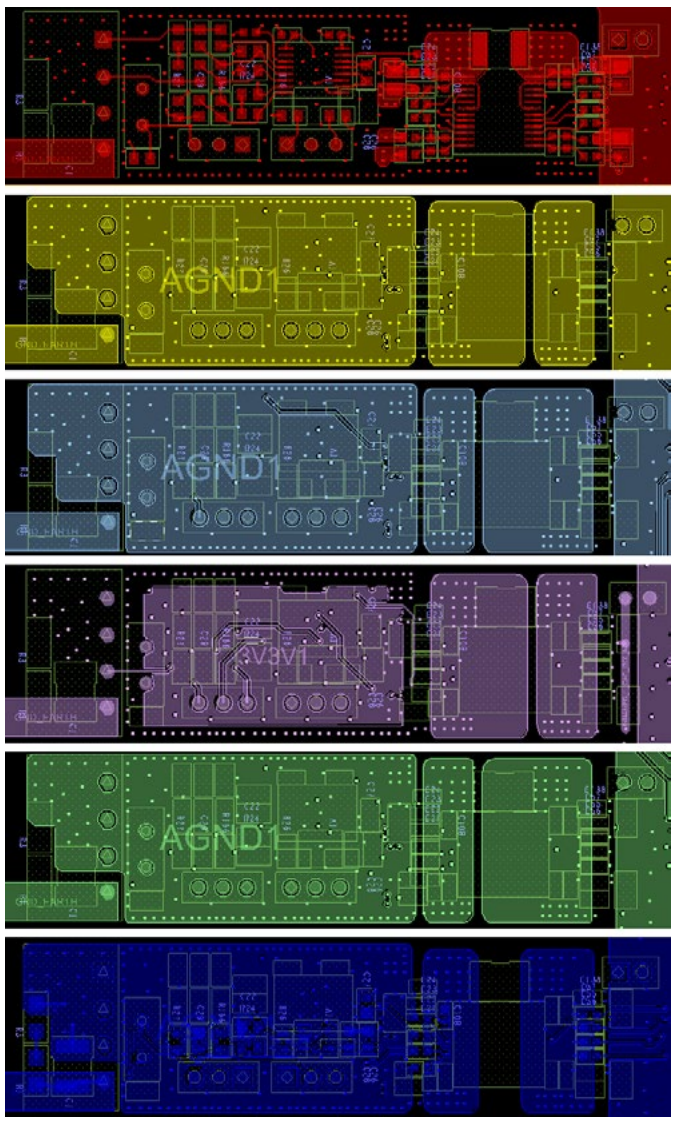

Figure 9. Six-layer PCB layout of the ADuM5411 area.

Test Results Against the EN55022 Specification

Two sets of EMI tests were performed at 10 m, as per the EN55022 specification. For the first test, a board with stitching capacitance was used, as shown in Figure 10. Figure 11 shows the results—it passed the EN55022 Class B standard with about 11.59 dB margin. For the second test, a board with no stitching capacitance was used, and, instead, external safety capacitors, KEMET C1812C102KHRACTU 3 kV, 150 pF, were mounted on the board. Figure 12 shows the results—it passed the EN55022 Class B standard with 0.82 dB margin.

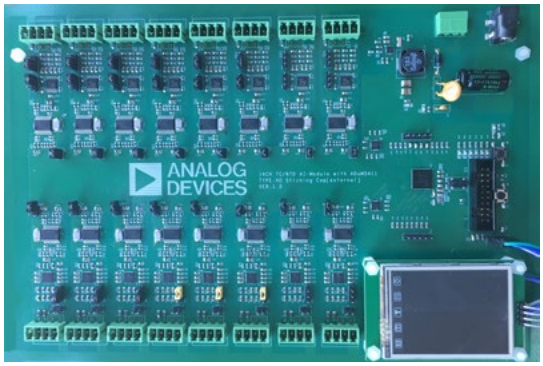

Figure 10. Stitching capacitors built into the PCB without safety capacitors.

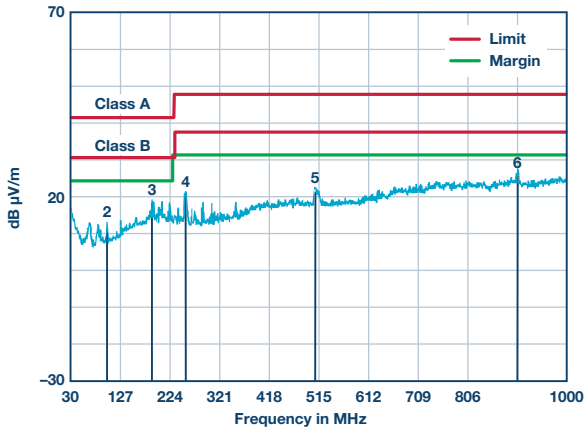

Figure 11. Stitching capacitors built into PCB EN55022 Class B test result.

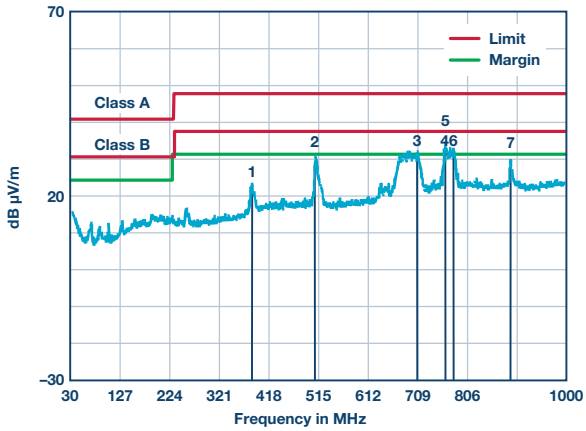

Figure 12. The no stitching capacitance, but with safety capacitors PCB, EN55022 Class B test result.

The results proved that stitching capacitors under the IC is a more effective decoupling method than the safety capacitors.

Conclusion

Channel-to-channel isolation is often viewed as a design challenge in high end process control systems. ADI's *iso*Power technology and *i*Coupler technology enables significant increases in channel density over traditional digital and power isolation approaches. They also greatly simplify the design task and can improve channel robustness and reliability. With stitching capacitor built into the PCB, or safety capacitor mounted aside the PCB, EMI radiation can be easily controlled to pass EN55022 Class B or Class A. It's a breakthough in technology.

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Also by this Author:

PLC Evaluation Board Simplifies Design of Industrial Process Control Systems

Next-Generation SAR ADC Addresses Pain Points of Precision Data Acquisition Signal Chain Design

By **Maithil Pachchigar** and **Alan Walsh**

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Introduction

Many applications require a precision data acquisition signal chain in order to digitize analog data so that it can be collected and processed accurately. Precision system designers are continually pressed to find innovative ways to improve performance and reduce power dissipation while accommodating increased circuit density in a small PCB footprint. This article discusses the common pain points encountered in designing a precision data acquisition signal chain and how to address them using the next generation of 16-/18-bit, 2 MSPS, precision successive approximation register (SAR) ADCs. Designed using ADI's advanced technology, the AD4000/AD4003 (16-/18-bit) ADC incorporates ease of use features that offer a multitude of system-level benefits that help to lower the signal chain power, reduce signal chain complexity, and enable higher channel density while pushing the performance level higher. This article will highlight data acquisition subsystem performance and design challenges and explain how this ADC family creates application level impact in multiple end markets.

Common Signal Chain Design Pain Points

Figure 1 shows a typical signal chain used in building precision data acquisition systems. Applications that require precision data acquisition systems such as automated test equipment, machine automation, industrial, and medical instrumentation have common trends that are typically considered technically conflicting. For example, system designers are forced to make performance trade-offs to keep a tight system power budget or small area on the board to achieve high channel density. System designers of these precision data acquisition signal chains face common challenges in terms of driving the SAR ADC inputs, protecting ADC inputs from overvoltage events, reducing the system power with single supplies, and achieving higher system throughput with low power microcontrollers and/or digital isolators.

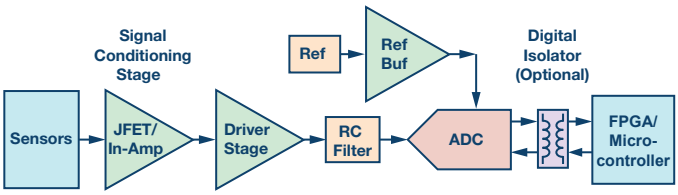

Figure 1. Typical precision data acquisition signal chain.

Driving high resolution precision SAR ADCs has been traditionally a tricky issue because of the switched capacitor inputs. System designers need to pay close attention to the ADC driver data sheet and look at the noise, distortion, input/output voltage headroom/footroom, bandwidth, and settling time specifications. Typically, high speed ADC drivers are required that are wide bandwidth, low noise, and high power in order to settle the switched capacitor kickback of the SAR ADC inputs within the available acquisition time. This significantly reduces the options available for amplifiers to drive the ADC and results in significant performance/power/area trade-offs. Furthermore, selecting an appropriate RC filter to place between the driver and the ADC inputs imposes further constraints on amplifier choice and performance. The RC filter between ADC driver output and SAR ADC input is required to limit wideband noise and reduce the effects of charge kickback. Typically, the system designer needs to spend significant time to evaluate the signal chain to ensure that the selected ADC driver and RC filter can drive the ADC to achieve a desired performance.

In power sensitive applications like battery-powered instrumentation, it is often desirable to run the system from a single low voltage supply. This minimizes the power dissipation of the circuitry but introduces issues with headroom and footroom for the amplifier front end. This means it may not be possible to use the full ADC input range because the driving amplifier cannot drive all the way to ground or all the way to the upper end of the ADC input range, reducing the performance of the overall system. This can be remedied by increasing the supply voltage at the cost of higher power dissipation or accepting the lower dynamic range performance from the system.

Most ADC analog inputs, IN+ and IN–, have no overvoltage protection circuitry apart from ESD protection diodes. In applications where the amplifier rails are greater than V_{REF} and less than ground, it is possible for the output to go outside the input voltage range of the device. During an overvoltage event, the ESD protection diode between either analog input (IN+ or IN–) pin to REF forward biases and shorts the input pin to REF, potentially overloading the reference, causing damage to the device, or disturbing a reference that is shared among multiple ADCs. This results in having to add protection circuitry like Schottky diodes to the ADC input to prevent overvoltage conditions from harming the ADC. Unfortunately, Schottky diodes could add distortion and other errors due to leakage currents.

Precision applications have different needs in terms of the processors that interface to the ADC. Some applications need to be electrically isolated for safety reasons and use digital isolators between the ADC and processor to achieve this. This choice of processor or need for isolation puts constraints on the efficiency of the digital interface used to connect with the ADC. Typically, lower end processors/FPGAs or lower power microcontrollers have relatively low serial clock rates. This can result in lower than desired throughput from the ADC because of a long ADC conversion time delay before the conversion result can be clocked out. Digital isolators can also limit the maximum serial clock rate that can be achieved across the isolation barrier due to propagation delays in the isolator limiting the ADC throughput. In these scenarios an ADC that can achieve a higher throughput rate without a significant increase in serial clock rate is desirable.

AD4000/AD4003 Precision SAR ADC Family Solves Common Design Challenges

The AD4000/AD4003 family is a fast, low power, single-supply, 16-/18-bit precision ADC based on a SAR architecture.

The AD4000/AD4003 precision ADC family uniquely combines high performance with ease of use features that reduce system complexity, simplify signal chain BOM, and significantly decrease time to market (see Figure 2). This family enables designers to solve the system-level technical challenges for their high precision data acquisition system without making significant trade-offs. For example, a combination of a long acquisition phase, high input impedance (Z) mode, and span compression mode of the AD4000/AD4003 ADC family reduces the design challenges associated with the ADC driver stage and increases the flexibility in ADC driver selection. This enables overall lower system power, higher density, and reduced customer design cycle time. Most of the ease of use features can be enabled/disabled through writing to the configuration register via an SPI interface. Note that AD4000/AD4003 ADC family is pin-compatible with the 10-lead AD798x/AD769x ADC family.

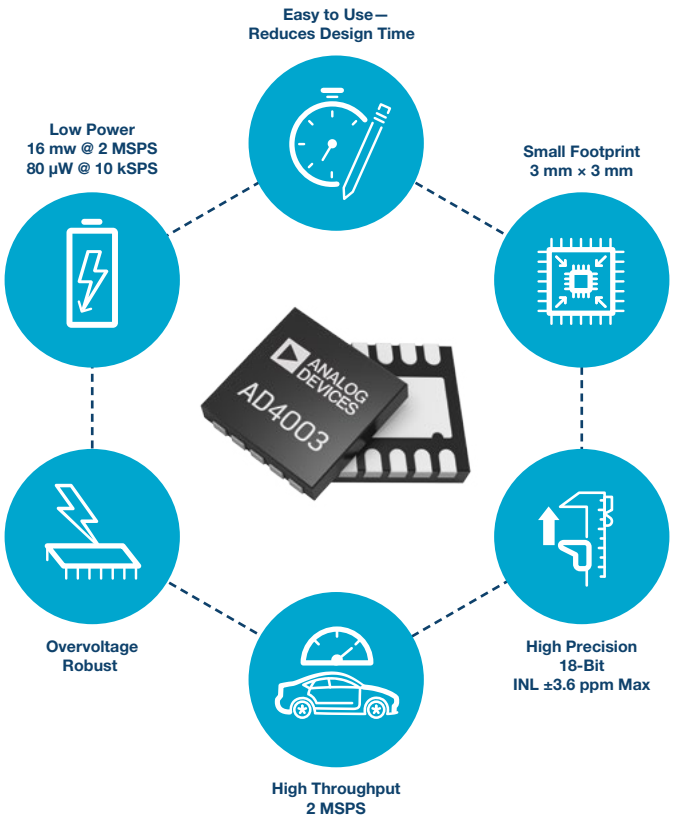

Figure 2. AD4000/AD4003 ADC key benefits.

AD4000/AD4003 ADC Ease of Use Features

Long Acquisition Phase

The AD4000/AD4003 ADC features a very fast conversion time of 290 ns and the ADC returns back to the acquisition phase 100 ns before the end of the ongoing conversion process. SAR ADC cycle time is comprised of conversion and acquisition phases. During the conversion phase, the ADC capacitor DAC is disconnected from the ADC inputs to perform the SAR conversion. The inputs are reconnected during the acquisition phase, and the ADC driver must settle the inputs to the correct voltage before the next conversion phase begins. A longer acquisition phase reduces the settling requirement on the driving amplifier and allows a lower RC filter frequency cutoff, which means a higher noise and/or lower power/bandwidth amplifier can be tolerated. A larger value of R can be used in the RC filter with a corresponding smaller value of C, reducing amplifier stability concerns without impacting distortion performance significantly. A larger value of R helps to protect the ADC inputs from overvoltage conditions. It also results in reduced dynamic power dissipation in the amplifier.

High Input Impedance Mode

To achieve the optimum data sheet performance from high resolution precision SAR ADCs, system designers are often forced to use a dedicated high power, high speed amplifier to drive the traditional switched capacitor SAR ADC inputs for their precision applications. This is one of the common pain points encountered in designing a precision data acquisition signal chain. The benefits of high-Z mode are low input current for slow (<10 kHz) or dc type signals and improved distortion (THD) performance over an input frequency range up to 100 kHz.

The AD4000/AD4003 ADC incorporates a high-Z mode that reduces the nonlinear charge kickback when the capacitor DAC switches back to the input at the start of acquisition. With high-Z mode enabled, the capacitor DAC is charged at the end of conversion to hold the previously sampled voltage. This process reduces any nonlinear charge effects from the conversion process affecting the voltage that is acquired at the ADC input prior to the next sample.

Figure 3 shows the input current of the AD4000/AD4003 ADC with high-Z mode enabled/disabled. The low input current makes the ADC a lot easier to drive than traditional SAR ADCs available in the market even with high-Z mode disabled. If you compare the input current in Figure 3 with high-Z mode disabled against that of the previous generation AD7982 ADC, the AD4003 has reduced the input current by 4× at 1 MSPS. The input current reduces further to submicroampere range when high-Z mode is enabled. High-Z mode should be disabled for input frequencies above 100 kHz or when multiplexing the input.

With the reduced input current of the AD4000/AD4003 ADC, it is capable of being driven with a much higher source impedance than traditional SARs. This means the resistor in the RC filter can have 10× larger value than traditional SAR designs.

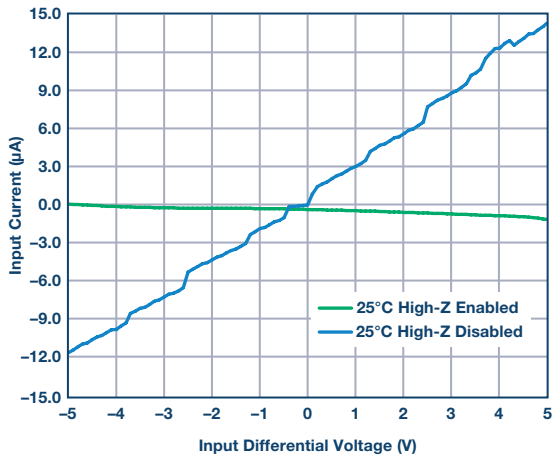

Figure 3. AD4003 ADC input current vs. input differential voltage with high-Z enabled/disabled.

As shown in Figure 4, the AD4000/AD4003 ADC allows a choice of lower power/bandwidth precision amplifiers with a lower RC filter cutoff to drive the ADC, removing the need for dedicated high speed ADC drivers, saving system power, size, and cost in precision, low bandwidth applications (signal bandwidths <10 kHz). Ultimately, the AD4000/AD4003 allows the amplifier and RC filter in front of the ADC to be chosen based on the signal bandwidth of interest and not based on the settling requirements of the switched capacitor SAR ADC inputs.

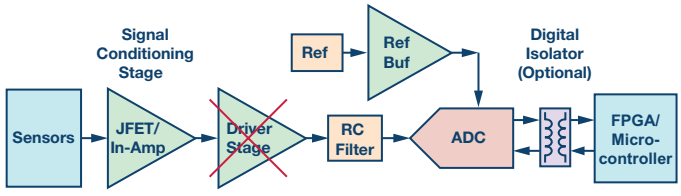

Figure 4. Traditional precision signal chain.

Figure 5 and Figure 6 show the AD4003 ADC's SNR and THD performance using the ADA4077 ($I_{QUIESCENT}$ = 400 µA/amplifier), ADA4084 ($I_{QUIESCENT}$ = 600 µA/amplifier), and ADA4610 ($I_{QUIESCENT}$ = 1.5 mA/amplifier) precision amplifiers when driving the AD4003 ADC at full throughput of 2 MSPS for both the high-Z enabled/disabled cases with various RC filter values. These amplifiers achieve 96 dB to 99 dB typical SNR and better than –110 dB typical THD with high-Z enabled for a 2.27 MHz RC bandwidth and 1 kHz input signal. THD is approximately 10 dB better with high-Z mode enabled even for large R values greater than 200 Ω. SNR holds up close to 99 dB even with a very low RC filter cutoff.

With high-Z enabled, the ADC will consume around 2 mW/MSPS extra power, but this would be still significantly lower than using dedicated ADC drivers like the ADA4807-1 and results in PCB area and bill of material savings. For most systems, the front end usually limits the overall ac/dc performance achievable by the signal chain. It's evident from the selected precision amplifier's data sheet in Figure 5 and Figure 6 that its own noise and distortion performance dominates the SNR and THD specification at a certain input frequency. However, the AD4003 ADC with high-Z mode allows a greatly expanded choice of driver amplifier including precision amplifiers used in signal conditioning stages along with more flexibility in the RC filter choice. For example, when the AD4003 ADC's high-Z is enabled and using the ADA4084-2 driver amplifier with a wideband input filter of 4.42 MHz, the SNR performance is about 95 dB. With more aggressive filtering of the ADC driver's noise using a 498 kHz filter, SNR improves by 3 dB, to 98 dB. The AD7982 ADC's SNR performance at lower RC cutoff is degraded because the ADC input does not settle the kickback within its short acquisition time.

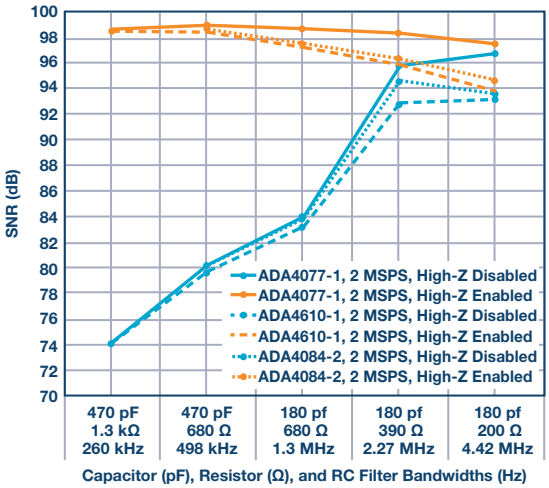

Figure 5. SNR vs. RC bandwidths using ADA4077, ADA4084, and ADA4610 precision amplifiers.

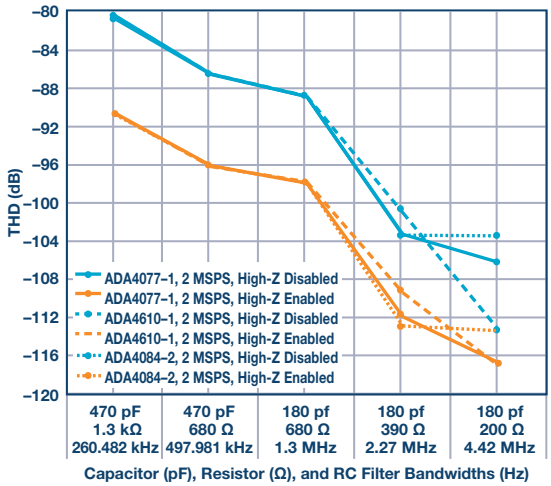

Figure 6. THD vs. RC bandwidths using ADA4077, ADA4084, and ADA4610 precision amplifiers.

Figure 7(a) shows that system designers can use the 2.5× lower power ADC driver ADA4077 (vs. the ADA4807), and the AD4003 ADC still achieves SINAD of about 97 dB (3 dB better than the AD7982 ADC) when high-Z mode is disabled. Even with a wider RC bandwidth of 2.9 MHz, the ADA4077 amplifier cannot drive the AD7982 ADC directly and achieve optimum performance. The driver cannot settle the ADC kickback within the available acquisition time with aggressive filtering at a lower RC bandwidth cutoff and hence the ADC SINAD performance is degraded. The AD4003 ADC's switched capacitor kickback with either high-Z mode disabled or enabled is much reduced and the acquisition time is 2.5× longer at 1 MSPS and hence its SINAD performance is still significantly better than that of AD7982 ADC.

With high-Z mode enabled, the AD4003 ADC's SINAD performance is better using both ADC drivers at lower RC filter cutoff, which helps remove more wideband noise coming from the upstream signal chain components when the signal bandwidth of interest is low. Without high-Z mode enabled there is a trade-off between RC filter cutoff and SINAD performance.

Span Compression

The AD4000/AD4003 ADC includes a span compression mode, which is useful for systems that only have a single positive supply to power the SAR ADC drivers. It eliminates the ADC driver's need for a negative supply while preserving the full resolution of the ADC, saving power and reducing power supply design complexity. As shown in Figure 8, the ADC performs a digital scaling function that maps zero-scale code from 0 V to 0.1 V ×

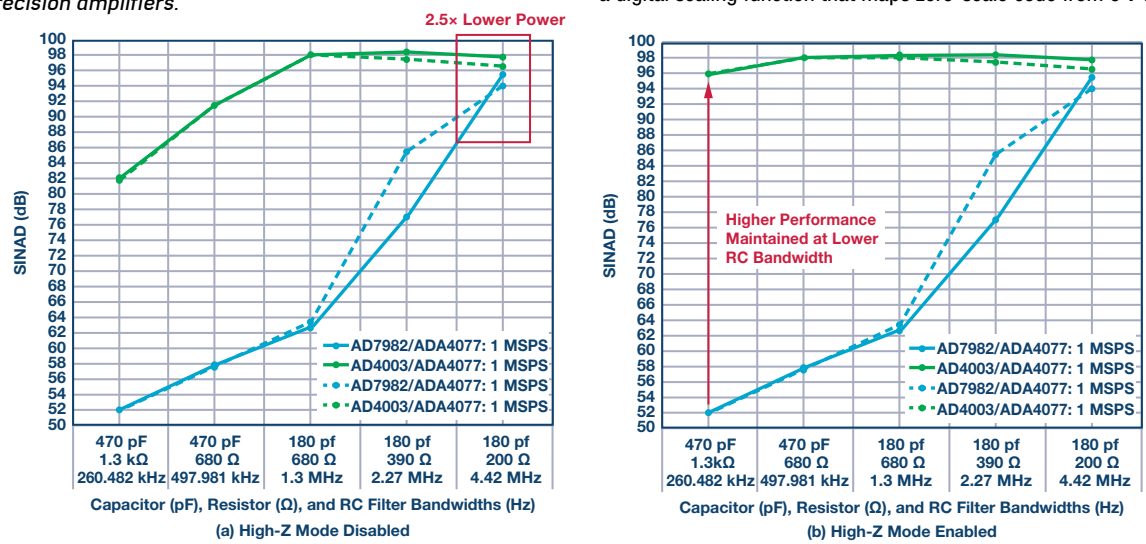

Figure 7. AD4003 ADC and AD7982 ADC amplifier driver comparison using ADA4077 and ADA4807: SINAD vs. RC bandwidths for high-Z mode disabled and enabled (F_S = 1 MSPS, f_{IN} = 1 kHz).

V_{REF} and full-scale code from V_{REF} to 0.9 × V_{REF}. The AD4000/AD4003 ADC's SNR takes a hit of about ~1.9 dB (20×log(4/5)) for the reduced input range. As an example, for a subsystem operating from a single 5 V supply and a typical reference voltage of 4.096 V, the full-scale input range is now ~0.41 V to 3.69 V, which provides adequate headroom for powering the driving amplifier.

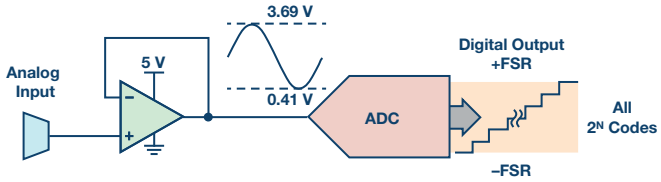

Figure 8. AD4000/AD4003 ADC span compression operation.

Overvoltage Clamp

In applications where the amplifier rails are greater than V_{REF} and less than ground it is possible for the output to violate the input voltage range of the part. When positive input is over-ranged, current flows through D1 into REF (see Figure 9), disturbing the reference. Even worse it could pull the reference above the absolute maximum reference value and hence could damage the part.

When the analog input exceeds the reference voltage by ~400 mV, the AD4000/AD4003 ADC's internal clamp circuit will turn on and the current will flow through the clamp into ground, preventing the input from rising further and potentially causing damage to the device.

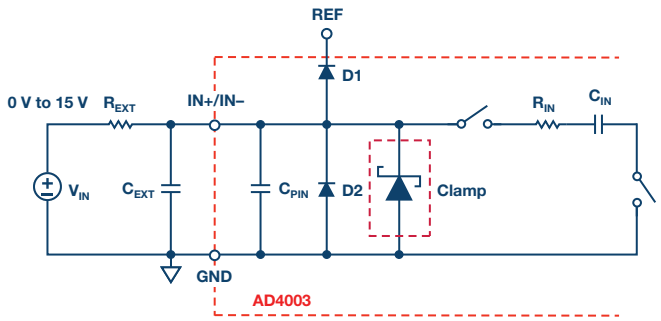

Figure 9. AD4003 ADC equivalent analog input circuit.

As shown in Figure 9, the AD4000/AD4003 ADC's internal overvoltage clamp circuit with a larger external resistor (R_{EXT} = 200 Ω) eliminates the need for external protection diodes (and hence the need for additional board space). The clamp turns on before D1 and can sink up to 50 mA of current. The clamp prevents damage to the device by clamping the input voltage to a safe operating range and avoids disturbance of the reference, which is particularly important for systems that share the reference among multiple ADCs.

Efficient Digital Interface

The AD4000/AD4003 ADC has a flexible digital serial interface that offers seven different modes with register programmability. Its turbo mode allows the user to start clocking out the previous conversion results while the ADC is still converting, as shown in Figure 10. A combination of short conversion time and turbo mode allows a lower SPI clock rate and simplifies the isolation solution, resulting in reduced latency requirements on digital isolators and broadening a choice of processors including lower end processors/FPGAs or low power microcontrollers with relatively low serial clock rates. For example, the AD4003 ADC can use a 2.5× slower SPI clock rate (25 MHz vs. 66 MHz) than the AD7982 ADC when running at 1 MSPS. The user can write/read back the register bits to enable the AD4000/AD4003 ADC's ease of use features and a 6-bit status word can be appended to the conversion result that allows diagnosis along with register read back. The serial interface is completely specified down to 1.8 V logic levels and can achieve the full 2 MSPS throughput under these conditions. A minimum SCK rate of 75 MHz is required to run the AD4003 ADC at 2 MSPS with turbo mode enabled.

AD4000/AD4003 ADC Performance

Operating from a 1.8 V supply, the AD4000/AD4003 ADC consumes typically 14 mW/16 mW at 2 MSPS and offers superior linearity of ±1.0 LSB (±3.8 ppm) max and guaranteed 18 bits no missing codes. Figure 11 shows the AD4003 ADC's typical INL vs. code performance. The AD4003 ADC achieves better SINAD performance than the AD7982 ADC over a wide range of input frequencies up to Nyquist (Figure 12), enabling system designers to develop wider bandwidth, higher precision instrumentation equipment. The AD4000/AD4003 ADC is available in a small 10-lead footprint (3 mm × 3 mm, LFCSP and 3 mm × 5 mm, MSOP options), and is pin-compatible with the AD798x/AD769x ADC family.

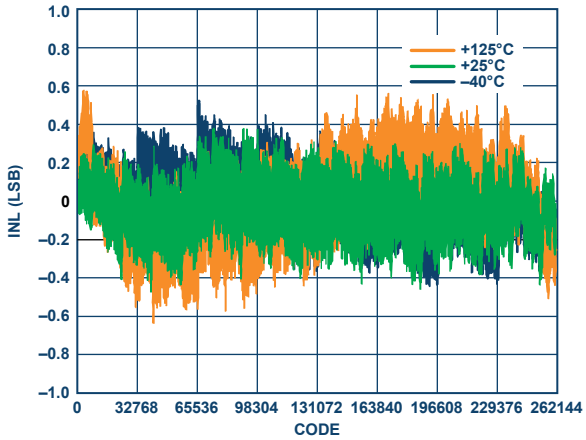

Figure 11. AD4003 ADC INL vs. code.

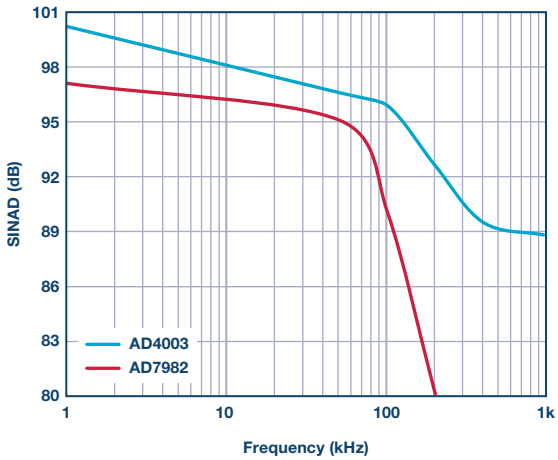

Figure 12. AD4003 ADC vs. AD7982 ADC SINAD vs. input frequency.

The AD4000/AD4003 ADC powers down automatically at the end of each conversion phase; therefore, its power scales linearly with the throughput as shown in Figure 13. This feature makes the device ideal for low sampling rates (even down to a few Hertz) and battery-powered portable and wearable systems. Even in low duty cycle applications, the first conversion result is always valid.

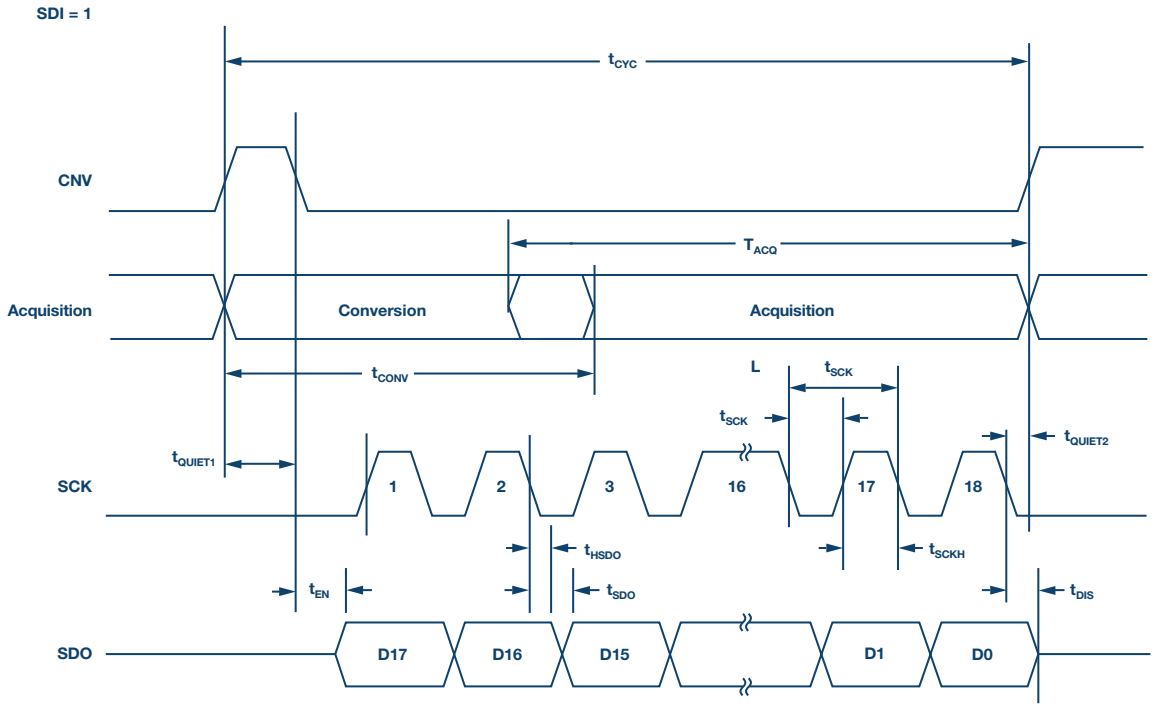

Figure 10. AD4003 ADC's turbo mode operation.

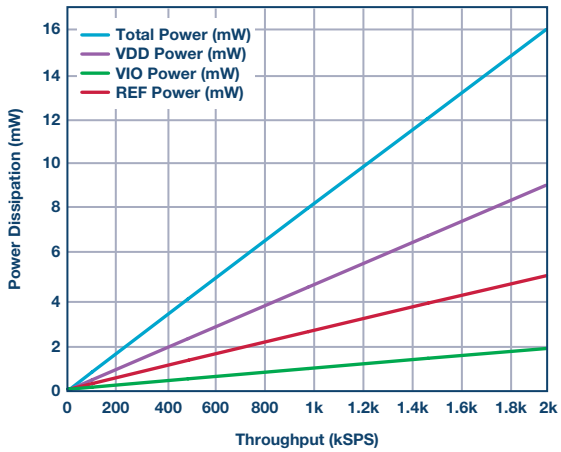

Figure 13. AD4003 ADC power dissipation vs. throughput.

System Applications

A combination of ease of use features and high performance, small footprint, and low power makes the AD4000/AD4003 ADC family a great solution for many precision control and measurement system applications as shown in Figure 14. The AD4000/AD4003 ADC reduces measurement uncertainty, increases repeatability, allows high channel density, and increases the throughput efficiency of automated test equipment, automated machine control equipment, and medical imaging equipment. This ADC is a good fit for systems that demand higher frequency performance to capture fast transients and time of flight information, such as power analyzer and mass spectrometer applications.

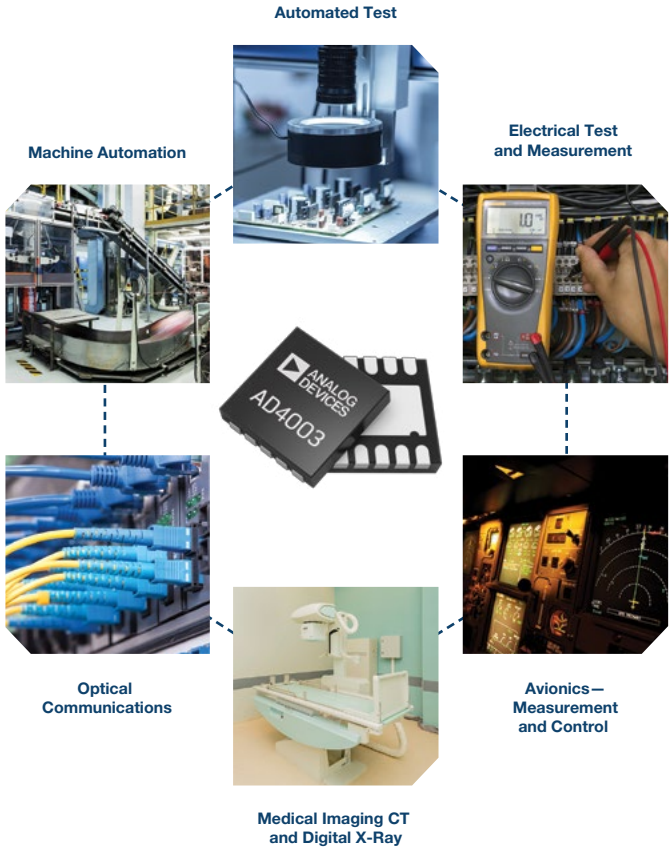

Figure 14. AD4000/AD4003 ADC end system applications.

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Rarely Asked Questions—Issue 136 Precision Current Outputs Are Easy to Make

By **James Bryant**

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Question:

How do I design a circuit with an accurate current output into a nonlinear load resistance?

Answer:

It's easy to make current output devices. A number of simple circuits can deliver unipolar constant current into a varying or nonlinear load. Bipolar circuit options are more limited, although still quite simple.

I recently needed power for some LED lamps. Several engineer friends thought that I would have trouble making the variable current supply that is needed to allow them to be dimmed. In fact, I quickly modified some black brick laptop power supplies (bought for pennies at a car boot sale) to do the job.[1]

If the input to the amplifier is also a stiff current source (that is, a current whose value does not vary with loading), a current mirror using two matched bipolar junction transistors (BJTs), on a single chip to ensure temperature matching, is often all that is needed. The current is applied to both bases and one collector, the two emitters are grounded and an equal current flows in the other collector—slightly more complex arrangements may improve performance but the basic circuit is often adequate.

It is far easier to obtain matched NPN BJTs than matched PNPs, although the latter are available. A current mirror of a current from positive supply to a grounded source with the mirrored current to a grounded load may be made with matched PNP transistors—but there are also a couple of fast current mirrors with a dynamic range of 10^6 (1,000,000:1), the ADL5315, and ADL5317.[2]

For a voltage input you simply need an op amp, a transistor (FET or BJT), and a resistor. The input is applied to the op amp noninverting input, the op amp drives the transistor gate/base, the resistor is connected to ground, and to the op amp inverting input and the source/emitter, and the output current flows in the drain/collector.

These circuits are normally grounded and their load is connected to a dc supply. Whether NPN/N-channel or PNP/P-channel devices are necessary depends on the supply polarity. If the current must drive a grounded load the circuit may be connected to the supply rail—but the signal input will require level shifting.[1]

If a bipolar current output is required, a standard voltage amplifier (probably an op amp) is used to drive the load through a small current sense resistor. Negative feedback to the amplifier is taken from a current sensing amplifier connected across this resistor. The supply voltage must be large enough to drive the maximum expected current into the maximum load under worst-case load bias conditions.

If a circuit requires a fixed current load despite varying voltage, a very simple (but not very stable with temperature) two terminal constant current device may be made from a depletion-mode JFET with a resistor connected between its source and its gate—the gate and the drain are the two terminals (with an N-channel JFET the drain is positive, with a P-channel one it's negative). The current is set by adjusting the resistor.

The short article mentioned below describes the circuits mentioned above in more detail, and with diagrams, but the basic principles of accurate current output amplifiers are simple.[1]

When I started to write this article I was going to describe how a precision two terminal floating current source could be built with an op amp, a precision voltage reference, three resistors, and a capacitor, but since Analog Devices and Linear Technology have announced that they are

merging, I'll recommend an integrated solution. Linear Technology has two such devices, ready-made, in their catalog—I have used them in my personal projects for some years but have not, of course, mentioned them in my articles for Analog Devices. I am very pleased that now I am able to do so.

They are actually three terminal devices—an external resistor between the negative supply and a reference pin and another between the negative output and the negative supply define the current. The LT3092[3] works from 500 µA to 200 mA, and the LT3083[4] from 500 µA to 3 A.

References

[1] James Bryant. "Current-Output Circuit Techniques Add Versatility to Your Analog Toolbox." *Analog Dialogue*, Apr 2014. Analog Devices, Inc.

[2] AD5315 data sheet/AD5317 data sheet. Analog Devices, Inc.

[3] LT3092 data sheet. Linear Technology.

[4] LT3083 data sheet. Linear Technology.

James Bryant [james@jbryant.eu] was a European applications manager at Analog Devices from 1982 to his retirement in 2009 and still writes and consults for the company. He holds a degree in physics and philosophy from the University of Leeds and is also C.Eng., EurEng., MIET, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

James Bryant

Also by this Author:

Who Killed the Component?

Volume 50, Number 4

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Conclusion

The AD4000/AD4003 ADC family enables designers to solve the system-level technical challenges for their high precision data acquisition system without making significant trade-offs, reducing the total system design time. The AD4000/AD4003 ADC's high performance increases measurement accuracy and its small footprint coupled with low system-level thermal dissipation enables higher density.

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Also by this Author:

Integrated Multiplexed Input ADC Solution Alleviates Power Dissipation and Increased Channel Density Challenges

Volume 50, Number 1

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Also by this Author:

Front-End Amplifier and RC Filter Design for a Precision SAR Analog-to-Digital Converter

Volume 46, Number 4

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