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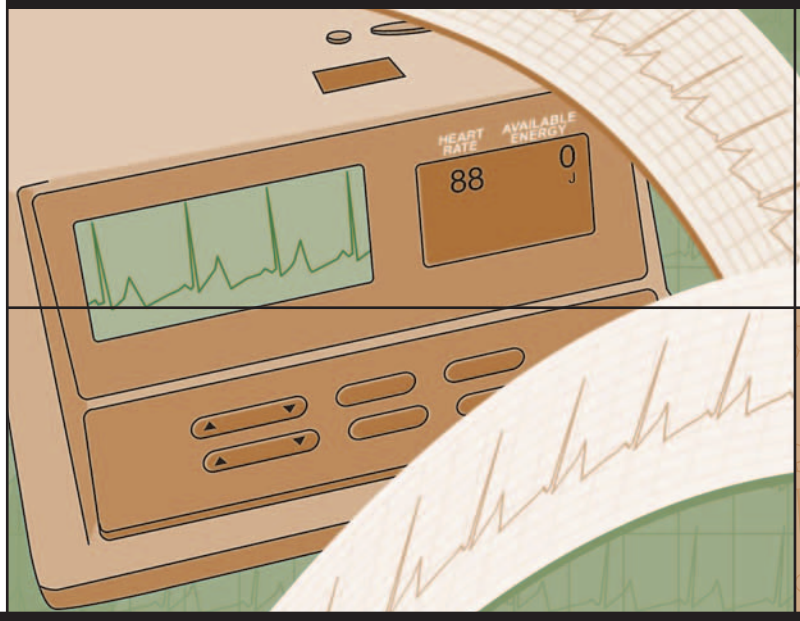
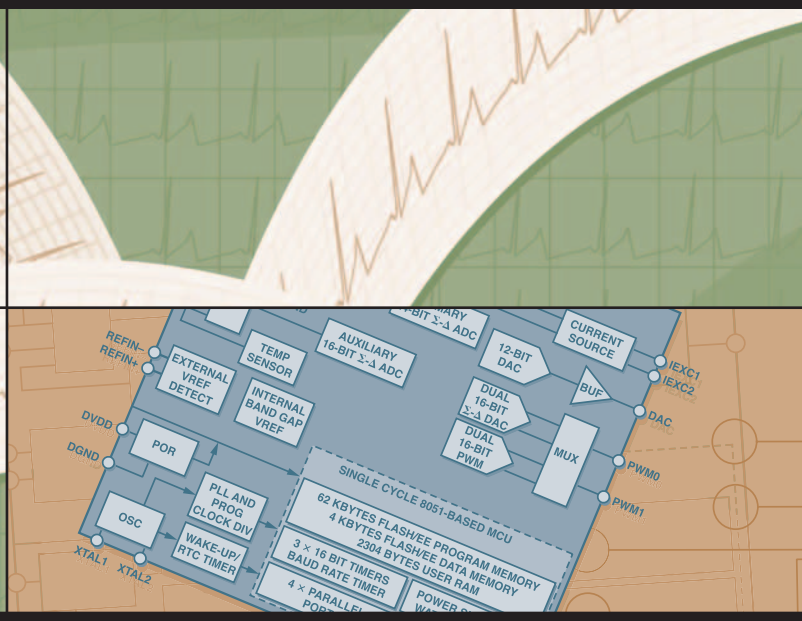
A forum for the exchange of circuits, systems, and software for real-world signal processing





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Editor's Notes

THEN AND NOW REVISITED

As 2003 transits into 2004, the article on page 3 brings to mind an article by one W. Paterson,[1] appearing in the December 1963 *Review of Scientific Instruments*—just 40 years ago—describing (for the first time, in our recollection) ways of generating logs and antilogs, and performing multiplication, by combining the natural characteristics of transistor junctions with the ability of op amps to sink current while maintaining a virtual ground. His perceptiveness was confirmed very soon thereafter in a paper by J. Gibbons and H. Horn,[2] published in the September 1964 *IEEE Transactions on Circuit Theory*, pointing out that the logarithmic relationship was usable over a range of at least nine decades.

These papers, and the subsequent manifestations of brisk creative activity in the field, culminated in Barrie Gilbert's 1975 landmark summation on *translinear circuits*,[3] published in *Electronics Letters*. The ideas it brought together became the foundation for whole generations of IC multipliers/dividers, log-ratio and rms devices, modulators, variable-gain amplifiers, automatic gain controls, gain- and phase meters, and more. This fallout is all documented in silicon-era patents, books, journals, and advertisements—as well as hardware embedded just about anywhere analog electronics has penetrated.

This wealth of functional capabilities was made possible by continued improvements in solid-state theory (now a long way from the "cats' whiskers" of the early 20th century) and the processing of silicon ingots and wafers. But for anyone growing up in the present era, it's hard to believe that, before the '60s, the "solid" foundation for the era of *electronics*—in which radio communications, radar, cinema, television, and automatic-control electronics were developed—was the flow of electrons through a *vacuum* (or of ions in a gaseous medium).

It was an era of low efficiencies, room-warming equipment, plentiful low-cost energy, vast military spending, with a generation of engineers and technicians inured to the routine use of ±300-volt power supplies. It was hard to believe, other than in dreams, that the future would involve miserly husbanding of energy, imploding price and size of electronic devices (and exploding functional density), and a mindset in which circuits using *±15-volt supplies* are considered to be energy-guzzling dinosaurs. The vocabulary of size reduction has devolved from tube-era "miniaturization" to "microcircuits" towards *nanocircuits*.

Op amps and analog computers: In 1963, at the time when increased awareness of silicon's vast repertoire of expected applications coincided with the initial availability of viable solid-state forms, the *operational amplifier*—as a low-cost, easy-to-handle, differential-input plug-in modular vacuum-tube device—had been on the market for a mere 10 years. The first appearance of the "operational" circuit architecture, as an element that made analog computer systems feasible, had been made only a dozen years before that, during World War II. Yet the op amp, a prime beneficiary of the solid-state era, was now ready to come into its own as a near-universal functional circuit block. Solving problems in the design of the op amp itself would imbue much of electronic circuit design with a large measure of *predictability*.

Electronic analog computers, in their heyday (the 1940s and '50s), were usually defined as a set of operational building blocks so interconnected as to model the behavior of a physical system (thermal, mechanical, chemical, nuclear). The model was an alternative electrical system whose performance is described by the same set of equations (with appropriate scale factors) that governs the performance of the system they are modeling. Analog and (later) digital I/O structures provided for any necessary services: initial conditions, driving functions, interconnection programming, calibration, display, etc.

When analog computers with adequate bandwidth were scaled so as to enable complete repetitive solutions, plotted on an oscilloscope or a raster display, the effects of adjusting system parameters were immediately visible—very helpful in seeing interrelationships among the variables, curing stability problems, optimizing parameters, and developing a description of system behavior in the time domain. When scaled to actual "real time," they could be used to simulate portions of systems whose parameters were inconvenient to adjust. For systems with stable continuous behavior, conveniently scaled frequency-response studies (and now FFTs) could be performed as if the model were the actual system. Nowadays digital computers, teamed up with analog, data-conversion, and DSP circuitry, can run rings around those paragons of yesteryear—but one must remember that, when vacuum-tube analog assemblages (like the dinosaurs) ruled the computer world, terms like "transistor" and "software" (like the humans) had not yet been created.

The basic *linear* unit operations of an electronic analog computer are *addition*, *coefficients* (gains/attenuations), and *integration* with respect to time. *Nonlinear* relationships are handled by associating or replacing linear coefficients with a block embodying (with vacuum-tube-diode circuitry, at that time) the appropriate nonlinear output/input relationship—such as hard nonlinearities (limits and dead zones), linear hysteresis, squaring, and square-rooting. The most stable way of implementing smooth functions (and multiplication) was by the piecewise-linear use of arrays of biased (vacuum-tube) diodes, with individually adjustable gains.

Little did we know that, within a couple of decades, a few silicon junctions, replacing and far surpassing multiple vacuum-tube diodes in versatility and stability, would enable the designer to create predictable and stable nonlinearities, even (especially!) the analog-era designer's *bête noire*, the *multiplier*. But that's a story for another time and place.

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Please join me in celebrating Dan Sheingold's 35th anniversary at Analog Devices. As Editor, Dan has succeeded in turning *Analog Dialogue* into the premier technical journal of the semiconductor industry, leading it from humble beginnings to the worldwide online and print readership that it enjoys today. I have had the pleasure of knowing Dan for almost 25 years, and the privilege of working with him for the last five. Here's to the next five!

Scott.Wayne@analog.com

[1] "Multiplication and logarithmic conversion by operational amplifier-transistor circuits," by W. Paterson. *Review of Scientific Instruments* 34-12, December, 1963.

[2] "A circuit with logarithmic transfer response over 9 decades," by J. Gibbons and H. Horn. *IEEE Transactions of the Circuit Theory Group* CT-11-3, September, 1964.

[3] "Translinear circuits: a proposed classification," by B. Gilbert. *Electronics Letters* 11-1, 1975, pp.14-16.

Analog Dialogue

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Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 37 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*online*, monthly at the above URL, and quarterly *in print*, as periodic retrospective collections of articles that have appeared online. In addition to technical articles, the online edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the **www.analog.com** site—the virtual world of *Analog Devices*. In addition to all its current information, the *Analog Dialogue* site has archives with all recent editions, starting from Volume 29, Number 2 (1995), plus three special anniversary issues, containing useful articles extracted from earlier editions, going all the way back to Volume 1, Number 1.

If you wish to subscribe to—or receive copies of—the print edition, please go to **www.analog.com/analogdialogue** and click on **<subscribe>**. Your comments are always welcome; please send messages to **dialogue.editor@analog.com** or to these individuals: *Dan Sheingold*, Editor **[dan.sheingold@analog.com]** or *Scott Wayne*, Managing Editor and Publisher **[scott.wayne@analog.com]**.

Closed-Loop Control of Variable Optical Attenuators with Logarithmic Analog Processing

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Achieving tight channel spacing in *dense wavelength-division-multiplexing* (DWDM) networks calls for precise control of spectral emissions and power. This requires continuous monitoring and adjustment of network elements—such as transmission laser sources, optical add-drops, optical amplifiers, and *variable optical attenuators* (VOAs). These last elements are typically used to adjust power levels across the DWDM spectrum in order to minimize crosstalk and maintain a desired signal-to-noise ratio.

For instance, a VOA can be cascaded with an *erbium-doped fiber amplifier* (EDFA) to help equalize the amplifier's non-uniform gain-versus-wavelength profile, improving linearity and enhancing control of the overall system. Recursive measurement-and-control algorithms can be used to provide quick and accurate dynamic closed-loop control, which ensures repeatability and minimizes production calibration and trimming. Logarithmic-amplifier front ends condition the wide-range input signal, thus allowing lower-resolution, lower-cost signal-processing components to be used downstream.

Classic Mixed-Signal Solutions

Classic solutions have combined linear *transimpedance amplifiers* (TIAs) and high resolution signal processing to measure and control the absorbance of the VOA. This, at first, seems like an attractive solution due to the low cost of the TIA front end. The TIA is linear, however, so calculating the decibel (logarithmic) attenuation across the VOA requires post-processing of the measured signal. Performed digitally, this requires floating-point processors to cope with the division and exponentiation processes involved in the calculation. Alternatively, integer-based processing can be performed—using exhaustive look-up tables that were generated during production calibration. Both approaches typically require analog-to-digital converters with at least 14-bit resolution, and moderately high processor speeds, to minimize measurement latency resulting from the inherent processing overhead. The cost advantage sought in selecting the linear TIA front end is often swamped by the cost of the higher priced converters and processors needed to acquire the measurement signal and compute the attenuation. Additional cost (and production delay) is incurred if lengthy look-up tables need to be generated during production testing.

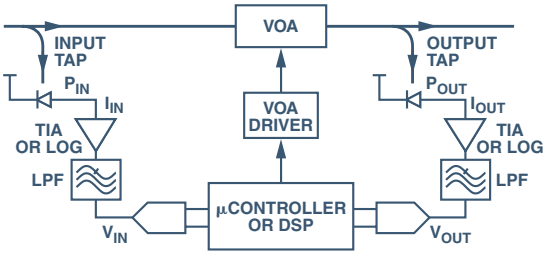

Figure 1. VOA adaptive control loop. Input and output optical taps are used to measure the attenuation of the VOA. The measured signal is compared to a desired setpoint level using an error integrator, implemented in software. The difference signal is used to control the attenuation of the VOA, yielding a closed-loop design.

Adaptive Control of a Variable Optical Attenuator

Figure 1 illustrates this classic solution applied around an adaptively controlled VOA. The amplified signal is low-pass filtered to help reduce measurement noise. The filtered signal is then digitized and the absorbance of the attenuator is computed.

If linear amplification is used to convert the measured photocurrents to proportional voltages, it will be necessary to calculate the ratio of the measured signals, followed by inverse exponentiation, and multiplication to compute the VOA's actual absorbance.

$$\alpha = 10\log\left(\frac{P_{IN}}{P_{OUT}}\right) \tag{1}$$

If the responsivities and transimpedance gain of the detector front ends are equal, then

$$\alpha = 10\times\log\left(\frac{\frac{I_{IN}}{\rho}R_{TIA}}{\frac{I_{IOUT}}{\rho}R_{TIA}}\right) = 10\times\log\left(\frac{V_{IN}}{V_{OUT}}\right) \tag{2}$$

where R_{TIA} is the *transresistance* in ohms

ρ is the *responsivity* of the photodiode in A/W

In reality the front end transresistances will not be equal, so additional calibration and correction is required. In a digital solution, in order to provide acceptable precision in calculation, the signal needs to be digitized using analog-to-digital converters (ADCs) with sufficient resolution to preserve a predetermined level of accuracy. The design can operate as a closed loop only as long as the input signal is large enough for the detected signals to be above the noise floor. Variable transresistance may be used to help extend the range of closed-loop operation. When the measured signal levels fall below an acceptable signal level for accurate detection, the VOA must indicate the lack of signal power and operate open-loop, and is no longer able to fulfill the accuracy requirement.

To the Rescue—Translinear Log-Amp Circuits

Published in 1953, the Ebers-Moll equations predicted the inherent logarithmic relationship between the base-emitter voltage (V_{BE}) and the collector current (I_C) of a bipolar transistor.[1] When fabricated on a high quality analog process, this relationship is remarkably accurate over an I_C range of up to 9 decades. Significant advances occurred, starting with the exploitation of the logarithmic properties in the 1960s.[2] A significant landmark was Barrie Gilbert's description of the power(s) inherent in their generalized *translinear* properties.[3] Over the years, the logarithmic and related properties of bipolar junctions have been used to create a variety of wide-range linear and nonlinear devices, including precision multipliers and dividers, rms-to-dc converters,[4] and modulators. They have made possible the compact, wide-range, precision analog solution to be described.

Briefly, over a range of about 9 decades, a BJT exhibits a naturally logarithmic relationship between its collector current and its base-to-emitter voltage,

$$V_{BE} = \frac{kT}{q}\ln\left(\frac{I_C}{I_S}\right) \tag{3}$$

where I_S is the transport saturation current, of the order of 10^{-16} A, k/q is the ratio of Boltzmann's constant to the charge on an electron (1/11,605 V/K), and T is the absolute temperature in kelvins. The thermal voltage, kT/q, is thus simply *proportional to absolute temperature* (PTAT), about 25.85 mV at 300 K. Unfortunately, the current I_S is poorly defined, differing significantly between

separate devices; it is also strongly dependent on temperature, varying by a factor of roughly 10^9 between –35°C and +85°C. A single BJT alone would be a highly impractical log-amp because of these strong temperature dependencies. To make use of BJTs for accurate logarithmic transformations, the temperature dependencies must be nullified.

The *difference* between the base-emitter voltages of a *pair* of BJTs, one operating at the photodiode current, I_{PD}, and the second operating at a reference current, I_{REF}, can be expressed as

$$V_{BE1} - V_{BE2} = \frac{kT}{q}\ln\left(\frac{I_{PD}}{I_{S1}}\right) - \frac{kT}{q}\ln\left(\frac{I_{REF}}{I_{S2}}\right) = \frac{kT}{q}\ln\left(\frac{I_{PD}}{I_{S1}} \times \frac{I_{S2}}{I_{REF}}\right) \quad (4)$$

If the two transistors are closely matched such that they exhibit nearly identical saturation currents, then Equation 4 can be written as

$$V_{BE1} - V_{BE2} = \frac{kT}{q}\ln\left(\frac{I_{PD}}{I_{REF}}\right) = \frac{kT}{q}\ln(10)\log\left(\frac{I_{PD}}{I_{REF}}\right) \quad (5)$$

At an ambient temperature of 300 K, the above equation evaluates to

$$V_{BE1} - V_{BE2} = 59.5\ mV \log\left(\frac{I_{PD}}{I_{REF}}\right) \quad (6)$$

The poorly defined and temperature dependent saturation current, I_S, which appears in Equation 1, has now been eliminated. To eliminate the temperature variation of kT/q, this difference voltage is applied to an analog divider with a denominator that is directly proportional to absolute temperature. The final output voltage is now essentially temperature independent and can be expressed as

$$V_{LOG} = V_Y \log\left(\frac{I_{PD}}{I_{REF}}\right) \quad (7)$$

The logarithmic slope, V_Y, is expressed in *volts per decade*. Typical translinear log-amps such as the ADL5306 and ADL5310 are scaled to provide a nominal 200 mV/decade slope. The logarithmic slope can be increased or decreased with the addition of a simple fixed-gain amplifier or voltage-attenuator network.

When light falls on a photodiode, the resulting photocurrent is directly proportional to the incident optical power in watts. On a decibel scale, the decibels of optical power are proportional to the logarithm of the photocurrent, scaled by the responsivity of the particular photodiode. The decibel power of any photodiode can be written as

$$P_{PD}(dB) = 10\log\left(\frac{P_{PD}}{watt}\right) = 10\log\left(\frac{\frac{I_{PD}}{\rho}}{watt}\right) \quad (8)$$

If the reference current in the denominator of Equation 7 is known, the absolute power incident on the photodiode can be calculated from the V_{LOG} voltage.

$$P_{PD} = \frac{I_{PD}}{\rho} = \frac{I_{REF}}{\rho} \times 10^{\left(\frac{V_{LOG}}{V_Y}\right)} \quad (9)$$

In terms of decibels of optical power

$$P_{PD}(dB) = 10\log\left(\frac{I_{REF}}{\rho} \times 10^{\left(\frac{V_{LOG}}{V_Y}\right)}\right) = 10\log\left(\frac{I_{REF}}{\rho}\right) + 10\frac{V_{LOG}}{V_Y} \quad (10)$$

Using Equation 10 we can solve for the log-voltage in terms of optical power in dB.

$$V_{LOG} = \frac{V_Y}{10}\left(P_{PD}(dB) - P_Z(dB)\right) \quad (11)$$

where

$$P_Z(dB) = 10\log\left(\frac{I_{REF}}{\rho}\right) \quad (12)$$

This provides a linear-in-dB transfer function, allowing a simple straight-line equation to describe the relationship of absolute optical power to the logarithmic output voltage. In practice, the actual reference current value and responsivity of the photodiode will be found through a simple two-point calibration process. By measuring the output voltage for two known values of optical power, the slope and intercept of the straight-line equation can be determined. Then simple subtraction and multiplication can be used to assess the optical power in decibels without the need for the exponentiation process or the exhaustive look-up table that would be required if a linear TIA front end were applied.

If the numerator current is derived from the photocurrent, I_{PD}, of an input tapped detector, and the denominator current, I_{REF}, is the resulting photocurrent after the input signal has passed through an absorptive element, such as a VOA, Equation 7 can then be used to derive the attenuation in terms of the log-voltage.

$$\alpha(dB) = 10\log\left(\frac{P_{PD}}{P_{REF}}\right) = 10\frac{V_{LOG}}{V_Y} \quad (13)$$

A similar expression could be derived for an optical amplifier design, where it is desirable to compute the gain in dB across the amplifier. As before, a simple two-point calibration is used to describe the straight-line equation relating the output voltage to the EDFA gain setting. In this manner, translinear log-amps provide the capability to measure absolute power, optical absorbance, and gain using a simple straight-line approximation.

Recent advances in monolithic integrated-circuit design now allow for the manufacture of translinear logarithmic amplifiers that provide wide-dynamic-range signal compression virtually free from the temperature dependencies inherent in a discrete implementation. The first complete monolithic translinear logarithmic amplifier (log-amp), the AD8304, designed by Barrie Gilbert, was introduced by Analog Devices in January 2002. Since the introduction of the AD8304, logarithmic devices have become available from other semiconductor manufacturers.

Application to a VOA

In a *digitally variable optical attenuator* (DVOA) application, input and output optical taps are used to measure the absolute optical power at the input and output ports. The power measurements can then be processed to compute the absorbance of the DVOA for a particular attenuation setting. Using closed-loop techniques,

the attenuation can be dynamically controlled to maintain a desired level of attenuation based on the input and output power measurements. This mode of operation is called *automatic attenuation control*, or AAC. An alternate mode, *automatic power control* (APC), is necessary when the output power of the DVOA is required to remain at a constant level regardless of input optical power variations (as long as the input level exceeds the desired output level by the minimum insertion loss of the VOA).

In either mode of operation, the loop is typically implemented in the form of a mixed-signal solution, where a digital MicroConverter® is programmed to process the analog inputs and drive the appropriate control signal to maintain the necessary level of attenuation. In a fast control loop, an analog solution may be required in order to eliminate the latency associated with the digital portion of the loop. The circuit described below utilizes the ADL5310 dual translinear logarithmic amplifier, which is capable of interfacing two independent photodiodes for measurement of the absolute power on two separate optical supervisory channels. This device allows for absolute measurement of the output optical signal, while simultaneously providing a measure of the attenuation.

Automatic Attenuation Control and Automatic Power Control

Two buffered outputs can be obtained by utilizing the ADL5310's on-chip op amps. The circuit configuration of Figure 2 makes available a measurement of the absolute power incident on photodiode PD1, as well as a measure of absorbance observed between the two ports. Test results using an uncalibrated VOA are provided in Figure 3. The outputs provide the desired linear-in-dB transfer functions needed for closed-loop analog control. Automatic attenuation and power control can be achieved by applying the appropriate output to a separate error integrator; its output drives the control voltage of the VOA.

The solution in Figure 2 assumes that the individual logarithmic-slopes of each channel are identical. In reality the channel-to-channel slope mismatch could be as high as 5%. This will result in a residual error as the overall power levels change. Over a 5-decade power range, the residual error could be as much as 2.5 dB. This can be acceptable in some situations—where fast all-analog closed-loop control is necessary, and accuracy can be compromised in order to allow a simple hardware solution. In a solution where mixed-signal techniques can provide fast enough response, the residual error could be predicted and minimized by monitoring the absolute power on one detector and using a look-up table for error correction.

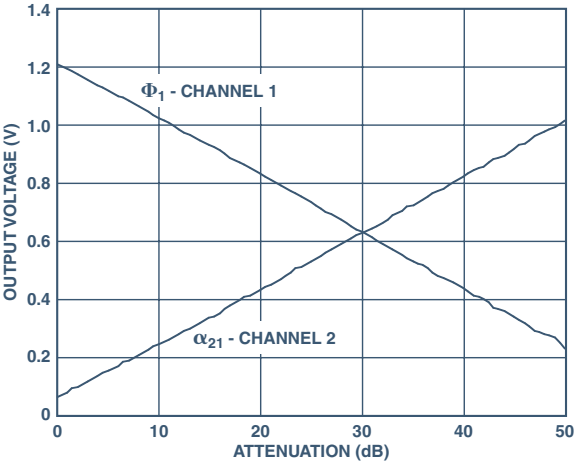

Figure 3. Transfer functions for the two outputs. Channel 1 provides the absolute output power, while Channel 2 provides the relative attenuation between the two channels.

The test results in Figure 3 are subject to the inaccuracies of the VOA used in the lab. The measurement was repeated with calibrated current sources to better assess the accuracy of the design. Figure 4 illustrates the full dynamic range capabilities and log-conformance of the circuit in Figure 2. The accuracy is better than 0.1 dB over a 5-decade range.

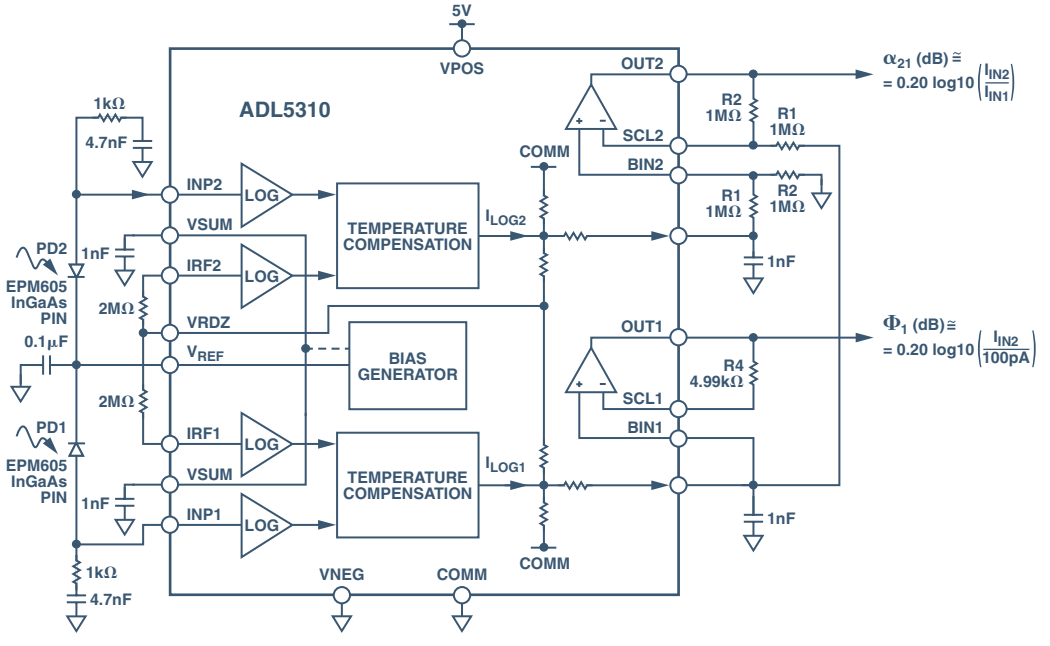

Figure 2. Hardware implementation of VOA control using a logarithmic front end. The ADL5310 is configured to provide an absolute power measurement of the optical signal power incident on PD1, while the difference voltage reveals the absorbance across the VOA. The wide dynamic range allows the loop to remain locked over a broad range of input signals.

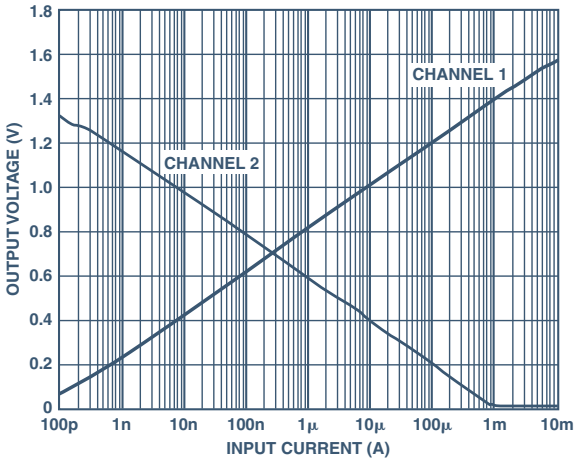

Figure 4. Transfer functions for the two outputs.

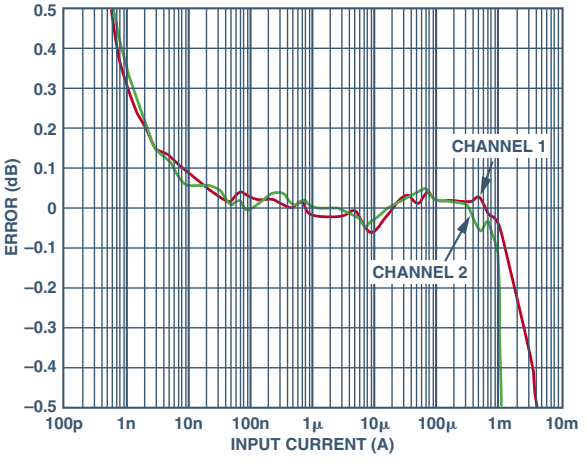

Figure 5. Log-conformance of the transfer functions.

An alternative solution is offered in Figure 6, where a current mirror is used to feed an opposite-polarity replica of the cathode photocurrent of PD2 into Channel 2 of the ADL5310. The current mirror shown is a modified Wilson mirror. While other current-mirror circuits would also work, this modified Wilson mirror provides fairly constant performance over temperature. To minimize the effects of temperature gradients and beta mismatch, it is essential to use matched-pair transistors when designing the current mirror.

The circuit of Figure 6 is no longer subject to the logarithmic-slope mismatch issues inherent in the previous solution. Individual channel slope and intercept characteristics can now be calibrated independently. The accuracy was verified using a pair of calibrated current sources in order to eliminate any error due to the integral nonlinearity of the VOA. The performance of the circuit depicted in Figure 6 is shown in Figures 7 and 8. Transfer functions and error plots are provided for several power levels. The accuracy is better than 0.1 dB over a 5-decade range. The dynamic range is slightly reduced for strong I_{IN} input currents. This is due to the limited available swing of the VLOG pin; it can be improved through careful selection of input and output optical-tap coupling ratios.

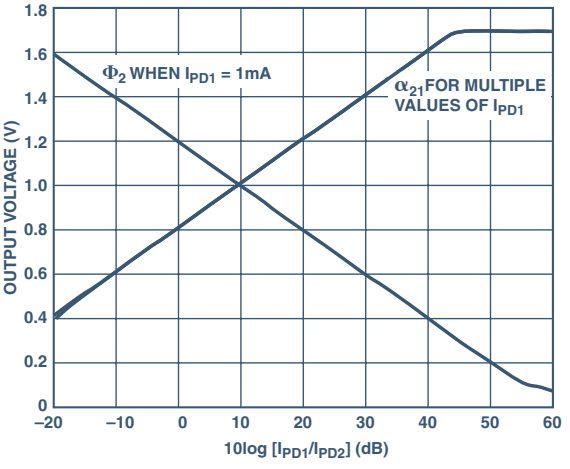

Figure 7. Absorbance and absolute power transfer functions for Wilson-mirror ADL5310 combination.

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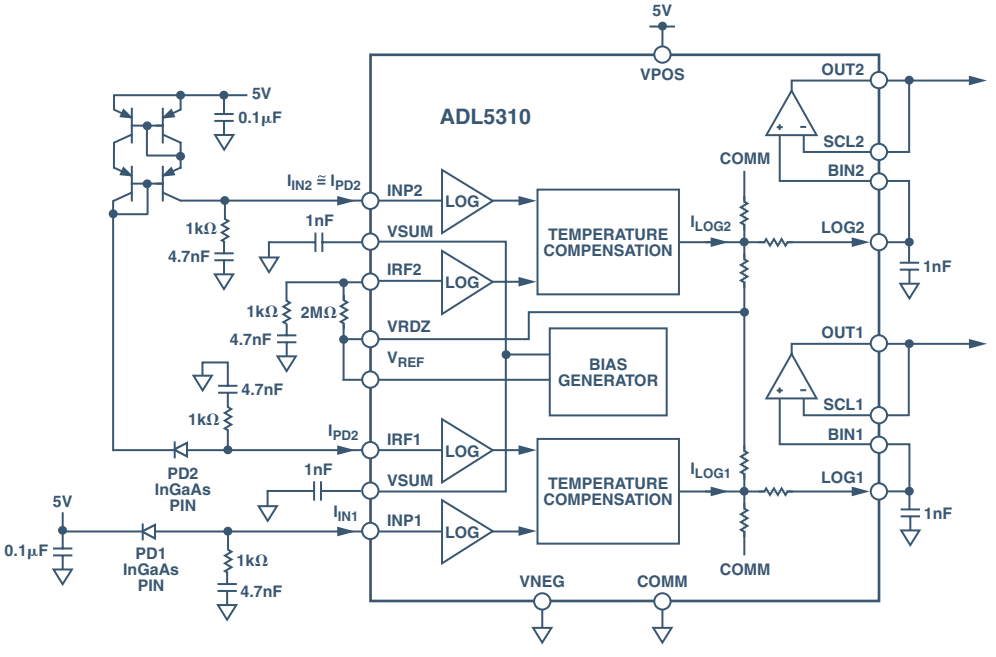

Figure 6. Alternative solution using a modified Wilson current mirror.

Fast-Locking, High Sensitivity Tuned-IF Radio Receiver Achieved with a 7-GHz Synthesizer

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Paul O'Brien [paul-p.obrien@analog.com]

INTRODUCTION

To improve sensitivity and selectivity in modern radios, there is a need to minimize phase noise and reference spurs, and to reduce the lock time. The circuit outlined in this article improves local oscillator (LO) performance with respect to each of these.

Phase noise is a measure of the purity of the LO signal. It is ascertained by taking the ratio of the output fundamental power to the noise power in a 1-Hz bandwidth at a given offset from the carrier. The result is expressed in dBc/Hz.

Spurious frequency elements (*spurs*) can occur in the output due to internal switching in the synthesizer. In an integer-*N* synthesizer, they are generally due to the phase-frequency detector (PFD) frequency; in a fractional-*N* device, they can be a result of the nature of the synthesizer architecture. In an integer-*N* phase-locked loop (PLL), they are called *reference spurs.*

Lock time refers to the time it takes to switch the output from one frequency to another—an important specification in many systems. In general, we say that the output is switched—or has locked—to the new frequency when it has settled to within a certain percentage, or parts per million (ppm), of the final desired frequency—or has locked to within a specified number of degrees of the final phase.

Traditional Receiver Implementation

Figure 1 shows the general block diagram for the most popular receiver architecture (*superheterodyne* receiver). The system shown here is typical for receivers designed to meet the DCS1800 standard for mobile phones. For this standard, the Receive (Rx) band is 1805 MHz to 1880 MHz.

In Figure 1, the RF input is applied to an RF filter, followed by a low-noise amplifier (LNA). The signal is then mixed down to the intermediate frequency (IF) by a mixer with a tuned LO input. Additional filtering follows, and a final mixer, using a single-frequency LO, takes the fixed IF down to baseband.

The tuned-RF LO starts with a clean and stable reference frequency, followed by an ADF4106 PLL synthesizer and a voltage-controlled oscillator (VCO). The reference is provided by a temperature-controlled (TCXO), voltage-controlled (VCXO), or oven-controlled (OCXO) crystal oscillator. The PLL synthesizer's R-divider conditions this reference to a value equal to the channel spacing in integer-*N* systems—or a multiple of the channel spacing in fractional-*N* systems. The PFD compares the loop output, F_{VCO}, divided by N, with the output of the R-divider, and the loop drives the PFD output toward zero by driving the VCO to make $F_{VCO} = F_{PFD} \times N$. *N* is varied to vary the LO output frequency, thus tuning the radio.

Phase noise of the LO depends on a number of factors: reference noise; noise in the synthesizer (R-divider, N-divider, PFD, and charge pump); the value of *N*; and the frequency at which the synthesizer PFD is operated.

The phase noise of the LO (dB) can be described by the general equation:

$$PN = PN_{SYNTH} + 20 \log N + 10 \log F_{PFD}$$

where:

PN_{SYNTH} is the phase noise contribution of the synthesizer (given in the appropriate data sheet, in dB)

20 log *N* is the additional noise due to the *N* value in the synthesizer

10 log F_{PFD} is the noise contribution due to the synthesizer PFD frequency.*

*For a more detailed explanation, please see "Design a Direct 6-GHz Local Oscillator with a New, Wideband, Integer-*N*, PLL Synthesizer" in *Analog Dialogue*, Volume 35 (print edition) or http://www.analog.com/library/analogDialogue/archives/35-06/ADF4106/index.html.

The level of reference spurs depends on: the PFD design, leakage in the charge pump section of the PFD, the PLL loop bandwidth, and VCO sensitivity. The lock time depends on: the PFD frequency and the PLL loop bandwidth.

In the receiver, with the IF chosen as 230 MHz, the tuned RF has to go from 2035 MHz to 2110 MHz (using high-side injection), in 200-kHz steps. Using an integer-*N* architecture to do this, a PFD frequency of 200 kHz is needed and the *N* value would vary from 10175 (2035 MHz) to 10550 (2110 MHz).

Using the best commercially available components (ADF4106 PLL synthesizer), the expected in-band phase noise in this system would be –85.6 dBc/Hz. Typical reference spurs in such a system would be –88 dBc at 200 kHz and –90 dBc at 400 kHz.

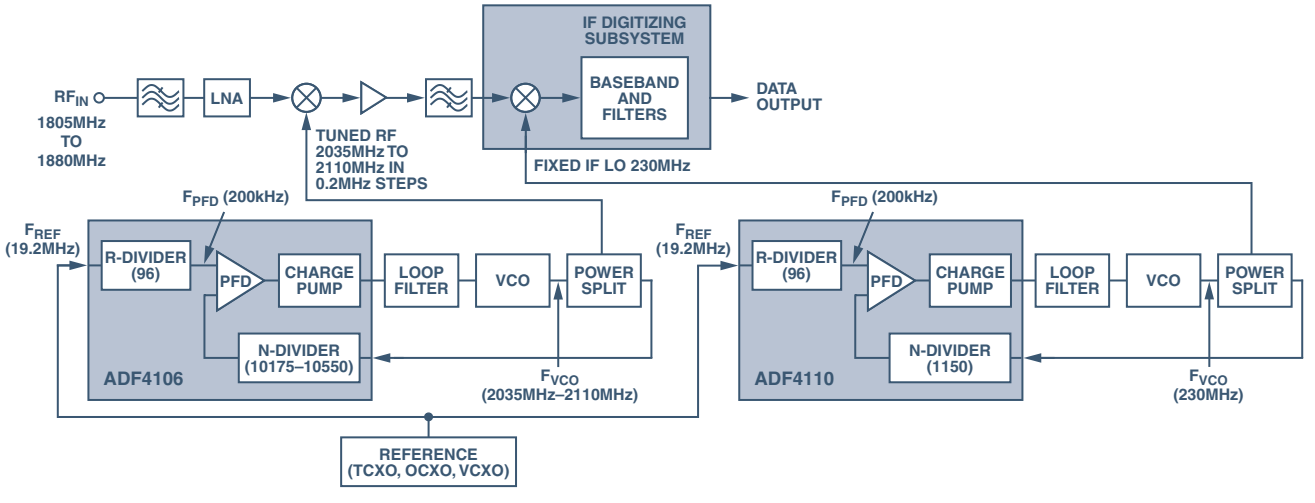

Figure 1. Block diagram of a traditional superheterodyne receiver.

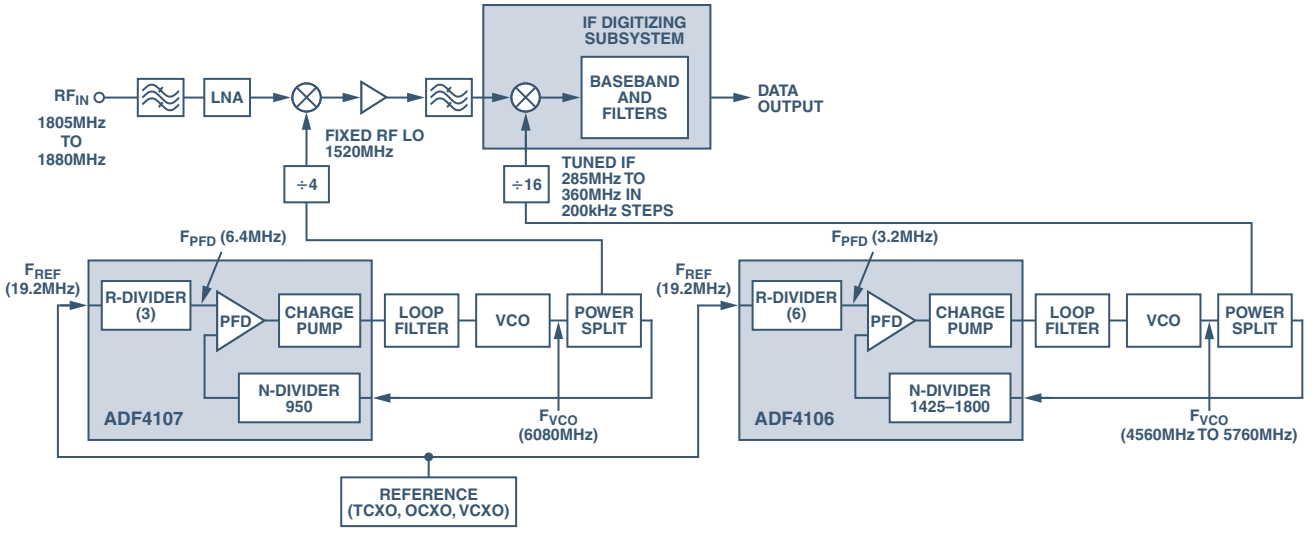

Figure 2. Alternative receiver block diagram

Using a loop bandwidth of 20 kHz, typical lock time to 10 degrees of phase error would be 250 μs.

Alternative Receiver Implementation

A new high-bandwidth PLL synthesizer, the ADF4107, is now available from ADI. Its RF stage is capable of operating at frequencies up to 7.0 GHz, while the PFD frequency is capable of operating at up to 104 MHz. This high-bandwidth capability can be used to implement novel receiver architectures, such as that shown in Figure 2. Here, the LO for each stage is derived from a higher frequency that is an integer multiple of the required frequency. In addition, the tuning is done in the IF section. This allows a very high multiple to be used, for an improvement in overall phase noise and lock time.

Fixed RF

In Figure 2, a fixed-frequency RF LO converts the signal down to the IF-band, and the channel is tuned in the IF-band. Again using the DCS1800 example, we can choose a fixed RF LO of 1520 MHz. This can be derived from a 6080-MHz signal by dividing by 4, as shown in Figure 2.

The phase noise of the RF LO will be:

$$-219 + 20 \log 950 + 10 \log (6.4 \times 10^6) - 20 \log 4$$
$$= -219 + 59.5 + 68 - 12$$
$$= -103.5 \text{ dBc/Hz}$$

The reference spurs will occur at 6.4 MHz offset from the carrier and will be very small (< –90 dBc), because (a) there will be 12 dB of attenuation due to the divide-by-4 circuit, and (b)—since this is a fixed-frequency LO—the loop bandwidth can be made low (say 20 kHz). A simple 20-dB/decade attenuation will give even further attenuation of the spurs.

There will be no spurs at 200 kHz, 400 kHz, 600 kHz, and 800 kHz; and lock time is not an issue, since no tuning occurs in the fixed-RF section.

Tuned IF

Continuing with the DCS1800 example, Figure 2 shows a tuned IF going from 285 MHz to 360 MHz in 200-kHz steps. To implement this, a PFD frequency of 3.2 MHz is used, producing an initial LO that goes from 4560 MHz to 5760 MHz, in 3.2-MHz steps. Dividing these frequencies by 16 gives the desired 285 MHz to 360 MHz in 200-kHz steps.

The worst-case phase noise of the tuned IF will be:

$$-219 + 20 \log 1800 + 10 \log (3.2 \times 10^6) - 20 \log 16$$
$$= -219 + 65 + 65 - 24$$
$$= -113 \text{ dBc/Hz}$$

Reference spurs will occur at a 3.2-MHz offset from the carrier. By choosing a loop bandwidth of 500 kHz, the spurs at 3.2 MHz will be below –90 dBc. In a DCS system, the important frequencies for spur reduction are 200 kHz, 400 kHz, 600 kHz, and 800 kHz. However, spurs will not exist at these frequencies in the proposed configuration, since we are operating at the high PFD frequency of 3.2 MHz.

With the loop bandwidth set at 500 kHz and the PFD frequency at 3.2 MHz, phase lock to within 10 degrees will occur in less than 10 μs. The frequency lock response is shown in Figure 3.

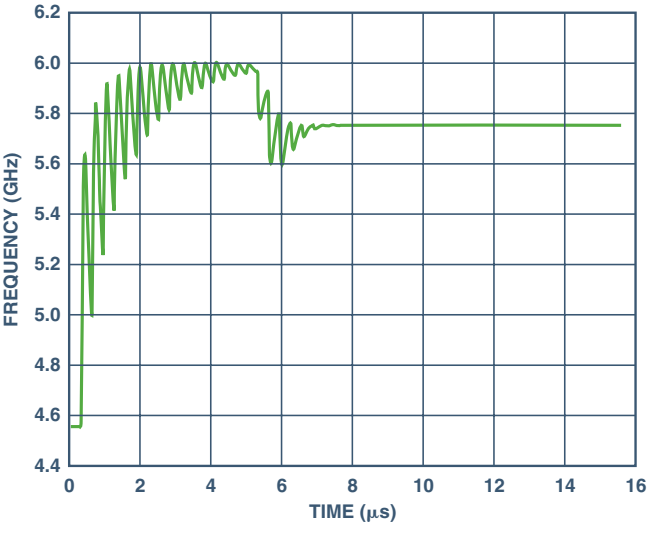

Figure 3. Lock time for the tuned IF.

Filtering Considerations

Both of the architectures considered are essentially superheterodyne, with two stages of downconversion. Filtering is critical in each of the stages.

In Figure 1, the RF filter that precedes the LNA rejects the very strong out-of-band interferers. The IF filter can be narrow-band (200 kHz in GSM) to reject the in-band interferers.

In Figure 2, the RF filter is the same as in Figure 1. However, the IF filter of Figure 2 cannot be narrow-band. It must pass the full band, since tuning has yet to occur. This means that the in-band interferers will have to be filtered later in the chain, as part of the baseband processing. Several IF-to-baseband receivers are available from ADI. These include the AD6650, AD6652, AD9870, and AD9874. They should be carefully considered when analyzing the architecture of Figure 2.

CONCLUSION

Operating the core of a PLL at a higher PFD frequency (an integer multiple of the final LO frequency) provides improved phase noise, output reference spurs, and lock time. Furthermore, a tuned-IF architecture provides even higher performance, as the integer multiple can be higher. However, filtering requirements need to be carefully considered.

The example used in this proposal is for an integer-*N* PLL, the ADF4107, but the configuration is not limited to this. It is also quite feasible to realize similar gains using this configuration with a fractional-*N* architecture.

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Phase-Locked-Loop (PLL) RF Frequency Synthesizers—Single

ADI Model	2nd Source?	Maximum RF Input Frequency F_{IN} (MHz)	Phase Noise @ 1 kHz ΦN dBc/Hz, 200 kHz Channel Spacing	Phase Noise Frequency (MHz)	Maximum REFIN Frequency (MHz)	RF Prescalers	Power Consumption (mA)	Package
ADF4001BRU	Proprietary	200	–99	200	100		4.5	TSSOP-16
ADF4001BCP	Proprietary	200	–99	200	100		4.5	CSP-20
ADF4110BRU	Proprietary	550	–91	540	100	8/9 16/17 32/33 64/65	4.5	TSSOP-16
ADF4110BCP	Proprietary	550	–91	540	100	8/9 16/17 32/33 64/65	4.5	CSP-20
ADF4111BRU	Proprietary	1200	–87	900	100	8/9 16/17 32/33 64/65	4.5	TSSOP-16
ADF4111BCP	Proprietary	1200	–87	900	100	8/9 16/17 32/33 64/65	4.5	CSP-20
ADF4112BRU	Proprietary	3000	–90	900	100	8/9 16/17 32/33 64/65	6.5	TSSOP-16
ADF4112BCP	Proprietary	3000	–90	900	100	8/9 16/17 32/33 64/65	6.5	CSP-20
ADF4113BRU	Proprietary	4000	–91	900	100	8/9 16/17 32/33 64/65	8.5	TSSOP-16
ADF4113BCP	Proprietary	4000	–91	900	100	8/9 16/17 32/33 64/65	8.5	CSP-20
ADF4106BRU	Proprietary	6000	–93	900	250	8/9 16/17 32/33 64/65	13	TSSOP-16
ADF4106BCP	Proprietary	6000	–93	900	250	8/9 16/17 32/33 64/65	13	CSP-20
ADF4107BCP	Proprietary	7000	–93	900	250	8/9 16/17 32/33 64/65	14	CSP-20
ADF4107BRU	Proprietary	7000	–93	900		8/9 16/17 32/33 64/65	14	CSP-20
ADF4116BRU	LMX2306TM	550	–89	540	100	8/9	4.5	TSSOP-16
ADF4117BRU	LMX2316TM	1200	–87	900	100	32/33	4.5	TSSOP-16
ADF4118BRU	LMX2326TM	3000	–90	900	100	32/33	6.5	TSSOP-16
ADF4153BRU	Proprietary	4000	–103	1740	150	4/5 8/9	12	TSSOP-16
ADF4153BCP	Proprietary	4000	–103	1740	150	4/5 8/9	12	CSP-20

For additional synthesizer types or an updated chart, see http://www.analog.com/analog_root/static/pdf/RFComms/SelectionGuides/phase.pdf

ECG Front-End Design is Simplified with MicroConverter®

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INTRODUCTION

An electrocardiogram (ECG) is a recording of the electrical activity on the body surface generated by the heart. ECG measurement information is collected by skin electrodes placed at designated locations on the body. The ECG signal is characterized by six peaks and valleys labeled with successive letters of the alphabet P, Q, R, S, T, and U (Figure 1).

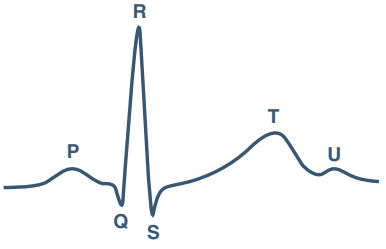

Figure 1. Form of ECG signal.

This article suggests some ideas for a low-cost implementation of an ECG monitor.[1] Its configuration is envisaged for use with a personal computer (PC). Although this article is written with patient safety in mind, any ideas presented are not by themselves necessarily compatible with all *system* safety requirements; anyone using these ideas must ensure that, in a particular design, the design as a whole meets required safety criteria.

First we provide an overview of typical analog ECG topology. Then a circuit is proposed which performs analog-to-digital conversion, digital filtering, and digital amplification—all by using a MicroConverter—an integrated "system on a chip" that combines an A/D converter, microcontroller, and flash memory. The article goes on to discuss considerations in the choice of components and programming of the MicroConverter.

Requirements for an Electrocardiograph

The front end of an ECG must be able to deal with extremely weak signals ranging from 0.5 mV to 5.0 mV, combined with a dc component of up to ±300 mV—resulting from the electrode-skin contact—plus a common-mode component of up to 1.5 V, resulting from the potential between the electrodes and ground. The useful bandwidth of an ECG signal, depending on the application, can range from 0.5 Hz to 50 Hz—for a monitoring application in intensive care units—up to 1 kHz for late-potential measurements (pacemaker detection). A standard clinical ECG application has a bandwidth of 0.05 Hz to 100 Hz.

ECG signals may be corrupted by various kinds of noise. The main sources of noise are:

- power-line interference: 50–60 Hz pickup and harmonics from the power mains
- electrode contact noise: variable contact between the electrode and the skin, causing baseline drift
- motion artifacts: shifts in the baseline caused by changes in the electrode-skin impedance
- muscle contraction: electromyogram-type signals (EMG) are generated and mixed with the ECG signals
- respiration, causing drift in the baseline
- electromagnetic interference from other electronic devices, with the electrode wires serving as antennas, and
- noise coupled from other electronic devices, usually at high frequencies.

For meaningful and accurate detection, steps have to be taken to filter out or discard all these noise sources.

Typical ECG Signal Chain

Figure 2 shows a block diagram of a typical single-channel electrocardiograph. In that chain it is apparent that all filtering is done in the analog domain, while the microprocessor, microcontroller, or DSP is used principally for communication and other downstream purposes. Thus the powerful computational properties of the digital core are not readily available to deal with the signal in its essentially raw state. In addition, sophisticated analog filters can be costly to the overall design due to their inflexibility—and the space, cost, and power they require.

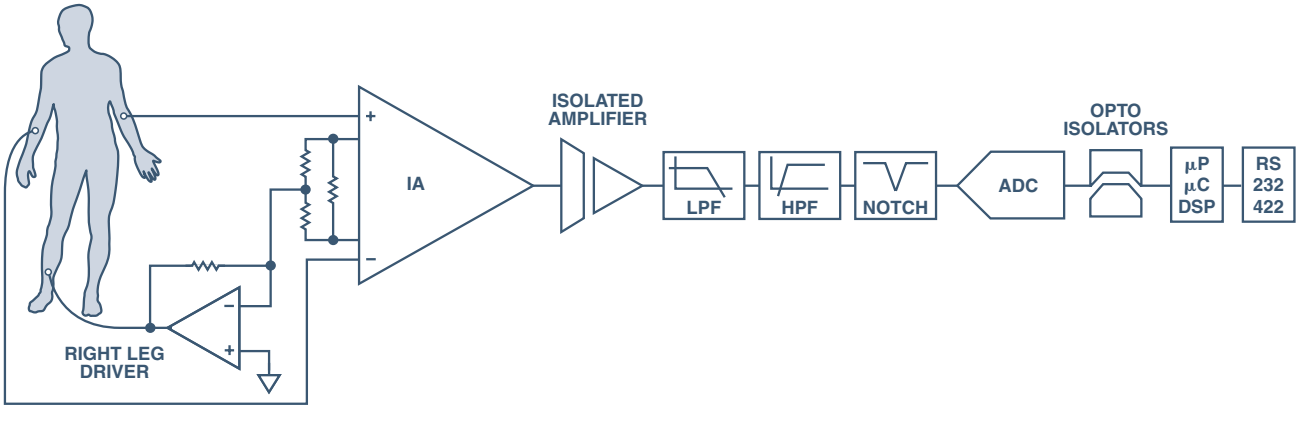

Figure 2. Typical single-channel electrocardiograph.

Proposed Circuit

The signal chain can be simplified by using an ADuC842 MicroConverter, which allows the ADC, filters, and microprocessor to be combined in a single integrated circuit. Additional advantages are flexibility of filter implementation and isolation in the digital domain. The proposed system design is shown in Figure 3.

Analog Input Processing

The analog front end uses the typical approach with an instrumentation amplifier (IA) and a right leg common-mode feedback op amp. The IA is the AD620, a low cost, high accuracy instrumentation amplifier, with excellent dc performance: CMR>>100 dB to nearly 1 kHz, 50-μV max offset voltage, low input bias current (1 nA max), and low input voltage noise (0.28 μV from 0.1 Hz to 10 Hz).

The AD620 requires only a single external gain-setting resistor, R_G. Resistors R2 and R3 change the normal gain equation to [$Gain$ = 1 + 49.4 k/R_G + (49.4 k/2)/22 k]. To avoid output saturation, the usable gain is limited by the output swing and the maximum input voltage to the IA. With a ±5-V power supply, the output swing of the AD620 is about ±3.8 V; and the maximum input is ±5 mV plus a variable normal-mode dc offset of up to ±300 mV, allowing a maximum gain of 12.45. Here, the gain is conservatively set to 8 (±1%), using R_G = 8.45 kΩ.

The op amp used in the right-leg common-mode feedback circuit is the OP97, a low power, high precision operational amplifier with extremely high common-mode rejection (114 dB minimum). This circuit applies an inverted version of the common-mode interference to the subject's right leg, with the aim of canceling the interference. The op amp has a voltage gain for the common-mode voltage of 91 [*viz.*, R4/(R2 || R3) = 1 MΩ/11 kΩ], with a 1.6-Hz rolloff and a low-pass cutoff at about 160 Hz for stability [$f_{-3\ dB}$ = 1/(2π × (10 kΩ × 0.1 μF)].

Digital Isolation

Digital isolation is at the heart of the RS232 interface to the PC, which is suggested for the display in this example. The isolator is the ADuM1301, a bidirectional digital isolator based on Analog Devices *i*Coupler® technology—a technology that eliminates the design difficulties commonly associated with optocouplers (uncertain current-transfer ratios, nonlinear transfer functions, etc.).

It also achieves high data rates with lower power consumption than optocouplers. The ADuM1301 has three independent isolation channels, two of which are used here—one for transmitting, the other for receiving data. (A further capability of the ADuM1301—not required here—is the ability to enable/disable the input/output data.) The power supply for the measurement side of the ADuM1301 is taken from the ADP3607-5 booster/regulator, which provides a fixed 5-V output. The power for the PC side is totally isolated from the circuit. It can be taken from the PC (as it is here) or from a different source.

Safe Power

The isolated power is supplied by a battery, which is recharged in a charging station when not in use. To handle a bipolar input signal, a ±5-V dual supply is required for the AD620 and OP97. The ADP3607-5 booster/regulator and the ADP3605 inverter serve as a regulated dual supply that provides positive and negative regulated voltages from a single 3-V battery.

The ADP3607 is a regulated-output switched-capacitor voltage doubler capable of providing up to 50 mA. Capable of operating from an input voltage as low as 3 V, it is offered in a version with the regulation fixed at 5 V (ADP3607-5)—the one used here. (It is also available in a form adjustable over a 3-V to 9-V range via an external resistor. It can produce an even larger positive voltage with an external pump stage consisting of passive components.)

The ADP3605 switched-capacitor voltage inverter, with a regulated output voltage, is capable of providing up to 120 mA. It is offered with the regulation fixed at –3 V (ADP3605-3) or adjustable via external resistors over a –3-V to –6-V range. (An even larger negative voltage can be achieved by adding an external pump stage, as with the ADP3607.) A –5-V supply is needed, with an input voltage of +5 V, so R is set to 31.6 kΩ (±1%), using the equation, V_{OUT} = –1.5 R/9.5 kΩ.

Both supply voltages (±5 V) are generated by capacitive charge pumps, which cannot generate unsafe voltages—even under fault conditions—because they do not require any inductors. These devices also feature a *shutdown* mode, which allows the MicroConverter to power down the devices when the system is not in use.

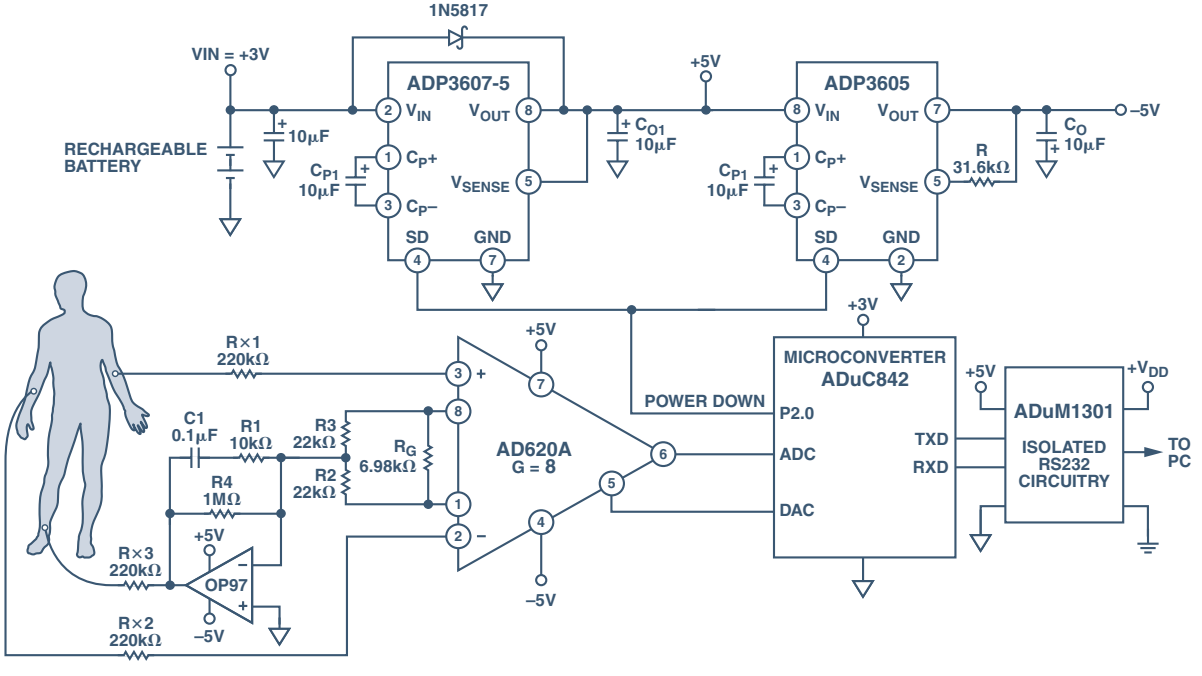

Figure 3. Proposed ECG configuration.

Patient Safety

In addition to the digital isolation and the safe power supply, the series resistors, Rx1, Rx2, and Rx3, provide protection for the patient—in order to comply with AAMI (Association for the Advancement of Medical Instrumentation) standards for safe current levels (*see* References). These standards require that rms ground currents or fault current from the electronics must be less than 50 μA.

Signal Processing

The ADuC842 MicroConverter is well suited for the main signal processing tasks. It features a fast, 12-bit ADC and other high-performance analog peripherals, a fast 8052 microprocessor core, integrated 62KB flash memory for code, and several other useful peripherals, as shown in Figure 4.

The key components of the MicroConverter for this design are the ADC and the 8052 core. The ADC converts the analog output of the instrumentation amplifier to a digital signal. The software written for the 8052 core processes the digitized signal to produce the data for the ultimate ECG trace. As in many MicroConverter designs, the software includes both complex high level code written in C and time sensitive routines written in *assembly code*. In this case, the implementation of band-pass filters and notch filters is in C, while the ADC is controlled by assembly code. Assembly code, combined with converter speed, enables the accumulation of multiple samples, enhancing the effective resolution of the ADC well beyond its normal 12 bits.

Figure 5 gives a good indication of the effectiveness of the MicroConverter. The top trace is the signal from the instrumentation amplifier applied to the ADC. The middle trace shows the initial results achieved using the C-code filtering only, while the bottom trace shows the final result after the processing of multiple conversions, using assembly code.

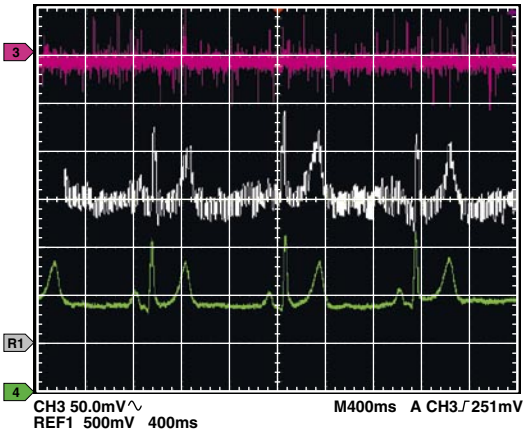

Figure 5. Oscilloscope traces.

Filters in C Code

The acquired signal is processed by digital filtering in the MicroConverter. For this purpose, we designed two second-order digital *infinite impulse-response* (IIR) filters, based on a sampling frequency of 500 Hz. A notch filter was designed to suppress the 50-Hz interference. The chosen design procedure was the *pole-zero placement method*, with a notch frequency of 50 Hz and notch width 10 Hz. To achieve this required the following transfer function:

$$H(z) = \frac{1 - 1.618z^{-1} + z^{-2}}{1 - 1.5164z^{-1} + 0.8783z^{-2}}$$

The transfer function can be converted into a programmable recursive algorithm:

$$NOut_k = NIn_k - 1.618NIn_{k-1} + NIn_{k-2} + 1.5164NOut_{k-1} - 0.8783NOut_{k-2}$$

In this equation the subindex, k, means the present value, k-1 means the value in the previous instant, and so on.

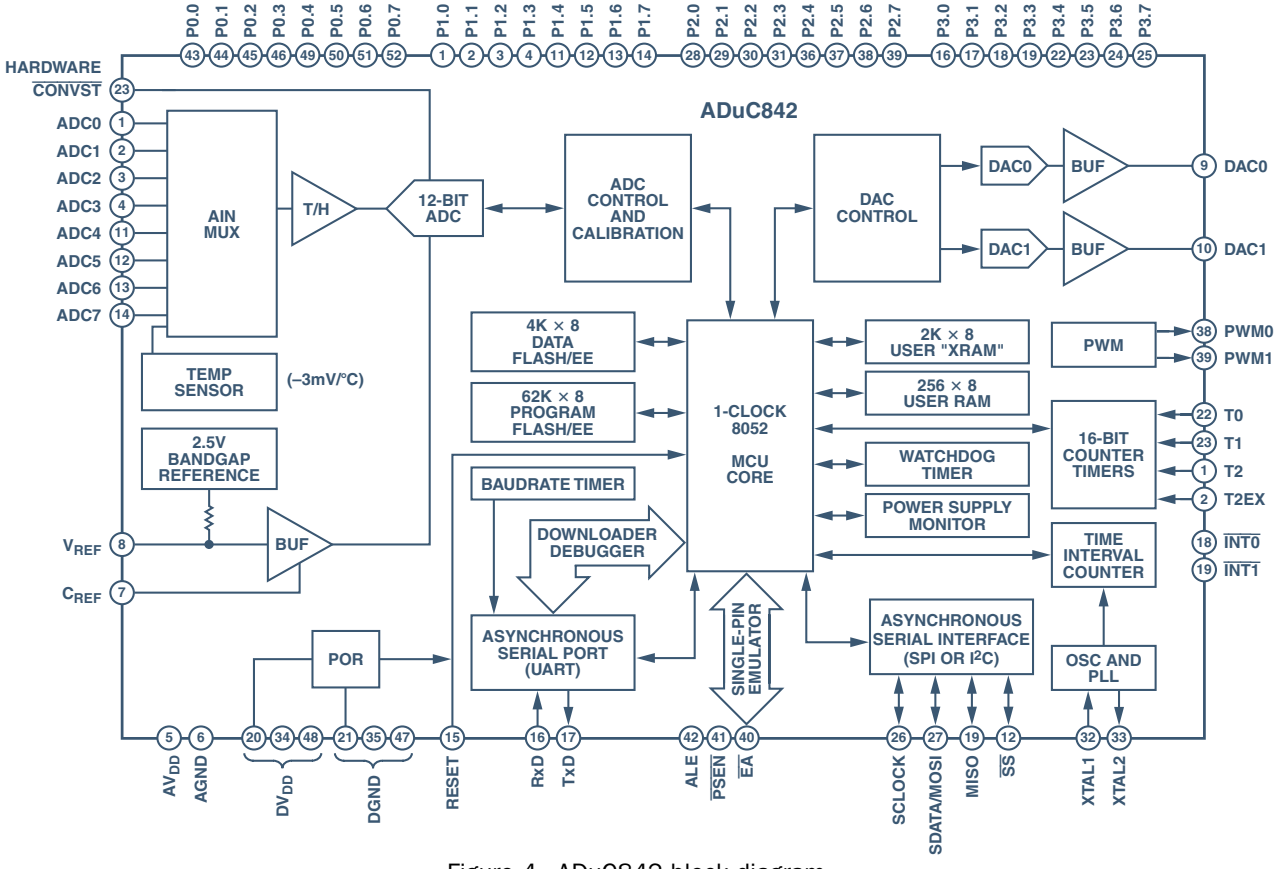

Figure 4. ADuC842 block diagram.

We now need to turn this equation into code. C coding was the automatic choice for this arithmetic-intensive processing, as programming it in assembly would have been too time consuming. Implementing the filter equations directly would be inefficient with the ADuC842, since it is not tailored for floating-point calculations. Fortunately we can just scale the coefficients (e.g. by 4096) and implement the notch code as:

```
iNOut = (4096L*iNIn-6627L*iNIn1+4096L*iNIn2+6211L*
iNOut1-3598L*iNOut2)/4096;
```

This implements a second-order filter. Although we can calculate higher order filters, in practice it seems workable to simply cascade second-order filters.

The second filter was a Butterworth pass-band filter with a 0.05-Hz low cutoff frequency and a 100-Hz high cutoff frequency. The transfer function and recursive algorithm are:

$$H(z) = \frac{0.4206 - 0.4206z^{-2}}{1 - 1.1582z^{-1} + 0.1582z^{-2}}$$

$$BOut_k = 0.4206BIn_k - 0.4206BIn_{k-2} + 1.1582BOut_{k-1} - 0.1582BOut_{k-2}$$

This is implemented in C code by:

```
iBOut = (1723L*iBIn-1723L*iBIn2+4745L*iBOut1-
650L*iBOut2) /4096;
```

Note that the outputs can be scaled simply by changing the coefficients of the inputs. Also note that, for efficiency (if the signals are all positive), the division by 4096 is accomplished at the end by shifting 12 right.

The implementation shown in Figure 6 is for a cascade of five band-pass filters and two notch filters. The signal is scaled up by a factor of 4 in each of the first and second band-pass filters. The 12-bit right shift accomplishes the divide-by-4096.

```
while(1)
        {
        while(c25ms<64);    //Wait for 64 measurements to be done.
        iBIn = iAdc0>>3;    //Save accumulated measurement.
        iAdc0 = 0;          //Zero for new measurement accumulation.
        c25ms = 0;          //Reset synchronization timer.
        // 5 Band pass 0.05 - 100Hz Fs=500 first 2 with gain of 4 each.
        iBOut = (6891L*lBIn-6891L*lBIn2+4745L*iBOut1-
        650L*iBOut2)>>12L;
        iBO10 = (6891L*iBOut-6891L*iBOut2+4745L*iBO11-
        650L*iBO12)>>12L;
        iBO20 = (1723L*iBO10-1723L*iBO12+4745L*iBO21-
        650L*iBO22)>>12L;
        iBO30 = (1723L*iBO20-1723L*iBO22+4745L*iBO31-
        650L*iBO32)>>12L;
        iNIn = (1723L*iBO30-1723L*iBO32+4745L*iNIn1-650L*iNIn2)>>12L;
               // 2 notch filters.
        iNOut = (4096L*iNIn-6627L*iNIn1+4096L*iNIn2+6211L*iNOut1-
        3598L*iNOut2)>>12L;
        iN3O = (4096L*iNOut-6627L*iNOut1+4096L*iNOut2+6211L*iN3O1-
        3598L*iN3O2)>>12L;

        iBIn2 = iBIn1;      //Save delayed values for filters.
        iBIn1 = iBIn;
        iBOut2 = iBOut1;
        iBOut1 = iBOut;

        iNIn2 = iNIn1;
        iNIn1 = iNIn;
        iNOut2 = iNOut1;
        NOut1 = iNOut;

        iBO12 = iBO11;
        iBO11 = iBO10;
        iBO22 = iBO21;
        iBO21 = iBO20;
          ...               //Other delayed values not shown.

        if(iBIn>24000)      iDac -= 1; //Control AD620 output level.
        if(iBIn<8000)       iDac += 1;
        iOut1 = (iDac)&0xfff;
        DAC0H = (iOut1>>8)&0xf;
        DAC0L = iOut1&0xff;

        if((iN3O+iOfs)>3000)    iOfs -= 1; //Control output level.
        if((iN3O+iOfs)<1000)    iOfs += 1;
        iOut = ((iN3O+iOfs))&0xfff;
        DAC1H = (iOut>>8)&0xf;  //Output to oscilloscope for
        evaluation.
        DAC1L = iOut&0xff;
        if(!(c2++&3))       printf("%4d\r\n",iOut);     //Output to PC.
        }
```

Figure 6. Essential part of C code.

Note the lines, `if(iAdc00>24000)iDac-= 1,`, and `if(iAdc00<8000)iDac += 1,`, which adjust the DAC output of the ADuC842 to drive the level-shifting input of the AD620 to shift the AD620 output to a comfortable value for the MicroConverter's ADC input. This is desirable to reduce the effects of the variable dc offsets that result from slight differences in the way the electrodes are applied to the skin. A similar technique is used to ensure that the output voltage is centered within the output range.

Processing in Assembly Code

The assembly code's main functions are to measure the input signal at regular intervals and to ensure that the C code calculations are repeated at the required rate of 500 times per second. In the first instance, we programmed Timer0 to run continuously and generate its interrupts at 1-ms intervals. Each interrupt restarts Timer0, gets an ADC conversion result, and increments a variable, c2ms, which is used to synchronize the C code. At this stage of code development, the first few lines of C code were:

```
while(c2ms<2);      //Used in first phase.
c2ms = 0;
iAdc00 = iAdc0;
```

Initially, c2ms is 0, and the C code will wait at the line `while(c2ms<2);`. After 1 ms, a Timer0 interrupt occurs, and c2ms is incremented to 1. After a further 1 ms, c2ms is incremented to 2. Now `while(c2ms<2);` is no longer satisfied, and the C code continues by resetting counter c2ms to 0 and doing the filter calculations. Thereafter, the C code shifts the results down the chain of variables representing the various delayed results ready for the next iteration of the loop. The final part of the loop is the `printf(...)`, which sends the result to the PC for display. The processing of the data on the PC, beyond the scope of this article, can be as simple as importing it to a spreadsheet for graphical display—or as sophisticated as the designer wishes to make it. This solution produced the middle trace of Figure 5.

To improve the result, the Timer0 interrupt rate was shortened to 1/32 ms, and the data was accumulated in iAdc0, to make use of multiple measurements instead of just a single measurement. At the same time, the `while` was changed to `while(c2ms<64)` so that the C code would wait for 64 measurements to be accumulated before doing each filter loop. The value in iAdc0 is saved in iAdc00 for further processing, and then iAdc0 is cleared—ready to accumulate the next 64 measurements. Figure 7 shows the assembly code. This improved solution produced the lower trace of Figure 5.

```
IntT0:   push    ACC
         push    PSW
         clr     TR0             ;Stop T0.
         mov     TH0,#0fdh       ;Reload 1/32ms.
         mov     TL0,#0f6h
         setb    TR0             ;Restart T0.
         mov     a,ADCDATAL
         add     a,iAdc0+3
         mov     iAdc0+3,a
         mov     a,ADCDATAH      ;Add a conversion to iAdc0.
         anl     a,#0fh
         addc    a,iAdc0+2
         mov     iAdc0+2,a
         clr     a
         addc    a,iAdc0+1
         mov     iAdc0+1,a
         mov     ADCCON2,#0      ;Start a conversion.
         mov     ADCCON2,#10h
         inc     c25ms           ;Imcrement ms counter.
IntT0R:  pop     PSW
         pop     ACC
         reti
```

Figure 7. Assembly code.

Gain

Signal gain is always an important consideration in an ECG signal chain. In the above-described design, it depends on a number of factors. The analog gain is set to 8×, as discussed previously. Next, a gain of 64× results from accumulating 64 measurements of this signal. Next there is a signal loss of 8× from the code `iBIn = iAdc0>>3;`, and finally, a gain of 4× twice from the scaling of the first two band-pass-filter equations. This results in a total gain of G = (8 × 64/8) × 4 × 4 = 1024, which is typical of analog ECG circuits.

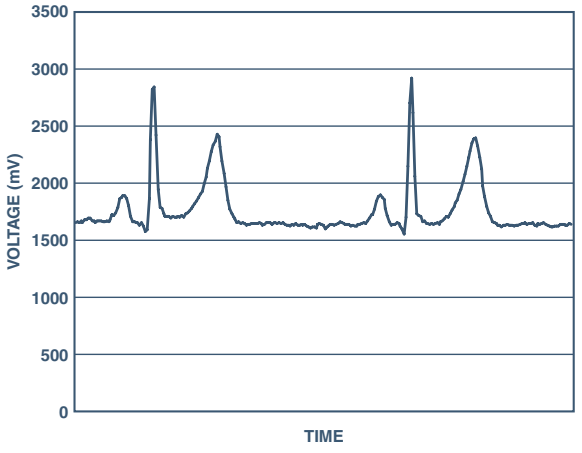

Figure 8. Graphs of practical measurements.

CONCLUSION

Figure 8 shows results for a subject connected in Einthoven lead I configuration. As can be seen, good results are achieved despite the simplicity of the electronic hardware used. The article demonstrates that significant improvements can be achieved with simple hardware combined with attention to software. The improvement in this example is by no means at the optimum level; it should be possible for a dedicated designer to significantly improve the results. Additional improvements could be made if code with different filter frequencies or other special characteristics were to be implemented. The code memory of the ADuC842 is flash based, allowing such customizations to be made after a product using it is manufactured—or even as the patients' needs change. An ultimate result could be a compact, inexpensive ECG for a potentially large-volume market.

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Firth J. and Errico P., "Low-Power, Low-Voltage IC Choices for ECG System Requirements," *Analog Dialogue*, Volume 29, Number 3, 1995.

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AD620 Data Sheet revision F. Analog Devices, Inc., ©2003.

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(continued from page 6)

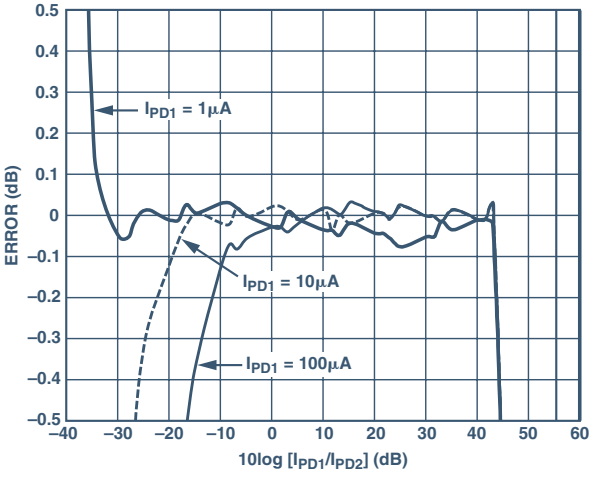

Figure 8. Log conformance for Wilson-mirror ADL5310 combination, normalized to 10-µA Channel 1 input current, I_{IN1}.

CONCLUSION

Translinear log-amps simplify VOA absorbance measurements by providing a linear-in-dB relationship between the input photocurrent and resulting output voltage. The division and exponentiation processes that would be required with a linear solution are eliminated when using logarithmic signal processing. There are several ways of using translinear log-amps to provide absorbance and absolute power measurements for AAC and APC control loops. A simple difference amplifier arrangement, using on-chip operational amplifiers, provides a compact solution, but it may require additional error correction if logarithmic slope mismatch is unacceptable. A slightly more complicated solution involves using a modified Wilson current-mirror. The current-mirror approach is essentially immune to channel-to-channel mismatch and is capable of providing more than 5 decades of measurement and control range.

NOTES

[1] This outstandingly important facet of the bipolar junction transistor (BJT) is a feature of the deeply fundamental physics that govern minority-carrier conduction in a junction device. An early paper on the subject is: "Large-signal behavior of junction transistors," Ebers, I., and J. Moll, *Proceedings of the IRE*, December 1954, pp. 1761-1772.

[2] "Multiplication and logarithmic conversion by operational-amplifier-transistor circuits," Paterson, W., *Review of Scientific Instruments*, 34-12, December 1963.

[3] "Translinear circuits: a proposed classification," Gilbert, B., *Electronics Letters*, 11- 1, 1975, pp. 14-16.

[4] *Nonlinear Circuits Handbook*, Engineering Staff of Analog Devices, Inc., Sheingold, D., ed. Norwood, MA: Analog Devices, Inc. (1974). (*out of print*)

This article can be found at http://www.analog.com/library/analogDialogue/archives/37-12/voa.html

PRODUCT INTRODUCTIONS: VOLUME 37, NUMBER 4

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