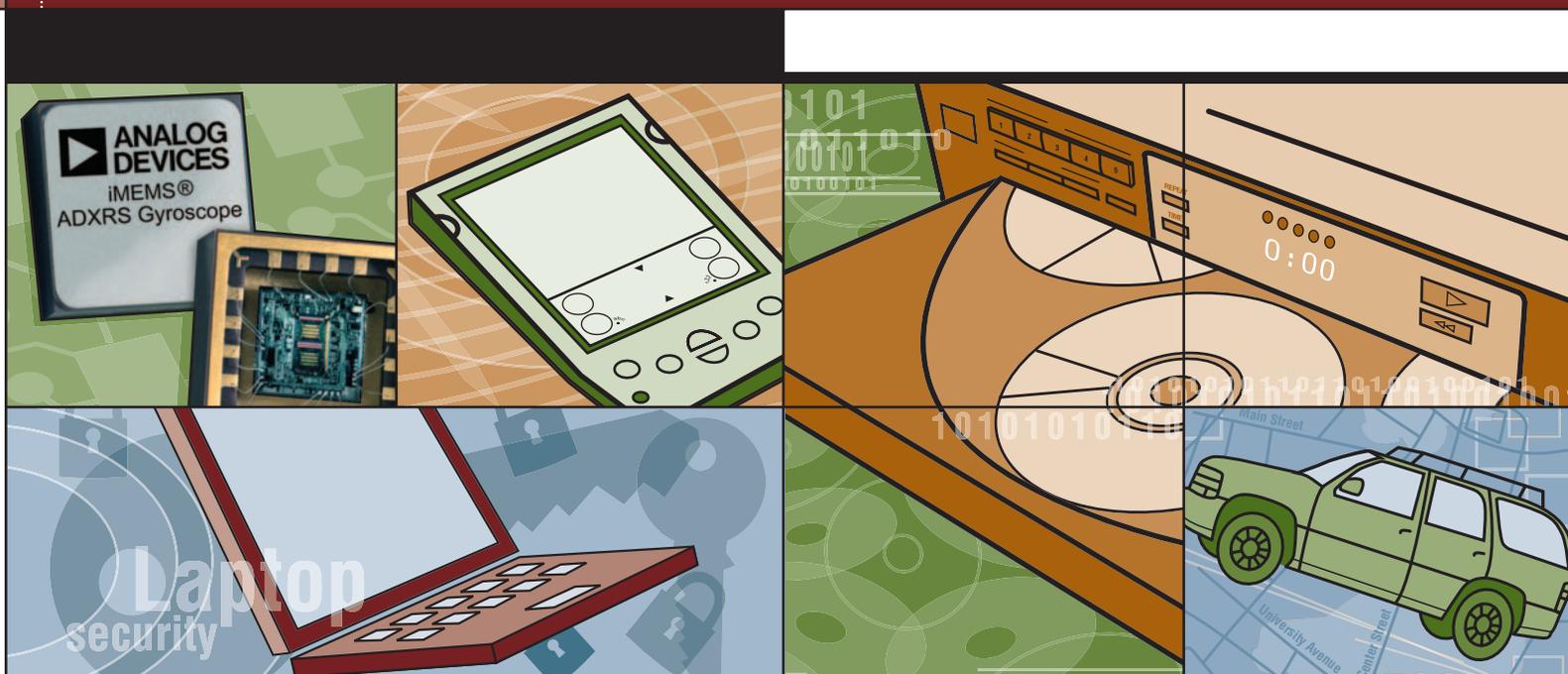


Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing



Volume 37, Number 1, 2003

Editor's Notes, Authors	2
Getting 14-bit Integral Linearity from a 32-Channel 14-Bit String DAC	3
Glueless, Hot-Swappable CompactFlash™ Interface	7
New iMEMS Angular Rate-Sensing Gyroscope	12
New Products	15



www.analog.com

Editor's Notes

Welcome to 4-12 publication

As a few of our most devout readers are perhaps already aware, we are now committed to a schedule that is a laid-back equivalent of "7-24"—i.e., distributing a print edition four times a year and hosting an online edition updated monthly. Each edition has its unique advantages—and disadvantages. Fortunately, the strengths and weaknesses of one complement the minuses and pluses of the other. Together they fill a multitude of needs.



Available free, the online edition¹ boasts freshness. It is here that the articles destined to endure in this print edition first see the light of the CRT or flat-panel display—both as informal HTMLs with useful hyperlinks to associated information, and as easy-to-print dressed-up PDFs.

The online edition also features brief descriptions of timely new products (available in quantity) and pre-release products (available for sampling), with links to data sheets and other information on the ADI website. Also included is "Potpourri," a user-friendly means to access a huge variety of current online information—both on the ADI website and elsewhere. Potpourri includes links to "what's new," *Analog Dialogue* archives, application notes, technical support, patents, data sheet revisions, articles in the trade press, book reviews, and much more. The online edition also gives you the power to immediately feed back questions and comments.

Its main weakness is that it's only available through an electronic medium. And you can't read it in hard copy unless you print it out. The print edition, on the other hand, can be carried and read just about anywhere, under any conditions (except darkness). It includes the articles published during the most recent calendar quarter (and their authors' bios), and it lists all the products released during that quarter. It may also include other material that we think you would like to see. Since it's printed on paper, you can make annotations, even write phone numbers and recipes in blank areas. If you wish, you can keep it for your print library—and you can trust that the contents will not change during its lifetime (but unfortunately, the rare mistake or typo will similarly be "cast in concrete"!).

The best news of all is that you can subscribe to both for free! Besides getting the best of both worlds, you'll find one more benefit: Your monthly visit to *Analog Dialogue* online will enhance your ability to penetrate the greater ADI website from a new point of view, one that may have even more immediacy than the design of the Analog Devices home page² allows.

—Dan Sheingold, Editor

Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing.

Analog Dialogue is the technical magazine of Analog Devices. It discusses products, applications, technology, and techniques for analog, digital, and mixed signal processing.

Home Archives Search Feedback Subscribe Analog Devices

Volume 37 - March 2003

Timely Information New-Product Briefs: Recently released products, normally available from stock. Pre-Release Products: These front-line products are on their way to being fully released. Potpourri: Links to all sorts of "good stuff": Application Notes, Articles, Books, Data Sheets, Patents... Editor's Notes: Do you like the full color articles? Please send us your feedback. Book Reviews myAnalog	Current Feature Articles New iMEMS Angular Rate-Sensing Gyroscope With full-scale ranges of 150°/s and 300°/s, the new ADXRS150 and ADXRS300 represent a quantum jump in gyro technology. The first commercially available surface-micromachined angular rate sensors with integrated electronics, they are smaller—with lower power consumption, and better immunity to shock and vibration—than any gyros having Getting 14-Bit Performance from a 32-Channel 14-Bit String DAC The AD5532 32-channel, 14-bit voltage output D/A converter can be used in DAC mode or <i>Infinite Sample-and-Hold</i> mode. The DACs have 14-bit monotonicity, but only $\pm 0.39\%$ integral nonlinearity. This article shows how the DACs can be calibrated to provide 14-bit performance. Glueless, Hot-Swappable CompactFlash™ Interface CompactFlash cards are used in MP3 players, digital cameras, handheld PCs, and many other electronic devices, and can be used for nonvolatile storage and transfer of music, pictures, and data. This article describes a simple interface between the ADSP-2191M digital signal processor and a CompactFlash card. Recent Feature Articles
---	--

ANALOG DEVICES
Copyright 1995-2003 Analog Devices, Inc. All rights reserved.

¹<http://www.analog.com/analogdialogue>

²<http://www.analog.com>

AUTHORS

John Geen (page 12) has been with Analog Devices (ADI) for nine years. He graduated with honors in Chemistry from the University of Manchester, England, in 1968, and subsequently earned degrees in Electrical Engineering and Mathematics. He has spent most of his working life designing precision electronics and inertial sensors for Sperry Gyroscope, British Aerospace, and Northrop. During that time he has been granted over 20 patents. He has concentrated on MEMS accelerometers and gyroscopes since 1988.



David Krakauer (page 12) is Program Manager for iMEMS gyro products in ADI's Micromachined Products Division. Previously, he was strategic marketing manager for mixed-signal DSPs. Prior to joining Analog Devices, David was a device and reliability engineer at Digital Equipment Corporation, and was also product development manager for Digital's graphics-accelerator ICs. He holds four US patents and has authored or co-authored more than 10 papers on solid-state physics and reliability. David holds bachelor's and master's degrees in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology—and an MBA from MIT's Sloan School of Management.



Albert O'Grady (page 3) is a Staff Engineer with the general-purpose digital-to-analog converter (DAC) product line Applications Group, in Limerick, Ireland. He works on new product definitions and provides product and customer support. Albert holds a BEng from the University of Limerick and has authored several technical articles on high resolution A/D and D/A converters. In his spare time, he enjoys reading and playing badminton and tennis.



John Tomarakos (page 7) is a DSP Field Applications Engineer for Analog Devices, focusing on automotive digital audio and telematics systems. He received a BSEE degree from the University of Pittsburgh in 1992. From 1995 to 2002, he was a member of ADI's DSP Central Applications Team, in Norwood, MA, supporting the ADSP-218x and ADSP-2116x digital signal processor families.



Analog Dialogue

www.analog.com/analogdialogue

dialogue.editor@analog.com

Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 37 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*on-line*, monthly at the above URL, and—less frequently—in *print*, as periodic retrospective collections of articles that have appeared on-line. In addition to technical articles, the on-line edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the www.analog.com site—the virtual world of *Analog Devices*. In addition to all its current information, the *Analog Dialogue* site has archives with all recent editions, starting from Volume 29, Number 2 (1995), plus three special anniversary issues, containing useful articles extracted from earlier editions, going all the way back to Volume 1, Number 1.

If you wish to subscribe to—or receive copies of—the print edition, please go to www.analog.com/analogdialogue and click on <subscribe>. Your comments are always welcome; please send messages to dialogue.editor@analog.com or to these individuals: Dan Sheingold, Editor [dan.sheingold@analog.com] or Scott Wayne, Managing Editor and Publisher [scott.wayne@analog.com].

Getting 14-Bit Performance from a 32-Channel 14-Bit String DAC

by Albert O'Grady [albert.ograde@analog.com]

OVERVIEW

The AD5532 32-channel, 14-bit voltage output D/A converter can be used in *DAC* mode (used for accessing multiple analog representations of *digital* data) or *Infinite Sample-and-Hold* (ISHA) mode (for storing and accessing analog representations of analog data). The DACs have 14-bit monotonicity, but only $\pm 0.39\%$ integral nonlinearity. This article shows how the DACs can be calibrated to provide 14-bit performance.

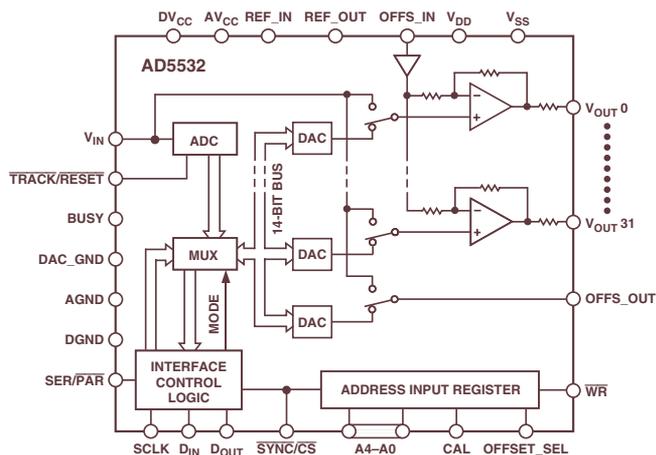


Figure 1. AD5532 Functional block diagram.

In *DAC* mode, the selected DAC register is written to via the 3-wire serial interface; the analog output (VOUT) for this DAC is then updated to reflect the new contents of the DAC register. DAC selection is accomplished via five address bits, A0-A4. The reference, the voltage applied to the OFFS_IN pin, and the gain of the output amplifier combine to determine the output range of the AD5532.

In *ISHA* mode, the input voltage, VIN, is sampled and converted into a digital word. The noninverting input to the selected (*n*th) output buffer (gain and offset stage) is tied to VIN during the acquisition period to avoid transient spurious outputs while the *n*th DAC acquires the correct code, a step completed in 16 μ s max. The updated DAC output then is connected to the noninverting input of the *n*th output buffer and assumes control of its output voltage. Since the channel output voltage is effectively the output of a DAC with a fixed input, there is no droop associated with it. As long as power is maintained to the device, the output voltage will remain constant until this channel is addressed again.

The analog output is restricted to a range from VSS + 2 V to VDD - 2 V because of headroom constraints in the output amplifier. The device is operated with AVCC = 5 V $\pm 5\%$, DVCC = 2.7 V to 5.25 V, VSS = -4.75 V to -16.5 V, and VDD = 8 V to 16.5 V; and it requires a stable +3-V reference on REF_IN, as well as an offset voltage on OFFS_IN.

In *DAC* mode of operation, the AD5532's DACs are guaranteed monotonic to 14 bits (differential nonlinearity <1 LSB)—thus ideally suiting them for closed-loop control applications. *Accuracy*, however, is limited by the space-saving string-DAC architecture. The DACs' specified *integral nonlinearity* (INL) error is 0.39% max of full scale (0.15% typical), or 64 (24.5) least significant bits in a 14-bit device. We can thus say that worst-case DAC integral linearity is comparable to that of an 8-bit device, even though it has 14-bit resolution.

This level of worst-case performance is acceptable for many applications, especially considering that the AD5532 can at any time economically and compactly store and read out 32 analog data points with 61-part per million resolution. But there are many applications where, although this kind of performance is essential, better accuracy is also necessary. Our purpose here is to show a way to calibrate the AD5532 for full 14-bit performance with a maximum of only 256 calibration coefficients (128 data points) per DAC, using a controller and a maximum of 8,192 slots of memory. Figure 2 shows the kind of improvement that can be obtained.

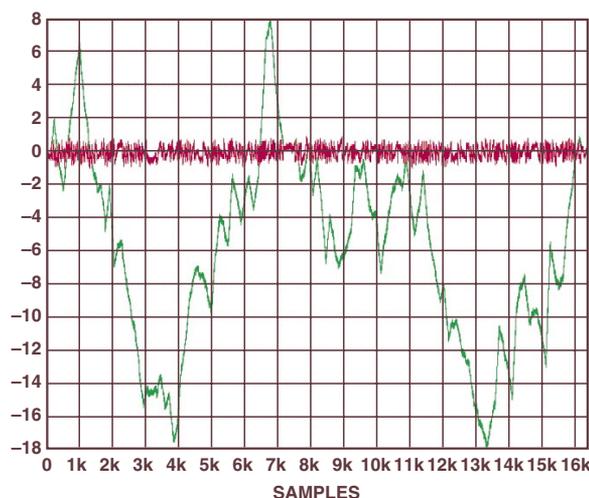


Figure 2. Uncalibrated linearity error compared with post-calibration linearity error for a 128-point calibration of a typical AD5532 channel at 25°C.

The following describes the basic DAC architecture and a method of calibration that can be easily implemented to achieve an INL error level of 1 LSB.

DAC Architecture

The common *string DAC* is one of the oldest and simplest DAC circuit concepts. Resistor-string DAC implementations are inherently monotonic by design and are characterized by simplicity, small size (per resistor), and low power consumption. But a major drawback is that 2^N resistors are required to implement it directly—e.g., 16,384 for 14 bits. In order to reduce the number of resistors and die size, the AD5532 incorporates two 128-resistor strings (7 bits)—a main string DAC for the 7 more significant bits, and a 7-bit sub string DAC. The basic architecture is shown in Figure 3 (US patent 5,969,657). The sub string DAC straddles up and down the main string, always in parallel with one of the main string resistors.

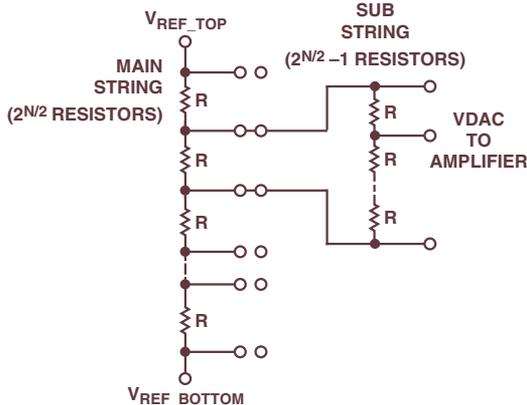


Figure 3. General string-DAC architecture.

Directly multiplying potentiometer-style resistive DACs suffer nonlinearity of the step size due to the variable loading of the sub string in parallel with the main string. But in DACs such as the AD5532, the loading of the sub string is the same at all levels and is treated not as a major error source, but as a characteristic of the DAC transfer function. The sub string loading error is 1 LSB.

The AD5532 DAC, using the architecture outlined above, is made up of a 7-bit-string main DAC (128 resistors) and a 7-bit-string sub-DAC (127 resistors) that bridges individual resistors of the main DAC. The integral nonlinearity error (INL) is determined by the matching of the main-DAC resistors. The sub-DAC provides the lower 127 codes of the transfer function. The linearity of the sub-DAC can be approximated by piecewise-linear segments.

DAC Transfer Function

The main DACs on the AD5532 are lifted off DACGND by typically 50 mV (by means of resistors at the bottom of the DAC). So the bottom of a DAC is typically at 50 mV, while the top of the DAC is typically at V_{REF} . Figure 4 shows how the nominal DAC transfer function is derived for a single channel.

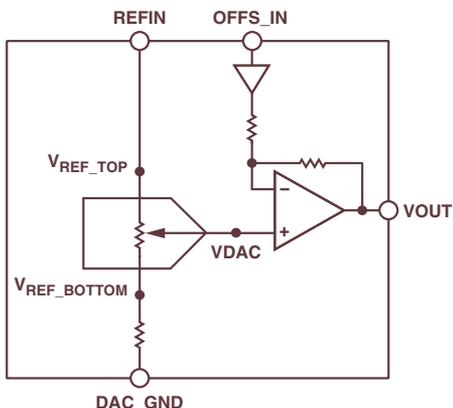


Figure 4. AD5532 DAC equivalent circuit.

The standard DAC transfer function that applies to the AD5532 is:

$$V_{DAC} = (V_{REF_TOP} - V_{REF_BOTTOM}) \frac{N}{16384} + V_{REF_BOTTOM}$$

where

N = DAC code value in decimal ($0 < N < 16383$)

$V_{REF_TOP} = V_{REF}$ and $V_{REF_BOTTOM} = 50 \text{ mV}$ (typ)

The output stage then amplifies and offsets the V_{DAC} output as follows:

$$V_{OUT} = Gain \times V_{DAC} - (Gain - 1) \times V_{OFFS_IN}$$

where $Gain$ is typically 3.52 and V_{OFFS_IN} is whatever the user programs.

For $V_{OFFS_IN} = 0$ and $V_{REF} = 3 \text{ V}$

$$V_{OUT} \text{ (zero code)} = 3.52 \times 50 \text{ mV} = 176 \text{ mV (typ)}$$

$$V_{OUT} \text{ (mid-scale)} = 3.52 \times 1.525 \text{ V} = 5.368 \text{ V (typ)}$$

$$V_{OUT} \text{ (full-scale)} = 3.52 \times 3 \text{ V} = 10.56 \text{ V (typ)}$$

Calibration Scheme

As noted above, this calibration scheme applies to all parts in the AD5532 family. The overall INL curve can be thought of as 128 piecewise-linear segments—corresponding to deviations in resistance value in the upper string—which are then interpolated linearly in the lower string. Because the small resistance deviations in the upper resistor string—which produce significant nonlinearities at the 14-bit level—will vary from channel to channel, and part to part, there is no “typical” INL curve; each DAC needs to be individually calibrated. The calibration scheme outlined here generates corrections to the lower 128 codes using an $Mx + C$ approximation for correction values in each segment. C is the required correction at the beginning of a segment, M is the stored slope to the beginning of the next segment, and x is the analog ratio corresponding to a given 7-bit code.

Thus the user can develop a calibration table by measuring the difference, C , between the expected value and the actual value at each of the upper 128 codes, calculating the incremental slopes (M), and storing both values in memory for every 128-point interval, as shown in Figure 5. Then, during run time, determine the segment, and thus C & M , from the upper 7 bits, compute the interpolation value determined by the lower 7 bits, and apply the correction to the DAC input.

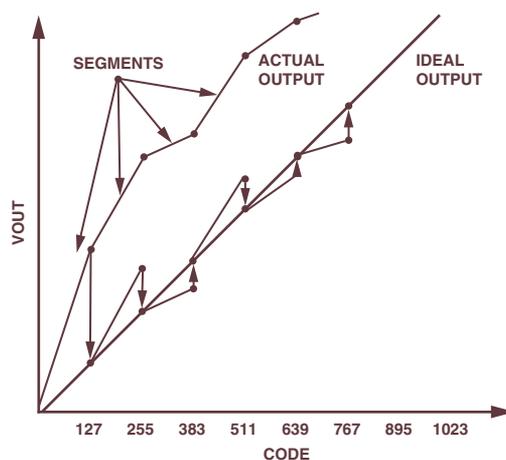


Figure 5. Using DAC segments to linearize the transfer function.

Calibrating every 128 codes—i.e., every segment, will reduce the INL error to less than ± 1 LSB at the 14-bit level from the worst case ± 64 LSBs for the uncalibrated DAC. If all the correction data must be stored in less memory than 8192 words, the number of calibration points can be reduced by increasing the calibration interval to 256 or 512 points—but this will reduce the overall integral linearity.

Figure 6 is a graph of linearity error for an AD5532 DAC channel before calibration, typically of the order of 10 bits. In all these plots, the Y axis represents the linearity error expressed in LSBs (1 LSB = 61 ppm), while the X axis is the 14-bit code loaded to the DAC.

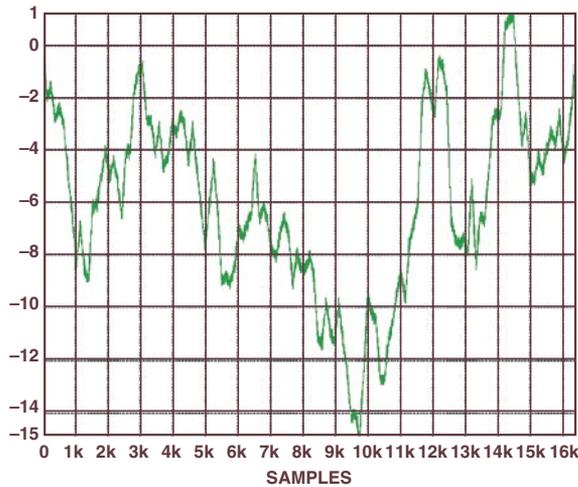


Figure 6. AD5532 Pre-calibration linearity plot.

Figure 7 shows the nonlinearity errors on the same channel, following the implementation of a 128-point calibration, as outlined above. It can be seen that the INL error is now within ± 1 LSB.

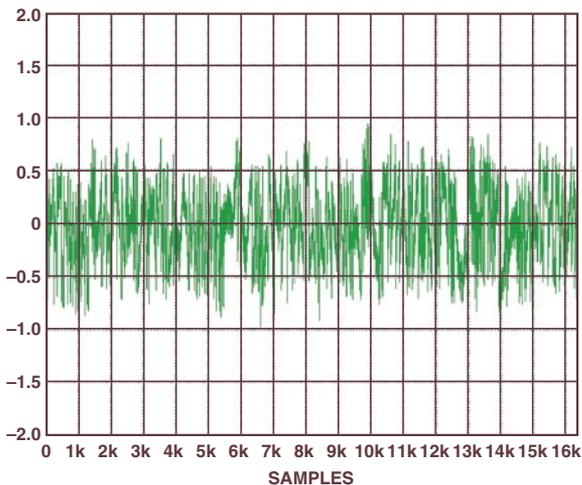


Figure 7. Post-calibration linearity errors after 128-point calibration.

The plots in Figures 6 and 7 are at 25°C. Appendix A shows the linearity errors at -40°C and +85°C following the implementation of a 128-point calibration scheme at 25°C. The worst-case errors appear to be about twice as great as at 25°C.

As noted above, calibration can also be implemented using a smaller number of calibration points. The increase in linearity errors that results from using fewer calibration points is demonstrated in Appendix B.

Hardware Implementation

Figure 8 shows a typical hardware implementation using the AD5532. Generally the controller writes directly to the AD5532, providing addressing and calculating calibrated data input values to update the relevant channels.

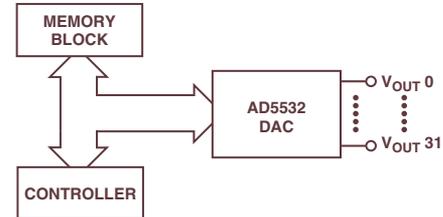


Figure 8. Typical hardware implementation.

The calibration scheme requires the addition of a memory block to store the M and C calibration data for each segment in the DAC transfer function. Using a 128-point calibration scheme, 256 calibration coefficients need to be stored for each DAC.

Calibrating the complete AD5532 requires that 8192 coefficients be stored. In terms of memory size, the slope coefficient (M) will typically require 6 bits, and the offset coefficient (C) also requires about 6 bits. The memory size required can be reduced at the expense of accuracy, as noted above and in Appendix B.

In writing data to a specific DAC, the controller takes the input code and goes to the memory to pick up the relevant M and C coefficients for the segment defined by the input code. The controller then performs a linear interpolation to determine the correct code to write to the DAC.

CONCLUSION

Using a simple interpolation scheme, it is possible to dramatically improve the linearity performance of the AD5532 family of DAC products.

We have shown that 14-bit linearity performance can be achieved following a 128-point calibration at 25°C. Pre-calibration linearity is typically at the 8-to-10-bit level.

All that is required to upgrade an existing AD5532 for improved performance in a system with computing power is the ability to generate calibration information and provide a memory block to store the calibration coefficients. ▶

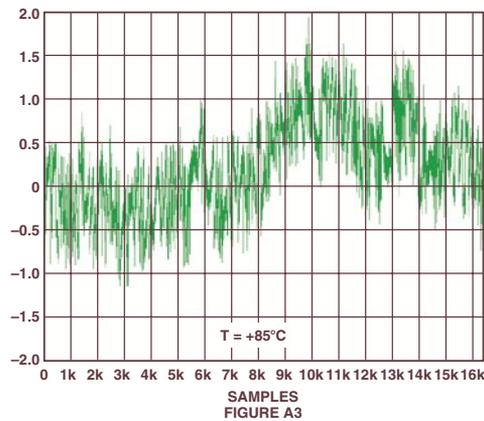
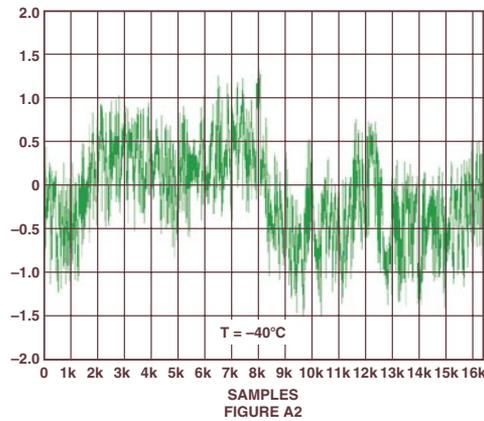
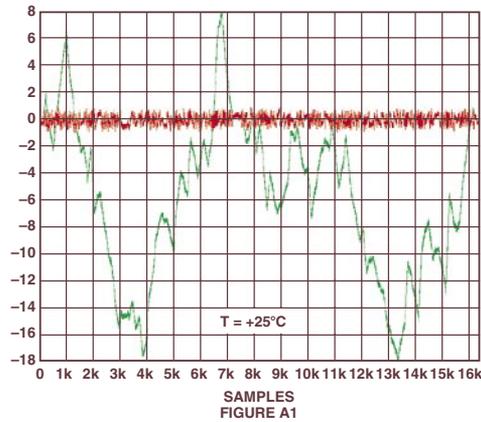
ACKNOWLEDGEMENTS

We wish to thank Donal Geraghty, Patrick Kirby, John O'Sullivan, and Catherine Redmond for their valuable contributions.

APPENDIX A

Linearity at other temperatures after calibration at 25°C

Figure A1 shows the uncalibrated linearity performance and the post-calibration linearity error following a 128-point calibration on a single AD5532 channel at 25°C. Figures A2 and A3 show the performance versus temperature following the calibration at 25°C. The plots show the linearity error (Y axis) in LSBs versus digital input code (X axis).

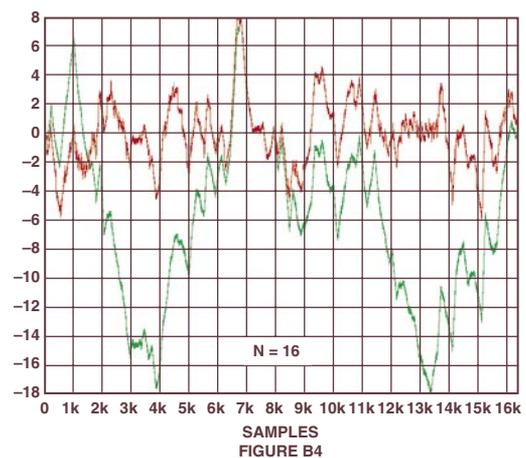
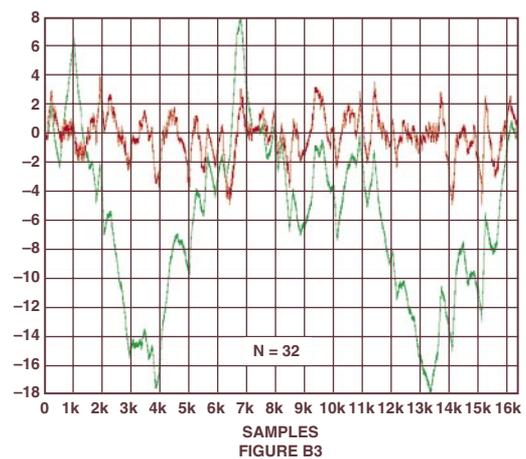
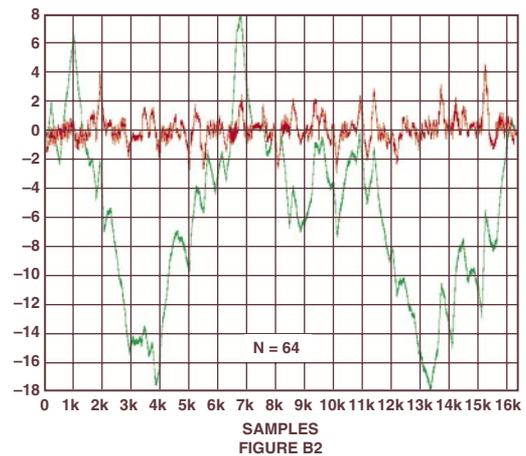
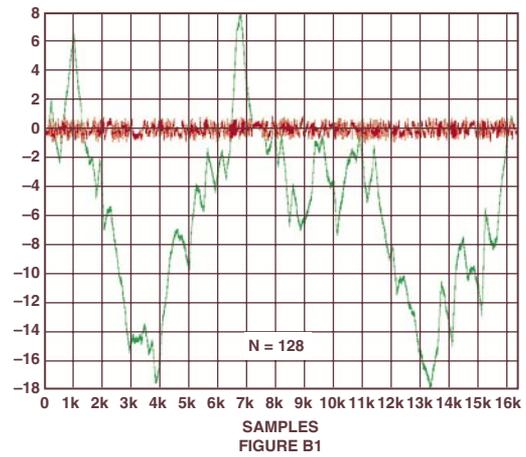


Figures A1,2,3. AD5532 uncalibrated linearity errors and the improved linearity following a 128-point calibration at +25°C, -40°C, and +85°C. Note the change in scale for A2 and A3.

APPENDIX B

Achievable performance with a reduced number of calibration points

Optimum performance in calibrating the AD5532—with reasonable effort—is achieved by implementing a 128-point calibration scheme. In order to reduce the calibration time and the memory requirement, the number of calibration points can be reduced at the expense of overall accuracy. The plots included in Figures B1, B2, B3, B4 compare the pre-calibration errors with the successively reduced improvement achieved using 128, 64, 32, and 16 calibration points (25°C).



Figures B1,2,3,4. AD5532 linearity performance without calibration—and following respective 128-, 64-, 32-, and 16-point calibrations at 25°C.

Glue-less, Hot-Swappable CompactFlash™ Storage-Card Interface with the ADSP-2191M Digital Signal Processor

by John Tomarakos [john.tomarakos@analog.com]

INTRODUCTION

Within the past few years, we have witnessed in the consumer marketplace a proliferation of portable handheld devices supported by the use of small, high-density, removable storage media. Walk into any consumer electronics store, and you will see the array of MP3 players, digital cameras, and PDAs, boasting hundreds of megabytes of expandable offline nonvolatile storage. With this impressive storage capability, users can download their favorite MP3s or upload their newly snapped JPEG image files between the portable device and a desktop PC. My first digital camera included a strange little matchbox-sized card that could be easily ejected and used to upload all of my JPEG files to the PC. This *CompactFlash™* storage card (Figure 1) has become a *de facto* standard for portable compact storage of multimedia files.

Today, card slots for CompactFlash exist in hundreds of digital cameras, handheld or palm-size PCs, MP3 players, voice-memo recorders, and other types of electronic equipment—including printers, heart monitors, and defibrillators—perhaps more so than any other competitive small form-factor cards. CompactFlash cards, designed to be small, removable, and durable, are offered in sizes from 8 megabytes up to 1 gigabyte.



Figure 1. CompactFlash storage card size comparison. CompactFlash and CF are trademarks of the CompactFlash Association.

In addition to its small size, the CompactFlash (CF) has the advantage of acting like any PC ATA (IDE) hard-disk, floppy, or zip disk drive in a Type II PC. (*ATA* was the standard bus interface on the original IBM AT computer and is also called *IDE*, for Integrated Drive Electronics.) CompactFlash supports the ATA command register set, but it is more reliable for data storage than an IDE hard disk drive, because it has no moving parts. It operates at speeds of traditional hard-disk drives, while consuming less power. Because it is ATA-compatible, it can be formatted like any hard drive or floppy diskette—as an alternative way of transferring files to or from a personal computer.

*All brand or product names mentioned are trademarks or registered trademarks of their respective holders.

A Windows/DOS-formatted file can easily be copied from a CF card that has been removed from any ATA-compatible device (such as a digital camera or Palm™-size PC). The data on the card can be transferred to (or from) a desktop personal computer through a high-speed, low-cost CompactFlash reader/writer attached to the computer's USB or parallel port. In fact, Windows 2000 and XP will automatically recognize a CF card inserted into a CF USB reader/writer and assign a logical drive letter to the card under Windows Explorer. Any software application then has access to it as file storage. Plug a CF card into a USB reader/writer connected to a PC, and your favorite MP3 song titles can be simply “dragged and dropped” to the card in a matter of seconds, ready for playback on a portable MP3 device. From the perspective of embedded digital signal processing (DSP), a CompactFlash is a great way to save recorded real-time digitized streams of data for temporary storage or off-line retrieval. Embedded-system designers have already begun to use them as a way to expand a processor's limited external-address-range capabilities.

When evaluating the use of a CompactFlash, designers will often ask these questions: How difficult is it to use a CompactFlash card in my DSP-based system? How do I physically connect a CompactFlash to a DSP? Can it be interfaced without any external components or logic? How difficult is it to program an ATA interface with a CompactFlash using a DSP? Can a DSP support a FAT-16 (16-bit cluster-addressed *file allocation table*) file system like that of an Intel-based PC?

This article will provide details on how to design a glue-less, hot-swappable interface to a CompactFlash storage card—using the ADSP-2191M digital signal processor—for a portable MP3 player application. The ADSP-2191 is a 16-bit, 160-MIPS (million-instruction-per-second) processor, which contains 64 K-words of internal on-chip memory and a variety of memory- and industry-standard peripheral interfaces. With its low dynamic power consumption, the ADSP-2191M was designed to be used in a variety of handheld portable devices—which are likely to use a compact, high-density, removable storage medium.

The interface was developed and tested using the ADSP-2191 EZ-KIT Lite Evaluation Platform. The completed prototype was ultimately used as a reference design for a 32-bit double precision MP3 player (decoder) based on an Analog Devices ADSP-219x DSP. In addition to describing the hardware interface between the ADSP-2191M and a CompactFlash, a DSP-based software assembly-language routine to execute read- and write-data sector transfers on the CompactFlash card using simple low-level ATA commands can be found at www.analog.com/library/analogDialogue/cf.html.

CompactFlash Overview

In 1995 the CompactFlash Association (CFA) was organized to develop a common standard interface format that would enable the capture, retention, and transportation of data—such as images or audio files—among a wide variety of digital systems. This collaboration resulted in the publishing of the CompactFlash specification. It defined a compact, high-density, removable storage interface that was basically a reduced 50-pin version of the PCMCIA or PC card specification, which was also electrically compatible with an IDE-hard drive. Because it is designed to be removable, the CF card can be “hot-swapped” in an active microprocessor-based system without requiring a system power-down or hard reset. The CompactFlash standard also supports three different industry-standard interfaces: *PC-Memory mode*, *PC-card I/O mode*, and *True-IDE mode*. When using *True-IDE* mode, the device can be connected to an IDE connector without requiring any extra supporting circuitry.

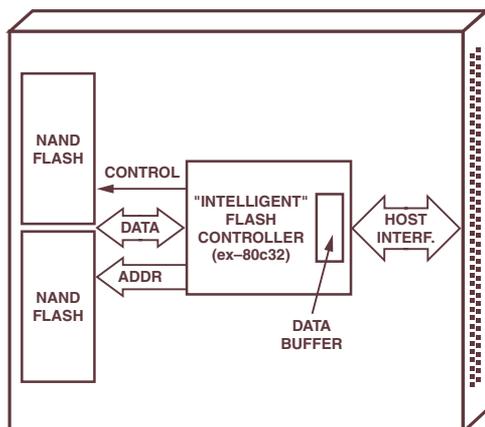


Figure 2. CompactFlash internal block diagram.

Figure 2 is a functional diagram common to a variety of CompactFlash storage cards. Hidden within the plastic casing is a small printed circuit board (Figure 3) containing a flash controller, some data-buffer memory, and flash modules. The flash controller chip executes disk-emulation software and contains some host-accessible memory-mapped registers that adhere to the ATA specification. To the host processor, the flash controller looks like a standard ATA (IDE) hard disk. The host processor (which might be a DSP) can access a set of ATA registers for command, status, and data words.



Figure 3. Inside printed circuit board of a CompactFlash (courtesy of Silicon Storage Technology, Inc.).

To transfer data, the host processor first loads seven ATA registers with configuration *data*; it then executes an operation by writing to an eighth *command* register. The flash controller, physically located between the nonvolatile (i.e., AND/NAND) memory chips and the external host interface, “emulates” the ATA command. The card also contains a memory buffer, which is controlled by the internal flash controller and used to transfer “sectors” (512-byte blocks) of information between the external processor and the memory chips. The flash controller is responsible for managing the interface protocol and also retrieving and placing data sectors between the external host processor and the storage memories. In addition, the flash controller handles error-correction code, performs diagnostics, identifies memory defects, and performs power-down operations when the card is in *idle* mode.

Using a CF Card with the ADSP-2191M

The ADSP-2191M digital signal processor (DSP) was chosen to implement an example of a functional low-cost, high-performance CompactFlash-based MP3 player, as Analog Devices already offers a commercially available double-precision 32-bit decoder design based on the ADSP-219x family. That solution was initially designed to read MP3 files from a CD drive. To demonstrate a functional glue-less, hot-swappable CF interface, we developed a modified version of the CD MP3 decoder to alternatively support

CF MP3 playback using the ADSP-2191 EZ-KIT Lite evaluation board and its associated software. Figure 4 shows a block diagram of the ADSP-2191 EZ-KIT CF-based MP3 decoder system. To identify and read MP3 DOS/WIN file clusters, the ADSP-2191 also executes a simplified FAT-16 file system to identify and load MP3 files downloaded to the card from a PC.



Figure 4. EZ-KIT Lite CF MP3 playback system.

The ADSP-2191M, a 16-bit, 160-MIPS single-chip microcomputer—optimized for digital signal processing and other high-speed applications—combines the ADSP-219x core architecture with three serial ports, two SPI-compatible ports, one UART port, a DMA controller, three programmable timers, and general-purpose I/O pins. The ADSP-2191M also integrates 64K words of on-chip memory; it thus has enough on-chip internal memory to easily integrate: an AC-97 audio driver, MP3 decoder, FAT-16 file system, low-level ATA commands, and host control commands—without requiring the use of external memory.

Figure 5 shows a functional block diagram of a CompactFlash 8-bit data interface to the ADSP-2191M DSP’s *external memory interface* (EMI) port. The CF *PC Card Memory mode* was selected as the mode of operation for connecting the CompactFlash to the DSP. This default mode of operation allows the ATA command/status registers to be simply memory-mapped to the ADSP-2191’s external address space. PC Card Memory mode access is very similar to *true-IDE mode* in that the ATA registers are accessed through an external memory address generated by the DSP core. However, while true-IDE mode is a 16-bit scheme, *PC-Card Memory mode* permits either 8- or 16-bit interfacing. Also, the two modes use different *read/write*-control strobes to transfer data. As we will see, this implementation also required neither external supporting glue logic for address decoding nor bus-isolation components for CF hot-swapping support. The only requirement is to include two 10-k Ω pull-up resistors on the *card detect 1* ($\overline{CD1}$) and *ready/busy* (RDY/ \overline{BSY}) pins.

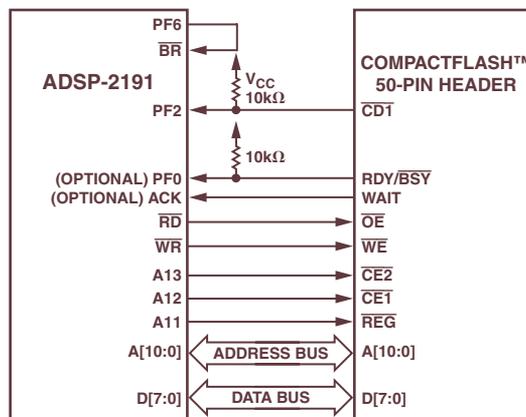


Figure 5. Block diagram of CompactFlash interconnection to the ADSP-2191.

Consider now the CF’s 8-bit memory-mode interface. While 16-bit accesses will improve data throughput by a factor of two, an 8-bit data bus will spare the 8 additional data lines required for a 16-bit implementation.

To address the ATA registers inside the card, the DSP’s A[10:0] address pins are connected to CF’s A[10:0] pins (refer to Table 1 for the DSP’s ATA register memory map).

Table 1. ADSP-2191-to-CompactFlash ‘PC Memory Mode’ Address-Map Truth Table.

DSP External Memory Address	A13 [CE2]	A12 [CE1]	A11 [REG]	A10	A[9:4]	A[3:0] (hex)	RD [OE] = 0 ATA Register Read	WR [WE] = 0 ATA Register Write
0x402800	1	0	1	0	X	0	Even RD Data	Even WR Data
0x402801	1	0	1	0	X	1	Error	Features
0x402802	1	0	1	0	X	2	Sector Count	Sector Count
0x402803	1	0	1	0	X	3	Sector Number	Sector Number
0x402804	1	0	1	0	X	4	Cylinder Lo	Cylinder Low
0x402805	1	0	1	0	X	5	Cylinder Hi	Cylinder Hi
0x402806	1	0	1	0	X	6	Select Card/Head	Select Card/Head
0x402807	1	0	1	0	X	7	Status	Command
0x402808	1	0	1	0	X	8	Dup Even RD Data	Dup Even WR Data
0x402809	1	0	1	0	X	9	Dup Odd RD Data	Dup Odd WR Data
0x40280D	1	0	1	0	X	D	Dup Error	Dup Features
0x40280E	1	0	1	0	X	E	Alt Status	Device Control
0x40280F	1	0	1	0	X	F	Drive Address	Reserved
0x402C08	1	0	1	1	X	8	Even RD Data	Even WR Data
0x402C09	1	0	1	1	X	9	Odd RD Data	Odd WR Data

REG pin activated when A11 is “0.” CE1 pin activated when A12 is “0.” CE2 deactivated by A13 set to “1” for 8-bit accesses.

Host-Processor Bus-Isolation Issues when Hot-Plugging a CompactFlash

A CompactFlash is designed so that the power pins can be connected first—before the bus signals are connected. This is defined in the CompactFlash specification as a recommendation that the power pins on the CF male 50-pin header be longer than the other pins—and that the card-detect pins be shorter than the other pins. The expectation here is that, as the card is inserted, the difference in the length of the pins would allow power to be applied to the card first—before all other address and data pins are connected to the host system—and, as the insertion is completed, the card detect pins will connect and signal to the host that the card is plugged in and ready to be accessed.

However, this is still not sufficient to protect the host processor from damage when “hot-swapping” or “hot-plugging” a CompactFlash into its host socket. A host processor’s address and data busses need to be isolated from transients produced by the CompactFlash device when it is undergoing a POR (power-on reset) and also while its internal pin capacitors are being charged. These operations can take up to 100 milliseconds after card insertion. The host’s run-time system should be designed such that it delays performing an external access and actively driving the external bus for at least 100 ms—avoiding bus contention with the CF’s POR sequence—after the CF is inserted into the slot. Immediate damage to the host’s pins could result; or damage could occur over the long term after dozens—or even hundreds—of slot insertions, depending on the duration of the bus contention.

What can be done to prevent bus contention during a POR phase after card insertion? The most commonly used design approach is to isolate the address and data bus lines with buffers or bidirectional bus transceivers, which would place the address and data lines in a high-impedance state until activated by a RD or WR strobe (see the article on bus switches in the last issue).

However, an attractive option is available when using the ADSP-2191M DSP, eliminating the need for external bus transceiver chips: The ADSP-2191M includes a pin called BR (Bus Request), which causes the DSP’s address and data pins to mimic the behavior of a bidirectional bus transceiver chip or buffer, such that when BR is driven low, all of the DSP’s address, data, and memory control strobes on the ADSP-2191’s external port will enter a high-impedance state and behave like inputs. Bus request is normally a function used by a DSP’s host processor to allow a host to gain control of the external bus and prevent the DSP from attempting an external memory access. When the granting of the external bus is given to a host with the use of BR (bus grant), the host can then access the same external memories or access

the DSP’s external port for host DMA transfers. However, to fully optimize for a glue-less CF interface, we can use the DSP’s own flag or GPIO pin to control the state of BR to disable the external bus.

In the case of an MP3 playback system, where no external memory or host parallel connection is required (a host processor alternatively would use the SPI port to control the MP3 player operation), the BR pin is free for use and hence can be controlled by the DSP itself. Under software control, an extra flag pin available on the DSP can be used to control the activation and de-activation of a “hot” DSP bus during CompactFlash card insertion and removal. In the system described here, the programmable I/O flag pin, PF6, is used to drive BR.

Initially, after the ADSP-2191M is powered up and executing initialization routines, it first disables the external bus through bus-request assertion to ensure that it will be safe for the CompactFlash device to be inserted. The ADSP-2191M then detects if the card has been inserted by periodically polling the CDI line connected to the PF2 flag pin, configured as an input (refer to BR connection in Figure 5). Once CDI is detected low, the ADSP-2191M, using a delay loop, will stall for a few hundred milliseconds (to allow for the 100-ms power-up reset and charging of the internal pin capacitors) before enabling the external bus out of its high-impedance state by releasing the Bus Request pin (which, again, is connected to the DSP’s own flag pin—configured as an output and controlled through software). After the bus is activated, the ADSP-2191M then resets the CF’s ATA registers, waits for the minimum CF reset period, and then polls the ATA status register to determine when the card is ready for read/write operations.

CONCLUSION

The ADSP-2191M DSP is well suited for low-cost, low-power portable applications requiring the use of compact, high-density, removable non-volatile storage cards. A glue-less, hot-swappable CompactFlash interface using the ADSP-2191M is demonstrated in the appendix. It does not require isolation buffers, discrete address decoding, or additional glue logic. To support hot-plugging of a CompactFlash, the ADSP-2191M offers the inherent ability, through the use of its Bus Request pin, to disable the external address and data buses during card insertion. This bus isolation is critical when power is first applied to a CompactFlash storage card, while it performs a power-on reset operation and internal pin capacitors are charged. Also included is a complete reference design based on the ADSP-2191 EZ-KIT Lite and an example of a DSP assembly-language program to execute ATA commands for transferring data between the ADSP-2191 and CompactFlash. 

APPENDIX

USING THE ADSP-2191 EZ-KIT LITE FOR COMPACTFLASH™ PROTOTYPING

CF Interfacing to ADSP-2191M

Using the EZ-KIT Lite, all eleven address lines on the CF header are connected to the DSP. However, the CF's A8, A7, A6, A5 and A4 pins can be tied to the GND pin on the CF 50-pin male header, since these are always driven to zero by the DSP for accessing common and attribute memory—they are also labeled as “don't care” in the CompactFlash Association specification. Since accesses to the card are performed at 8 bits, the DSP's D[7:0] pins are simply connected to CF's D[7:0] pins. The DSP's \overline{RD} and \overline{WR} , pins are connected to \overline{OE} and \overline{WE} respectively. To read and write internal control/status registers and read data sectors, the DSP performs asynchronous READ/WRITE cycles by driving the CF card's \overline{OE} and \overline{WE} strobes low. Additional DSP address lines, A11, A12, A13, are used as additional card select lines. A11 is connected to \overline{REG} , A12 is connected to $\overline{CE1}$, and A13 is connected to $\overline{CE2}$. When performing 8-bit accesses, by simply driving A[13:11] to certain combinations (see Table 1), we can control whether the access is to attribute or common memory, and whether the even or odd sector data byte is accessed.

So far, we've discussed the CF's address, data and control strobes. Now consider the remaining CF pins required to complete the interface. One general purpose I/O flag pin is used for CF card detection when it is inserted into the CF slot. The CF's $\overline{CD2}$ and $\overline{CD1}$ (card detect pins) are grounded internally to indicate that the CF card has been inserted. In this interface, the DSP's PF2 flag pin is connected to $\overline{CD1}$ pin. When the state of the $\overline{CD1}$ pin is '0', the DSP recognizes the insertion of the card. A pull-up resistor is recommended on $\overline{CD1}$ to keep PF2 high and prevent it from floating when the card is not inserted.

The CF's RDY/ \overline{BSY} pin can be connected to another programmable flag pin (PF0) to test whether the card is ready for data transfer or is busy performing internal operations. However, the BUSY and RDY bits can be also polled in the ATA Status or Alternate Status registers to detect whether the host is locked out or ready for data transfer; this removes the requirement for a physical connection to RDY/ \overline{BSY} .

Finally, the CF's \overline{WAIT} pin can be optionally connected to ACK to delay the completion of a \overline{RD} or \overline{WR} access by the DSP. This also is optional, because the ADSP-2191's MSxCTL register can be programmed to add *wait* states and divide the external port clock to meet the CompactFlash maximum read- or write-cycle times. By slowing down the DSP's external asynchronous read or write cycle to meet or exceed worst case CF access times, one can guarantee that data will be valid or latched upon release of the DSP's \overline{RD} or \overline{WR} memory strobes. To summarize, only 18 interconnections are required to develop a functional interface between the DSP and the CF.

To allow for the card to be reset under software control, while also providing access to the card's ATA registers, I mapped the CompactFlash card's Common and Attribute Memory banks. Bank 1 ($\overline{MS1}$) was mapped to *common memory* to access ATA registers, while Bank 2 ($\overline{MS2}$) was used to access *attribute memory* to make it feasible to perform a reset of the card under software control. This made unnecessary a hardwire connection of the CF's RESET line to a DSP flag pin. Notice however, that while the CF card is mapped to two different DSP external memory spaces, the $\overline{MS1}$ and $\overline{MS2}$ pins are not physically connected to the card's chip/memory enable pins (\overline{REG} , $\overline{CD2}$, $\overline{CD1}$) on the card. Simply generating the proper bank addresses will ensure whether attribute or common memory is being accessed (since \overline{REG} is connected to the A11 address pin and can be activated or deactivated regardless of bank address). The mapping to two different banks is necessary—as both memory spaces have different read/write

timing requirements, complying with the CFA's specification. Therefore, both memory banks are programmed using different wait-states and peripheral clock divide values.

Adapting the ADSP-2191 EZ-KIT Lite

Figure 6 shows the CF prototype system developed using the ADSP-2191 EZ-KIT Lite. Connecting the CF to the EZ-KIT is accomplished through the use of a PLCC-to-PGA adapter mounted over the EZ-KIT's PLCC boot flash, and a row of 0.1-inch headers to connect to some GPIO pins and also supply 3.3 volt power and GND to the card.

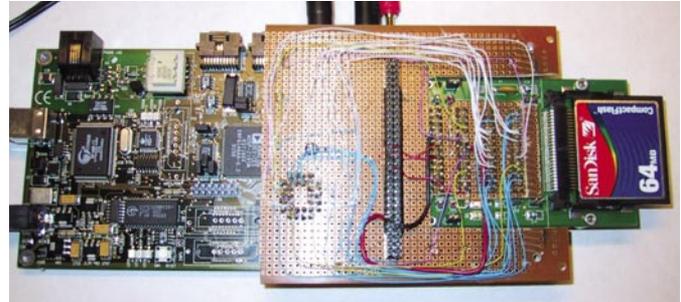


Figure 6. Sycard CompactFlash CF Extend 180 CIB connected to the ADSP-2191 EZ-KIT Lite.

The CompactFlash development board chosen for the interface was the CF Extend 180 Card Interface Board (CIB), manufactured by Sycard Technology (part #: 180CIB, which can be ordered online at www.sycard.com). The Sycard Technology card interface board allows for easy prototyping with a host processor and a CompactFlash card. The CompactFlash to be tested is simply inserted into the CIB's 50-pin CF male header. The CIB routes all CF signals to four sets of 0.1 inch standard 26-pin headers, providing easy access for soldering connections to a host and for mounting to a perforated board with 0.1-inch spaced holes. The connections were soldered, but I encountered no noise or signal integrity problems to interfere with the operation of the CF card (the CIB is a four-layer board with a separate VDD and GND plane for supplying power to the CF card).

To connect the accessed CF pins on the Sycard CIB to the ADSP-2191 on the EZ-KIT Lite, I chose to use a 32-pin PLCC-to-PGA LoClip adapter from Ironwood Electronics (part # LC-PLCC32-01, available at www.ironwoodelectronics.com). Figure 7 shows a top-, bottom- and side view of the adapter, and the way it is inserted over the EZ-KIT's ST Micro boot flash (M29W040B). The top PGA pins provided by the adapter are used to wire up to the Sycard CIB.

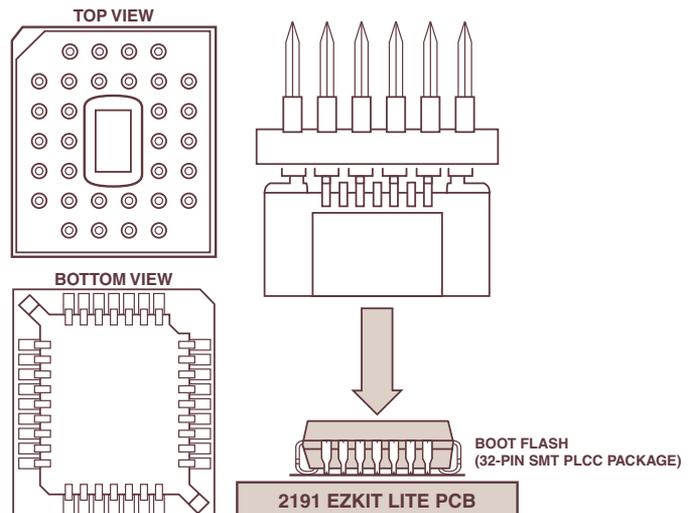


Figure 7. Ironwood Electronics PGA-to-PLCC Adapter.

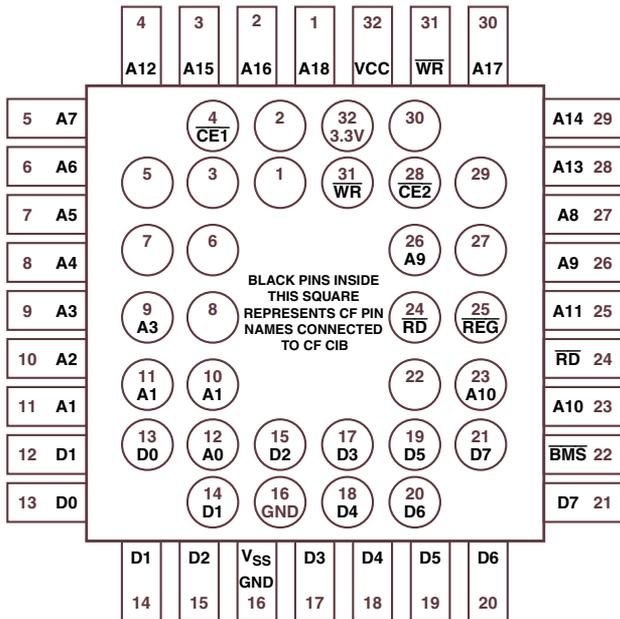


Figure 8. Ironwood Electronics PLCC-to-PGA adapter pin connections used for CompactFlash access.

Why was this adapter chosen—instead of accessing the external bus pins available on the EZ-KIT Lite? The EZ-KIT EMI external port P9/P10 headers (which provide access to all external port address and data bus pins) are not populated on currently shipping 2191 EZ-KITs, which offers a significant design challenge for wiring up a CompactFlash—otherwise a 16-bit data bus interface would have been chosen. However, with the use of the handy 32-pin PLCC-to-PGA LoClip connected over the boot flash on the EZ-KIT, we could then easily access data pins D[7:0], address pins A[18:0], \overline{RD} and \overline{WR} through standard 0.1-inch PGA headers; this is sufficient to enable 8-bit CompactFlash accesses (refer to Figure 8 for actual location of PGA pins used on the adapter).

The Ironwood Electronics LoClip allows the required number of DSP-to-CF interconnections to be kept to a minimum. As with a 16-bit data bus, 8-bit accesses provide the capability to address all data on the card, just by doubling accesses from 256

to 512 sector read/write cycles. In the case of MP3 playback on the ADSP-2191, 8-bit accesses are fast enough to meet MP3 input data-fill requirements, as the MP3 playback data rates (44.1 kHz) are much slower than the 160-MHz internal core clock rate. The MP3 block decoder is running in the background and accesses the card only when the next 4 sectors of data are needed in the input MP3 buffer. In fact, the FAT16 file system used here for reading MP3 file data clusters takes only about 2% of the ADSP-2191's 160 available MIPS.

Figure 9 shows the remaining connections needed by the CompactFlash via the EZ-KIT P9 and P14 headers. P9 provides access to the DSP's PF[7:0] pins through standard 0.1-inch headers. P9 is used to connect the CF's $\overline{CD1}$ and RDY/ \overline{BSY} pins to PF2 and PF0, respectively. \overline{BR} on the DSP is connected to PF6. No pull-up is needed since the board already ties \overline{BR} to 3.3 V through a 10 k Ω pull-up resistor. Lastly, to complete the connections between the card and the DSP, 3.3-volt VDD supply and GND are supplied through header P14 to the CompactFlash VDD and GND pins.

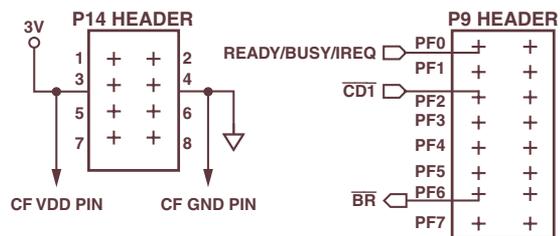


Figure 9. Signal connections required on EZ-KIT Lite P9 and P14 headers for supplying power.

Example of Assembly-Language Program for ATA Read/Write-Sector Command Implementation

ADSP-2191 assembly language subroutines demonstrating how to program the ATA interface to transfer sectors of data between the DSP and a CompactFlash storage card can be found at <http://www.analog.com/library/analogDialogue/cf.html>. These routines use the C/H/S mode of addressing (versus logical block addressing) to access the CompactFlash storage card's memory. As lowest-level access routines, they do not include any error or timeout code. They can serve as a basis for developing a standard file system format, such as FAT-16 used on PC-DOS/Windows machines.

New iMEMS® Angular-Rate-Sensing Gyroscope

by John Geen [john.geen@analog.com] and David Krakauer [david.krakauer@analog.com]
ADI Micromachined Products Division

INTRODUCTION

The new ADXRS150 and ADXRS300 gyros from Analog Devices, with full-scale ranges of 150°/s and 300°/s, represent a quantum jump in gyro technology. The first commercially available surface-micromachined angular rate sensors with integrated electronics, they are smaller—with lower power consumption, and better immunity to shock and vibration—than any gyros having comparable functionality. This genuine breakthrough is possible only because of the Analog Devices proprietary *integrated micro electro-mechanical system* (iMEMS) process, proven by use in millions of automotive accelerometers.

Product Description

Gyroscopes are used to measure *angular* rate—how quickly an object turns. The rotation is typically measured in reference to one of three axes: yaw, pitch, or roll.

Figure 1 shows a diagram representing each axis of sensitivity relative to a package mounted to a flat surface. A gyroscope with one axis of sensitivity can also be used to measure other axes by mounting the gyro differently, as shown in the right-hand diagram. Here, a yaw-axis gyro, such as the ADXRS150 or ADXRS300, is mounted on its side so that the yaw axis becomes the roll axis.

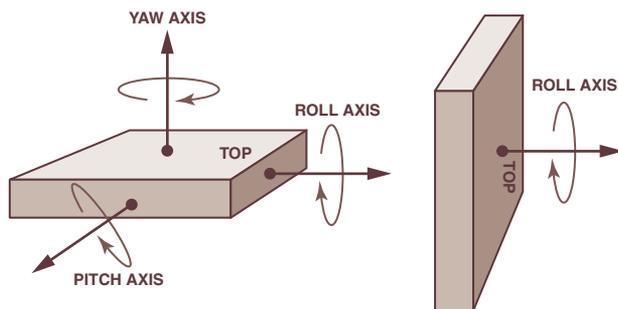


Figure 1. Gyro axes of rotational sensitivity. Depending on how a gyro normally sits, its primary axis of sensitivity can be one of the three axes of motion: yaw, pitch, or roll. The ADXRS150 and ADXRS300 are yaw-axis gyros, but they can measure rotation about other axes by appropriate mounting orientation. For example, at the right: a yaw-axis device is positioned to measure roll.

As an example of how a gyro could be used, a yaw-axis gyro mounted on a turntable rotating at 33 1/3 rpm (revolutions per minute) would measure a constant rotation of 360° times 33 1/3 rpm divided by 60 seconds, or 200°/s. The gyro would output a voltage proportional to the angular rate, as determined by its sensitivity, measured in millivolts per degree per second (mV/°/s). The full-scale voltage determines how much angular rate can be measured, so in the example of the turntable, a gyro would

need to have a full-scale voltage corresponding to at least 200°/s. Full-scale is limited by the available voltage swing divided by the sensitivity. The ADXRS300, for example, with 1.5 V full-scale and a sensitivity of 5 mV/°/s, handles a full-scale of 300°/s. The ADXRS150, has a more limited full-scale of 150°/s but a greater sensitivity of 12.5 mV/°/s.

One practical application is to measure how quickly a car turns by mounting a gyro inside the vehicle; if the gyro senses that the car is spinning out of control, differential braking engages to bring it back into control. The angular rate can also be integrated over time to determine angular position—particularly useful for maintaining continuity of GPS-based navigation when the satellite signal is lost for short periods of time.

Coriolis Acceleration

Analog Devices' ADXRS gyros measure angular rate by means of Coriolis acceleration. The Coriolis effect can be explained as follows, starting with Figure 2. Consider yourself standing on a rotating platform, near the center. Your speed relative to the ground is shown as the blue arrow lengths in Figure 2. If you were to move to a point near the outer edge of the platform, your speed would increase relative to the ground, as indicated by the longer blue arrow. The rate of increase of your tangential speed, caused by your radial velocity, is the *Coriolis* acceleration (after Gaspard G. de Coriolis, 1792-1843—a French mathematician).

If Ω is the angular rate and r the radius, the tangential velocity is Ωr . So, if r changes at speed, v , there will be a tangential acceleration Ωv . This is half of the Coriolis acceleration. There is another half from changing the direction of the radial velocity giving a total of $2\Omega v$ (see the Appendix). If you have mass, M , the platform must apply a force, $2M\Omega v$, to cause that acceleration, and the mass experiences a corresponding reaction force.

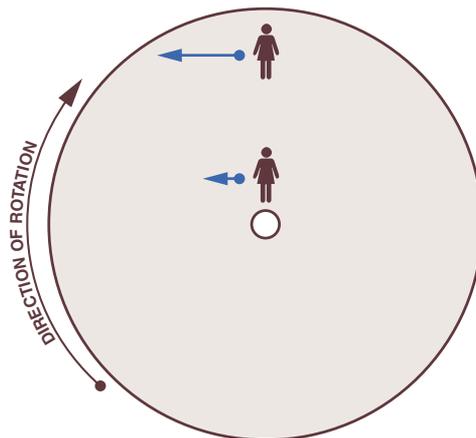


Figure 2. Coriolis acceleration example. A person moving northward toward the outer edge of a rotating platform must increase the westward speed component (blue arrows) to maintain a northbound course. The acceleration required is the *Coriolis acceleration*.

The ADXRS gyros take advantage of this effect by using a resonating mass analogous to the person moving out and in on a rotating platform. The mass is micromachined from polysilicon and is tethered to a polysilicon frame so that it can resonate only along one direction.

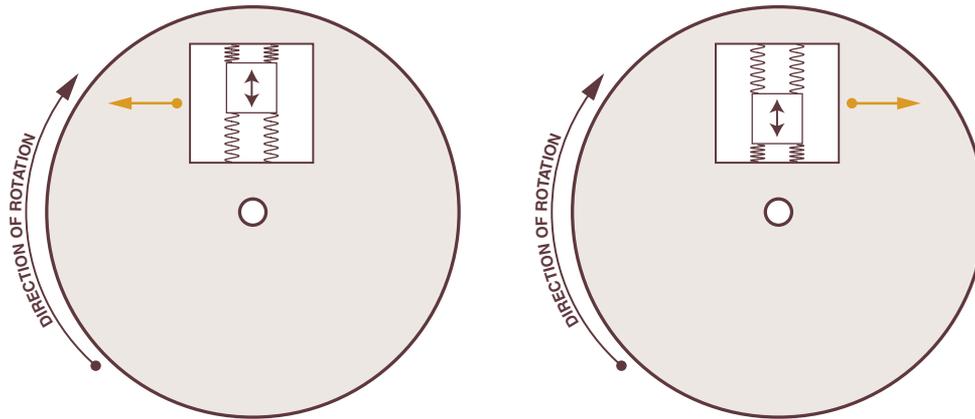


Figure 3. Demonstration of Coriolis effect in response to a resonating silicon mass suspended inside a frame. The orange arrows indicate the force applied to the structure, based on status of the resonating mass.

Figure 3 shows that when the resonating mass moves toward the outer edge of the rotation, it is accelerated to the right and exerts on the frame a reaction force to the left. When it moves toward the center of the rotation, it exerts a force to the right, as indicated by the orange arrows.

To measure the Coriolis acceleration, the frame containing the resonating mass is tethered to the substrate by springs at 90° relative to the resonating motion, as shown in Figure 4. This figure also shows the Coriolis sense fingers that are used to capacitively sense displacement of the frame in response to the force exerted by the mass, as described further on. If the springs have a stiffness, K , then the displacement resulting from the reaction force will be $2 \Omega v M / K$.

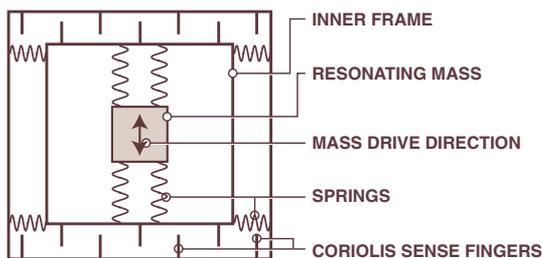


Figure 4. Schematic of the gyro's mechanical structure.

Figure 5, which shows the complete structure, demonstrates that as the resonating mass moves, and as the surface to which the gyro is mounted rotates, the mass and its frame experience the Coriolis acceleration and are translated 90° from the

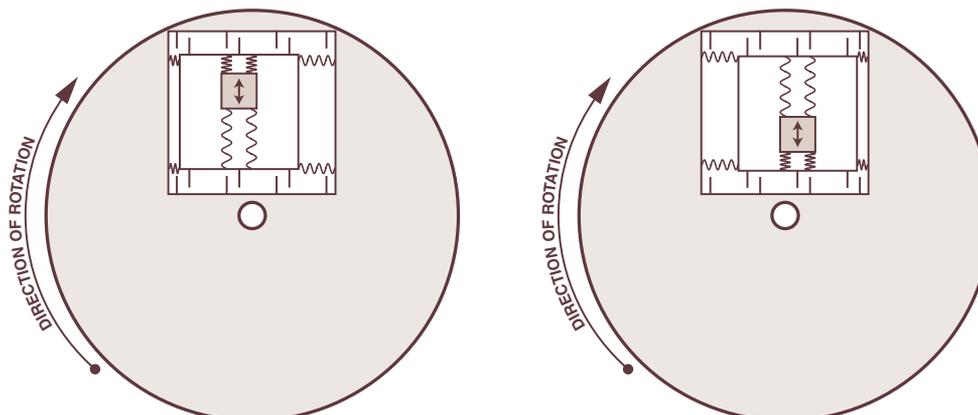


Figure 5. The frame and resonating mass are displaced laterally in response to the Coriolis effect. The displacement is determined from the change in capacitance between the Coriolis sense fingers on the frame and those attached to the substrate.

vibratory movement. As the rate of rotation increases, so does the displacement of the mass and the signal derived from the corresponding capacitance change.

It should be noted that the gyro may be placed anywhere on the rotating object and at any angle, so long as its sensing axis is parallel to the axis of rotation. The above explanation is intended to give an intuitive sense of the function and has been simplified by the placement of the gyro.

Capacitive Sensing

ADXRS gyros measure the displacement of the resonating mass and its frame due to the Coriolis effect through capacitive sensing elements attached to the resonator, as shown in Figures 4, 5, and 6. These elements are silicon beams inter-digitated with two sets of stationary silicon beams attached to the substrate, thus forming two nominally equal capacitors. Displacement due to angular rate induces a differential capacitance in this system. If the total capacitance is C and the spacing of the beams is g , then the differential capacitance is $2 \Omega v M C / g K$, and is directly proportional to the angular rate. The fidelity of this relationship is excellent in practice, with nonlinearity less than 0.1%.

The ADXRS gyro electronics can resolve capacitance changes as small as 12×10^{-21} farads (12 zeptofarads) from beam deflections as small as 0.00016 Angstroms (16 femtometers). The only way this can be utilized in a practical device is by situating the electronics, including amplifiers and filters, on the same die as the mechanical sensor. The differential signal alternates at the resonator frequency and can be extracted from the noise by correlation.

These sub atomic displacements are meaningful as the *average* positions of the surfaces of the beams, even though the individual atoms on the surface are moving randomly by much more. There are about 10^{12} atoms on the surfaces of the capacitors, so the statistical averaging of their individual motions reduces the uncertainty by a factor of 10^6 . So why can't we do 100 times better? The answer is that the impact of the *air molecules* causes the structure to move—although similarly averaged, their effect is far greater! So why not remove the air? The device is not operated in a vacuum because it is a very fine, thin film weighing only 4 micrograms; its flexures, only 1.7 microns wide, are suspended over the silicon substrate. Air cushions the structure, preventing it from being destroyed by violent shocks—even those experienced during firing of a guided shell from a howitzer (as demonstrated recently).

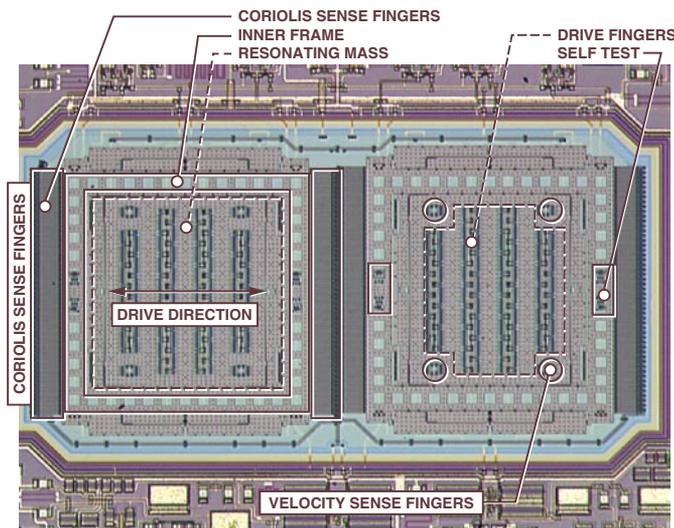


Figure 6. Photograph of mechanical sensor. The ADXRS gyros include two structures to enable differential sensing in order to reject environmental shock and vibration.

Features

Integration of electronics and mechanical elements is a key feature of products such as the ADXRS150 and ADXRS300, because it makes possible the smallest size and cost for a given performance level. Figure 7 is a photograph of the ADXRS die.

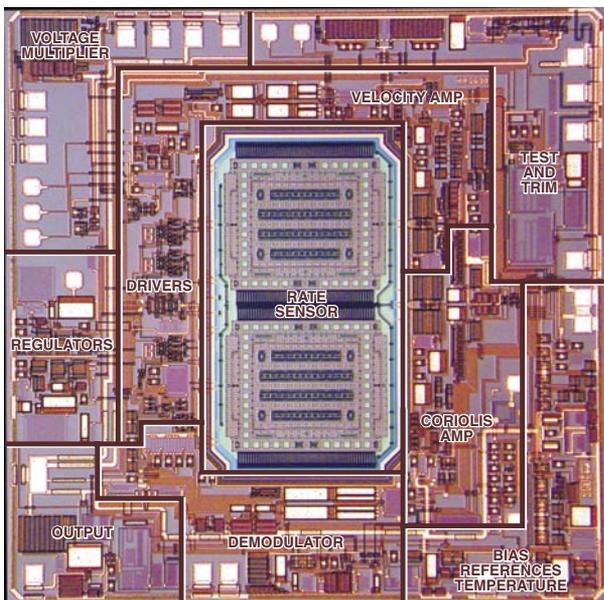


Figure 7. Photograph of ADXRS gyro die, highlighting the integration of the mechanical rate sensor and the signal conditioning electronics.

The ADXRS150 and ADXRS300 are housed in an industry-standard package that simplifies users' product development and production. The ceramic package—a 32-pin ball grid-array, (BGA)—measures 7 mm wide by 7 mm deep by 3 mm tall. It is at least 100 times smaller than any other gyro having similar performance. Besides their small size, these gyros consume 30 mW, far less power than similar gyros. The combination of small size and low power make these products ideally suited for consumer applications such as toy robots, scooters, and navigation devices.

Immunity to Shock and Vibration

One of the most important concerns for a gyro user is the device's ability to reliably provide an accurate angular rate-output signal—even in the presence of environmental shock and vibration. One example of such an application is automotive rollover detection, in which a gyro is used to detect whether *or not* a car (or SUV) is rolling over. Some rollover events are triggered by an impact with another object, such as a curb, that results in a shock to the vehicle. If the shock saturates the gyro sensor, and the gyro cannot filter it out, then the airbags may not deploy. Similarly, if a bump in the road results in a shock or vibration that translates into a rotational signal, the airbags might deploy when not needed—a considerable safety hazard!

As can be seen in Figures 6 and 7, the ADXRS gyros employ a novel approach to angular rate-sensing that makes it possible to reject shocks of up to $1,000g$ —they use two resonators to differentially sense signals and reject common-mode external accelerations that are unrelated to angular motion. This approach is, in part, the reason for the excellent immunity of the ADXRS gyros to shock and vibration. The two resonators in Figure 6 are mechanically independent, and they operate anti-phase. As a result, they measure the same magnitude of rotation, but give outputs in opposite directions. Therefore, the difference between the two sensor signals is used to measure angular rate. This cancels non-rotational signals that affect both sensors. The signals are combined in the internal hard-wiring ahead of the very sensitive preamplifiers. Thus, extreme acceleration overloads are largely prevented from reaching the electronics—thereby allowing the signal conditioning to preserve the angular rate output during large shocks. This scheme requires that the two sensors be well-matched, precisely fabricated copies of each other.

SUMMARY

Analog Devices has used its iMEMS process to achieve a breakthrough with the development of the World's first fully integrated angular rate sensor. Integration yields a revolution in reliability, size, and price. The result is a gyro that is suited for a much wider range of applications than previously thought possible or affordable. The device's low power and small size will benefit small consumer and industrial products that run on batteries, such as toys, scooters, and portable instruments. The tremendous immunity to shock and vibration benefits automotive and other applications that are subject to harsh environmental conditions.

Looking forward, it is possible to exploit the iMEMS process and gyro design techniques to achieve even higher levels of integration. Just as Analog Devices has developed dual-axis accelerometers, it will be possible to produce multi-axis gyroscopes. It will even be possible to integrate both accelerometers and gyros on a single die. The resulting inertial measurement unit would enable even tiny vehicles to be stabilized and navigated autonomously. ▣

APPENDIX

Motion in 2 dimensions

Consider the position coordinate, $z = r\epsilon^{i\theta}$, in the complex plane. Differentiating with respect to time, t , the velocity is

$$\frac{dz}{dt} = \frac{dr}{dt} \epsilon^{i\theta} + ir \frac{d\theta}{dt} \epsilon^{i\theta}$$

the two terms are the respective radial and tangential components, the latter arising from the angular rate. Differentiating again, the acceleration is

$$\frac{d^2z}{dt^2} = \left[\frac{d^2r}{dt^2} \epsilon^{i\theta} + i \frac{dr}{dt} \frac{d\theta}{dt} \epsilon^{i\theta} \right] + \left[i \frac{dr}{dt} \frac{d\theta}{dt} \epsilon^{i\theta} + ir \frac{d^2\theta}{dt^2} \epsilon^{i\theta} - r \left(\frac{d\theta}{dt} \right)^2 \epsilon^{i\theta} \right]$$

The first term is the radial linear acceleration and the fourth term is the tangential component arising from angular acceleration. The last term is the familiar centripetal acceleration needed to

constrain r . The second and third terms are tangential and are the Coriolis acceleration components. They are equal, respectively arising from the changing direction of the radial velocity and from the changing magnitude of the tangential velocity. If the angular rate and radial velocities are constant,

$$\frac{d\theta}{dt} = \Omega \text{ and } \frac{dr}{dt} = v$$

then

$$\frac{d^2z}{dt^2} = i2\Omega v \epsilon^{i\theta} - \Omega^2 r \epsilon^{i\theta}$$

where the angular component, $i\epsilon^{i\theta}$, indicates a tangential direction in the sense of positive θ for the Coriolis acceleration, $2\Omega v$, and $-\epsilon^{i\theta}$ indicates towards the center (i.e., *centripetal*) for the $\Omega^2 r$ component.

NEW PRODUCT BRIEFS VOLUME 37, NUMBER 1

January

8-channel, 24-bit **Sigma-Delta ADC** is optimized for fast channel switching **AD7738**
16-bit, 65-Msps **ADC** provides 80-dB SNR to Nyquist .. **AD10677**
Low-cost **Variable-Gain Amplifier** provides precise gain from dc to 150 MHz **AD8330**
Dual VGA has ultralow-noise preamp and programmable input impedance **AD8332**
100-dB **Logarithmic Converter** for optical network measurements **AD8305**
Mixed-Signal Front-Ends (MxFE™) for broadband communication systems **AD9860/62**
High-performance **OOK/ASK/FSK/GFSK Transmitter** for ISM band systems **ADF7010**
Quad 12-/10-bit **voltage output DACs** provide bipolar output spans **AD5582/83**
Digital Potentiometer features one-time-programmable, set-and-forget operation **AD5273**
High-performance, dual-core 16-bit fixed-point **DSP Microcomputer** **ADSP-2192M**
Three-phase **Energy Meter** measures average real power **ADSST-EM-2030**
Complete **Smart Transducer Front End** includes ADCs, DACs, and flash MCU **ADuC831/32**
3-phase **IMVP-II/IMVP-III Core Controller** for mobile CPUs **ADP3204**
dBCOOL™ Remote Thermal Controllers **ADT7460/63**

February

16-bit, 900-ksps **Sigma-Delta ADC** has programmable 130-MMAC postprocessor **AD7725**
8-channel, 1-Msps, 12-/10-/8-bit **ADCs** have programmable sequencer **AD7928/18/08**
Low-power 250-ksps, 12-/10-bit **ADCs** in 6-lead SC-70 packages **AD7920/AD7910**
4-/8-channel, 200-ksps, 12-bit **ADCs** have programmable sequencer **AD7923/AD7927**
14-bit, 40-/65-Msps **ADC** consumes only 300/550 mW .. **AD9244**
Programmable-Gain Difference Amplifier accepts high common-mode voltages **AD628**
Precision **FastFET™ Op Amp** has high gain-bandwidth product **AD8067**
Precision Low-Power **JFET Op Amp** in 5-lead SC-70 package **AD8627**
AC'97 SoundMAX® Codec **AD1980**
RMS-Responding Power Detector has 60-dB measurement range from 50 Hz to 2.7 GHz **AD8362**

Digitally Controlled **Variable-Gain Amplifier** provides 45-dB gain range from LF to 600 MHz **AD8369**
12-V **ADSL Central Office Line Driver** features Adaptive Linear Power architecture **AD8393**
Dual-Loop Laser Diode Drivers operate at up to 3.3 Gbps with 3-V supplies **ADN2847/48**
16-/14-bit **DACs** have serial input, current output, and low noise **AD5543/53**
Polyphase **Energy Metering IC** with pulse output **ADE7752**
Single-Chip **Gyroscope** with integrated signal-conditioning electronics **ADXRS150/300**
Precision 1.8-V **Reference** in SOT-23 package has shutdown function **ADR318**
Complete 10-bit, 25-MHz **CCD Signal Processor** **AD9943**

March

4-channel, 16-bit **Successive-Approximation ADC** is industry's fastest **AD7655**
2-/4-channel, 24-bit **Sigma-Delta ADCs** are optimized for fast channel switching **AD7732/34**
Dual 12-bit, 20-/40-/65-Msps **Multistage-Pipelined ADC** **AD9238**
16-bit, 80-Msps **ADC** provides 80-dB SNR to Nyquist .. **AD10678**
Low-distortion, high-speed **Op Amp** has rail-to-rail inputs and outputs **AD8027**
High efficiency X-PA™ **Power Amplifier** for mobile handsets has integrated RF power control **ADL5551**
Low-cost, low-power **Audio Codec** for speech and telephony **AD74111**
Low-noise, low-distortion **Audio Preamplifier** **SSM2019**
80-Msps **Receive Signal Processor** can process four W-CDMA channels **AD6635**
8-bit, 165-Msps **TxDAC® D/A Converter** **AD9748**
CDMA Power Management System **ADP3502**
GSM Power-Management System **ADP3522**
2-channel single-supply 12-bit **DAC** accepts two-complement inputs **AD5399**
Programmable Waveform Generator has 0- to 12.5-MHz frequency range **AD9833**
Lowest-power, 50-MHz **Complete DDS** **AD9834**
Three-Phase Electronic **Energy Meter Chipset** **ADSST-EM-3035**
Complete **Smart-Transducer Front-Ends** include ADCs, DACs, and flash MCU **ADuC834/36**
2-, 3-, 4-phase **Synchronous Buck Controller** uses 6-bit VID code **ADP3168/80**
Precision 2.5-V **Bandgap Reference** is available in 5-lead SC-70 package **ADR03**
Charge-Pump Regulator for color TFT LCD panel .. **ADM8839**

Analog Dialogue



Analog Devices, Inc.
393 Manley Street
West Bridgewater, MA 02379-1039

Return Service Requested

Worldwide Headquarters

One Technology Way
P.O. Box 9106
Norwood, MA
02062-9106 U.S.A.
Tel: 781.329.4700,
(1.800.262.5643,
U.S.A. only)
Fax: 781.326.8703

Analog Devices, Inc. Europe

c/o Analog Devices SA
17-19, rue Georges Besse
Parc de Haute
Technologie d'Antony
F-92182
Antony Cedex, France
Tel: 33.1.46.74.45.00
Fax: 33.1.46.74.45.01

Analog Devices, Inc. Japan Headquarters

New Pier Takeshiba
South Tower Building
1-16-1 Kaigan,
Minato-ku, Tokyo
105-6891, Japan
Tel: 813.5402.8210
Fax: 813.5402.1063

Analog Devices, Inc. Southeast Asia Headquarters

4501 Nat West Tower
Times Square
1 Matheson Street
Causeway Bay
Hong Kong, PRC
Tel: 852.2.506.9336
Fax: 852.2.506.4755



Purchase of licensed IC components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips IC Patent Rights to use these components in an IC system, provided that the system conforms to the IC Standard Specification as defined by Philips.

© 2003 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective companies.
Printed in the U.S.A. AD02003-100-5/03(O)