

# analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

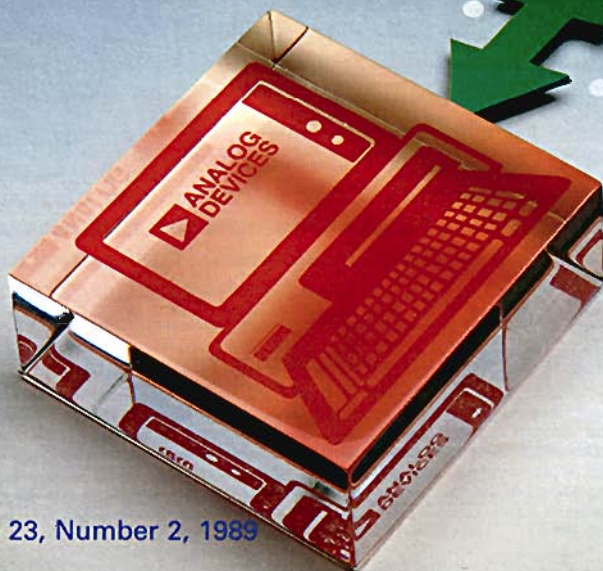
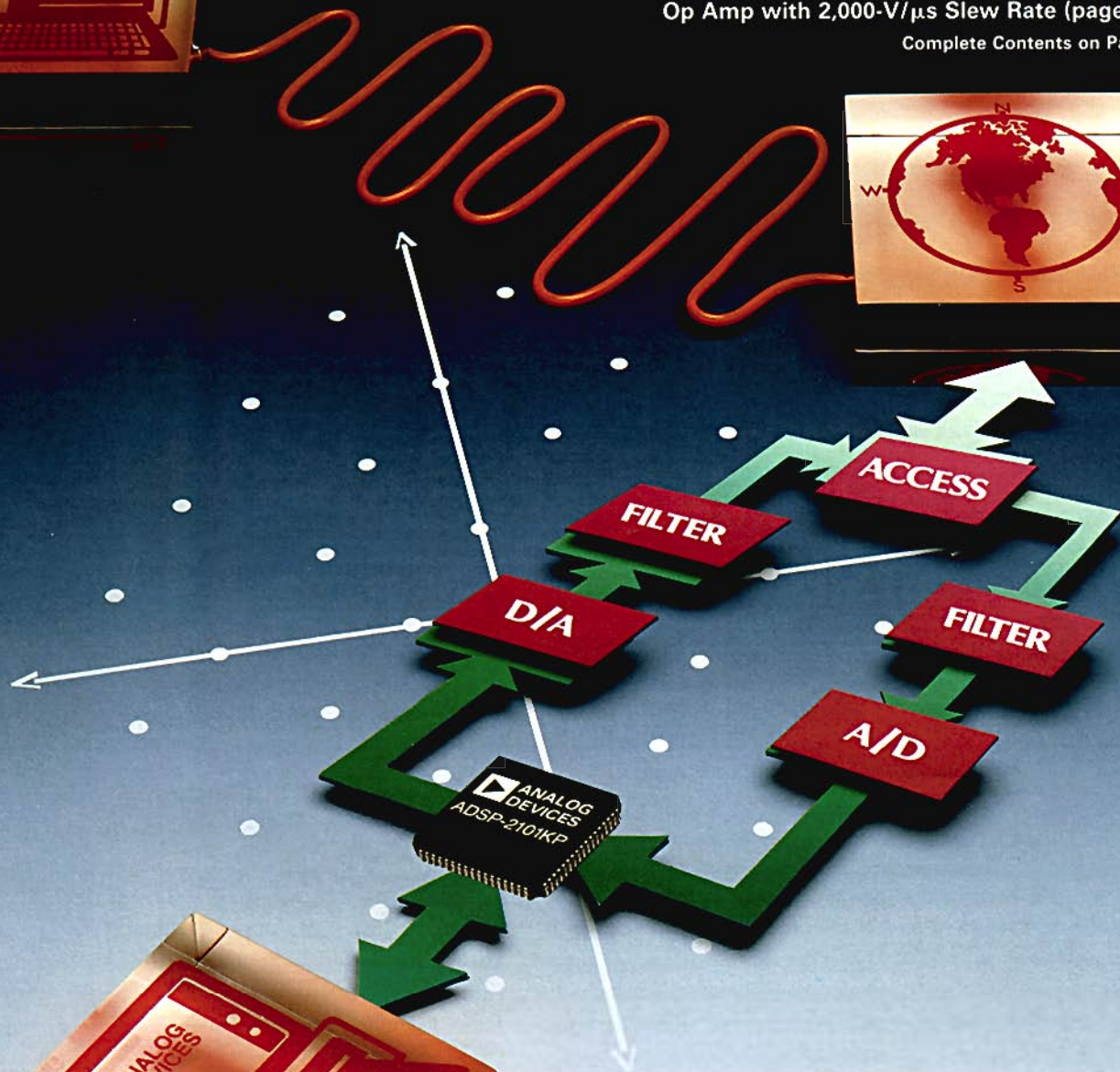
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# Editor's Notes

## THOUGHTS ABOUT TIME

We received a letter from Professor Sergio Franco, of San Francisco State University, stimulated by some comments in this space, under the heading, "Tempus Fugit" (22-2, 1988). His first paragraph read (in part) as follows:

"I just received the latest issue of *Analog Dialogue* and was shocked to learn that 22 years have elapsed since I received its first issue, in my glorious days as a graduate student (by the way, I still have it!)... Did you really have to bring that number up? May I suggest that Analog Devices concentrate on the development of an IC to slow down the flow of time, just a bit. Please send me samples as soon as you can."

The question was of course posed tongue-in-cheek, but let's pursue it. If we could slow time electronically, how might it be accomplished? What is "time", anyway? Can it be modified? Is there enough time and space here to deal with the question? (No—but let's air a few ideas, just to stimulate thought.)

Of time's many facets, quite a few are not germane to this discussion—for example, the cosmic nature of time-space (except perhaps for the possibility of slowing a clock by sending it on a voyage at relativistic speeds).<sup>\*</sup> We might also do well to avoid philosophical issues such as cause-and-effect or time reversal.


Since the flow of time could be slowed *if processes could be slowed, or the internal clock used to perceive time were speeded up*, some aspects worth thinking about include: the objective passage of time (e.g., clocks, dynamic phenomena), the subjective feeling of the passage of time, time for bodily processes, and time's extent (from seconds to human lifetimes).

A way to increase the objective passage of time is: use slower clocks with lower-frequency resonant elements. (There might be an opportunity for ICs here.) But our clocks are tied to the rotation frequencies of the Earth around its axis and around the sun (which ICs can't change). So time would need rescaling.

But even with slower clocks, a pitched baseball would seem to whizz by just as fast. We'd have to speed up whatever internal clock governs our time perception. Drugs might achieve that effect, but they're not acceptable. Electronically, "all we have to do" is find our subjective clock, and implant an IC "pacemaker".

So we see the ball in "slow motion," but how get the bat around "in time"? Not only our perceptions, but our whole mechanical system, and the motor nerves that serve them, would have to develop faster response: (with faster muscular chemical reactions, lower-mass body structures, and "bionic" neural nets (ICs?)).

But this doesn't address the question behind the question. Professor Franco is really concerned about the perceived passage of days and years—this concern would also embrace the rate at which we breathe, metabolize food, replace cells, etc., all of which would have to be slowed. It might take a long, slow wait (on any time scale) before ICs become useful in this quest.

Dan Sheingold 

<sup>\*</sup>This is not discussed here, but do see *A Brief History of Time*, by Stephen Hawking.




## THE AUTHORS

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## analog dialogue

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# ADVANCED MICROCOMPUTER IS OPTIMIZED FOR DSP

## ADSP-2101 Features On-Chip Program- and Data Memories Includes Serial I/O Ports, Timer; Compatible with ADSP-2100

by Denis Regimbal and Jim McQuaid

The ADSP-2101\* is a single-chip CMOS microcomputer optimized for digital signal-processing applications. The ADSP-2101 combines core features of the ADSP-2100 DSP microprocessor (*Analog Dialogue* 20-2, pp. 3-6) with 1K of on-chip data memory and 2K of on-chip program memory; it also adds two serial ports and other features. The internal program memory can be loaded into the microcomputer from an inexpensive external read-only memory. An alternative choice for higher volume applications is a mask-programmed version, the ADSP-2102.

Readers of these pages know that Analog Devices has been actively developing digital signal processing (DSP) circuitry for the better part of a decade, following the introduction of the industry's first low-power CMOS fixed-point multipliers and MACs in 1983 (see *Analog Dialogue* 17-1, pp. 3-7).

Digital processing is inherently reliable and stable; For example, unlike analog filters, equivalent digital filters do not drift with ambient temperature. DSP can implement functions that are difficult to achieve with analog circuitry or simply not realizable, thus providing new capabilities in advanced signal processing. Equally important, it offers flexible programmability to meet changing system requirements adaptively. As advances in the density and speed of CMOS digital logic continue, DSP is replacing analog signal processing in many applications.

### APPLICATIONS FOR THE ADSP-2100

Announced in 1986, the ADSP-2100 (*Analog Dialogue* 20-2), a 16-bit, fixed-point microprocessor, supports both processing of real-world digitized signals and high-speed numeric applications ("number-crunching"). Originally produced in 1.5- $\mu\text{m}$  CMOS, the ADSP-2100 offers a modified off-chip Harvard architecture; unlike a strict Harvard-architecture machine, where instructions and data are stored in separate memories, ADSP-2100 systems also store data in program memory as needed. The processor addresses 16K of external data memory and up to 32K of external program memory.

With this architecture, the ADSP-2100 can fetch two pieces of data from external memories on every cycle with no performance penalties. An on-chip instruction cache supports loops of up to sixteen instructions; the instructions are fetched once and then supplied by the cache on subsequent passes. The cache permits the ADSP-2100 to achieve the performance of a three-bus machine for the majority of DSP algorithms.

With its one-cycle-per-instruction performance, the ADSP-2100 is best-suited for applications that require efficient access to large amounts of memory, such as radar, sonar, image processing, and medical instrumentation. In 1988, Analog Devices introduced the ADSP-2100A, a 1- $\mu\text{m}$  "shrink" of the ADSP-2100.† It supported an increase in the microprocessor's speed from 8 MHz to 12.5 MHz.

\*Use the reply card for technical data. Consult the sales force about availability of sample units.

†We will use the universal nomenclature, ADSP-2100, throughout this text to include all versions.



### THE ADSP-2101 (AND ADSP-2102)

Advances in process technology make it possible to integrate sufficient memory into the IC to execute DSP applications entirely on-chip, for reduced cost and greater efficiency. The one-micron process supports a practical microcomputer version of the basic ADSP-2100 processor. The ADSP-2101 adds 1K of data memory and 2K of program memory to the basic ADSP-2100 core. The on-chip memory, like off-chip memory (if used), appears as a part of the total address space; *no special addressing is required to access it*. This amount of memory is enough for the ADSP-2101 to execute a complete 1,024-point FFT entirely from on-chip memory.

Besides incorporating on-chip memory, the ADSP-2101 includes dual serial ports with companding hardware and a timer. With this combination of features, the ADSP-2101 is suitable for applications such as cellular telephones, modems, facsimile machines, and guidance systems, where serial communications are important

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and on-chip memory is typically sufficient. The ADSP-2101 is packaged in a 68-lead PLCC or a low-cost 68-pin PGA; the lower pin count is achieved by multiplexing access to off-chip memory. Together, the ADSP-2100 and the ADSP-2101 form the foundation for a complete family of digital signal-processors. The essential core architecture and instruction set of the ADSP-2100 have been proven and validated by hundreds of DSP applications. Because of this common core, program code developed for the ADSP-2100 is upward compatible when migrating to the ADSP-2101. Of equal importance, the common core means that basic applications experience, including most of the code in the *ADSP-2100 Family Applications Handbook* series, is transportable to the new processor. Future members of the family will be based on the same core architecture.

### INTERNAL ARCHITECTURE: THE ADSP-210X CORE

The shaded area in Figure 1 shows the basic ADSP-210X core (the "X" denotes its incorporation in the ADSP-2101 and -2102 as well as in the ADSP-2100). The five buses that can be seen support the rapid processing speed of the design. There are individual program-memory data (PMD) and address (PMA) buses for the program memory side—and data-memory data (DMD) and address (DMA) buses for the data memory side. In addition, there is an internal results ("R") bus.

All address buses are 14 bits wide, capable of addressing up to 16K words. The data-memory data (DMD) bus is 16-bits wide and the program-memory data (PMD) bus has 24 bits, to match the 24-bit ADSP-2100 opcode width. The program memory can also store 16-bit data values. The fifth bus, the internal R bus, which is not extended off-chip, interconnects the three computational units: the arithmetic-logic unit (ALU), multiplier-accumulator (MAC) and barrel shifter. They sit side-by-side and also have individual feedback paths. This multiplicity of interconnections makes it possible for the results of any computation to be used as the operands for a computation in any unit—ALU, MAC, or shifter—on the very next cycle.

All computational units operate on 16-bit data with provisions for multiword (e.g., extended precision, complex numbers, or

floating-point) operations. The ALU executes a standard set of arithmetic operations (add, subtract, with borrow or carry, decrement, increment) and logical operations (OR, AND, NOT, XOR). The MAC takes two 16-bit operands and generates a 32-bit product. However, the accumulator/subtractor result register set is 40 bits wide, to allow up to 256 successive multiplication-accumulation operations to occur before there is any possibility of overflow. The shifter can place its 16-bit operand anywhere in a 32-bit field, optionally XORing it with the current contents of the shifter result registers. This makes it possible to reconstruct normalized 32-bit results in a small number of instructions.

The chips include two independent data address generators (DAG), which support automatic circular buffer wraparound for greater efficiency in implementing many algorithms. In addition, DAG1 can bit-reverse addresses, a feature useful in FFT calculations; DAG2 can address both program and data memory.

The program sequencer supports zero-overhead looping and single-cycle branching on conditional arithmetic instructions. A cache memory (found only on the ADSP-2100) permits the processor to store most loops on-chip and achieve three-bus performance, fetching instructions (from cache) and two operands (one from each external memory) on every cycle.

### NEW FEATURES OF THE ADSP-2101 (& ADSP-2102)

The right side of Figure 1 shows the new features added to the ADSP-210X core for the ADSP-2101 (and ADSP-2102, unless stated otherwise). Along the top of the figure are the on-chip program memory and data memory. They are addressed and accessed via the same PMA/PMD and DMA/DMD buses used for off-chip memory. The on-chip program memory can also feed the sequencer directly; it is fast enough to provide a data value and the next instruction in a single-cycle.

The boot address generator controls the loading of the microcomputer from external storage (typically EPROM) shown in the system interface, Figure 2. Up to eight different "pages" of boot memory can be stored, albeit all may physically reside within a single memory IC. They can be dynamically selected under software control, and the processor can then force itself to reboot,

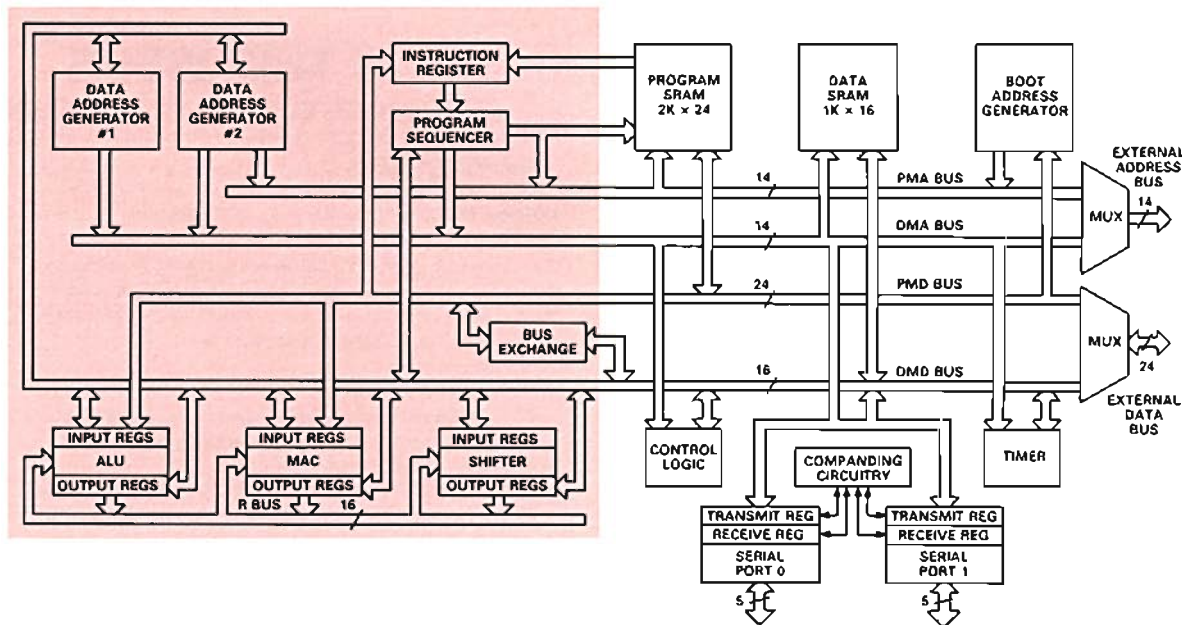


Figure 1. Block diagram of ADSP-2101 showing ADSP-2100 core on left.



loading a different page (and program) from EPROM.

At the far right of the figure the on-chip address buses are multiplexed into a single 14-bit external address bus. Likewise the two on-chip data buses are multiplexed into a single 24-bit external data bus. A memory select signal indicates whether data-, program-, or boot memory is being accessed.

The timer, which provides a periodic interrupt, is controlled by a 16-bit count register and an 8-bit prescaler. It can therefore operate over a wide dynamic range of resolution and elapsed time. Up to 1.34 seconds can be timed (in a 12.5-MHz-clock device).

The two double-buffered bidirectional serial ports, SPORT0 and SPORT1, are configurable with a wide variety of framing, clocking and data-wordlength options. The ports are supported by shared companding hardware which can execute  $\mu$ -law or A-law compression or expansion (standard in many telecommunications systems) in a single cycle. The serial ports can *autobuffer* their data, transferring it to and from memory with the absolute minimum of CPU overhead. A single cycle is taken, transparently, for transferring each data word. Only when a full buffer of data has been sent or received is a serial-port interrupt generated. (The serial ports can also generate an interrupt on every data word if desired.)

SPORT0 also provides a multichannel option for selectively receiving or sending channels from a 24- or 32-channel time-division multiplexed serial bitstream, such as a T1 or CEPT interface. When not needed for serial data, SPORT1's pins can be alternately configured as a flag in and flag out pin and two additional external interrupts.

The speed of a 12.5-MHz ADSP-2100 is a good indicator of the performance of the ADSP-2101. A 1,024-point FFT (radix 4), *executing entirely on-chip*, requires <2.9ms. The ADSP-2101 can implement an *adaptive differential pulse code modulation* (ADPCM) transcoder program (ADSP-2100 Family Application Handbook, Vol. 2) every 62  $\mu$ s, fast enough for the standard two-channel 125- $\mu$ s update rate. To permit their configuration and activation, while preserving the programming features of the ADSP-2100, the ADSP-2101's special features are controlled by a set of memory-mapped control registers that appear in the upper 1K of data memory and are reserved for this purpose.

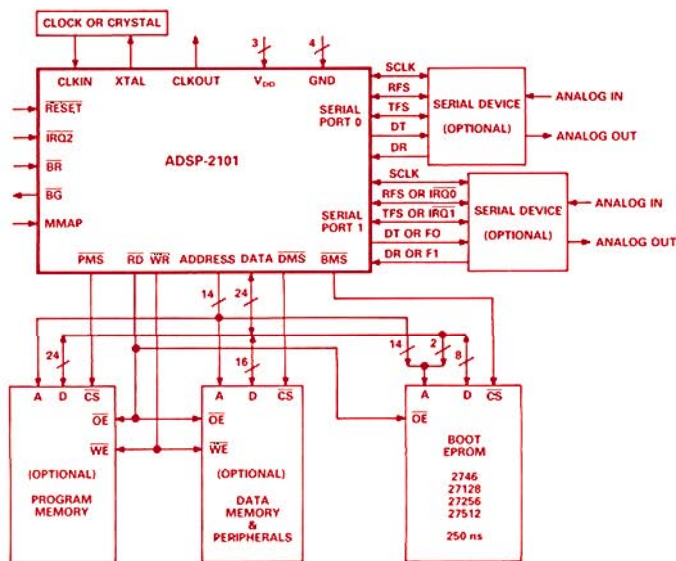


Figure 2. ADSP-2101 Basic system configuration.

## EASE OF INTERFACING

The ADSP-2101 requires little external circuitry to interface to standard a/d and d/a converters, codecs (*coder/decoder*, a type of a/d converter and d/a converter pair optimized for communications), and boot memory. A complete system can be constructed with just the ADSP-2102, a system clock, and codecs.

Access to slower off-chip memories, if required, is simplified by a system of programmable wait-state zones. The data-memory map is divided into sections, each associated with one to seven wait states. Slow peripherals can be clustered into sections of memory with appropriate common wait states, while faster memories can operate at full speed. This simplifies external timing hardware and allows the maximum potential speed of each memory or peripheral device to be realized.

## A HIGH-PERFORMANCE MODEM EXAMPLE

The ADSP-2101 is practical in high-speed V.32 modem applications (Figure 3), in which the CCITT recommendation requires a signal map with 32 *trellis-coded* carrier states for data transmission. The on-chip memory and serial ports provide the key elements required in a digital signal processor for these applications. The basic processing power is essential for the many computational tasks required in the V.32 "data pump." In such an application, a single ADSP-2101 can do the work of two or more general-purpose predecessor DSPs.

A major requirement of V.32 modems is the ability to implement *trellis coded modulation* (TCM), a combined coding and modulation technique for digital transmission<sup>1</sup>. TCM modulates the in-phase and quadrature components of the carrier in a way that minimizes errors introduced during transmission of data over general-switched telephone networks; simple TCM schemes can increase the bit-error-rate performance of a modem by three orders of magnitude.

In V.32 TCM, each 4 data bits are transformed into a 5-bit code word prior to transmission. With the 5-bit format, the 32 possible combinations of in-phase and quadrature modulations (forming the carrier state signal map) are divided into 8 four-element subsets. The first three bits specify one of eight subsets (Y0 Y1 Y2). The last two bits specify one of four elements (Q3 Q4).

Each element within a subset is mapped as far away from other elements within that subset as possible (Figure 4) so that, when received, closely related elements can be easily differentiated, thus reducing possible errors due to noise. Trellis-coding modulation further limits transition of successive words from one subset by one-half (or to 4 other specified subsets). This limitation guarantees that transmitted data points are always at maximum distances on the signal map, thus making low error-rate data recovery possible.

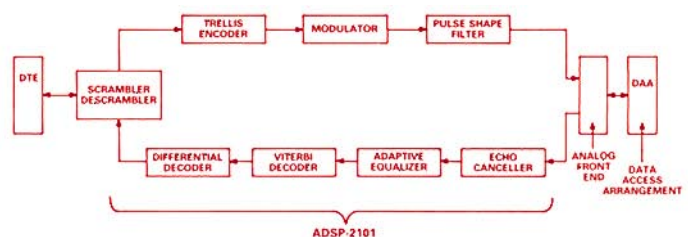


Figure 3. Modem block diagram.

The modem must also implement a data-decoding algorithm (such as Viterbi decoding) to recover the original data bits from the received, encoded bit pattern. The significant improvement in bit error rate that TCM provides at a given signal-to-noise ratio has a cost of just one extra bit per four original data bits. The ADSP-2101 can perform differential encoding, convolution encoding, and required data formatting in 58 processor cycles, or 4.64  $\mu$ s, with a 12.5-MHz clock.

### DEVELOPMENT TOOLS

Like the ADSP-2100, the ADSP-2101 is supported by a set of software and hardware development tools. The *Cross-Software* system runs on IBM® PCs and compatibles, VAX/VMS® and Sun-3 workstations. The *System Builder* is a module that allows the software developer to define target hardware configuration in a simple notation. The location of memory-mapped ports, the amount of memory available, or the address of specific memory segments can be changed via the System Builder without the need to rewrite source code.

**ADSP-210X Assembly Language: Easier to Read, Write and Debug:** The *Assembler* supports the uniquely readable ADSP-210X assembly language. Unlike most assemblers, this language uses an algebraic notation. For example, the multiplication/accumulation operation can be expressed as

$$Z = Z + X * Y$$

and is coded in a remarkably similar form

$$MR = MR + MX0 * MY0 (SS);$$

where MR is the MAC result register and MX0 and MY0 are the MAC X and Y input registers. The (SS) notation tells the multiplier to treat both operands as signed values.

The *Linker* reads the architecture description produced by the System Builder module and uses that information to place code and data in the appropriate locations. For ADSP-2101 systems,

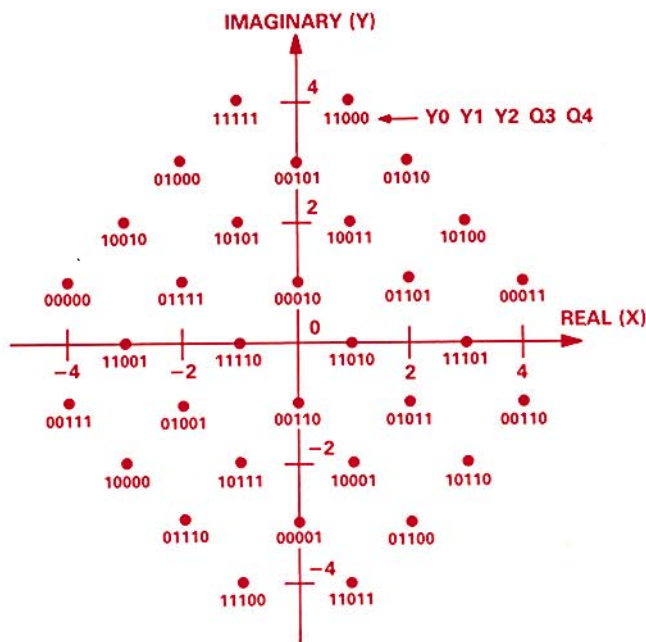


Figure 4. TCM signal map.

memory image. A PROM splitter reads the image file and creates the byte-wide files needed for boot memory (or for ROM memory, in the ADSP-2100 case).

### NEW WINDOW-ORIENTED SIMULATOR

An interactive *Simulator* (Figure 5), offers a window-oriented way to execute and debug ADSP-210X programs. Windows containing processor register groups and program and data memory can be opened on the screen and modified directly. *Trace* and *break-point* capabilities support debugging.

Windows may be interactively resized and repositioned on the screen by the user. Frequently used command strings can be "aliased" to avoid repetitive typing. Both the screen configurations and command aliases may be stored and automatically booted with the Simulator, delivering a customized version of the Simulator interface programmed to suit the individual user's needs.

Best of all, the Simulator interface is virtually identical to the ADSP-2101 Emulator interface. No additional learning is required when the design moves from software debugging to hardware debugging.

**Other requirements** The ADSP-2101 requires a single +5-volt supply and consumes less than 80 mW while executing the *idle* instruction. Prices for commercial-temperature grades (0 to +70°C) start at \$54 (1,000 pieces). For mask-programmed ADSP-2102 pricing, consult the factory. C compiler and cross-software packages cost \$2,450, \$5,460, and \$3,740 respectively for the IBM PC, VAX/VMS, and Sun-3 versions.

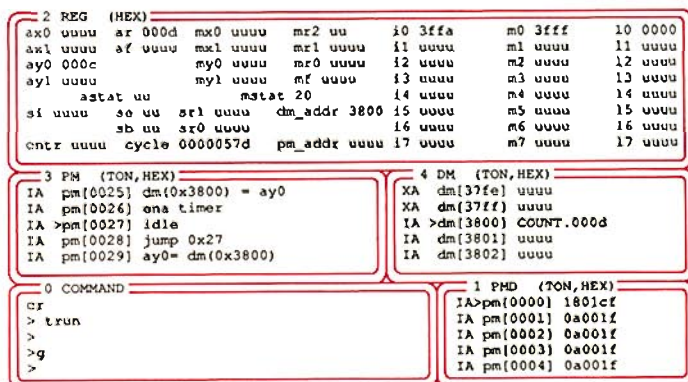


Figure 5. Typical simulator screen.

*The ADSP-2101 was created at Analog Devices' DSP Division (Norwood, Mass.) and Development Labs (Salt Lake City, Utah) by a team founded by Dan Essig and now headed by Greg Koker. The team's members include: Mont Buckles, Marc Diamondstein, Doug Hester, Paul Koralishn, Paul Kramarz, Kevin Leary, Dennis Lewis, Gerald McGuire, Kirk Peterson, Russ Rivin, Laura Swaris, Peter Szabo, Jr., Peter Szabo, Sr., Steve Tsang, and Bill Waddington.* ▶

<sup>1</sup>Ungerboeck, Gottfried, "Trellis-Coded Modulation with Redundant Signal Sets." *IEEE Communications Magazine*, February 1987.

# CONVERTER/FILTER CHIP SET FOR VOICEBAND APPLICATIONS

## 14-Bit AD7871/AD7872 A/D and AD7840 D/A Converters

## AD7371/AD7341 Switched-Capacitor Filters for Antialias/Reconstruction

by Mike Curtin and Bill Schweber

The monolithic AD7871\*/AD7872\* sampling analog-to-digital converters and AD7840\* digital-to-analog converter provide fast 14-bit interfacing of microprocessors to analog signals. When accompanied by the AD7371\* pre-digitizing antialiasing filter and the AD7341\* reconstruction filter, which employ switched-capacitor circuitry (see page 10), they form a complementary 4-chip set for digitizing analog waveforms and generating analog signals in digital-signal-processing applications. These devices are designed and specified with an eye towards voiceband applications such as echo-cancelling modems (Figure 1).†

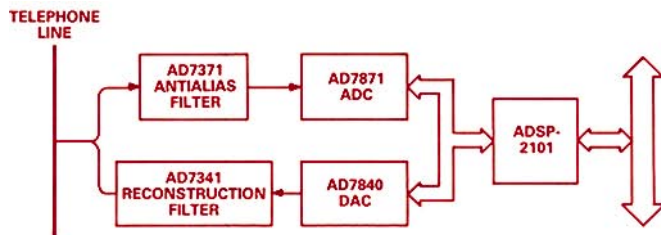


Figure 1. Modem analog front end and interface to ADSP-2101 DSP.

**AD7871 and AD7872 a/d converters:** Complete monolithic sampling ADCs (Figure 2), they incorporate a 2- $\mu$ s track/hold amplifier, 8- $\mu$ s successive-approximation ADC (based on a fast-settling voltage-output DAC), built-in reference, and laser-trimmed internal clock. They differ in their ability to communicate digitally. The 28-pin AD7871 provides a choice of three output data formats—a single parallel 14-bit word, two 8-bit parallel bytes, and a 14-bit serial bit stream, while the AD7872 is a complete 16-pin serial-only device.

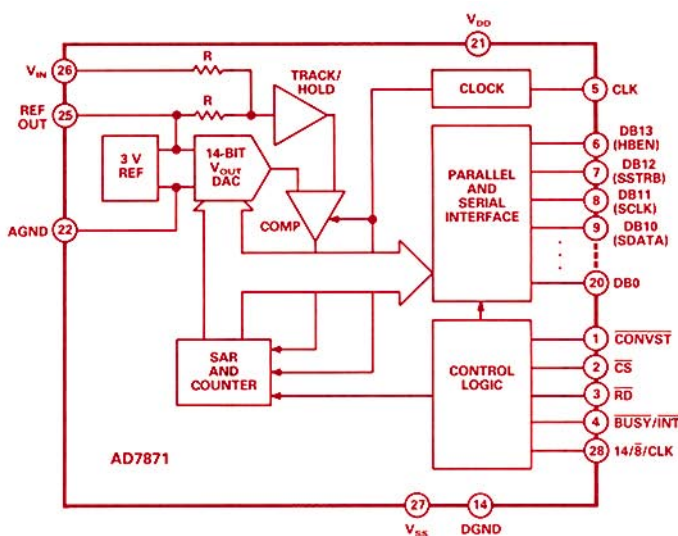
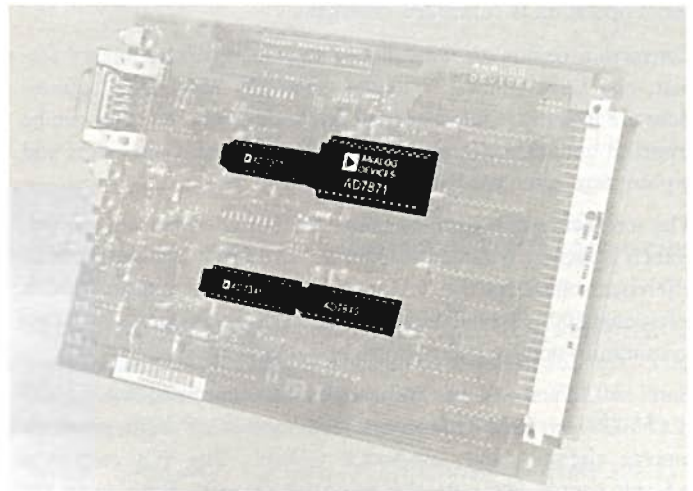


Figure 2. AD7871 ADC functional block diagram.

\*Use the reply card for technical data.

†A demonstration board is available combining the converters and filters for a modem application.



The converters' track-and-hold amplifier handles bipolar signals to  $\pm 3$  V peak-to-peak and settles to 14-bit accuracy in less than 2  $\mu$ s. To ensure accuracy and low distortion, its 500-kHz full-linear bandwidth ( $-0.1$  dB) is far greater than the 50-kHz-max Nyquist bandwidth at a maximum throughput rate of 100 kHz (allowing 8  $\mu$ s for conversion and 2  $\mu$ s for signal acquisition). Both traditional dc accuracy and ac-dynamic performance are fully specified for these converters; for a 10-kHz input sine wave sampled at 100 kHz, SNR is  $> 80$  dB and THD is  $< -84$  dB. Figure 3 shows an FFT analysis of J-grade device performance with a 7.525-kHz sine wave ( $f_0$ ) input sampled at 51.2 kHz.

No external clock components are required for operation with the internal clock; however, the on-chip successive-approximation clock can be overridden by an external clock of up to 2.5 MHz, if desired. Free-running conversions using the internal clock always take 19 clock periods, but an externally triggered conversion cycle may consist of 19 or 20 clock periods, depending on the synchronization between the conversion Start signal and the master-clock edge. Maximum conversion time at full speed is  $(20 \times 1/2.5 \text{ MHz}) = 8 \mu$ s.

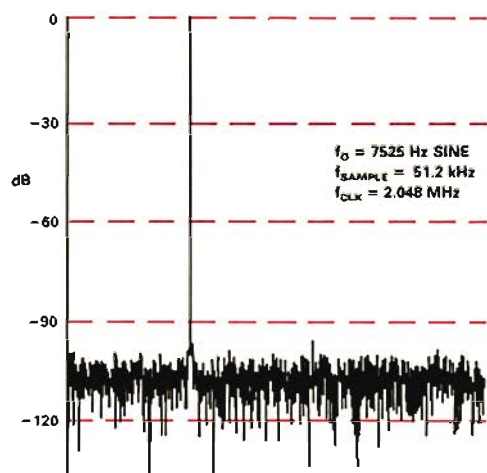


Figure 3. FFT performance of AD7871J.



Conversions can be initiated either by an external signal (Mode 1) or by the read/write cycle of the microprocessor (Mode 2). Mode 1 is intended for DSP applications, where precise sampling times are needed to minimize errors due to timing jitter and sampling uncertainty. Mode 2 is suitable where processor-converter timing is precise enough for the application. The compact serial-only AD7872 offers Mode-1 operation alone, since serial operation is controlled externally.

Conversion results are available in two's-complement binary format; one LSB equals  $6\text{ V}/16,384 = 366\text{ }\mu\text{V}$ . Most DSP applications are insensitive to offset- and full-scale errors, but they can be trimmed out with external circuitry if necessary. Gain errors and bipolar zero error are both less than  $\pm 10$  LSBs.

The internal temperature-compensated buried-Zener voltage reference is factory trimmed to  $3.00\text{ V} (\pm 10\text{ mV})$ . It provides both reference voltage for the DAC and bipolar offset voltage, with an additional  $500\text{ }\mu\text{A}$  available for external loads; it can be bypassed to minimize voltage spikes caused by digital activity.

Both a/d converters are fabricated in linear-compatible CMOS (LC<sup>2</sup>MOS), a BiCMOS process that comprises both precision bipolar circuitry and low-power CMOS. The ICs require a  $\pm 5$ -volt supply and consume less than  $60\text{ mW}$ . Both types are available in plastic or hermetic DIPs, and the AD7871 is also available in LCC and PLCC. Pricing (100s) begins at \$39 for the AD7871 and \$34 for the AD7872.

**The AD7840 14-bit voltage-output DAC** (Figure 4) has both serial and parallel interfaces, an internal 3-volt reference, output amplifier, and double-buffered data latches. Fabricated with the same process as the AD7871 and AD7872 ADCs, it too is fully specified for dynamic as well as dc performance. Data setup time and write pulse-width for the *parallel* interface are 21 and 45 ns, compatible with high-speed  $\mu\text{Ps}$ . The *serial*-data clock- and bit-transfer rates can be as great as 6 MHz.

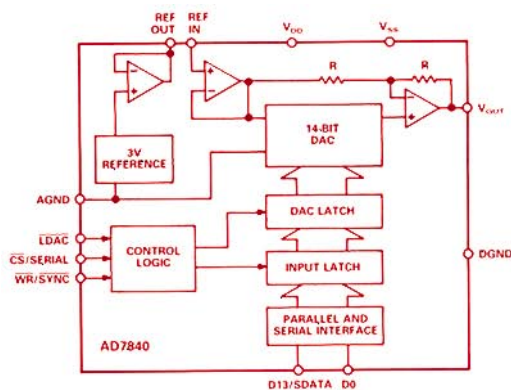


Figure 4. Functional block diagram of AD7840 DAC.

The AD7840 can produce full-power output ( $\pm 3$  volts full scale) for inputs up to 20 kHz. In a typical application, it would output digitally generated signalling tones and reconstructed analog voice signals onto the communications link as part of a modem function. Dynamic performance is measured by updating the DAC at 100 kHz and applying its output to a 9th-order, 50-kHz low-pass filter. Figure 5 shows a typical FFT analysis of the filtered output, re-digitized to 16 bits, for a 1-kHz sinusoid.

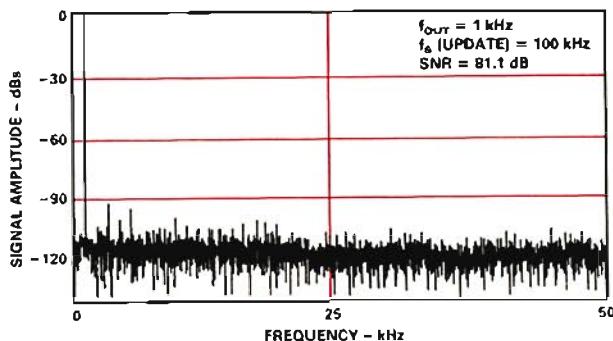


Figure 5. AD7840 FFT plot.

Depending on grade, output SNR is at least 76 to 80 dB for a 1-kHz waveform, and THD is below  $-78$  to  $-84$  dB. The output, guaranteed monotonic, has integral nonlinearity ranging from  $\pm 2$  LSB for the lowest grade to  $\pm 1/2$  LSB for the highest grade, with zero- and full scale errors less than  $\pm 10$  LSB. Settling time to within 1/2 LSB is typically less than  $2\text{ }\mu\text{s}$  for a positive full-scale change and  $2.5\text{ }\mu\text{s}$  for a negative change; maximum settling time is  $4\text{ }\mu\text{s}$ . Also important, the glitch impulse is only  $10\text{ nV}\cdot\text{s}$ .

The AD7840 contains a 3-volt  $\pm 10$ -mV internal reference (usable externally, like the reference in the ADC), but an external system reference can be used instead. With the same reference for ADC and DAC, the system benefits by ratiometric tracking. The AD7840 is available in 24-pin, 0.3"-wide plastic and hermetic DIPs and a 28-terminal PLCC. Price begins at \$10.50 in 100s.

**The AD7371 antialiasing filter.** Optimized for use with (but not limited to) the AD7871 and AD7872 ADCs, the AD7371 antialiasing filter is designed for high-speed voice-band modems operating at speeds up to 14.4 kbps, following CCITT V.32 and V.33 recommendations. A high-order bandpass filter, it has cutoff frequencies of 180 Hz and 3.5 kHz. With digitally settable gain from 0 to 24 dB, set by an 8-bit code, this filter rejects 50- and 60-Hz line noise as well as out-of-band signals.

The filter cascades a second-order low-pass active filter (continuous-time—CT), a fourth-order Chebyshev high-pass SCF (switched-capacitor filter—sometimes referred to as a sampling filter) with 180-Hz cutoff, and a seventh-order elliptical low-pass SCF with 3.5-kHz cutoff (Figure 6).

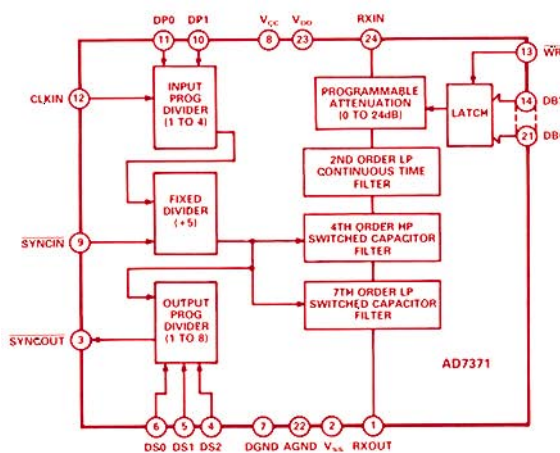


Figure 6. Functional block diagram of AD7371 antialias filter.



The input signal is applied to the programmable gain stage and converted from single-ended to differential. The filters use differential circuitry for low THD and to improve the rejection of common-mode noise, such as SCF clock feedthrough. The second-order CT filter prevents aliasing in the SCF stages; high-frequency components in the input signal would alias back into the switched-capacitor filter's passband, appearing as noise. The signal is finally converted back to a single-ended output.

Like its companion ADC, the filter is designed for a  $\pm 3$ -volt input range. Using a 288-kHz clock, the AD7371 has a SNR of better than 72 dB in the passband from 180 to 3,500 Hz, with passband ripple of  $\pm 0.2$  dB. Rejection in the stopband is 70 dB. Overall frequency response is shown in Figure 7.

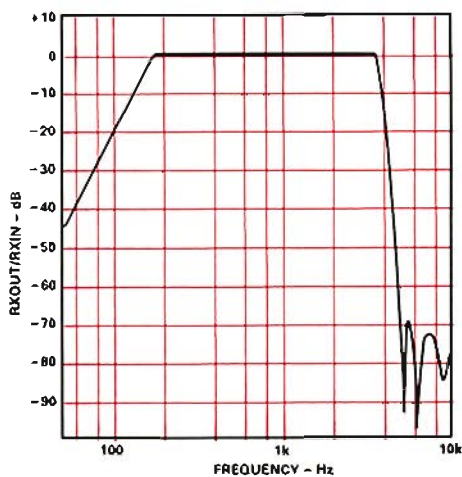


Figure 7. AD7371 amplitude response.

While the role of the AD7341 antialiasing filter ("receive" filter in modems) is to prevent aliasing in the converter and reject line noise, the **AD7341 reconstruction filter** (modem "transmit" filter) is designed to smooth the steplike AD7840 DAC output and reconstruct a continuous analog signal from discrete samples. Filtering is implemented with a seventh-order elliptical low-pass SCF, followed by a second-order continuous time filter, providing a cutoff frequency of 3.5 kHz (Figure 8). Like the AD7371 receive filter, the AD7341 transmit filter internally converts signal-ended signals to differential for filtering, and reconverts them to single-ended signals for external application.

The filter provides user-settable attenuation from 0 to 38 dB via a 6-bit code, to allow the user to adapt the output to different telecommunications line specifications. Stopband attenuation is at least 70 dB above 6.1 kHz, with a 288-kHz clock (Figure 9), and THD through the filter is less than  $-75$  dB.

**Filter Clocks** The 57.6-kHz switch drive, to set the SCFs for the specified response, is provided by an external 288-kHz clock, via an internal 5:1 divider. An additional divider with software-programmable ratios from 1 to 4 provides flexibility; the user can supply a clock at 288, 576, 864, or 1,152 kHz, synchronized with the ADC and DAC via a Sync pin to ensure no low-frequency beating. When used with converters in systems typically having sampling rates of 9.6-kHz or 7.2-kHz, the SCFs are substantially oversampled and pose no aliasing problem.

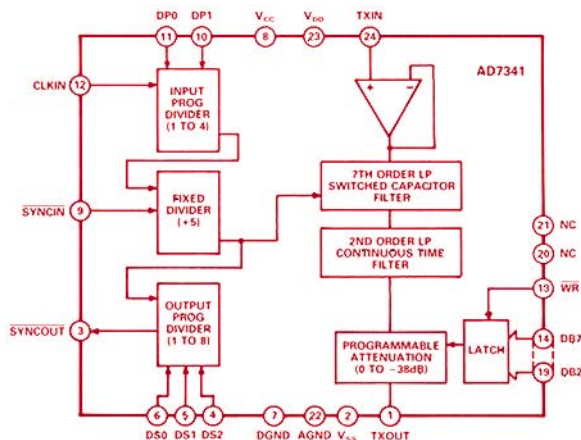


Figure 8. Functional block diagram of AD7341 reconstruction filter.

Both filters are fabricated in LC<sup>2</sup>MOS (linear-compatible CMOS) and require  $\pm 5$ -volt supplies, consuming less than 265 mW. They are available in 24-pin 0.3"-wide DIPs and 28-pin PLCCs. Prices (100s) are \$19.50 for the AD7371 and \$16.50 for the AD7341.

**Modem application:** The primary application for these ICs as a group is in the analog portion of echo-cancelling modems. Echoes occur when line discontinuities or unavoidable mismatch in the 2-wire-to-4-wire converter hybrids reflect some of the transmitted signal back to the sender. Echos include: *near-end* from the local hybrid with a short echo time, and *far-end* from the remote hybrid with a much longer echo time. They have a serious effect on signal quality, adding to the original signals in a full-duplex modem (both transmit and receive signals in the same frequency band), increasing apparent SNR and the bit error rate.

Figure 1 shows a modem application in which an ADSP-2101 digital signal processor provides entirely digital echo-cancelling. The received signal, filtered and digitized to 14-bits, is processed by various algorithms to extract the echo and subtract it from the original signal; then the corrected signal is retransmitted in analog form. Alternative analog echo-cancelling schemes, requiring costly high-precision filters, don't have flexibility to quickly vary specific filter parameters, or to adaptively change the entire filter structure (equivalent to a new algorithm) as conditions require. Only five signals communicate between the processor and the four-chip-set: clock, transmitted serial bits, received serial bits, framing for transmitted bits, and framing for received bits.

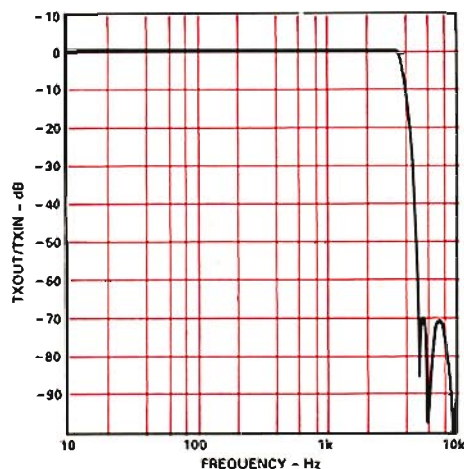


Figure 9. AD7341 amplitude response.



## A REVIEW OF SWITCHED-CAPACITOR FILTERS

Signals were once filtered entirely in the continuous analog domain by configurations of *passive* components (typically, inductors and capacitors). Later, *active filters*, with op amps for buffering and gain, provided filter designers with additional flexibility and performance, but still operated continuously on analog signals. Digital signal processing led to stable and flexible discrete-time filters, where sampled analog signals are processed entirely by numerical calculations with filtering algorithms—some of which cannot be realized with continuous filters.

Switched-capacitor (SC) filters are an intermediate class, combining both continuous- and discrete-time aspects. They use MOS switches and capacitors to simulate the behavior of resistors in the manner of Figure A (1). If the switch is initially at left, capacitor  $C$  charges to voltage  $V_1$ . When the switch is thrown to the right, the capacitor discharges to voltage  $V_2$ , and the net charge,  $\Delta Q$ , that flows into (or from)  $V_2$  is

$$\Delta Q = C (V_2 - V_1).$$

When the switch is thrown back and forth at a clock rate,  $f_C = 1/(\Delta t)$ , the average current flow,

$$i = \Delta Q/\Delta t = C \Delta V/\Delta t$$

from  $V_1$  to  $V_2$ , will be  $C (V_2 - V_1) f_C$ . The equivalent resistance,  $R$ , that would give the same average current is:

$$R = V/I = 1/(C f_C)$$

In practice, the single-pole double-throw switch is embodied by MOS switches driven by a non-overlapping two-phase clock (Figure A (2)). The actual model and analysis are more involved, but the above discussion should get the point across.

Using this SC resistor-equivalent, many conventional passive and active filter configurations can be realized. Figure B shows a single-pole RC low-pass filter and its SC equivalent. The  $-3$ -dB frequency is  $1/(2\pi R_1 C_1)$ ; for the SC version, it is:

$$f_{3dB} = f_C C_1/(2\pi C_2)$$

for  $f_C \gg f_{3dB}$  (to minimize effects of time sampling of the input and charge sharing). The key idea is that the *bandwidth depends entirely on the clock rate and the ratio of capacitor values*, which can be established in MOS technology with high precision. This RC becomes an active filter when buffered by a follower-connected op amp with any value of gain. A first-order *inverting* low-pass filter and its SC equivalent are shown in Figure C.

**Benefits of Switched Capacitor Filters:** With switched capacitors replacing resistors, many filter architectures can be realized entirely by a monolithic device without external components. Critical frequencies are determined by capacitor ratios and the clock frequency, both of which can be precise and drift free. Adjustable filtering is practical with precise variable clocks.

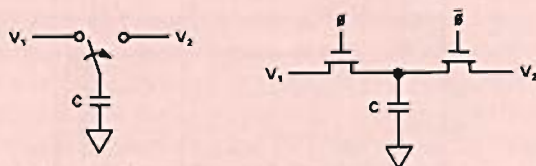


Figure A. Switched-capacitor "resistor." (1) Concept. (2) MOS implementation.

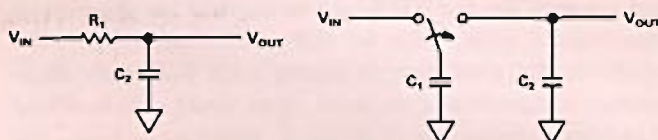


Figure B. Single-pole low-pass RC filter. (1) Continuous-time version. (2) Switched-capacitor version.

Audio-frequency filtering with SC filters can reduce passive-component size. A  $10\text{-M}\Omega$  resistor, accomplished by switching a  $1\text{-pF}$  capacitor (approximately  $0.01\text{ mm}^2$ ) at  $100\text{ kHz}$ , requires about  $1/100$ th the area of a silicon-based resistor.

**Other SC Filter Issues:** Besides parasitic capacitances and MOS switch imperfections—which make actual monolithic SC filters less than ideal and their real models more involved—the designer must understand additional aspects of SC filter performance. The switched capacitors and the op amps introduce random noise, and leakage currents result in offset error. Another (non-random) noise source is clock feedthrough via the switching transistors.

Also, as they sample analog signals, SC filters must be preceded by continuous-time antialiasing prefilters to eliminate input-signal spectral components beyond the Nyquist frequency (one-half the sampling rate). This is usually much higher than the SC filter passband, so a single- or double-pole RC filter is sufficient.

References (both reprinted in *Analog MOS Integrated Circuits*, IEEE Press, 1980):

1. Brodersen, Gray, and Hodges, "MOS Switched-Capacitor Filters," *Proc. IEEE*, Jan. 1979.
2. Caves, et al., "Sampled Analog Filtering Using Switched Capacitors as Resistor Equivalents," *IEEE J. Solid-State Circuits*, Dec. 1977.

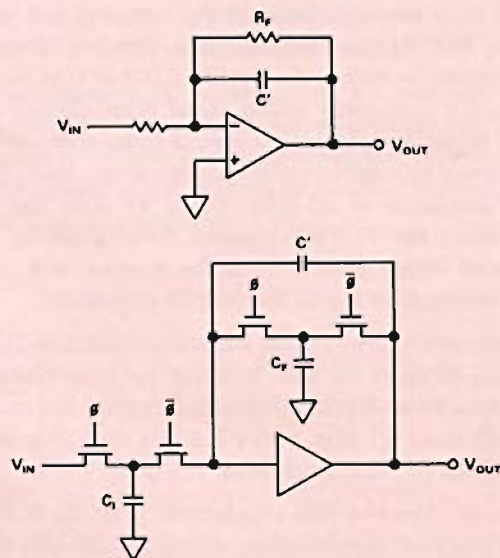


Figure C. First-order active low-pass RC filter. (1) Continuous-time version. (2) SC version.

*The converters were designed by Ken Deevy and Ray Speer (AD7871 and AD7872), and P.J. Garavan (AD7840) at Analog Devices, BV, Limerick, Ireland. The filters (AD7341 and AD7371) were designed by Doug Calder and Tony Gribben at Analog Devices, Newbury, U.K.*



# ISOLATED STRAIN-GAGE MODULE JOINS 5B CONDITIONER FAMILY

## 5B38 Has 10-kHz Bandwidth, 1,500-Vrms Isolation, Filtering; Provides 10-Volt Excitation; Amplified, MUXable $\pm 5$ -Volt Output

The 5B38 Strain-Gage Input Module\* is another direct-application 5B Series signal conditioner (*Analog Dialogue* 20-2). It provides the necessary excitation, conditioning, filtering, and amplification for 300-ohm to 10-k $\Omega$  full- or half-bridge strain gages, with input-to-output isolation of 1,500 Vrms—which minimizes ground loops and suppresses voltage transients. Its 10-kHz input bandwidth allows the 5B38 to be used with pressure, position, and torque transducers, in both low- and high-rate applications, such as fatigue testing and stress/strain investigations.

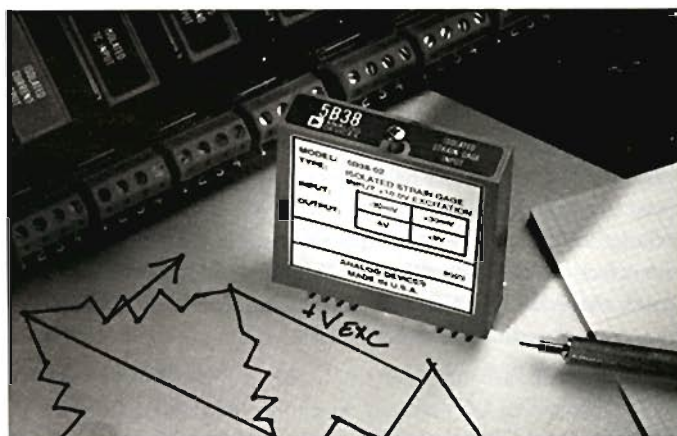
The 5B38 provides +10.0-volt excitation for the strain gage. Standard versions can be purchased for use with strain gages having optional full-scale sensitivities of 2 mV/V or 3 mV/V of excitation (20 mV or 30 mV full-scale with a +10-volt supply); the -5 to +5-volt output range corresponds to full-scale input spans of  $\pm 20$  and  $\pm 30$  mV. Custom spans are also available.

The 5B38 can be used with *half-bridge* transducers at lower-cost (compared to full bridges) since it contains a pair of laser-trimmed bridge-completion resistors, matched to within  $\pm 1$  mV (with 10-volt excitation). *Quarter-bridge* gages, when completed externally, can also use the half-bridge completion resistors.

Common-mode rejection (50 and 60 Hz), with a 1-k $\Omega$  resistance in series with one or both leads, is 100 dB. A low-drift amplifier in the front end contributes to low input- and output offset drifts (1  $\mu$ V/ $^{\circ}$ C and  $\pm 20$   $\mu$ V/ $^{\circ}$ C), and gain-temperature coefficient ( $\pm 25$  ppm of reading per degree Celsius).

In addition to its 1,500-volt isolation specification, which meets IEEE-STD 472 for surges, the input circuit has protection for up to 240-Vrms-continuous line faults. The isolation prevents sensor shorts to "hot" wires from damaging the rest of the data acquisition and control system, even if the input stage is "zapped." The input circuit also has a one-pole filter for antialiasing for the device's internal modulation circuitry.

Like the other modules in the 5B Series, the 5B38 uses transformer isolation between its input and output circuits. A proprietary modulation technique is used; the transformer output is demodulated to recover the original signal, which is then filtered by an active two-pole low-pass filter and buffered to provide a




low-impedance output. The result is linear, stable performance, with overall nonlinearity of  $\pm 0.02\%$  of span, while total error (gain, excitation, nonlinearity, offset, etc.) amounts to  $\pm 0.08\%$  of span  $\pm 10$   $\mu$ V, referred to the input (RTI).

The output of each 5B Series module (including the 5B38) can be multiplexed via a series switch (that closes in 20  $\mu$ s) to a common line on the backplane controlled by a single active-low Enable input (the 5B02 backplane capitalizes on this feature). When multiplexing is not used, Enable is connected to power common (the 5B01 backplane handles this grounding automatically). The built-in multiplexed output is a convenience to designers; a single ADC can serve many 5B Series channels.

A single +5-V supply is required for the module, capable of supplying up to 200 mA, depending on the excitation load presented by the bridge resistance. A clock oscillator within the module drives power transformers, which develop all necessary input and output power. In addition to the fully floating input circuit, the output section also floats (for common-mode voltages within  $\pm 3$  V of power common). This eliminates ground-loop and supply-noise problems. The use of internal power transformers in 5B Series modules also provides *channel-to-channel* isolation.

The design of the 5B38 provides low noise performance, critical in many strain gage applications. For an input bandwidth of 10 kHz, noise is 70 nV/ $\sqrt{\text{Hz}}$ ; for a 100-kHz bandwidth, noise is below 10 mV peak-to-peak. For relatively narrow-band applications, the 10-Hz-bandwidth noise is 0.4  $\mu$ V rms, RTI.

Housed in a standard 2.25"  $\times$  2.25"  $\times$  0.60" 5B Series module package, the 5B38 is specified for rated performance from -25 $^{\circ}$ C to +85 $^{\circ}$ C and will operate down to -40 $^{\circ}$ C. Price (100s) is \$126.

The 5B38 was designed by Joshua Israelsohn of the Industrial Products Division of Analog Devices, Norwood, Mass. 

Reference: Sheingold, D.H., ed., *Transducer Interfacing Handbook* (1980), available from Analog Devices, Inc. (\$14.50).

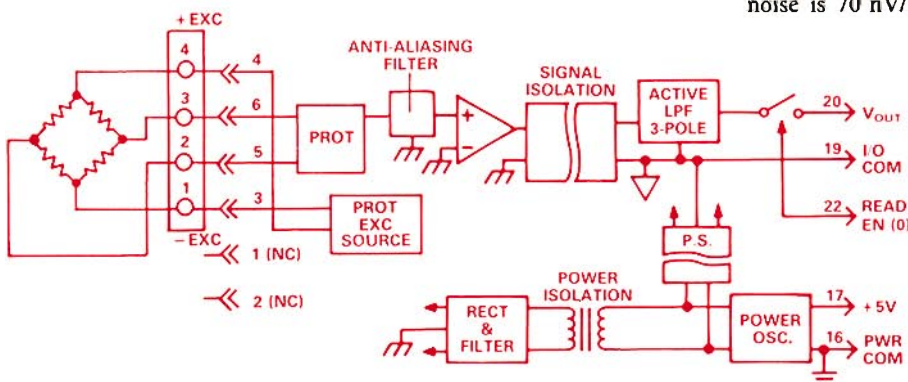


Figure 1. Functional Block Diagram.

\*Use the reply card for technical data.

# 6-BIT MONOLITHIC FLASH ADCs SAMPLE AT UP TO 500 MHz

## AD9006 AND AD9016 HAVE 550-MHz Analog Bandwidth

### Demultiplexed AD9016 Feeds Alternate Samples to Two Databanks

The AD9006 and AD9016\* are fast monolithic 6-bit "flash" a/d converters. They typically encode analog signals at rates up to 500 MSPS (470 MSPS min). The AD9006 provides output data via a 6-bit ECL latch; the AD9016 feeds its output data alternately to two 6-bit ECL latches (*demultiplexing*); this permits data to be read out of each at one-half the conversion rate, reducing the speed requirements for external logic. Each output data bank includes a signal overflow bit; it is also used as the MSB when two converters are wired together for 7-bit resolution. An evaluation board, the AD9016/PCB, can be used to observe device performance in an optimized setting.

Where are such fast a/d converters used? In applications for which the highest speeds are essential, and 6-bit (64-point) resolution is adequate; these include fast transient recorders and digital oscilloscopes, plus a variety of defense applications, including electronic countermeasures and radar warning receivers. The AD9006/16 can directly digitize intermediate-frequency signals, eliminating the need for analog demodulation of IF signals to lower bandwidths.

#### HOW IT WORKS

The AD9006/16 use a *flash* converter architecture employing 64 comparators that compare an analog input voltage with a set of tap voltages on a resistive voltage divider (Figure 1). The comparators are latched on an Encode command, and the results are applied to the decoding logic. The aperture delay of 1.2 ns, with jitter of 3 ps, makes it unnecessary to use a track-and-hold (T/H) ahead of the converter in many applications.

From the decoding logic, the data are applied to output latches as six bits of data and an overflow bit, which can be used when

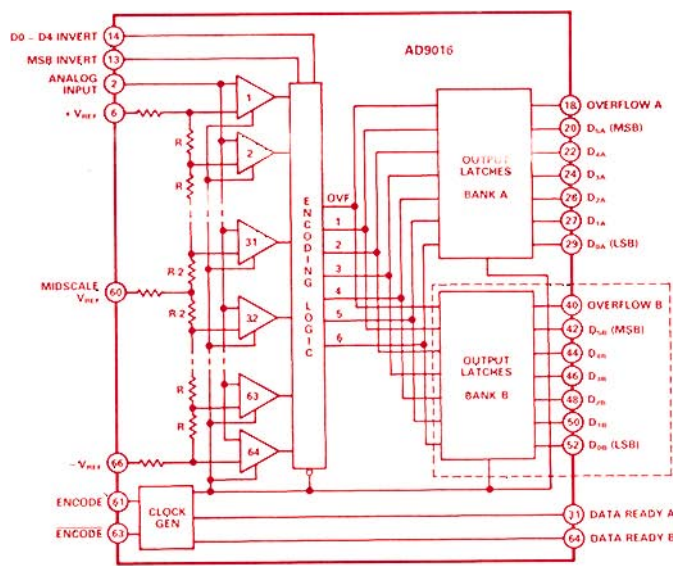
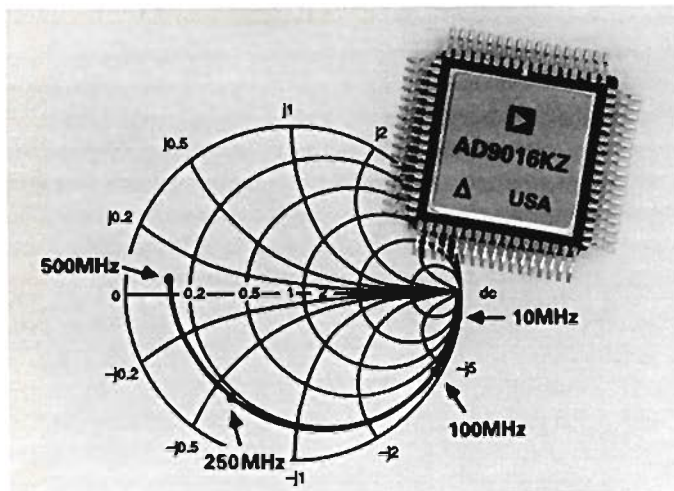


Figure 1. Block diagram of the demultiplexed AD9016. The AD9006 lacks the second latch bank, B, enclosed by dashed line.

\*Use the reply card for technical data.



stacking converters to obtain additional bits of resolution; it is also used as a "flag" for indicating positive out-of-range outputs.

Capturing output data at the (guaranteed) 470-MSPS encode rate of the AD9016 is simplified by the availability of two Data-Ready pulses (Figure 2); they track the propagation delay of the output data and alleviate the need to build an external clock circuit for tracking propagation delay over temperature.

Output words are directed alternately to Bank A and Bank B; this allows clocking of demultiplexed data from the AD9016 at one-half the converter's sample rate. The user can thus capture output

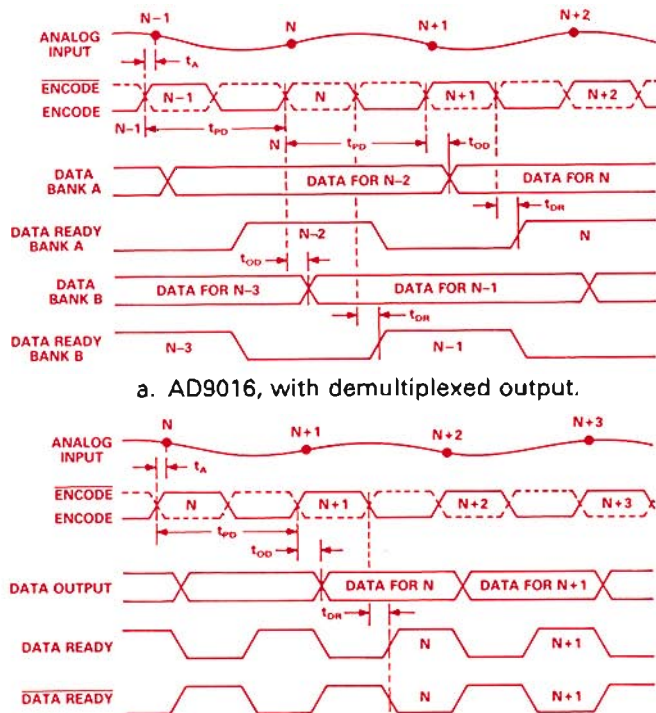


Figure 2. Timing diagrams. Delay intervals are:  $t_A$ -aperture delay,  $t_{PD}$ -pipeline delay,  $t_{OD}$ -output delay, and  $t_{DR}$ -data-ready output delay.



data with 100K ECL logic, even when the converter is operating at 470 MSPS.

The AD9016 introduces only one pipeline delay in the processing of the digital output data, thereby reducing the number of clock cycles required to obtain the digital representation of the analog input at the appropriate output port.

Here's a summary of the AD9016's timing (Figure 2a): the  $(N-1)$ th cycle starts with the Encode command. The  $(N-1)$ th point is sampled shortly thereafter (aperture time,  $t_A$ ) and encoded during the time for one Encode cycle (pipeline delay,  $t_{PD}$ ). After the next Encode command ( $N$ ), data for the  $(N-1)$ th point is latched into Bank B (output delay,  $t_{OD}$ ), and the Data Ready line for Bank B goes positive after the midpoint of the Encode cycle (Data Ready output delay,  $t_{DR}$ ). Note that the  $(N-1)$ th data remain latched for two whole cycles (until Encode  $N+2$ ), and the Data Ready flag remains up for one cycle, until the midpoint of cycle  $(N+1)$ .

Meanwhile, after command  $N$ , the  $N$ th point is sampled, processed, and latched into Bank A after the  $(N+1)$ th Encode command; and Data Ready Bank A goes up shortly after the midpoint of the  $(N+1)$ th cycle. It remains latched until Enable  $(N+3)$ ; and Data Ready Bank A goes down at the midpoint of  $(N+2)$ .

The AD9006 is designed for applications that require a single output port and can handle the fast data. Its timing is illustrated in Figure 2b. The first part of the cycle is similar to that for the AD9016, the output data for cycle  $N$  is latched after the  $(N+1)$ th Encode command, and Data Ready goes up† after the midpoint of the  $(N+1)$ th cycle. However, data for  $N$  remains latched only for one cycle, until cycle  $(N+2)$ 's encode command; and Data Ready goes down at the same time, after only one-half cycle.

The output data can be set in binary, inverted (complementary)-binary, twos-complement, and inverted twos-complement formats. The format of the output data is determined by two control pins: BIT INVERT (MSB) allows the most-significant bit (D5) to be inverted; D0-D4 INVERT allows the other five bits to be inverted.

## ANALOG INPUT

The analog input range is determined by user-supplied voltage references,  $+V_{REF}$  and  $-V_{REF}$ , having values between  $+1$  V and  $-1$  V, with  $+V_{REF} > -V_{REF}$ . The reference divider is tapped at midscale; with equal and opposite reference voltages, the MID-SCALE  $V_{REF}$  terminal can be connected to reference common for improved integral linearity.

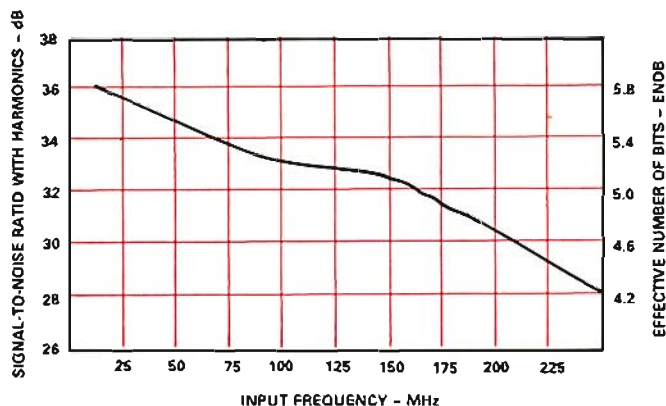


Figure 3. Signal-to-noise (SNR)—including harmonics—and effective number of bits (ENOB).

The AD9006/16 have a low 10-pF maximum input capacitance to minimize loading at high frequencies—an essential feature, since the low-pass formed by a 50- $\Omega$  source, a 50- $\Omega$  termination, and 10 pF has a  $-3$ -dB frequency of about 640 MHz, which is comparable to the devices' analog bandwidth of 550 MHz.

## PERFORMANCE

The AD9000/16 are specified for both dc and ac performance. Integral and differential nonlinearity are 1/2 LSB max, with no-missing-codes guaranteed over the operating temperature range.

Dynamic specifications include a typical 1.2-ns aperture delay and 3-ps aperture jitter. With a sinusoidal input 1 dB below full-scale at 196 MHz, encoded at 400 MSPS, the ADCs guarantee a minimum 29 dB of signal to noise, including distortion (SNR); the corresponding effective number of bits (ENOB) is 4.4. For input frequencies from 93 to 196 MHz, minimum ENOBs range from 5.2 to 4.4 bits, minimum in-band harmonics vary from 42 to 31 dBc, and minimum SNR spans a range from 34 to 29 dB. Figure 3 is a plot of typical values of SNR and ENOB vs. frequency for narrow-band input signals, while Figure 4 shows FFT data for 14.8 and 192-MHz sine waves.

The ADCs are manufactured in an advanced bipolar process, delivering high speed while consuming only moderate amounts of power. The AD9006 typically dissipates 1.7 watts, while the AD9016 dissipates 2.0 W. The 68-terminal ceramic leaded- and leadless-chip-carrier packages effectively dissipate heat, eliminating the need for external heat sinks.

Power supply requirements are  $+5$  V and  $-5.2$  V. Two grades are available, K and T/883, for 0 to  $+70^\circ\text{C}$  and  $-55$  to  $\pm 125^\circ\text{C}$ , respectively. An evaluation board, AD9016/PCB, is available. Prices in 100s are \$200 (K) and \$400 (T/883); the evaluation board, with an AD9016KE installed, is \$690 in small quantity.

*The AD9006 and AD9016 were designed by Charles Lane, at the Analog Devices Computer Labs Division, in Greensboro NC.*

†Data Ready for the AD9006 consists of a complementary pair of outputs. "Up" or "positive" for the direct output in these descriptions implies "down" or "negative" for the complementary output.

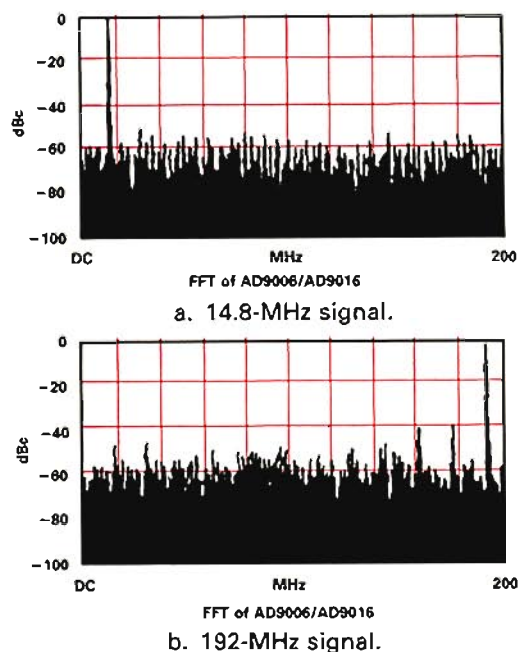


Figure 4. Output spectrum of AD9006/AD9016, for sine wave sampled at 400 MSPS,  $V_{IN} = 1$  dB below FS.

# FASTEST SLEWING MONOLITHIC OPAMP HAS WIDE BANDWIDTH

AD844 Slews at 2,000 V/ $\mu$ s with 60-MHz Unity-GBW, 0.005% THD

Low Offset & Drift: 50  $\mu$ V & 1  $\mu$ V/ $^{\circ}$ C,  $\pm$ 50-mA Output Drive

The AD844 op amp\* slews at 2,000 V/ $\mu$ s—twice as fast as existing silicon monolithic devices—and has 60-MHz unity-gain bandwidth with 20-MHz, 20-V peak-to-peak full-power bandwidth. Its high speed and excellent dc specifications, combined with low power consumption and high output drive capability, make it desirable for fast a/d-converter buffers, video signal amplifiers, cable drivers, and pulse circuitry.

Like the rest of the AD840 series of op amps (*Analog Dialogue* 22-2, page 12), the AD844 is fabricated in a complementary bipolar process, which combines speed, precision, and low power. Due to its current-feedback design, the -3-dB bandwidth does not decrease significantly at higher gains. Rise and fall times are essentially independent of output level.

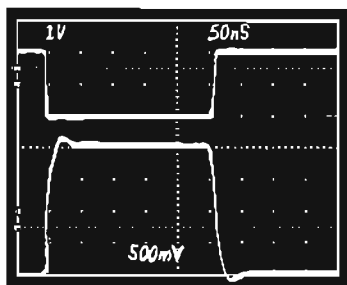


Figure 1. Cable-driver transient response.

**Performance** Small-signal bandwidth at gain of -1 is 60 MHz for a 10-pF, 500- $\Omega$  load; at a gain of -10 it is 33 MHz. The AD844 output slews at 2,000 V/ $\mu$ s for a full 20-V output swing, and settles to within 0.1% in 100 ns. Total harmonic distortion is below 0.005% at 100 kHz; differential gain and phase errors are < 0.1% and 0.1 $^{\circ}$  at 3.58 MHz—critical in video applications.

The AD844 can operate from  $\pm$ 4.5-V to  $\pm$ 18-V supplies, with less than 7.5 mA of quiescent current. The robust output stage drives 50- $\Omega$  loads to 2.5 V but is short circuit protected to 80 mA. The AD844 is primarily intended for high-speed applications, but its low offset and drift suit it for precision applications as well: typical offset is 50  $\mu$ V (300  $\mu$ V max—A grade, 150  $\mu$ V max—B grade), with 1  $\mu$ V/ $^{\circ}$ C drift.

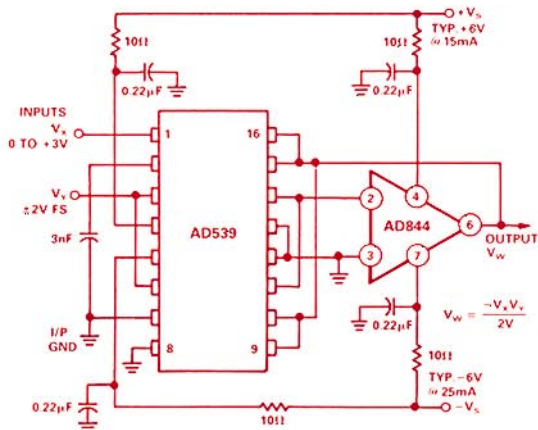
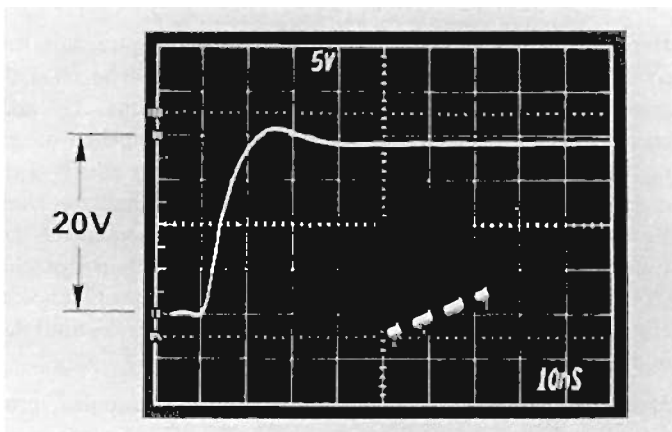


Figure 2. 20-MHz variable-gain amplifier using AD539 multiplier.

\*Use the reply card for technical data.



**Cable-Driving Application** Figure 1 shows the transient response (source and far-end load) of the AD844 connected for gain-of-2 as a 50- $\Omega$  cable driver, with matched source and load (overall gain of 1) and 30-MHz -3-dB bandwidth.

**20-MHz, Two-Quadrant Variable Gain Amplifier (VGA):** The wide bandwidth and high slew rate of the AD844 make it an excellent output amplifier for the AD539 multiplier (Figure 2), when used as a variable-gain amplifier. The output voltage is equal to  $-V_x V_y / (2 V)$ , where  $V_x$  acts as a gain control (0 to +3.2 V), and  $V_y$  is the signal voltage (up to  $\pm$ 4.2 V). Using the AD539's application resistors, the AD844 circuit has a bandwidth of about 22 MHz, independent of  $V_x$ .

The small-signal response (Figure 3) for a 50-dB gain-control range ( $10 \text{ mV} < V_x < 3.16 \text{ V}$ ) at small values of  $V_x$  is affected by PC-board capacitive feedthrough. Careful layout and a ground strip between the pins of the AD539 eases the problem.

Three performance grades in 8-pin plastic miniDIP and cerdip packages are available for operation over the -40 to +85 $^{\circ}$ C and -55 to +125 $^{\circ}$ C temperature ranges. Devices processed to MIL-STD/883B are also available. Prices begin at \$4.50 (100s).

The AD844 was designed by Fellow Barrie Gilbert, and Ken Wiegel, of Analog Devices' Semiconductor Division, based in Wilmington MA.

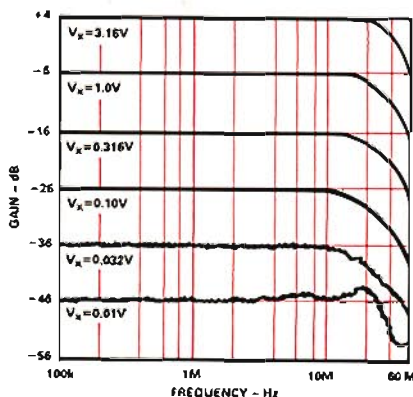


Figure 3. VGA ac response.



# FAST, LOW-POWER OP AMPS OFFER GAIN-BANDWIDTH CHOICE

## AD848 and AD849 Feature 175- and 725-MHz GBW

### Both Are Fully Spec'd for $\pm 5$ and $\pm 15$ -Volt Operation at 6 mA Quiescent

The AD848 and AD849 op amps\* are wideband devices offering designers a choice of gain  $\times$  bandwidth (GBW) for optimum response in specific applications. The uncompensated AD849, with 725-MHz GBW, for gains  $\geq 25$ , and the AD848, partially compensated for GBW of 175 MHz and gains  $> 5$ , join the 50-MHz, unity-gain-stable AD847 (*Analog Dialogue* 22-2). Using Analog Devices' proprietary complementary-bipolar (CB) process to combine high speed with excellent dc performance, they need only 6 mA of quiescent current. They are fully specified for both  $\pm 15$ -V supplies for data acquisition and  $\pm 5$ -V supplies—common in video applications.

Most popular op amps are *internally* compensated to remain stable and not oscillate in unity-gain applications. This compensation reduces both usable bandwidth in higher-gain applications and closed-loop accuracy at the upper end of the frequency range. For maximum bandwidth at high gains, some op amps, including AD848 and AD849, are *decompensated* by reduced internal feedback—which makes them unstable in low-gain applications without additional external components. A set of interchangeable op amps—the AD847, AD848, and AD849—with differing compensation levels, allows the user to maximize bandwidth for the desired gain without external compensating components, while other aspects of the design stay put.

Especially useful for up to 30 MHz, the AD848 and AD849 can slew at 300 V/ $\mu$ s (with  $\pm 15$ -V supplies) and settle to 0.1% in 100 ns (AD848) and 80 ns (AD849). For video applications, differential gain- and phase errors at 3.58 MHz (the video chroma subcarrier) are 0.1 dB and 0.1°. Both devices are stable into any capacitive load, but pulse integrity is degraded as load increases. Figure 1 shows square-wave response for the AD848 driving  $\pm 5$  V into 100- and 1,000-pF loads.

DC open loop gain for these op amps is also high: 8 V/mV into 150  $\Omega$  and 13 V/mV into 500  $\Omega$  for the AD848, using  $\pm 5$ -volt supplies. Input offset voltage is below 1 mV, eliminating the need for offset nulling in many applications. Input voltage noise is 5 nV/ $\sqrt{\text{Hz}}$  and 3 nV/ $\sqrt{\text{Hz}}$  for the AD848 and AD849, respectively, from 1 kHz to 10 MHz. Both offer full-power bandwidth greater than 20 MHz, for 2-V peak-to-peak output swing and  $\pm 5$ -volt supplies.

Settling time is nearly symmetrical for both positive and negative output swings, due to matching of NPN and PNP devices in the

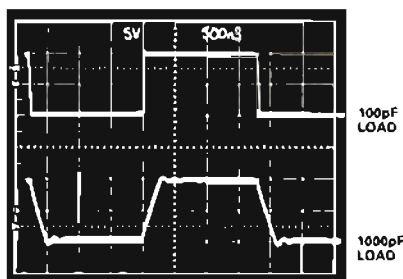
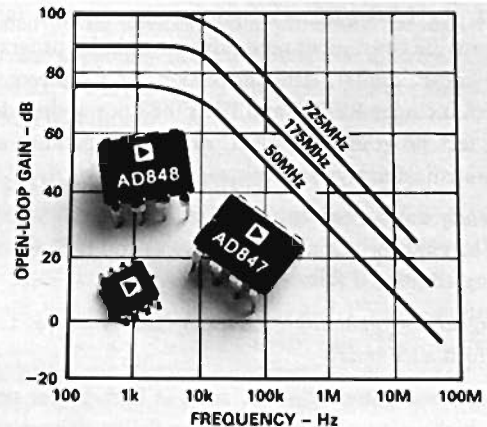


Figure 1. AD848 Driving Capacitive Loads.

\*Use the reply card for technical data.



complementary-bipolar process. For steady-state inputs, the low distortion (generally below  $-100$  dB for frequencies up to 100 kHz) is shown in Figure 2, with  $G = -5$  (AD848) and  $-25$  (AD849); each op amp drives 3 V<sub>rms</sub> into a 1-k $\Omega$  load.

The AD848 and AD849 are available for commercial, industrial, and military temperature ranges, in plastic miniDIP, cerdip, and small-outline surface-mount packages; parts processed to MIL-STD-883B are also available. Prices begin at \$2.95 (100s).

The AD848 and AD849 were designed by Wyn Palmer, of Analog Devices' Semiconductor Division, Wilmington, MA.

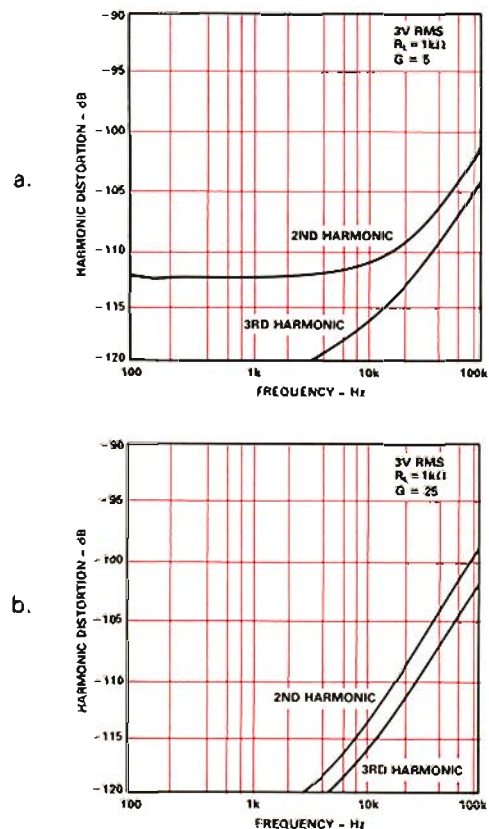


Figure 2. Harmonic Distortion vs. frequency. a. AD848. b. AD849.

# ENHANCEMENTS TO LTS-2020 BENCHTOP IC TESTERS

## Test Repertoire Expands to Include Wide Parameter Ranges for New Mixed-Signal, Smartpower-Device, and Opto-Isolator Capabilities

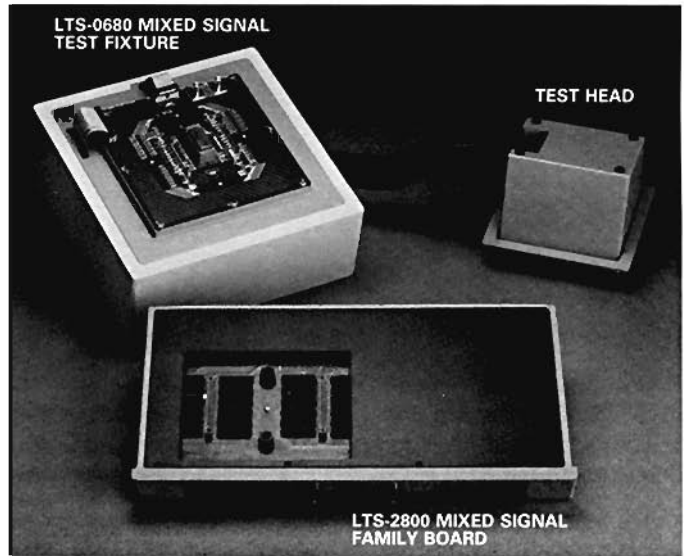
Since 1984, the LTS-2020\* Component Test System family has grown to provide convenient menu-driven, BASIC-programmable testing of linear, digital, data-conversion, and discrete devices. Each system includes RS-232 and IEEE-488 ports, disk drives for storage of test programs and data, network capability and self-test, and statistical-analysis software.

Three recently announced enhancements to the LTS-2020 series allow it to be used for testing newer devices and functions, as well as providing additional flexibility to users:

- *Mixed-signal test capability*—via a new family board, test head, and performance board
- *Testing of "smartpower" devices*, such as high-power peripheral drivers, high-voltage arrays, differential line drivers/receivers, and repeaters—using a new test fixture and DUT (device-under-test) board
- *Ability to test opto isolators*—using a newly available socket assembly, DUT board, and software.

### MIXED-SIGNAL TESTING

The LTS-2800 Mixed-Signal Family Board and LTS-0680 Mixed-Signal Test Head,\* shown in the photo and diagrammed in Figure 1, perform a wide variety of ac and dc parameter tests on analog and digital devices. The family board supplies the dc pin drivers, the dc force-and-measure system, a  $V_{CC}$  buffer, an rms-to-dc conversion circuit, voltage- and current sources, and a  $24 \times 5$  switching matrix. With its 24 programmable pin drivers, the system can provide high- and low-digital voltages, a three-



state (high-impedance) output mode, and accurate voltages and currents ( $V/I$  source).

The family board incorporates a series of 12-bit, calibrated sources, used for programming  $V_{OL}$  and  $V_{OH}$  voltage levels at the digital inputs of the device under test. A threshold source for programming voltage levels on a comparator, located on the pin driver, is used to detect digital output voltage levels accurately. For forcing and measuring currents, a  $V/I$  source provides and measures  $10 \mu A$  to  $400 mA$  and voltages to  $\pm 20 V$ .

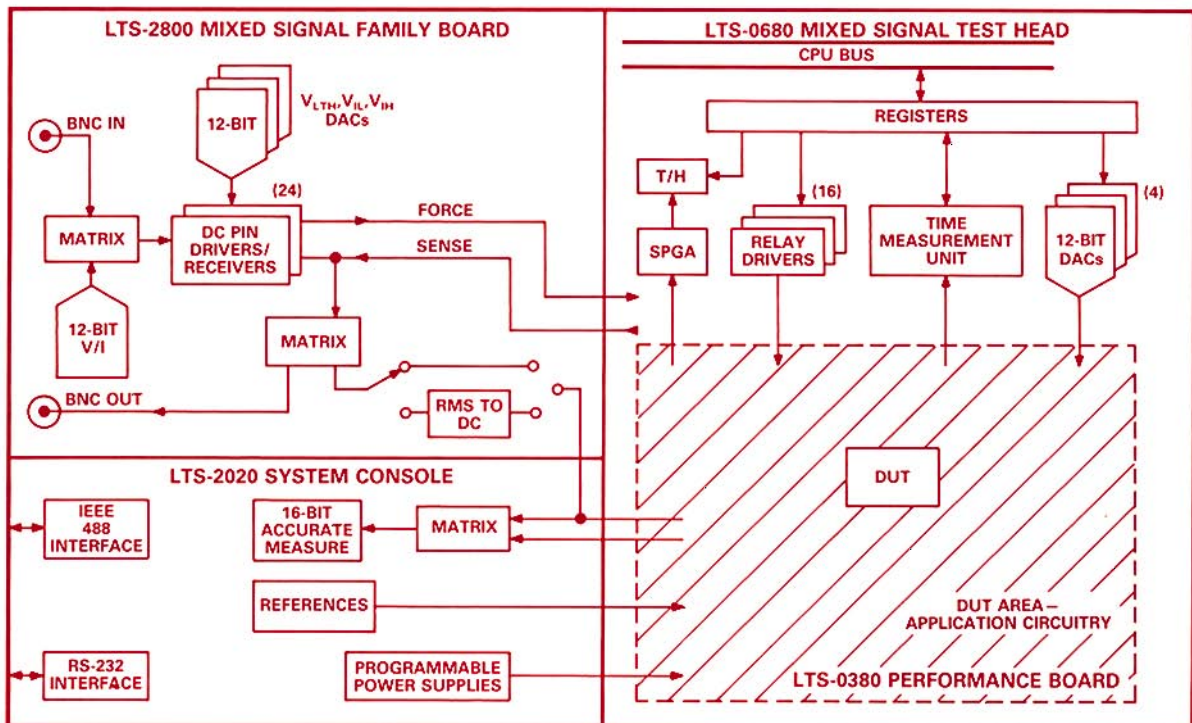


Figure 1. Functional block diagram, mixed signal fixture.

\*Write to Analog Devices Component Test Systems, 181 Ballardvale St., Wilmington MA 01887, or telephone (508) 658-9400 for information.



The switching matrix provides system flexibility by allowing any one of several capabilities to be switched to any of the pin drivers. These include the measure system,  $V/I$  source,  $V_{ih}$  and  $V_{il}$  sources, the rms-to-dc circuit (a wideband, precision circuit based on Analog Devices' AD637K\*), and BNC input and output connectors for interconnection with external instruments (such as programmable signal sources) using the IEEE-488 bus.

The LTS-0680 Mixed Signal Test Head contains a precise and versatile time measure unit, which provides accurate ac measurement of propagation delays, slew rates, pulse widths, and rise- and fall times—for both linear and digital devices. It also incorporates a 16-bit user data bus, 16-bit relay-driver bus, four 12-bit programmable sources, and a user's expansion board. A square-wave source for the DUT provides up to  $\pm 10$ -volt signals, from 1.22 kHz to 2.5 MHz.

For accurate measurement capability in the test head, the system uses an instrumentation amplifier, with software-programmable gain, and a track/hold (based on the AD365\*). With the calibrated 16-bit programmable source as one input to the amplifier, measurements are made differentially between that source and the voltage to be measured; small differences are amplified to levels allowing 16-bit-accurate measurements.

The LTS-0380 Performance Board holds the DUT and also provides space for user circuitry; the LTS-0400 User Expansion Board (located in the test head) is available for additional user circuitry. The LTS-2800, LTS-0680, LTS-0380, and LTS-0400 are priced at \$7,500, \$6,500, \$550, and \$300, respectively.

## SMARTPOWER TESTING

The LTS-0690 Smartpower Test Fixture,\* (Figure 2), together with the LTS-0390 DUT Board, performs a large variety of tests, including (but not limited to):  $I_{off}$ ,  $I_{on}$ ,  $H_{fe}$ ,  $BV_{ceo}$ ,  $V_{CEsat}$ ,  $V_{on}$ , and  $V_{off}$ . It works in conjunction with the existing LTS-2600 Discrete Family Board. The Smartpower Test Fixture contains a matrix board to facilitate multiplexing of high voltage/high

current  $V/I$ s, a nanoammeter, a differential amplifier, a 16-bit measuring system, and a central ground reference to any one of eight matrix points at the DUT.

In addition, this fixture contains eight dc pin drivers that are programmable to any one of four modes:  $V/I$ ,  $V_{ih}$ ,  $V_{il}$ , or three-state. This allows true digital dc parametric testing of the front end of smartpower devices, while providing the high voltage and high current capability needed to test the discrete output stage. Prices are \$3,300 for the LTS-0690 Test Fixture and \$275 for the LTS-0390 DUT Board.

## OPTO ISOLATOR TESTING

The Opto Isolator Test Package\* consists of a Socket Assembly (LTS-0664), DUT Board (LTS-0368), and software (LTS-0951) for fast and accurate testing of twelve parameters, including breakdown voltages ( $BV_{ceo}$ ,  $BV_{cbo}$ , and  $BV_{cbo}$ ), saturation voltages ( $V_{CEsat}$ ,  $V_F$ , and  $V_R$ ) and current gain ( $H_{fe}$ ), current transfer ratios (CTR), and leakage currents ( $I_R$ ,  $I_{CEO}$ , and  $I_{CBO}$ ). All parameters can be tested with a wide range of available static voltage- and current level conditions, programmed by the user.

The socket assembly provides electrical and mechanical connections with the LTS-2600 Transistor Family Board. Ground planes minimize noise, while relays on the DUT board provide high-current switching in under 8 ms. A special cover protects the user from high voltages (up to 600 V maximum) and high currents (up to 20 A) that may be present during the test.

Like the Smartpower software, the OPTO test package has the same easy-to-use menu-driven software as JFET and MOSFET test packages. The LTS-0664 Socket Assembly, LTS-0368 DUT Board, and LTS-0951 software are priced at \$825, \$275, and \$660, respectively.

At the Analog Devices Component Test Systems division in Wilmington, Mass., the Mixed-Signal system was designed by Ron Delgado, Woody Beckford, and John Huppe; the Smartpower system and the Optoisolator system were designed by Rick Carrier. ▶

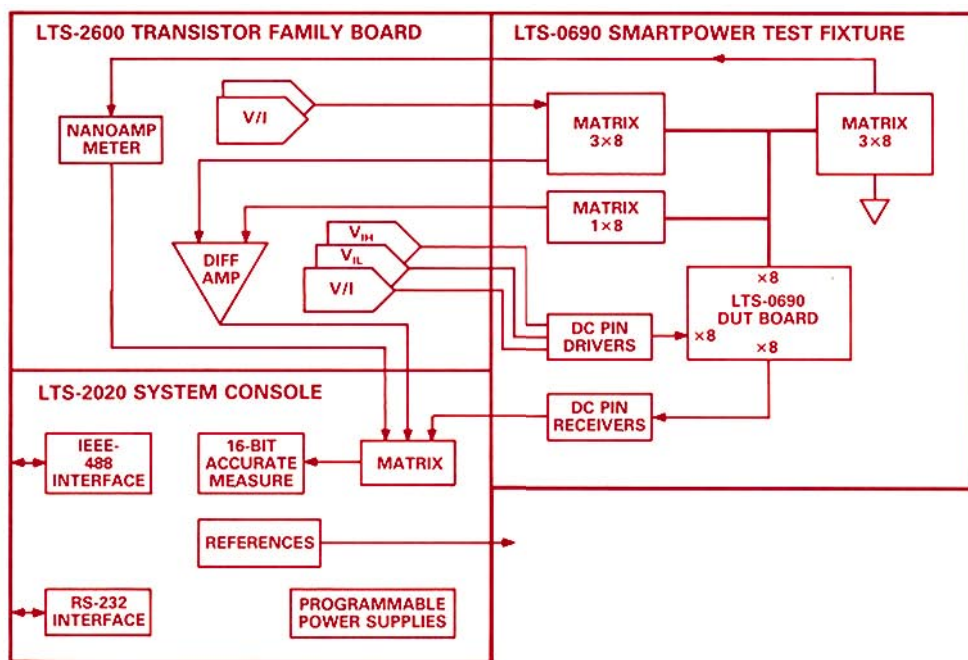


Figure 2. Functional block diagram, smartpower test fixture.

## 16-BIT ADC

**AD1377 Converts in 10  $\mu$ s  
 $\pm 0.003\%$  Max Nonlinearity**



The AD1377\* complete 16-bit a/d converter includes an internal reference and clock and is packaged in a compact 32-pin ceramic DIP. It is compatible with the industry-standard pinout and complementary digital coding used by the AD1376 (see *Analog Dialogue* 22-2) and ADC76 for easy performance upgrading of sockets designed for those types.

It performs a 16-bit conversion in less than 10  $\mu$ s, and the K grade has a maximum nonlinearity of  $\pm 0.003\%$ . 16-bit converters with the AD1377's combination of speed and linearity are typically used in high-resolution signal-processing and data-acquisition systems for automatic test equipment, professional audio, and medical or analytical instrumentation.

Its precision laser-trimmed thin-film scaling resistors can be jumpered for full-scale analog input ranges of  $\pm 2.5$  V,  $\pm 5$  V,  $\pm 10$  V, 0 to +5 V, 0 to +10 V, and 0 to  $\pm 20$  V.

Both serial and parallel digital outputs are available and are accompanied by corresponding clock and status outputs. Output coding is complementary binary (unipolar) and complementary offset binary for bipolar inputs. (Complementary twos complement can be obtained by inverting the MSB.) In applications where faster conversions with fewer bits may be required, the output can be short-cycled to any bit value from 8 to 15.

The AD1377 operates from  $-25$  to  $+85^\circ\text{C}$  and is available in two grades specified for 0 to  $+70^\circ\text{C}$ : The AD1377JD/KD have 0.006%/0.003% max nonlinearity, 3/2ppm/ $^\circ\text{C}$  nonlinearity tempco, and 13/14-bit no-missing-code resolution over temperature. Prices (100s) are \$116/\$140. ▶

\*Use the reply card for technical data.

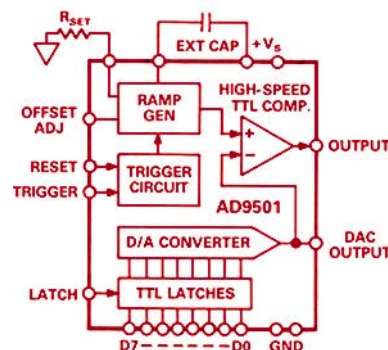
## PROGRAMMABLE DIGITAL DELAY GENERATOR

**AD9501 Is a TTL/CMOS-Compatible Version of the AD9500  
Has 50-MHz Maximum Trigger Rate, 10-ps Delay Resolution**

The AD9501\* is a monolithic programmable delay generator. Like its ECL companion, the AD9500 (*Analog Dialogue* 22-1, pp. 14-15), it delays an input edge by an interval proportional to an 8-bit word. Operating from a single +5-volt supply, the AD9501 is TTL- or CMOS-compatible; it can adjust timing accurately with  $\geq 10$ -ps resolution.

Its accuracy and programmability make it ideal for use in data deskewing and pulse-delay applications, as well as in clock timing adjustments. Typical end uses include disk-drive deskewing, data communications, test equipment, and radar I & Q matching.

Full-scale delay range is set by an external resistor-capacitor combination for any value from 2.5 ns to 10  $\mu$ s. An eight-bit digital word selects a time delay as a fraction of full-scale range. When triggered by the leading edge of an input pulse, the output of



the AD9501 will be delayed by an interval equal to the selected delay ( $t_D$ ) plus an inherent propagation delay ( $t_{PD}$ )

The AD9501 operates from a +5-V supply; it is available in 20-pin plastic DIPs, PLCCs and ceramic DIPs for 0 to  $70^\circ\text{C}$  operation, and in ceramic DIPs and (soon) LCCs for  $-55$  to  $+125^\circ\text{C}$  operation. Prices (100s) start at \$8.60. ▶

## 16-BIT SAMPLING A/D CONVERTER

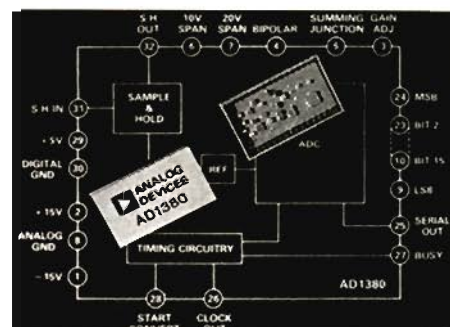
**AD1380 Is Complete with Reference, Clock, Sample-Hold  
Has Throughput Rate of 50 kHz, 0.003% Max Nonlinearity**

The AD1380\* complete 16-bit a/d converter has an internal sample-hold amplifier, reference, and clock. It has a throughput rate of 50 kHz; maximum conversion time of 14  $\mu$ s and acquisition time of 6  $\mu$ s. Typical applications are in instrumentation, signal processing, and automatic test equipment.

Maximum low-frequency performance specifications include  $\pm 0.1\%$  gain error,  $\pm 0.05\%$  bipolar-zero error, and  $\pm 0.003\%$  differential- and integral linearity errors (K grade). Over temperature, maximum drift specifications are  $\pm 20$  ppm/ $^\circ\text{C}$  gain,  $\pm 5$  ppm/ $^\circ\text{C}$  unipolar offset, and  $\pm 5$  ppm/ $^\circ\text{C}$  bipolar zero drift, with no-missing-codes to 14 bits (K).

In addition to dc accuracy specifications, the AD1380 is tested for dynamic performance. Typical aperture time and jitter are 50 ns and 100 ps, respectively. Typical measured SNR for a  $-10$ -dB, 13.2-kHz signal is 83.2 dB, corresponding to a noise floor of  $-93.2$  dB.

The AD1380 accepts 0 to +5-volt and 0 to



+10-volt unipolar inputs and  $\pm 2.5$ ,  $\pm 5$ , and  $\pm 10$ -volt bipolar input ranges. Data output can be either 16-bit parallel or 16-bit serial. Coding is complementary binary (unipolar) and complementary offset binary (bipolar).

Available in two grades, the AD1380JD/KD operate from  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$ , are packaged in a 32-pin triple-width ceramic DIP, and are specified for 0 to  $+70^\circ\text{C}$ . Power supply requirements are  $\pm 15$  and +5 volts, with typical power dissipation of 900 mW. Prices (100s) are \$126 and \$152 for J/K. ▶



## WRITE ADSP-2100A PROGRAMS IN C C Compilers Available for VAX/VMS, IBM-PC, and Sun-3 They Produce ADSP-2100 Assembly-Language Source Code

The C compiler is a Cross-Software development tool\* from Analog Devices to facilitate development of applications software for implementation on ADSP-2100-family DSP microprocessors. Other tools include System Builder, Assembler, Linker, PROM Splitter, and Simulator. Associated hardware tools include an Evaluation Board and In-Circuit Emulator.

The C compiler allows ADSP-2100A users to save time by writing application programs in the popular high-level C programming language. It generates ADSP-2100 assembly code, which can be assembled, linked, and debugged, using the Assembler, Linker, and Simulator, then stored in ROM. Debugged applications and libraries written in C can be run on the ADSP-2100A.

Assembly-coded routines may be used for time-critical operations (such as real-time filters); they are either in-line or subroutine-callable, through the use of the *#pragma*

directive, which allows the user to execute efficient assembly-language routines within the C environment.

The C compiler supports integer data directly, floating-point data (*float* data type) through a library routine, and fractional data (widely used in DSP in the 1.15 data format, but unavailable in standard C) through an extension of C created for the purpose (*fract* data type).

The compiler also supports all standard storage classes (*auto*, *extern*, *register*, *static*, *typedef*), types (all, including *void*), and modifiers (*const*, *volatile*, plus the extensions, *pm*, *dm*, *ram*, *rom*).

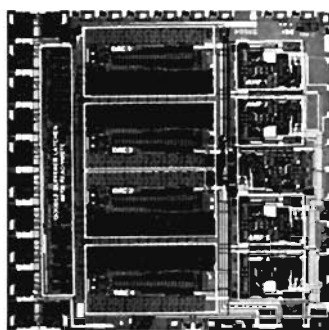
Another extension is the *fastswitch* statement, which supports the zero-overhead looping available in the processors' DO UNTIL capability; syntactically similar to the standard *switch* statement, it produces faster ADSP-2100 assembly code. ▣

## QUAD 12-BIT DAC IS MIL-STD-883-QUALIFIED V-out Monolithic AD664 Multiplies in Four Quadrants Throughput Rate is 50 kHz, Nonlinearity 0.012% Max

The AD664\* is a monolithic chip with four 12-bit voltage-output multiplying d/a converters that share a bidirectional  $\mu\text{P}$  interface (*Analog Dialogue* 22-1, 1988). These DACs save time and money when many reliable high-resolution voltage-output channels are needed for systems where real estate, power dissipation, and design effort are costly; for example, ATE and avionics.

The AD664 has 4 DAC cells, 4 output amplifiers, a control amplifier, and switches. The unipolar or bipolar output range of each DAC cell is independently programmed through the digital I/O port (LCC-packaged units), with a gain of 1 or  $2 \times$  the reference voltage (70-kHz bandwidth); with a 10-V reference,  $\pm 15\text{-V}$  analog supplies, and a 5-V logic supply, the specified ranges are 0 to +10 V, -5 to +5 V, and -10 to +10 V.

The AD644 is available in two versions, a



44-pin LCC ("E" package) with all functions described here—and a 28-pin ceramic DIP ("D") with unity gain and optional unipolar (*UNI*, 0 to  $+V_{\text{REF}}$ ) or bipolar (*BIP*,  $\pm V_{\text{REF}}$ ) range. The D interface with 12- or 16-bit buses; the E versions' three 4-bit nybbles allow them to communicate with 4- and 8-bit buses. The  $-55$  to  $\pm 125^\circ\text{C}$  AD664T grade is available in three /883 versions, with these suffixes: E/883B, D-UNI/883B, and D-BIP/883B. Prices (100s) start at \$250 (D-UNI/883B). ▣

## 45-ns, $16 \times 16$ -BIT Multiplier/Accumulator Low-Power ADSP-1010B



The ADSP-1010B\* is a high-speed, low-power  $16 \times 16$ -bit parallel multiplier/accumulator (MAC). A pin-for-pin speeded-up  $1\text{-}\mu\text{m}$ -CMOS replacement for the ADSP-1010A, it is also pin-compatible with TDC1010J1 and similar popular devices—but dissipates less power than competing devices.

It can multiply and accumulate the results every 45 ns at clocked rates up to 22.2 MHz, worst case (K version), combining high speed and low dissipation: 170 mW, typical, clocked at 10 MHz—and only 550 mW max at maximum speed.

The ADSP-1010B is especially useful for upgrading performance in digital signal-processing systems designed originally for slower devices. It is also useful for new designs of microcoded processors to solve demanding DSP applications in filtering, Fourier transformations, and correlation.

The ADSP-1010B has two 16-bit input ports (X and Y), a 16-bit most-significant-product (MSP) port, a 16-bit least-significant-product (LSP) port (shared with the Y-input port), and a 3-bit extended-product (XTP) port to avoid overflows. The *bidirectional* output ports permit initializing the output registers with external data.

Inputs can be represented in either two's-complement or unsigned-magnitude formats. When not extended, the output is a 32-bit-wide product, which can be rounded to 16 bits (1 is added to the most-significant bit of the LSP).

Devices are available in two grades for both 0 to  $70^\circ\text{C}$  (J, K) and  $-55$  to  $+125^\circ\text{C}$  (S, T) operation; /883B versions of the latter are available. Standard packages include 64-pin ceramic DIPs and 68-lead PLCCs and pin-grid arrays. Prices (100s) start at \$21. ▣

# Ask the Applications Engineer—3

by James Bryant

## V/F CONVERTERS

**Q.** How do I send an analog signal a long distance without losing accuracy?

**A.** An excellent solution to this common problem is to ship the signal as frequency using a *voltage-to-frequency converter* (VFC), a circuit whose output is a frequency proportional to its input. It is relatively easy to send a frequency signal over a long transmission path without interference via optical isolators, optical fibre links, twisted-pair or co-axial lines, or radio links.

If the data must be digital, the receiver will consist of a frequency counter, easily implemented in a single-chip micro-computer. Frequency is reconverted to analog voltage by a “frequency-to-voltage converter” (FVC)—generally a VFC configured to perform its inverse function, often using a phase-locked loop.

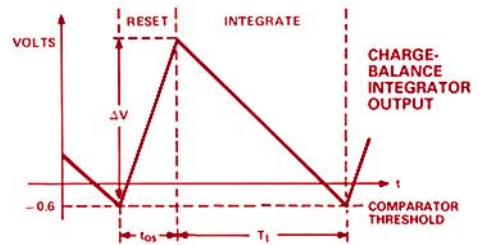


**Q.** How does a VFC work?

**A.** There are two common types: multivibrator- (AD537) and charge-balance (AD650) VFCs.\*

In the *multivibrator* type, the input voltage is converted to a current which charges and discharges a capacitor. The switching thresholds are set by a stable reference, and the output, which has unity mark-space ratio, is a frequency proportional to the input.

The *charge-balance* VFC uses an integrator, a comparator and a precision charge source. The input is applied to the integrator, which charges. When the integrator output reaches the comparator threshold, the charge source is triggered and a fixed charge is removed from the integrator. The rate at which charge is removed must balance the rate at which it is being supplied, so the frequency at which the charge source is triggered will be proportional to the input to the integrator.



**Q.** What are the advantages and disadvantages of the two types?

**A.** The multivibrator is simple and cheap, demands little power, and has unity mark-space (M-S) output—very convenient with some transmission media. But it is less accurate than the charge-balance type and cannot integrate negative input transients.

The charge-balance type is more accurate, and negative input transients are integrated to contribute to the output. It has more-demanding supply requirements and a lower input impedance, and its output is a pulse train, not a unity M-S square wave.

**Q.** What are the important types of error in a VFC?

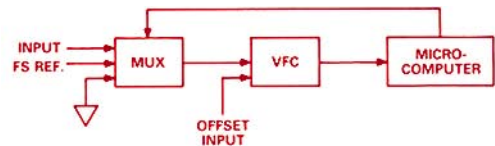
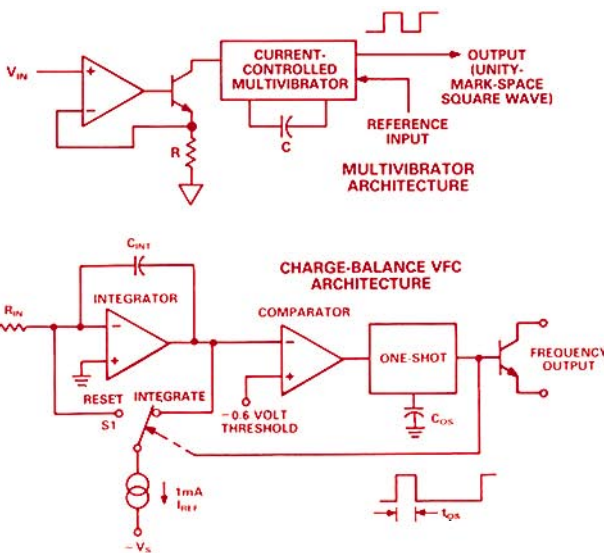
**A.** The same three as in most precision circuitry: offset errors, gain errors and linearity errors—and their variation with temperature. As with most precision circuitry, offset and gain can be trimmed by the user, but linearity cannot. However, the linearity of VFCs is normally very good (if the capacitors are properly chosen—see below).

**Q.** How do you trim gain and offset in a VFC?

**A.** The procedure suggested by theory is to trim offset first at zero frequency and then gain at full scale (FS). But this can give rise to problems in recognizing “zero frequency,” which is the state when the VFC is just not oscillating. It is therefore better to trim offset with a small input (say 0–1% FS) and adjust for a nominal frequency, then trim gain at FS, and then repeat the procedure once or twice.

For example, suppose a VFC is being used with FS of 100 kHz at 10-volt input. Ideally, 10 V should give 100-kHz output and 10-mV input should give 100 Hz. Offset is, therefore, trimmed for 100 Hz with 10 mV applied; gain is then trimmed to give 100 kHz at 10 V. But gain error affects the 10-mV offset trim slightly, so the procedure may have to be repeated to reduce the residual error.

If a VFC is used with software calibration a deliberate offset is often introduced so that the VFC has a definite frequency for zero input voltage. The microcomputer measures the VFC outputs at 0 V and FS inputs and computes the offset and scale factor. It may also be necessary to reduce the gain so that the VFC cannot try to exceed its maximum rated frequency.



\*Data sheets are available for any of the Analog Devices products mentioned here. An Application Note: “Operation and Applications of the AD654 V-to-F Converter,” is also available without charge.



Q. What circuit precautions are necessary when using a VFC?

A. Apart from the usual precautions necessary with any precision analog circuitry (grounding, decoupling, current routing, isolation of noise, etc., a subject for a book, not a paragraph) the main precautions necessary when using a VFC are the choice of capacitor and separation of the input and output.

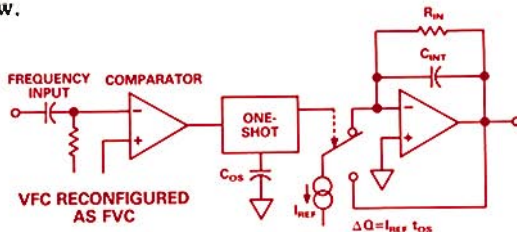
The critical capacitors in a precision VFC (the multivibrator's timing capacitor, and the monostable timing capacitor in a charge-balance type) must be stable with temperature variation. Furthermore, if they suffer from *dielectric absorption*, the VFC will be nonlinear and may have poor settling time.

If a capacitor is charged, discharged and then open-circuited it may recover some charge. This effect, known as dielectric absorption (DA), can reduce the precision of VFCs or sample-and-hold amplifiers using such capacitors. VFCs and SHAs should therefore use Teflon or polypropylene, or zero-temperature-coefficient (NP0, C0G) ceramic capacitors with low DA.

Coupling between output and input of a VFC can also affect its linearity. To prevent problems, decoupling practices and the usual layout precautions should be observed. This is critically important with opto couplers, which require high current drive (10-30 mA).

Q. How do you make a frequency-to-voltage converter?

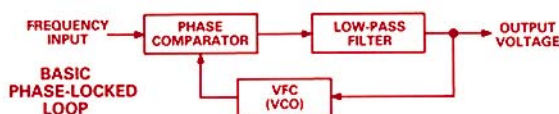
A. There are two popular methods: the input frequency triggers the monostable of a charge-balance VFC that has a resistor in parallel with its integration capacitor; or the input frequency can be applied to the phase/frequency comparator of a phase-locked loop (PLL), which uses a VFC (of either type) as its oscillator. The basic principle of the first type is illustrated below.



For each cycle of the input frequency, a charge,  $\Delta Q$ , is delivered to the leaky integrator formed by  $R$  and  $C$ . At equilibrium, an equal charge must leak away during each period,  $T (= 1/f)$ , of the input, at an average rate,  $I = V/R$ . Thus,  $V = \Delta Q \cdot f \cdot R$ .

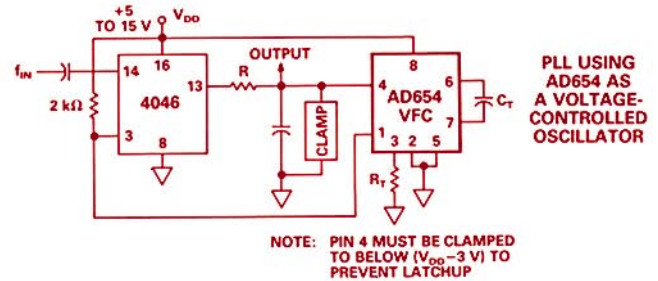
Though the mean voltage is independent of  $C$ , the output ripple is inversely dependent on  $C$ . The peak-to-peak ripple voltage,  $\Delta V$ , is given by the equation,  $\Delta V = \Delta Q/C$ . This indicates that ripple is independent of frequency (assuming that the charge,  $Q$ , is delivered in a short time relative to the period of the input). The settling time of this type of FVC is determined by the exponential time constant,  $RC$ , from which the time to settle within a particular error band may be calculated.

From these equations, we see that the characteristics of this type of FVC are interdependent, and it is not possible to optimize ripple and settling time separately. To do this we must use a PLL.



The phase-locked-loop FVC illustrated differs from any other PLL in only one respect: the voltage-controlled oscillator of the normal PLL, which must be monotonic but not necessarily linear, has been replaced by a VFC with a linear control law. In the servo system, negative feedback keeps the VFC's output frequency equal to the input frequency. The output voltage, the VFC's input, is accurately proportional to the input frequency.

Designing PLL systems is beyond the scope of this discussion,<sup>1</sup> but if a 4000-series CMOS PLL, the 4046, is used just as a phase detector (its VCO's transfer characteristic is not sufficiently linear), we can build the FVC shown here, with an AD654 VFC.



Q. What is a synchronous VFC?

A. A charge-balance VFC with improved linearity and stability, where the monostable is replaced by a bistable, driven by an external clock. The fixed time during which the precision current discharges the integrator is one clock period of the external clock.

A further advantage of the SVFC is that the discharge does not start when the integrator passes the comparator threshold (at a non-critical rate), but on the next clock cycle. The SVFC output is synchronous with a clock, so it is easier to interface with counters,  $\mu$ Ps, etc.; it is especially useful in multi-channel systems: it eliminates problems of interference from multiple asynchronous frequency sources.

There are two disadvantages. Since the output pulses are synchronized to a clock they are not equally spaced but have substantial jitter. This need not affect the user of a SVFC for  $a/d$  conversion, but it does prevent its use as a precision oscillator. Also, capacitive coupling of the clock into the comparator causes injection-lock effects when the SVFC is at  $2/3$  or  $1/2$  FS, causing a small (4-6 bit at 18-bit resolution at 1-MHz clock) dead zone in its response. Poor layout or device design can worsen this effect.

Despite these difficulties the improvement in performance produced by the abolition of the timing monostable makes the SVFC ideal for the majority of high-resolution VFC applications.

Q. Can you have a synchronized FVC?

A. Yes, and with very good performance; it is best done with an FVC-connected SVFC and a clock that is common to both ends of the transmission path. If the input signal to a synchronized FVC is *not* phase related to the clock, severe timing problems can arise, which can only be solved by the use of additional logic (two D flip-flops) to establish the correct phase relationship.

<sup>1</sup>See Gardner, F. M., *Phase-lock Techniques*, 2nd ed., New York: Wiley, 1979, for more detail; also Analog Devices' *Analog-Digital Conversion Handbook*.

## CATALOG\*

### Personal-Computer-Based Measurement & Control Solutions:

224 pages of descriptions, data, and ordering guides for data acquisition and control boards, signal conditioners and software from ADI. Its 7 sections describe: RTI-200 Series—IBM PS/2 Micro Channel Architecture boards; RTI-800 Series—IBM PC/XT/AT-compatible boards; Modular Signal Conditioners (including the new 6B Series of isolated digitizing signal conditioners); Signal-conditioning panels, including STB-HLI & STB-TCI for isolated high-level & thermocouple signals; Digital subsystems; DOS driver software; and Application software, including SNAPSHOT & SNAP-STREAM, LABTECH NOTEBOOK & LABTECH Control, ASYST, and THE FIX†. Each section ends in an ordering guide, including a telephone-order (1-800-4-ANALOG) worksheet and planning guide.

## SERIAL PUBLICATIONS\*

**DSPatch—The Digital Signal Processing Applications Newsletter:** Number Eleven is now available. It features a description of the new Atari arcade game, *Hard Drivin'*, a driving simulator with a new level of realism. The ADSP-2100 DSP microprocessor is the key to rapid computation of the highly convincing translations, rotations, and shape changes for the nearly 1,000 polygons that portray the visible features of the road, scenery, and traffic as the car moves. The game includes an instant replay from *outside* the car.


In this issue is also a description of GPR (*Getris Processeur Rapide*), a plug-in coprocessor and image-processing tool for IBM PCs, developed by Getris (Grenoble, France). Naturally, it uses the ADSP-2100. The Analog Devices DSP Bulletin-Board Service (617-461-4258) is described, with sample menus. Also included: an invitation to sample the ADSP-2100A at very low cost; plus the regular features, "Q & A," "How to Talk Analog" (featuring anti-aliasing filters), and other matters.

**Briefings—The Newsletter for Military/Avionics Industry:** Volume 5, Number 1 covers the AD574A's attainment of QPL status as the first—and *only*—JAN-qualified 12-bit monolithic ADC. Also described are newly qualified monolithic MIL-STD-883B parts, including the AD588 voltage reference, the AD767 complete  $\mu$ P-compatible 12-bit DAC, and the AD664 12-bit quad multiplying DAC (4 DACs on a chip). Additional items include a notification of process change for the ADSP-2100SG/883B and a DESC part number change for the ADSP-2100 DSP microprocessor, as a result of adding new higher-speed grades.

## APPLICATION NOTES\*

**Changing Your VGA Design from a 171/176 to an ADV471,** by Bill Slattery.

**Improved PCB Layouts for Video RAM-DACs Can Use Either PLCC or DIP Package Types,** by Bill Slattery.

**Video Formats and Required Load Terminations,** by Bill Slattery. 

\*Use the reply card to request your copy. Write on letterhead to subscribe to *DSPatch* and *Briefings*. VGA, IBM PC, PS/2, and Micro Channel are registered trade marks of International Business Machines Corporation.

†Trademarks of HEM Data Corporation, Laboratory Technologies Corporation, ASYST Software, Inc., and Intellution, Inc., respectively.

# Analog Devices Names Fellow

Fred Mapplebeck

Analog Devices has named a new Fellow, Fred Mapplebeck—Group Leader for Product Trim Engineering at Analog Devices Semiconductor—in recognition of his continuing valuable contributions to the growth of Analog Devices and its young technologists.




Analog Devices has achieved industry leadership as a manufacturer of reliable high-precision analog and data-converter circuits. Laser-trim of ICs, pioneered at ADI, is a key technology that kept us ahead of the pack, making possible levels of performance that were simply unavailable (by orders of magnitude) with silicon alone. Fred was the key technologist whose imagination, persistence, and leadership turned an "iffy" vision into a practical, everyday technique, widely used in the industry.

While design engineers get the glory for innovative designs of high-performance products, the unsung hero of the piece in many cases is the equally innovative *manufacturing process*, LWT—laser wafer-trim. Fred created a highly competitive trim process and developed workable trim algorithms for generations of products. Not only does LWT trim static parameters, such as gain and offset; Fred also developed *drift-trim* algorithms—a prime example is the 1.5-ppm/°C (max) AD588 voltage reference.

Fred has BSEE and MSEE degrees from Northeastern University. Before joining Nova Devices (which later became Analog Devices Semiconductor) in 1971, he worked at Transitron Electronics, Inc., as a Test Engineer. During his career at Analog Devices, he has been Test Engineer, Group Leader Test Engineering, Senior Product Engineer, Product Engineering Group Leader for Computational Circuits, and Group Leader Product Trim Engineering.

Besides his contributions to product design and manufacturing, he has also served as mentor to a number of younger engineers, helped a test-equipment vendor develop a new laser trim system, helped engineers in other Divisions develop trim techniques, written conference papers on trimming, and maintained close relationships with trim technologists in major test-equipment vendor companies. He has also worked with a U.S. Government committee on Trim-Resistor Visual Criteria.

Fred is married, with two children, and lives in Windham, New Hampshire. He enjoys playing tennis.

Fellow is the highest level of technical advancement within Analog Devices. Fellows are recognized for their innovativeness and outstanding technical contributions to the company, for acting as mentors to young technologists, for having demonstrated leadership of outstanding technical groups or in generating new business opportunities, and for having developed valuable industry and academic relationships for the company. 

Fred is our tenth Fellow. He joins the select company of *A. Paul Brokaw* (1980), *Lew Counts* (1984), *Barrie Gilbert* (1980), *Peter R. Holloway* (1985), *Jody Lopham* (1988), *Jack Memishian* (1980), *Michael P. Timko* (1982), *Robert W. K. Tsang* (1988), and *Mike Tuthill* (1988).



An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

## IN THE LAST ISSUE

Volume 23, Number 1, 1989, 24 Pages

Editor's Notes, Authors

*Hook Up Sensor-to-Serial Communications with a Scribe/Driver (6B Series)*

*8.192-Volt Reference Provides Maximum Resolution from 12-Volt Supply (AD689)*

*High-Accuracy Widest-Bandwidth Analog Multiplier (AD834)*

*Ultra-High-Speed Phase Discriminator Has No Dead Zone (AD9901)*

*New Monolithic 12-Bit Sampling ADCs Digitize Fast AC Waveforms (AD7870, AD1678)*

*Dual Bipolar Op Amp Provides Superior Matching of Specifications (AD708: dual AD707)*

*Low-Power 16-Bit DAC Provides High Accuracy At Low Cost (AD1145)*

*Isolated mV/TC Conditioner Has High Gain, Low Drift (1B51)*

*Four Sample/Holds on a Chip Feature 1-µs Max Acquisition Time (AD684)*

New-Product Briefs:

True 16-Bit IC DAC Is Monotonic, Has Voltage Output, Readback, (AD7846)

PS/2-Compatible Monolithic Color Palette 6-Bit RAM-DAC (ADV476)

8-Bit 256 × 24 Color Palette RAM-DAC with 3 × 24 Overlay Palette (ADV453)

I/O Boards for STD Bus: ADI Hardware & PC Software Compatible

(RTJ-1265/66/67)

Signal-Conditioning Panels for Data Acquisition with PCs, STD Bus,

µMACs (STB)

DAS Front End for 12 Bits: Hybrid with MUX, Diff Amp, S/H, Buffer Amp (AD1362)

Ask the Applications Engineer—2

Worth Reading, More Authors

Potpourri

Advertisement

**ERRATA:** . . . AD846 data sheet (C1155-10-9/88): Noise equations on pages 10 and 11 are in error. Expression for amplifier output noise (spectral density) should read:

$$V_{ON}^2 = (RFIN)^2 + (1 + RFRS)^2(VN^2 + (RFINP)^2)$$

To this should be added (noise)<sup>2</sup> due to resistors  
 $4kTRF(RFRS + 1)$

where  $k$  is Boltzmann's constant and  $T$  is absolute temperature. The equation on page 11 should be modified similarly . . . AD847 data sheet (C1191-10/488), page 6, Figure 21, IMPORTANT: wiper of trim potentiometer should be wired to Vs-, not Vst . . . AD9901 data sheet (C1272-10-2/89), page 10: replace left-hand 182-ohm resistor by a line; label AD9901 outputs (upper-OUT, lower OUT) . . . AD9048 data sheet (C1212-11-7/88), page 5, LCC and PLCC pin configuration drawings: pin 26 should be labeled R<sub>B</sub>; label pin 28 NMINV . . . AD9521 Log Amp data sheet (C1128-9-9/87): new specifications are available for Detected Video output current (max) at 120 MHz, all grades and conditions. Consult your local sales office

**PRODUCT NOTES:** . . . AD9611: Permanent degradation in performance is possible (a) when a differential input voltage applied to the inverting input is > +4 V or < -1 V with respect to the non-inverting input (b) if the negative power-supply voltage is applied to the device in the absence of positive supply voltage. Bias-current spec change—new low-temp, 25°C, high-temp limits are: inverting, ±45, ±7, ±24 µA; non-inverting, ±30, ±7, ±20 µA . . . AD9300, new specs on Crosstalk Rejection, One Channel—AD9300KQ/TQ: 75 dB min, 78 dB typ; AD9300KP/TE: 78 dB min, 80 dB typical . . . LABTECH Software is available to support the RTI-204/205 data-acquisition boards for PS/2 Micro Channel and the 6B11/12 configurable digitizing signal-conditioning modules; CONTROL EG now supports the RTI-204/205 and the 6B11/12; ASYST now supports the RTI-820 and RTI-1265 (STD Bus) series; THE FIX is now compatible with ProLog System 2 for use with the RTI-1265 Series. For hardware or software information on data-acquisition modules and subsystems, call 1-800-4-ANALOG or the nearest sales office . . . An ADSP-2100 sample kit is now available to provide DSP designers with everything they need to take a long, serious look at our powerful family of processors. The ADSP-2100A Sample Pack contains an ADSP-2100AJG 10-MHz processor, a software-simulator demo disk and manual, and data sheets covering software and hardware development tools. It is priced at \$49.95—one to a customer, please!

**PACKAGING** . . . Five more SOIC (small-outline IC) packaged op amps join the AD711, AD707, AD548, and ADOP07: The AD712 4-MHz dual-channel bipolar-FET (dual AD711), the 13-MHz AD744, with 750-ns max 0.01% settling time, the 50-MHz-GBW 300-V/µs low-quiescent AD847, and the AD848 and AD849 (see page 15 of this issue) . . . The AD1856 and AD1860 16- and 18-bit audio DACs, each in three grades of THD, are now available in SOICs—16-lead widebody "R" packages.

**APPLICATIONS:** . . . A way of interfacing the AD7878 a/d converter with microprocessors asynchronously is described in a short note by John Reidy, of Analog Devices BV. Ask your nearby sales office for a copy . . . A series of intensive, hands-on three-day DSP workshops, "System Development and Programming with the ADSP-2100 family," is available for interested persons. For information, call (617) 461-3672 or your nearby sales office . . . The AD1856 and AD1860 audio-DAC data sheets show applications with digital filter chips from YAMAHA and NPC. Your nearby sales office can tell you how to get in touch with the manufacturers.

**PATENTS RECEIVED** . . . 4,703,283 to Howard Samuels for Isolation Amplifier with T-Type Modulator . . . 4,791,551 to Douglas Garde for Microprogrammable Devices Using Transparent Latch . . . 4,804,960 to John W. Fernandes, Gerald A. Miller, Andrew M. Mallinson, and Stephen R. Lewis for Sub-Ranging A/D Converter with Improved Error Correction . . . 4,814,767 to John W. Fernandes, Gerald A. Miller, and Andrew M. Mallinson for Sub-Ranging A/D Converter with Flash Converter Having Balanced Input.

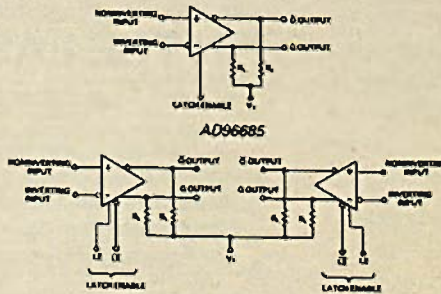


**FEATURES**

2.5ns Propagation Delay  
Consistent 50ps Propagation Delay Dispersion  
0.5ns Latch Setup Time  
Stable Transition Zones  
Low Power Dissipation

**APPLICATIONS**

High Speed Triggers  
High Speed Line Receivers  
Peak Detectors  
Threshold Detectors



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50V TO 200V CONNECTED TO -1.5V ON 200K1 - 200M1

**AD96687**
**Functional Block Diagrams**
**PRODUCT DESCRIPTION**

The AD96685 (single) and AD96687 (dual) are ultrafast voltage comparators with short, consistent propagation delays and setup times. Both devices feature an incredible 50ps propagation delay dispersion for any overdrive from 100mV to 1V.

Propagation delays for both units are 2.5ns, and both have stable transition zones. They are manufactured with a high performance bipolar process and have differential inputs and complementary outputs (fully compatible with ECL logic levels). Their 30mA output currents are capable of driving 50 $\Omega$  terminated transmission lines; a latch enable input allows operation in either a sample mode or a track mode.

There are six models of the single AD96685 comparator; three operate over an industrial temperature range of -25°C to +85°C, and the other three are for extended temperatures of -55°C to +125°C. Two of the four models of the dual AD96687 unit operate over industrial temperatures, and the other two are for extended temperatures.

**PRODUCT HIGHLIGHTS**

1. Propagation delay dispersion of 50ps is the lowest available. Because of this extremely low dispersion, the AD96685 and AD96687 comparators can be used to make very fast, accurate and repeatable measurements despite wide variations in input overdrive; this improves performance for systems using these units.
2. The ultrafast latches allow the comparators to operate in a high speed sample (track)-and-hold mode. When the latch is used properly, input pulses of extremely short duration can be accurately detected and held for additional processing.
3. Since the latch operates on the input state of the comparator, the output state is dependent on the input at the time of the LATCH ENABLE command. This contrasts with strobed comparators, which operate on the output regardless of the input conditions at the time of the strobe.
4. Due to the elegant design of the AD96685 and AD96687 comparators, oscillation-free performance extends over a wide variation of input slew rates and overdrive conditions. This characteristic is not available in many other pin-compatible devices; they often have severe restrictions on how they can be used.

# COMPARED TO WHAT'S ON THIS PAGE, NO OTHER COMPARATORS ARE EASIER TO USE.



If the output from your present comparator makes it difficult to use, take a look at the incomparable AD96685 and AD96687. They're the only comparators whose propagation delays remain constant to within 50 picoseconds for any overdrive from 100mV to 1V, so you always get consistent output.

The AD96685 and AD96687 also give you consistent speed, since they switch in 2.5ns, with a setup time of 0.5ns. And they have remarkably stable transition zones, which minimize oscillation.

But speed isn't achieved at the expense of power.

The single AD96685 dissipates a mere 118mW, and the dual AD96687 needs just 237mW.

In addition, the AD96685 and AD96687 each have an offset voltage of 1mV typical for a consistent starting point, and an input voltage range of -2.5V to +5V.

Now despite all these advantages, you won't have to change your board design for the AD96685 and AD96687. They're ECL-compatible and drop-in replacements for standard devices. If you'd like a further comparison of the AD96685 and AD96687, call your nearest Analog Devices sales office.



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