The Implementation of the New Type Impedance Measurement System

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Abstract

The design principle and implementation scheme of a new type FPGA-based RLC impedance analyzer within the scope of 100Hz～100kHz is designed. The system adopts FPGA and DA framework to realize the DDS signal output with low distortion, takes DA of multiplication type as phase sensitive detector, uses the orthogonal decomposition method to decompose the measured signals into orthogonal component and in-phase component to raise the signal-to-noise ratio, and uses the dual slope integral circuit with zero crossing compensation as signal acquisition circuit to make the acquired signal to be the quotient between orthogonal component and in-phase component, which greatly decrease the drift error of the electric circuit. The experiment verified that the system index can reach 0.1％.

1. Introduction

Impedance is an important parameter used to characterize component, electronic circuits, and the materials used to make components. Impedance not only is an important parameter in the electricity metrology, but can also reflect other indicators of physical and chemical properties at the same time. Therefore, the metrology of impedance becomes more and more important.

Currently, the commonly used measuring methods of impedance [1] include bridge method, resonant method, I-V method, RF I-V method and network analysis method. The RF I-V method and the network analysis method are often used in the high-frequency impedance measurement, and currently, the low and medium frequency impedance analyzers are normally adopt the principle of I-V method.

The system adopts the DDS-based low distortion signal source, multiplicative DAC-based phase sensitive detector and the improved dual slope integrator to make up the new type impedance analyzer. Followings are detail working principles and implementations.

2. Working Principle

The working process is as follows: The frequency resolution generated by DDS that is consisted of FPGA and DA is 0.009Hz within frequency domain of 100Hz～100kHz, which will produce low distortion excitation signal with high quality after smoothing and amplifying. The frequency of output is settled through software control.

The excitation source is exerted on the device under test, and after standard impedance selection and signal conditioning, the two-circuit voltage signal of the device under test and standard impedance passes the two-circuit DA of multiplication type and multiplies the local oscillator with the same frequency, and then, goes through the low pass filter to filter the alternating component and enter into the dual slope integral AD in turns before finally being calculated out the impedance data by ARM.

The signal demodulation adopts the I-V method [2~4] as shown in Figure 1, and the two-circuit signal will undergo orthogonal decomposition after signal conditioning and calculate the projections U1a, U1b, U2a and U2b on the in-phase direction and the orthogonal coordinate axis on the basis of the voltage vectors on both ends of the device under test and both ends of the standard impedance, to obtain the impedance

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$$|Z_1| = \frac{\sqrt{U_{1a}^2 + U_{1b}^2}}{\sqrt{U_{2a}^2 + U_{2b}^2}} |Z_2| \tag{1}$$

From the formula, the proportional relation of the concerned U1a, U1b, U2a and U2b can be seen without paying attention to the absolute information, so we compute the proportion between projections instead of the absolute value. The advantage of doing this is to change the absolute measurement into proportional measurement, which can reduce the influence from the component temperature drift and long term drift.

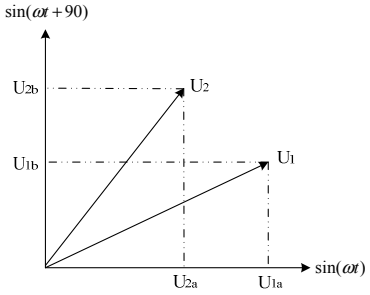

Figure 1: Principle of Voltage-Current Vector Method

3. Hardware

The working principle of the system is shown as Figure 2:

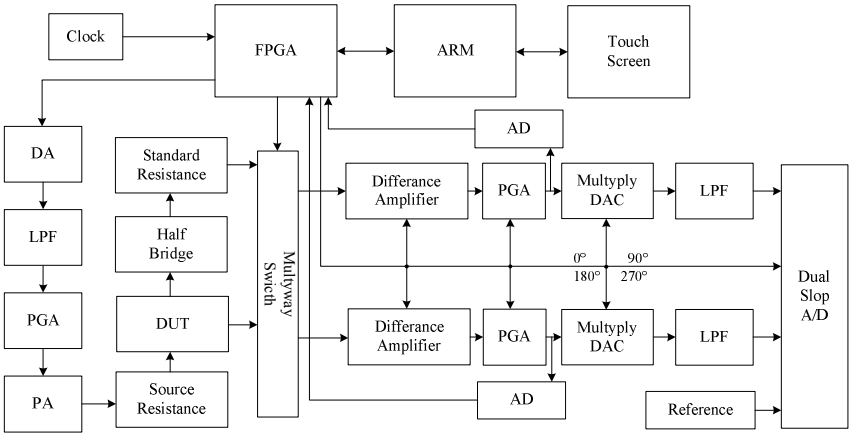

Figure 2: Functional Block Diagram of Impedance Analyzer

3.1 DDS Signal Source

The design of the signal source includes clock circuit, DA circuit and filter circuit.

The fundamental part of the DDS includes: Reference clock, phase accumulator, sine lookup table, DA convertor and low-pass filter. The principle is shown as in Figure 3:

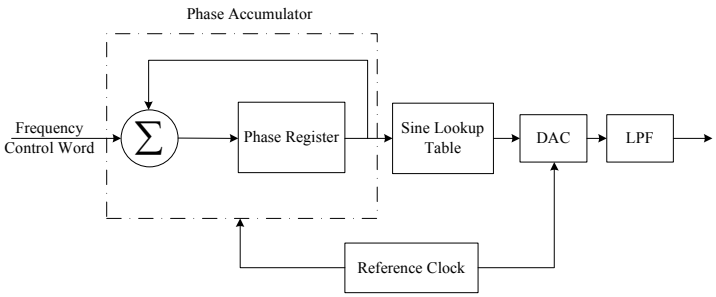

Figure 3: DDS Schematic Diagram

The reference clock adopts high stable temperature-compensation crystal oscillator, phase accumulator and sine

lookup table to realize through FPGA, and DAC adopts DA chip AD9744 with 14 digits resolution.

Since any figure of the DA output chip, phase accumulator and sine lookup table is not high enough, and they will produce truncation spurious noise, so certain research scholars have carried out theoretical analysis in 1998[5], giving the approximate mathematic relation between the synthetic waveform distortion and the M and N when the discrete point M and DAC resolution N are limited. Combining the formula and the experiment [6] we find:

（1）The discrete point M has bigger influence on the THD, and in the case of fewer points, THD decreases rapidly with the increase of the point.

（2）When the discrete points M is relatively small, the DA digit N has insignificant influence on the wave form distortion, but with the increase of M, the DA digit N has more and more significant influence on the THD.

In order to lower the THD, on the one hand, use the high frequency clock （40MHz）to control the DA input to increase the discrete point rather than use the fixed point waveform synthesis such as 1024 points, and on the other hand, use the 14-digit DA chip AD9744.

After lowering the DDS direct output spurious noise, it is needed to add a low pass filter on the output end to reduce the wave distortion at a maximum degree, so the characteristics of the filter have crucial influence on the output signal performance. In consideration of the relatively wide system band, the system design a 7-stage low pass elliptic filer and 4 sets of low pass active filter to filter out the low-frequency interference on the basis of the different frequency bands.

3.2 Signal Conditioning and Phase Sensitive Detection

In signal conditioning, the appropriate standard impedance and programmable gain amplification factor are selected based on the size of the two-circuit signal, and after the mixing by multiplication type DA and smoothing, the signal is sent to the dual slope integral circuit for data acquisition. The circuit and integral process of the dual slope integrator is shown as in Figure 4.

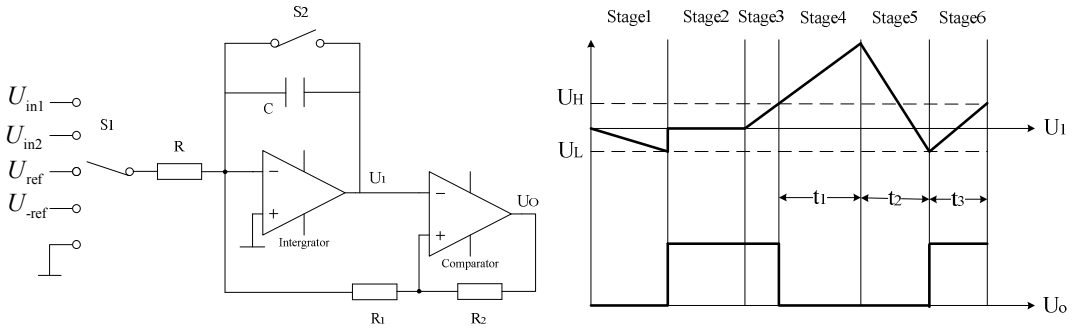

Figure 4: Schematic Diagram of Dual slope Integrator

The error from the dual slop integrator is the start voltage of integrator and the end voltage of integrator which usually is zero crossing voltage of the comparator are not equal. To solve the problem, the positive feedback of the comparator and additional reference voltage are used. From Figure 4, we get that the start voltage of integrator and the end voltage of integrator are both U_H. U_H and U_L are the feedback voltage of the comparator when the output of comparator is high or low. The proportional integral procedure is divided into six stages to eliminate the zero crossing error. Then the proportion of the two voltages shall be $U_{in1}/U_{in2}=t_2/(t_1+t_3)$. This method eliminates the zero crossing error of the integrator.

4. Experiment

Part of The experimental results are shown in chart 1, The experiment verified that the system index can reach 0.1％.

Chart 1: Experiment data

Test Point	Standard Value	Measurement Value	Error
1nF/1kHz	0.9999	1.0002	0.03%
10nF/1kHz	10.0007	10.0013	0.01%
100nF/1kHz	100.001	100.021	0.02%
1mH/1kHz	1.0001	1.0000	-0.01%
10mH/1kHz	10.0000	9.9980	-0.02%
100mH/1kHz	100.0100	99.96	-0.05%
100Ω/1kHz	100.0000	99.9500	-0.05%
1kΩ/1kHz	1.0000	0.9997	-0.03%
10kΩ/1kHz	10.0000	9.9980	-0.02%

5. Conclusion

The system uses the orthogonal proportion decomposition method to demodulate the two-circuit voltage vector signal, uses the DA of multiplication type to complete the frequency mixing function, and uses the dual slope integral type AD to collect the signals, by measuring the proportion of voltage and eliminating the zero crossing error, we decrease part of the drift of circuit, improving performance.

6. References

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