



UltraZed-EG SOM

Revision 1

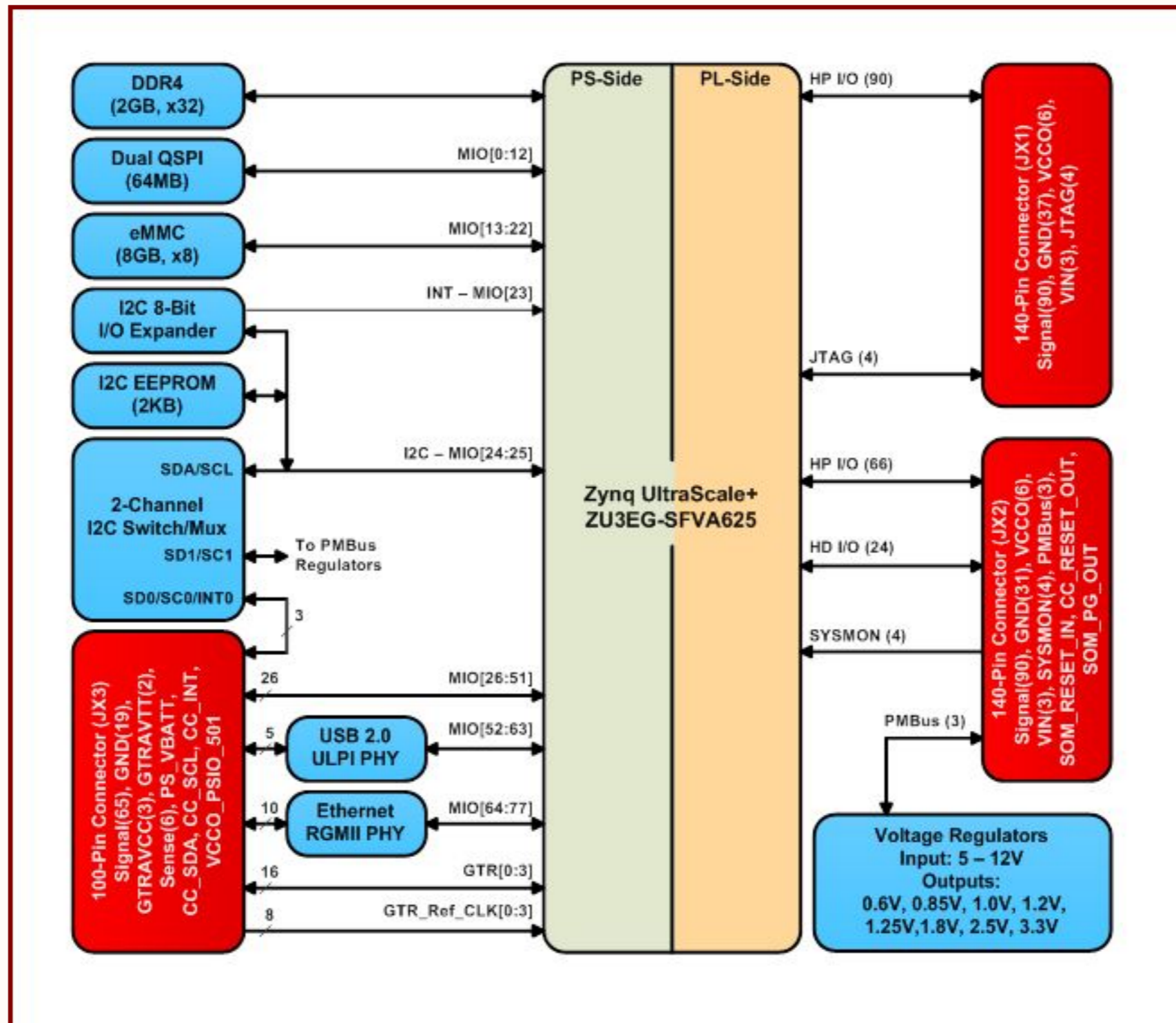
UltraZed-EG SOM	
Avnet Engineering Services	
www.avnetkits.com	
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Project Name:	UltraZed-EG SOM	PCB Rev:	BOM:	Variant:	
		1	02	01	
Doc Num:	SCH-US1SOM	Date:	8/13/2018	Time:	10:17:13 AM
Sheet Title:	01 - Avnet Lead Sheet.SchDoc	Size:	B	Sheet:	1 of 18

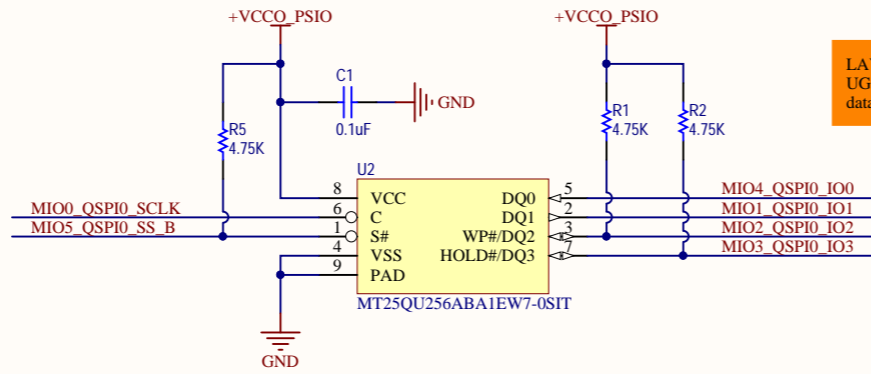


U1C

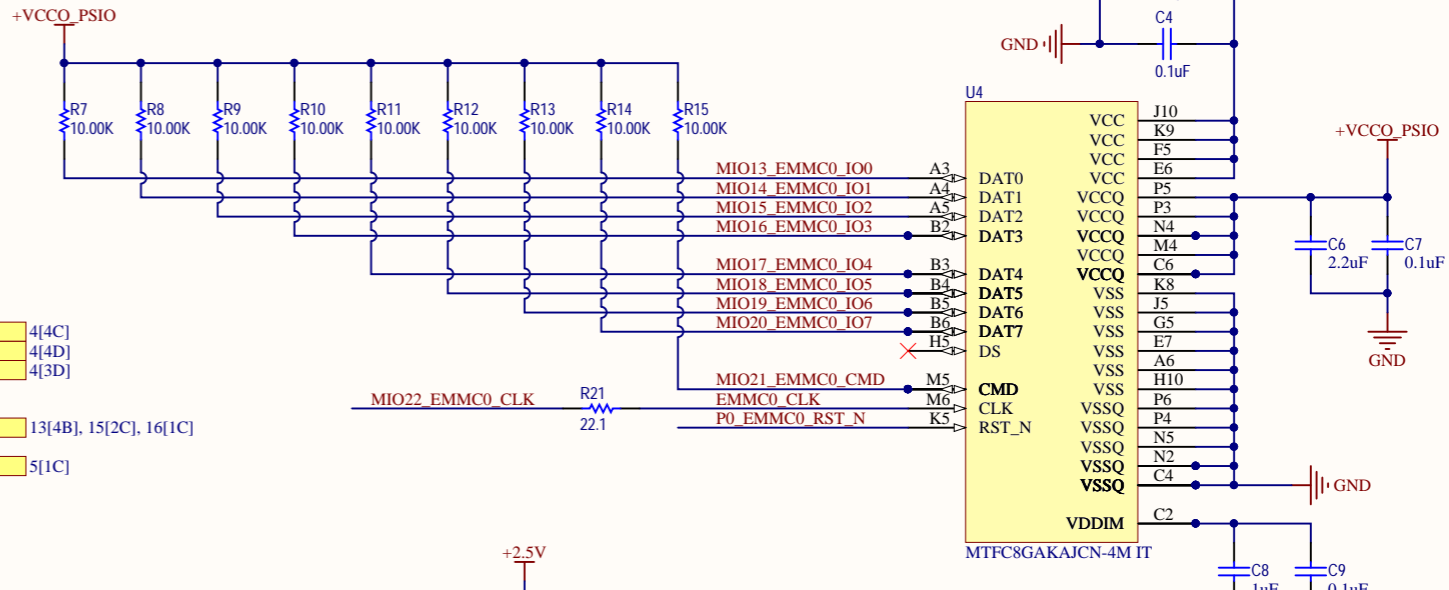
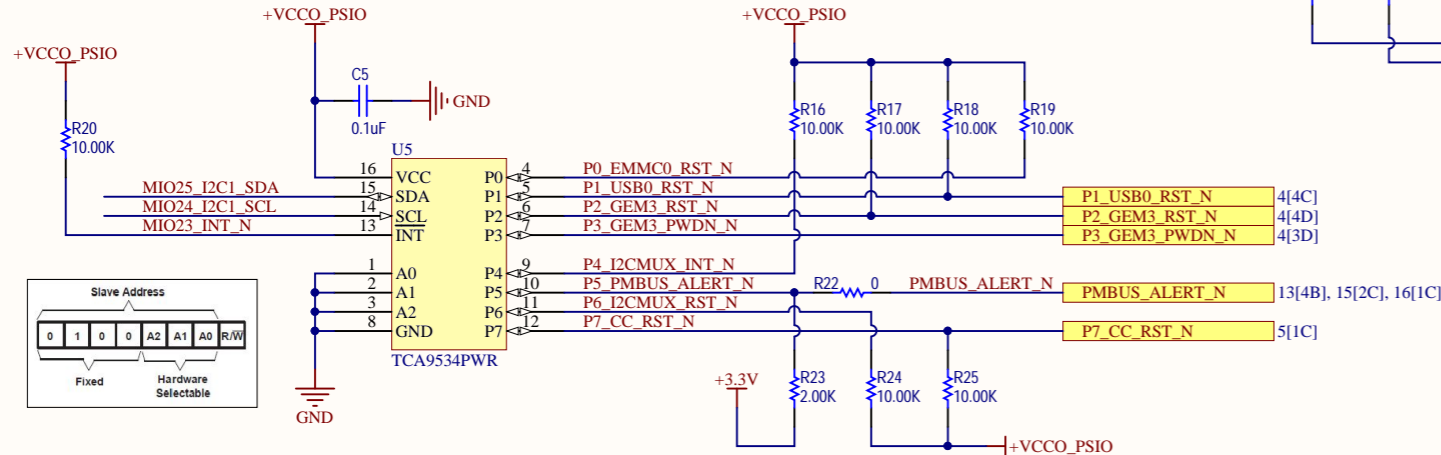
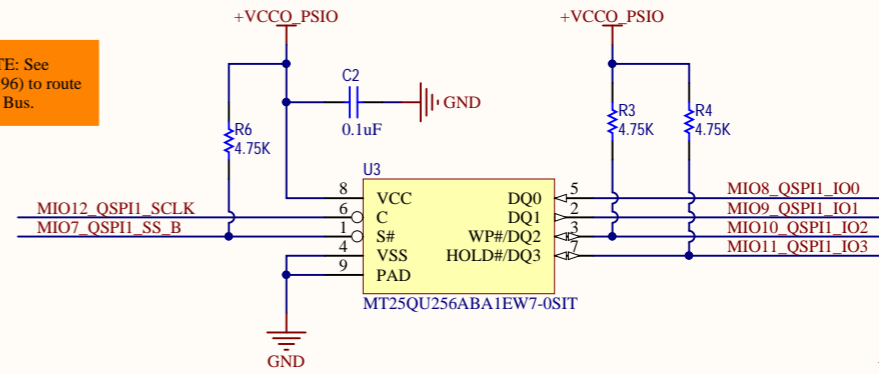
BANK 500

PS_MIO0	V10	MIO0_QSPI0_SCLK
PS_MIO1	W11	MIO1_QSPI0_IO1
PS_MIO2	V11	MIO2_QSPI0_IO2
PS_MIO3	W9	MIO3_QSPI0_IO3
PS_MIO4	Y9	MIO4_QSPI0_IO0
PS_MIO5	AA10	MIO5_QSPI0_SS_B
PS_MIO6	Y10	
PS_MIO7	Y11	MIO7_QSPI1_SS_B
PS_MIO8	AC10	MIO8_QSPI1_IO0
PS_MIO9	AB10	MIO9_QSPI1_IO1
PS_MIO10	W12	MIO10_QSPI1_IO2
PS_MIO11	AE10	MIO11_QSPI1_IO3
PS_MIO12	AB11	MIO12_QSPI1_SCLK
PS_MIO13	Y12	MIO13_EMMC0_IO0
PS_MIO14	AC11	MIO14_EMMC0_IO1
PS_MIO15	W13	MIO15_EMMC0_IO2
PS_MIO16	V13	MIO16_EMMC0_IO3
PS_MIO17	AD11	MIO17_EMMC0_IO4
PS_MIO18	AB12	MIO18_EMMC0_IO5
PS_MIO19	AE11	MIO19_EMMC0_IO6
PS_MIO20	AA12	MIO20_EMMC0_IO7
PS_MIO21	AD12	MIO21_EMMC0_CMD
PS_MIO22	W14	MIO22_EMMC0_CLK
PS_MIO23	V14	MIO23_INT_N
PS_MIO24	Y14	MIO24_I2C1_SCL
PS_MIO25	AE12	MIO25_I2C1_SDA

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LAYOUT NOTE: See UG583 (Page 196) to route data as an 8-bit Bus.

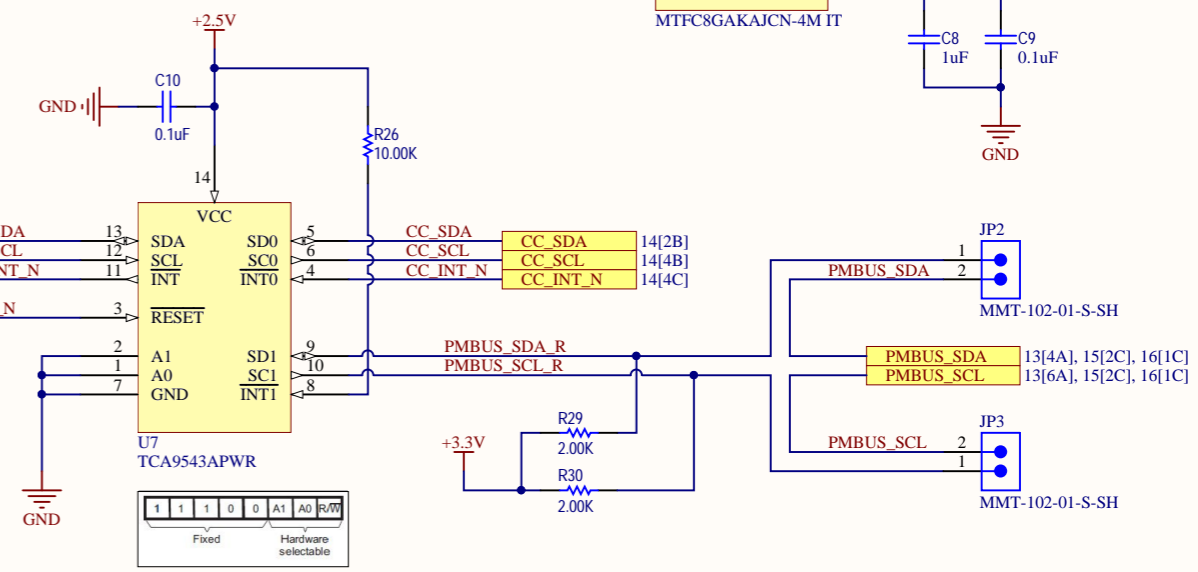
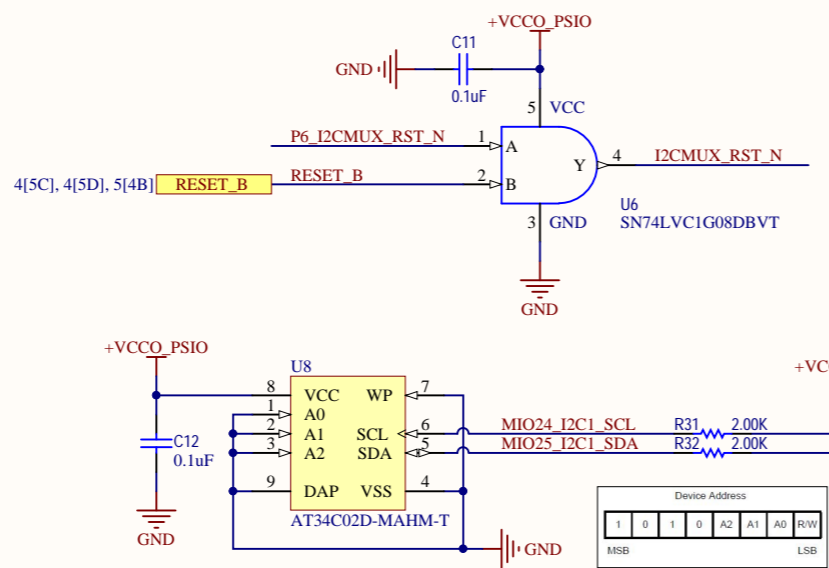


U1D

BANK 501

PS_MIO26	H13	MIO_26	14[2C]
PS_MIO27	G13	MIO_27	14[4C]
PS_MIO28	H14	MIO_28	14[2C]
PS_MIO29	B13	MIO_29	14[4C]
PS_MIO30	A13	MIO_30	14[4C]
PS_MIO31	C13	MIO_31	14[2C]
PS_MIO32	D13	MIO_32	14[2C]
PS_MIO33	F13	MIO_33	14[2C]
PS_MIO34	E14	MIO_34	14[2C]
PS_MIO35	F14	MIO_35	14[4C]
PS_MIO36	D14	MIO_36	14[2C]
PS_MIO37	H15	MIO_37	14[4C]
PS_MIO38	C14	MIO_38	14[2C]
PS_MIO39	A14	MIO_39	14[2C]
PS_MIO40	G15	MIO_40	14[4C]
PS_MIO41	A15	MIO_41	14[4C]
PS_MIO42	F15	MIO_42	14[2C]
PS_MIO43	B15	MIO_43	14[2C]
PS_MIO44	E15	MIO_44	14[4C]
PS_MIO45	H16	MIO_45	14[2C]
PS_MIO46	C15	MIO_46	14[2C]
PS_MIO47	B16	MIO_47	14[4C]
PS_MIO48	C16	MIO_48	14[4C]
PS_MIO49	G16	MIO_49	14[2C]
PS_MIO50	E16	MIO_50	14[4C]
PS_MIO51	D16	MIO_51	14[4C]

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			10:17:13 AM	
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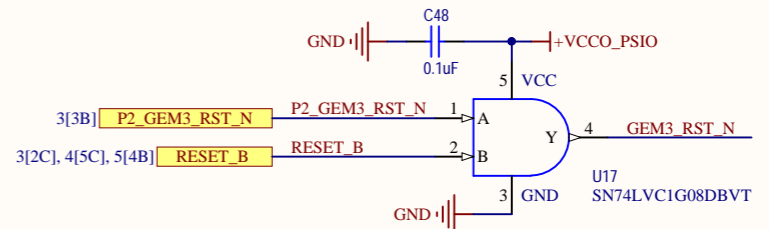
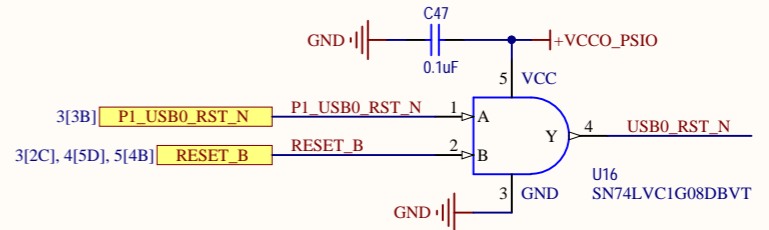
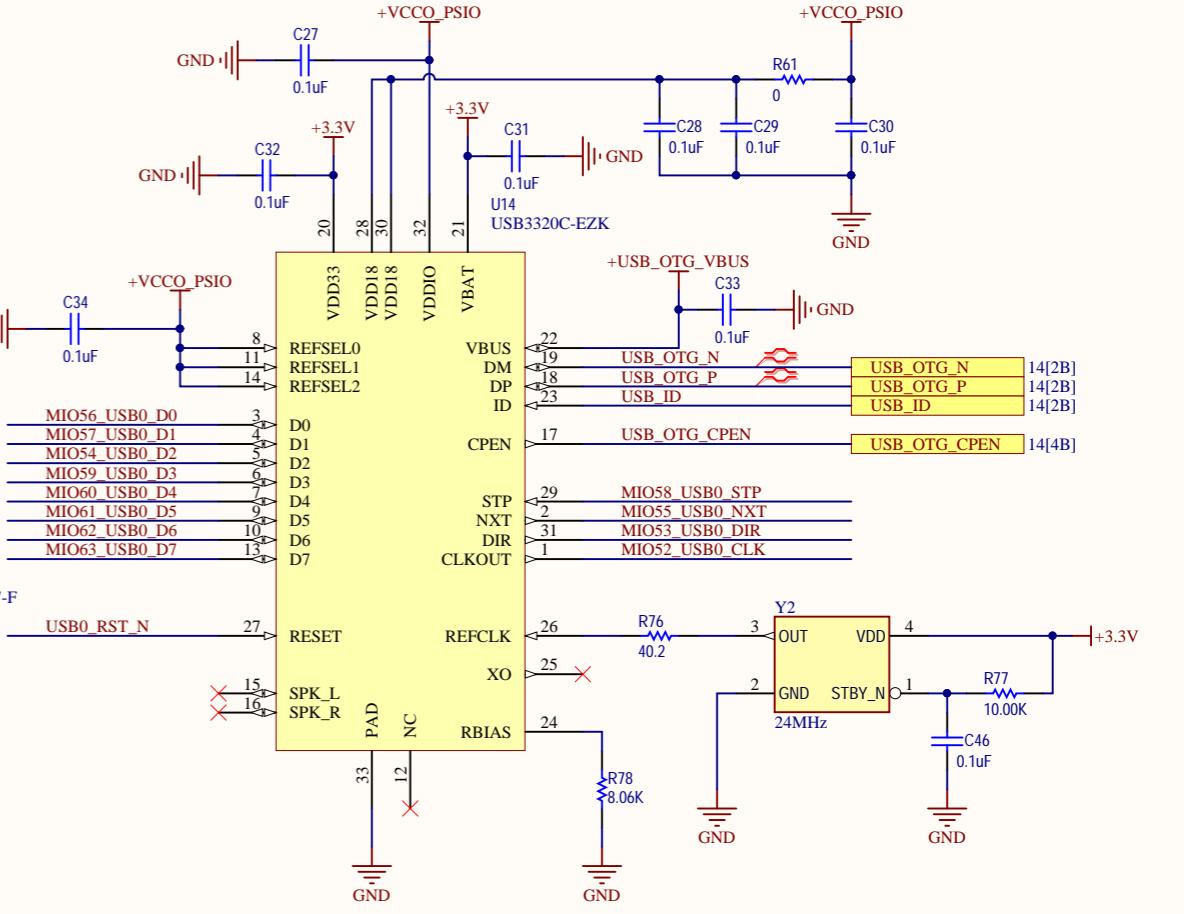
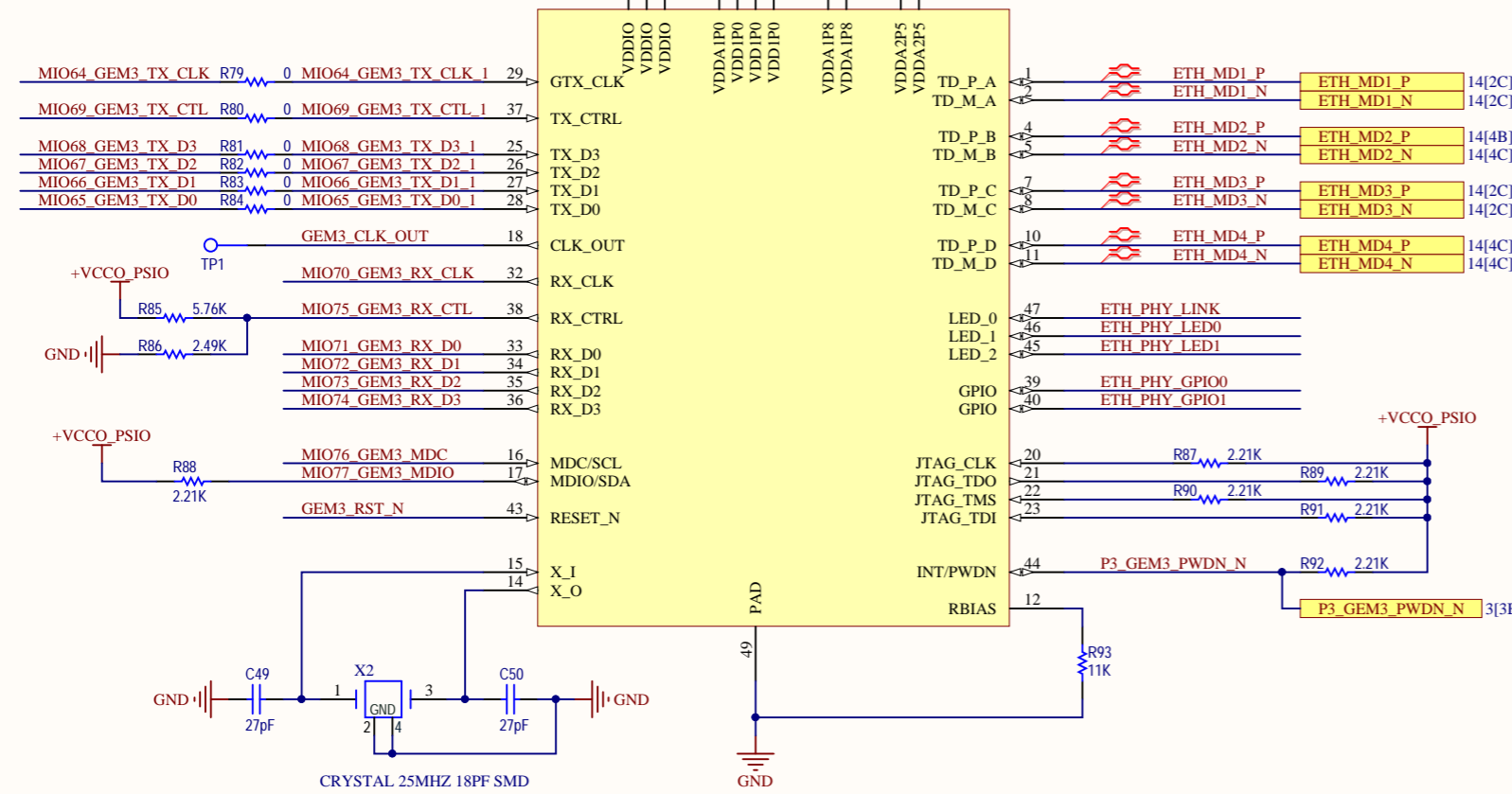
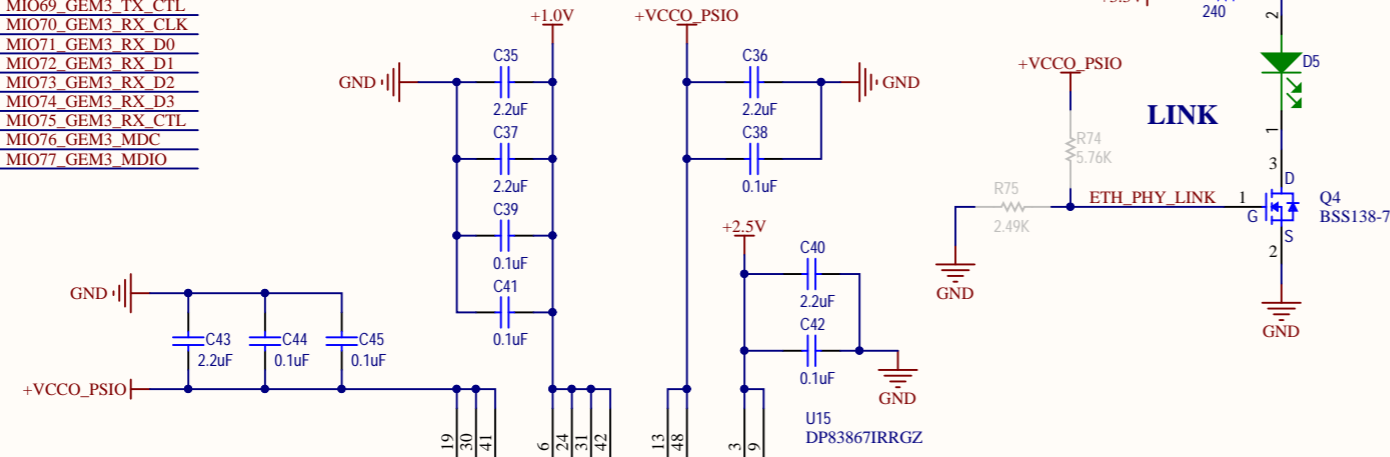
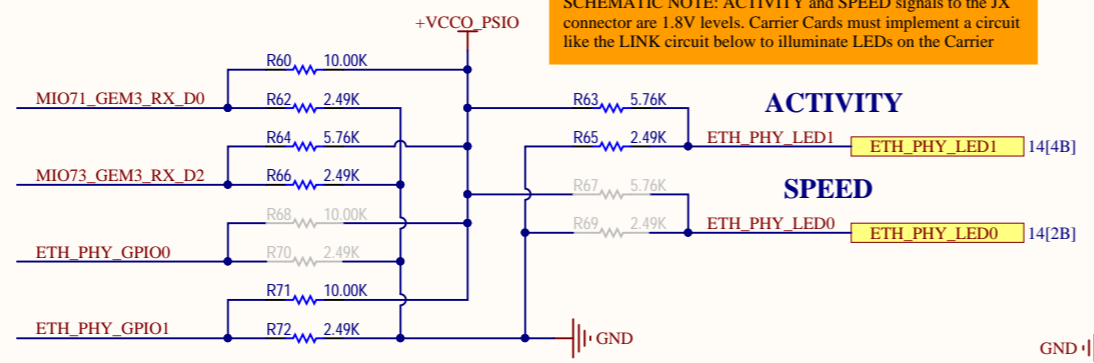
SCHEMATIC NOTE: ACTIVITY and SPEED signals to the JX connector are 1.8V levels. Carrier Cards must implement a circuit like the LINK circuit below to illuminate LEDs on the Carrier

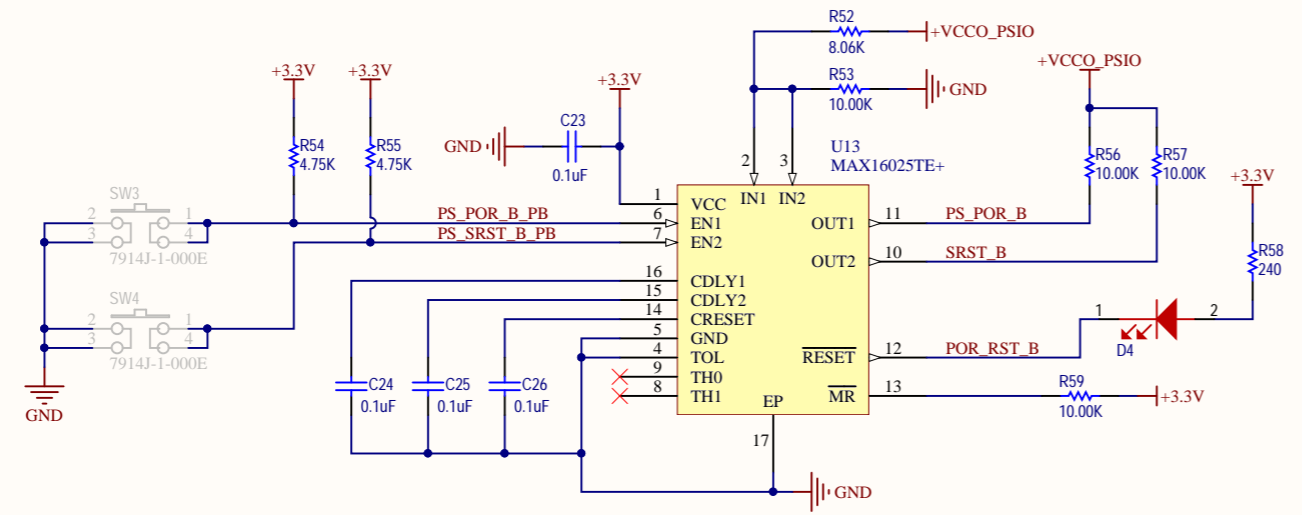
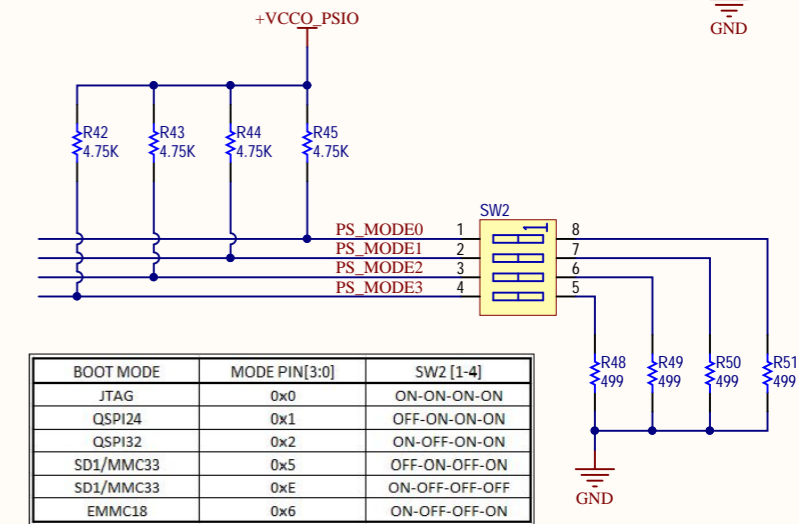
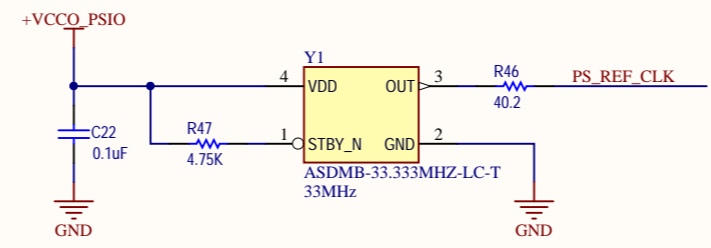
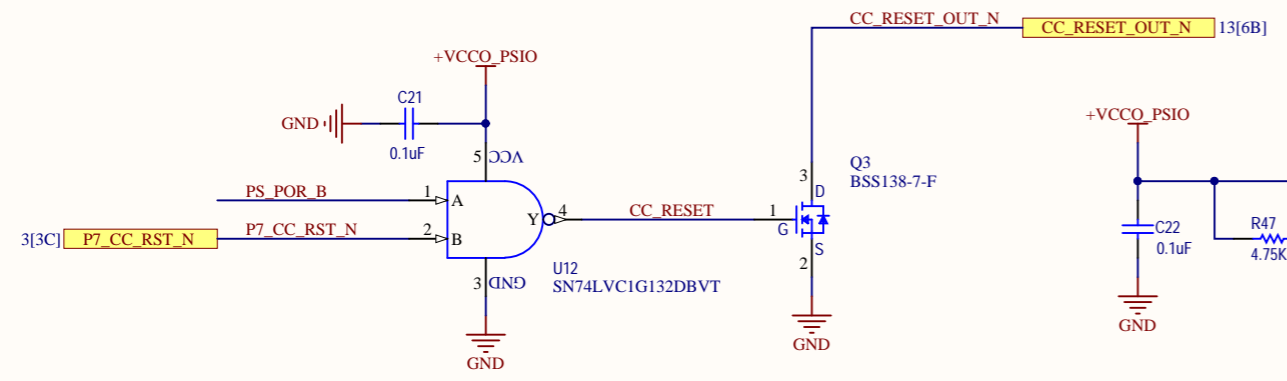
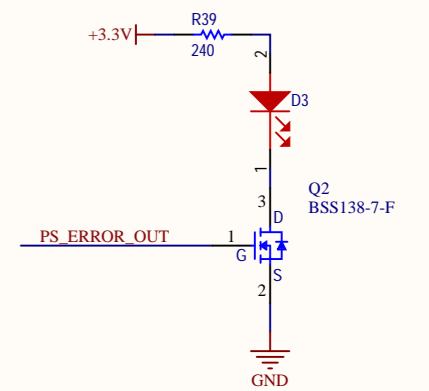
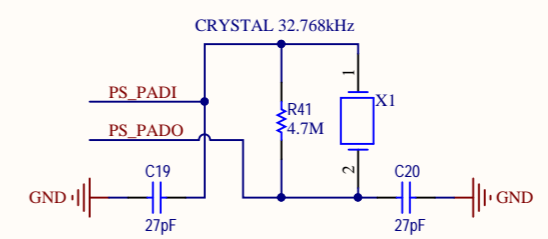
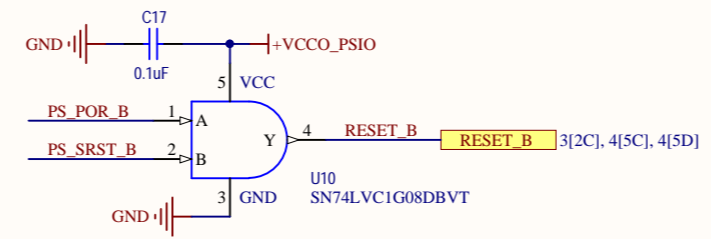
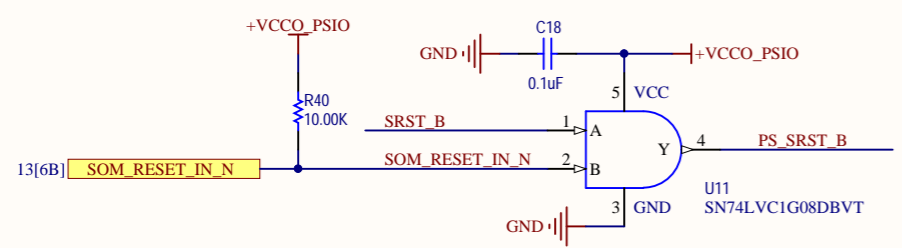
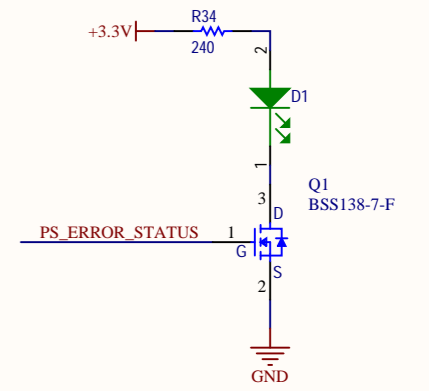
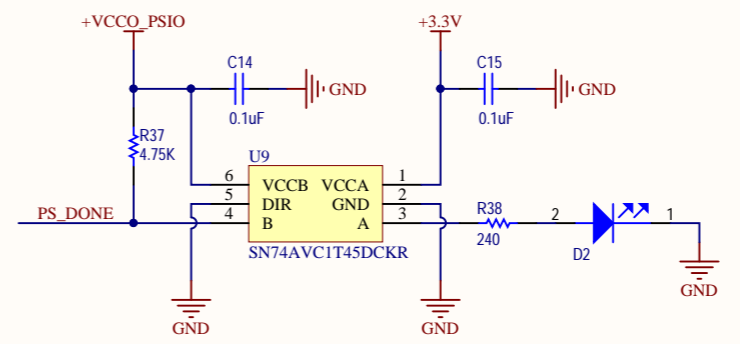
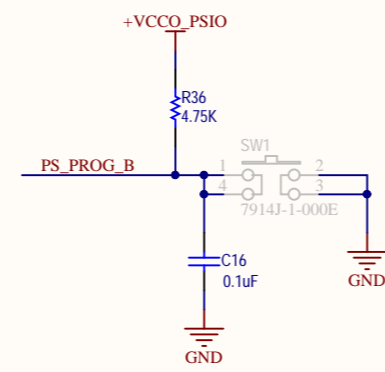
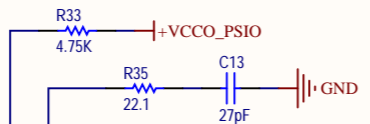
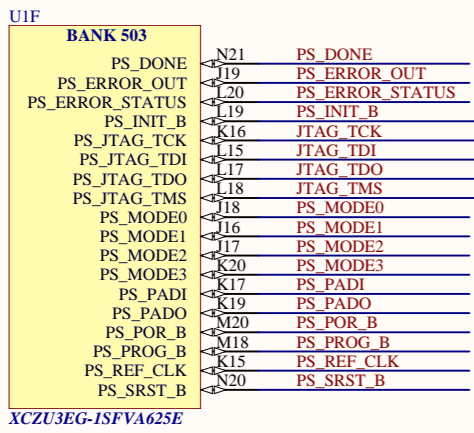
U1E

BANK 502

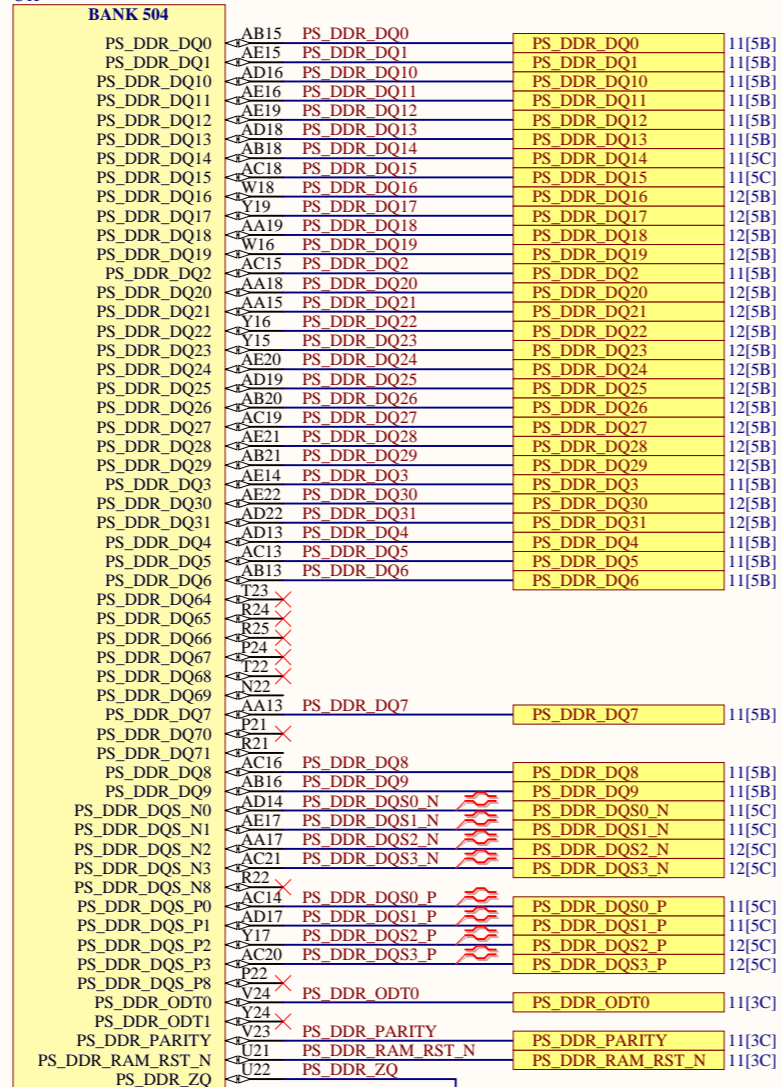
PS_MIO52	G17	MIO52_USB0_CLK
PS_MIO53	E17	MIO53_USB0_DIR
PS_MIO54	F17	MIO54_USB0_D2
PS_MIO55	B17	MIO55_USB0_NXT
PS_MIO56	D17	MIO56_USB0_D0
PS_MIO57	A17	MIO57_USB0_D1
PS_MIO58	A18	MIO58_USB0_STP
PS_MIO59	B18	MIO59_USB0_D3
PS_MIO60	A19	MIO60_USB0_D4
PS_MIO61	C18	MIO61_USB0_D5
PS_MIO62	C19	MIO62_USB0_D6
PS_MIO63	D18	MIO63_USB0_D7
PS_MIO64	F18	MIO64_GEM3_TX_D0
PS_MIO65	A20	MIO65_GEM3_TX_D1
PS_MIO66	D19	MIO66_GEM3_TX_D2
PS_MIO67	H18	MIO67_GEM3_TX_D3
PS_MIO68	G18	MIO68_GEM3_TX_D4
PS_MIO69	B20	MIO69_GEM3_TX_CTL
PS_MIO70	C20	MIO70_GEM3_RX_CLK
PS_MIO71	E19	MIO71_GEM3_RX_D0
PS_MIO72	E20	MIO72_GEM3_RX_D1
PS_MIO73	F20	MIO73_GEM3_RX_D2
PS_MIO74	G20	MIO74_GEM3_RX_D3
PS_MIO75	F19	MIO75_GEM3_RX_CTL
PS_MIO76	H20	MIO76_GEM3_MDC
PS_MIO77	H19	MIO77_GEM3_MDIO

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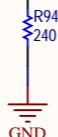


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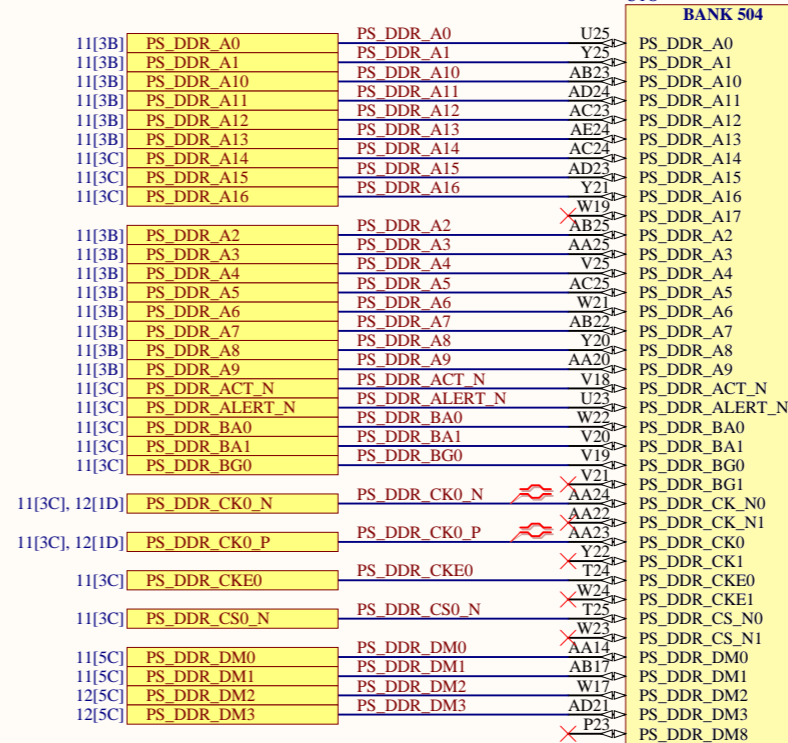


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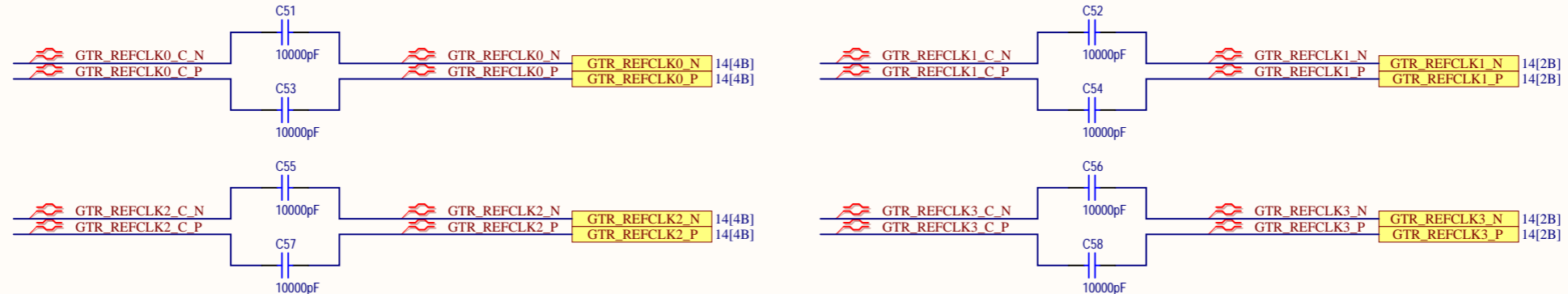
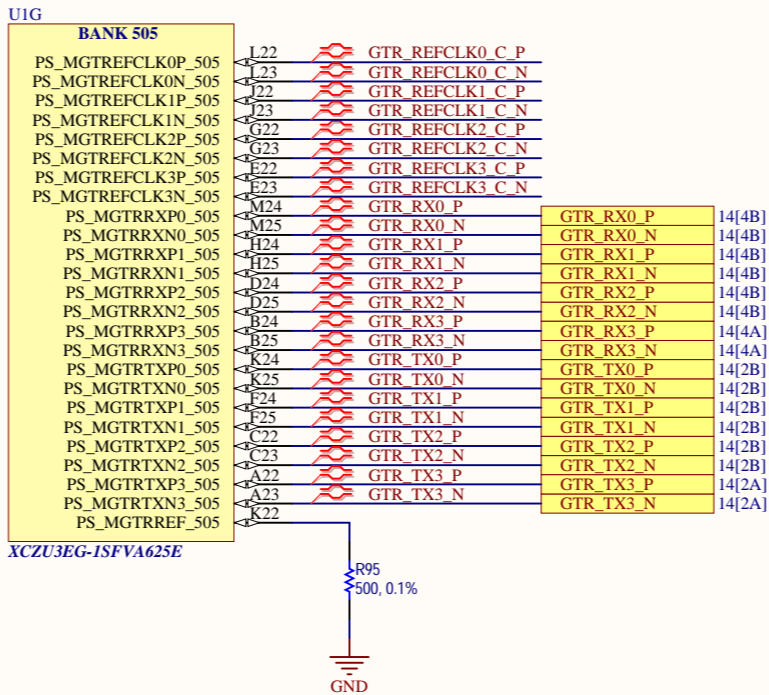
LAYOUT NOTE:
Place ZQ resistor
close to U1.



UI0

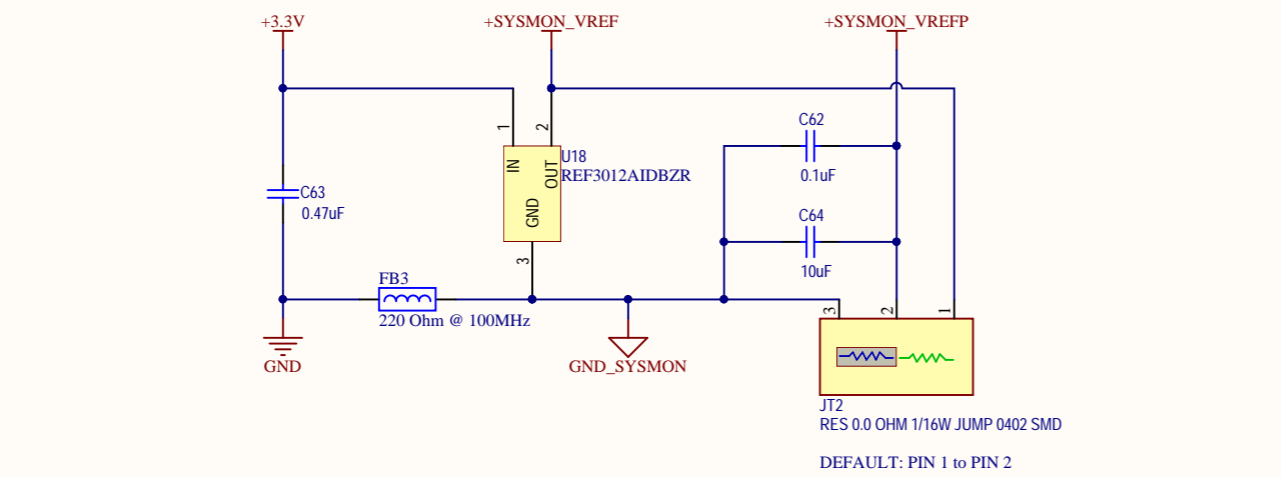
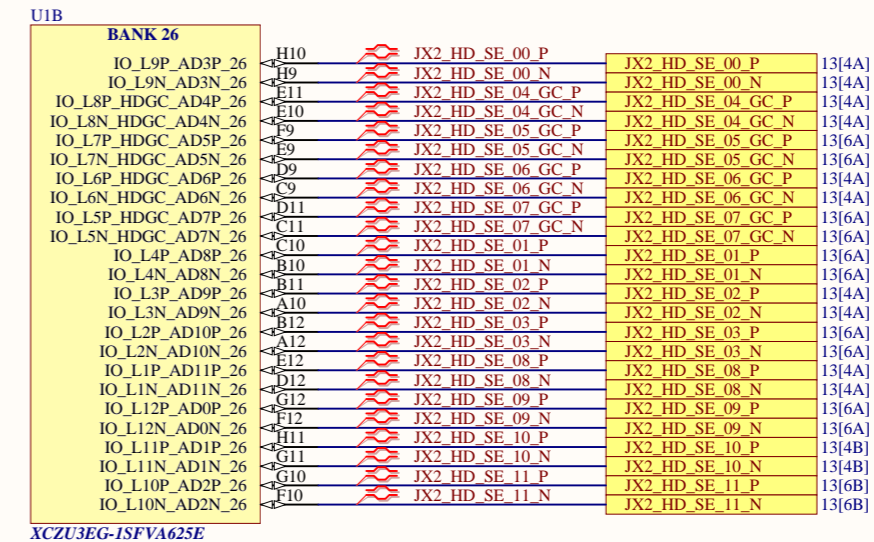
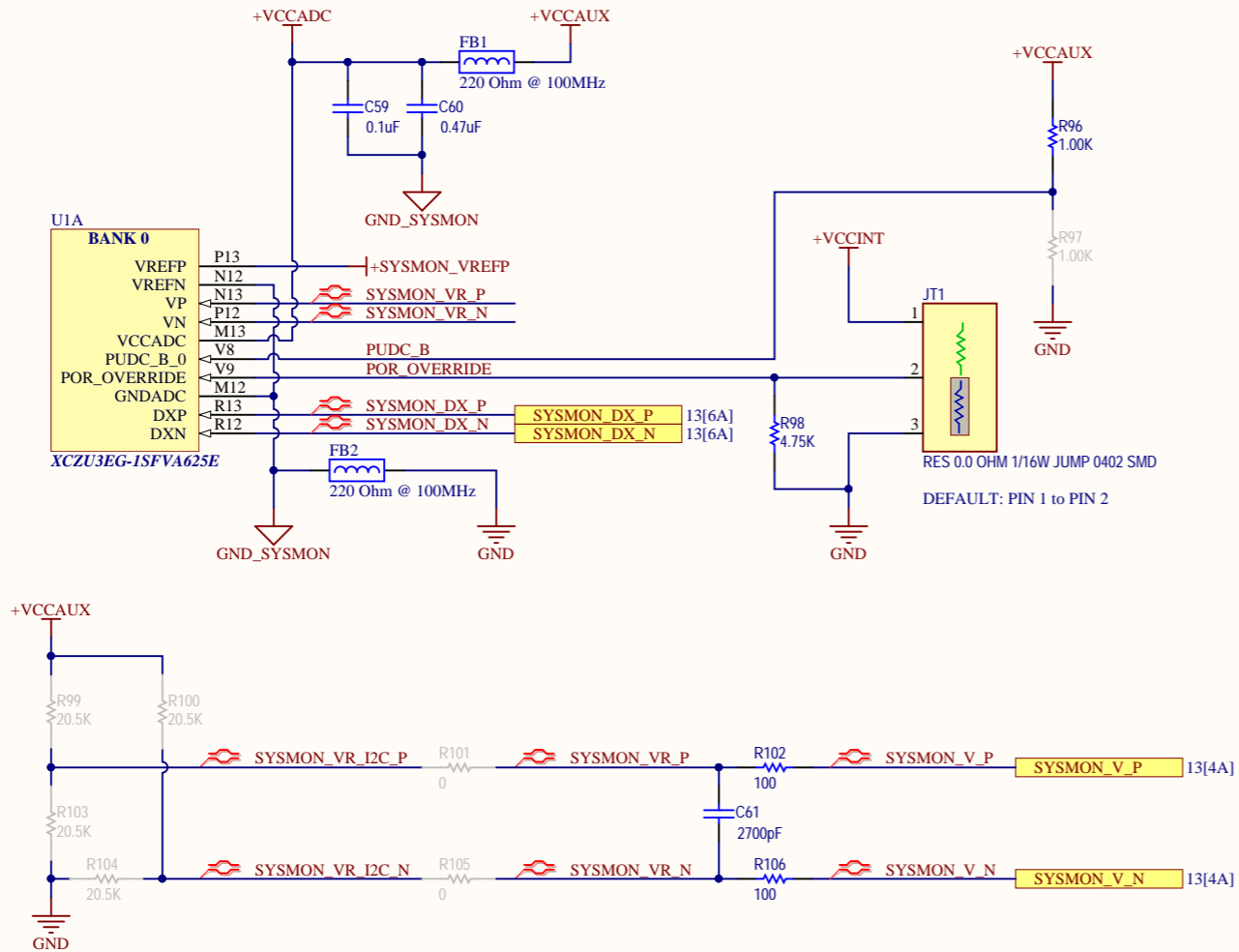


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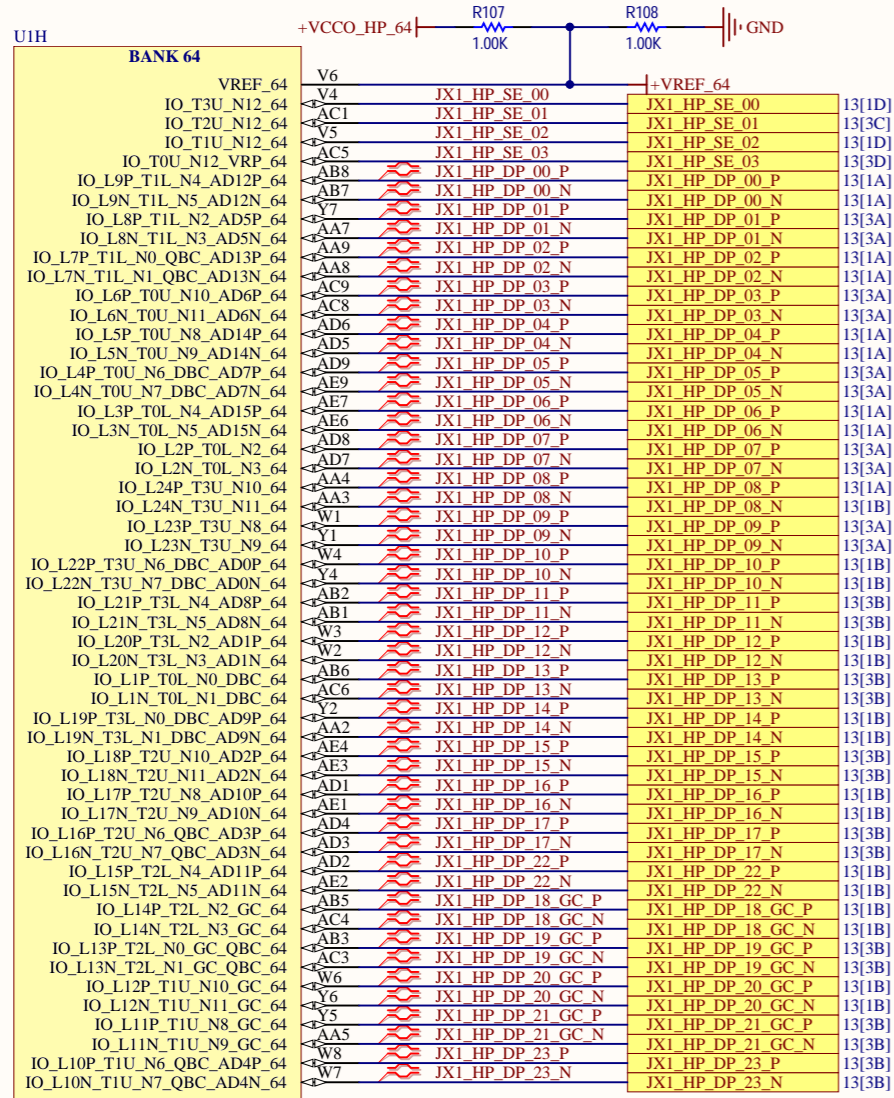
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Sheet Title:	07 - Bank 505.SchDoc	Size:	B	Sheet:	7	of 18	

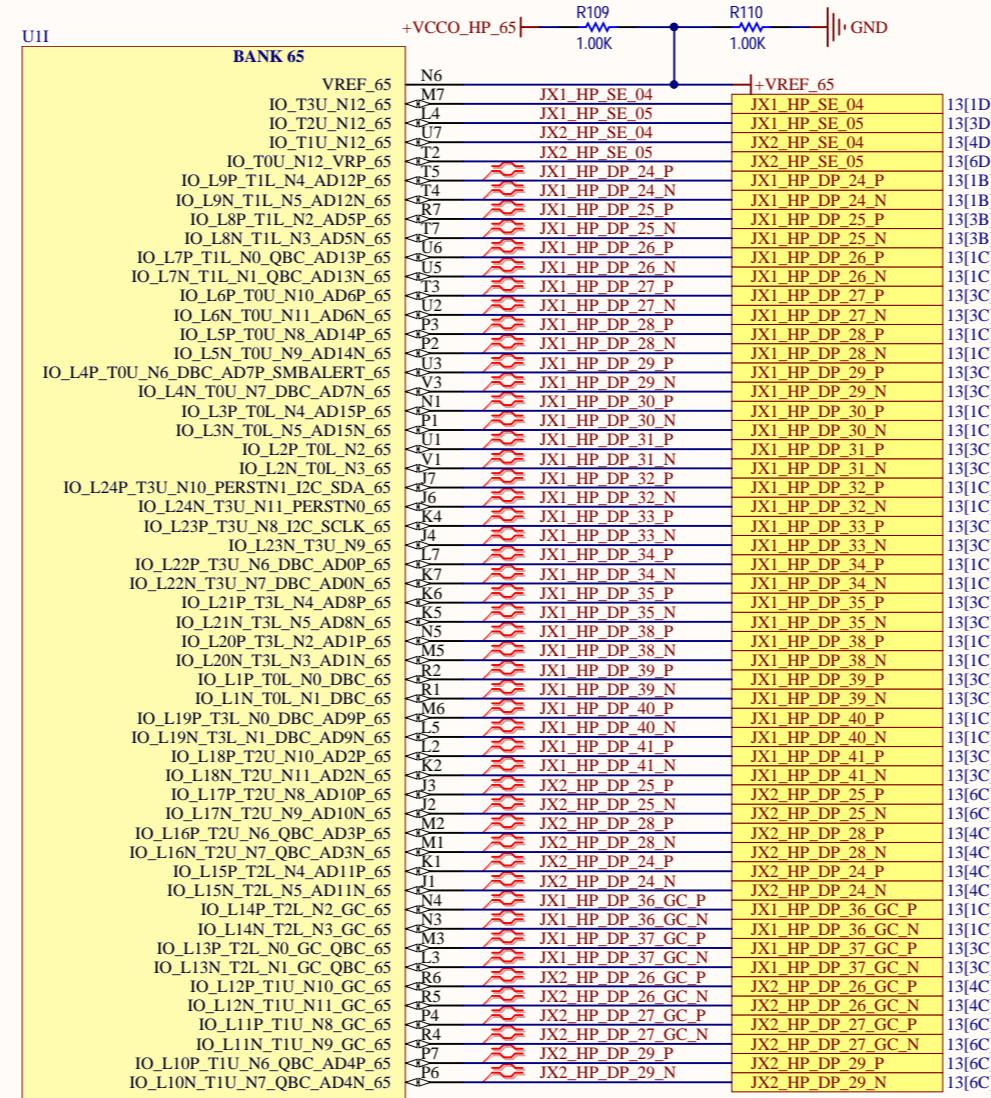


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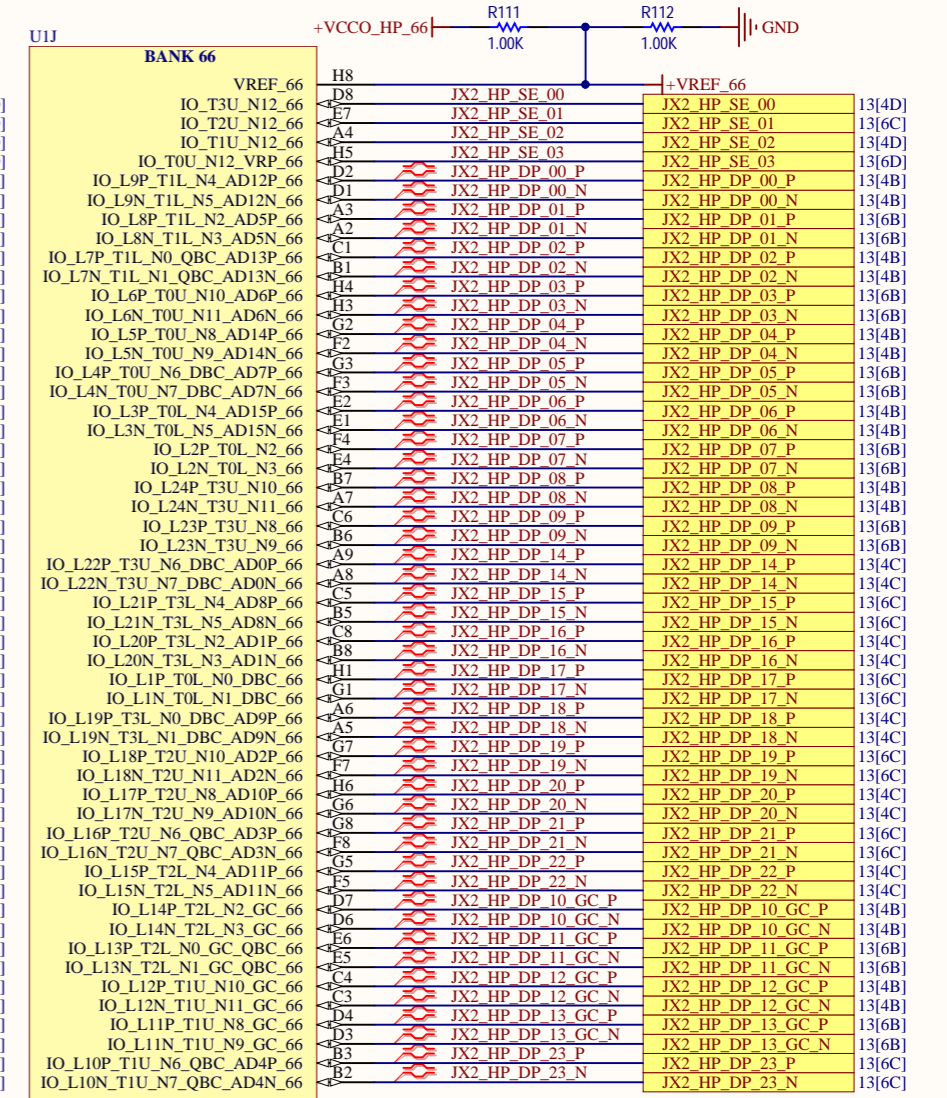
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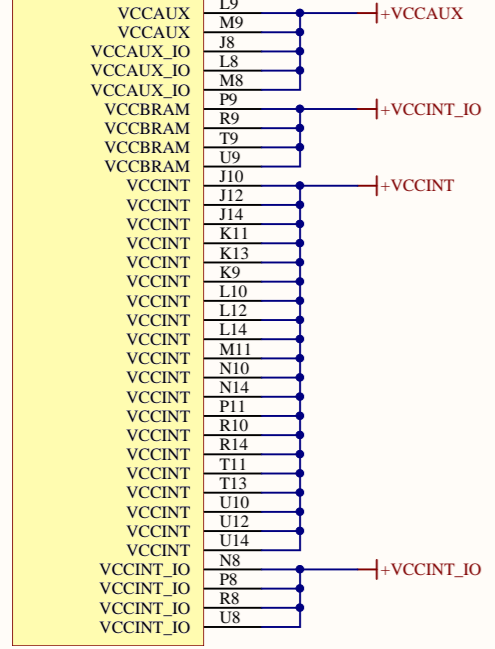


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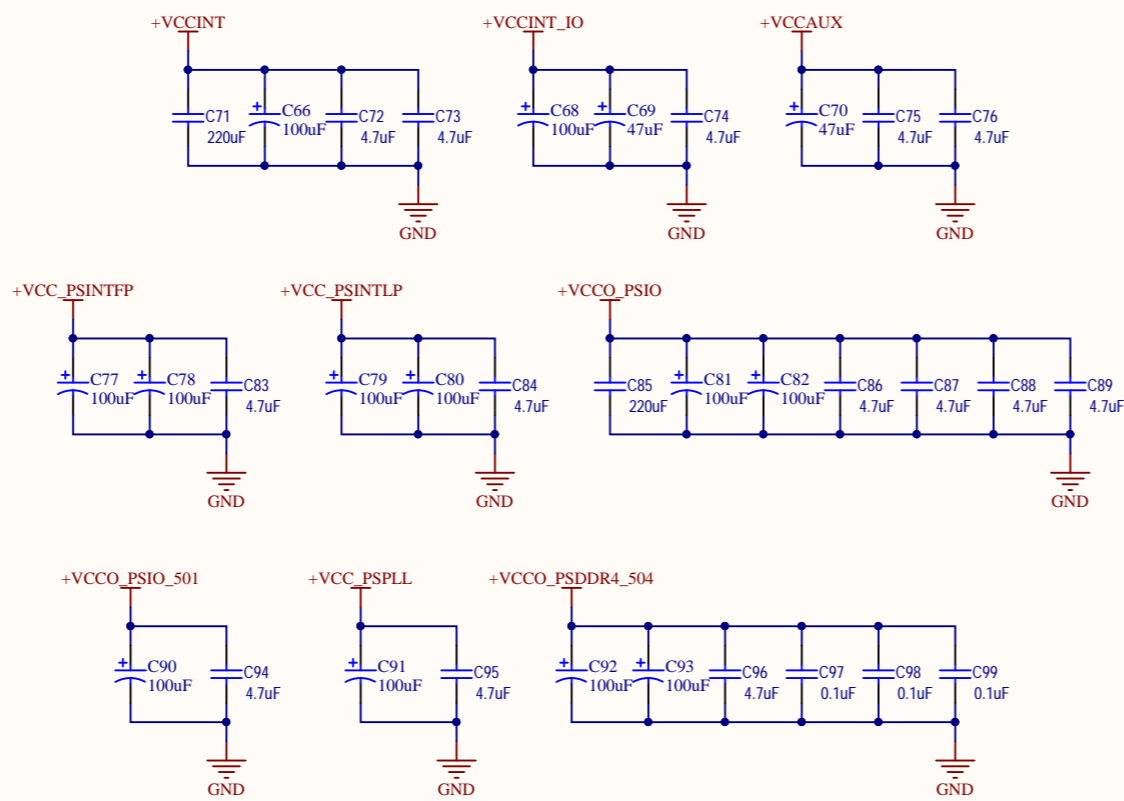


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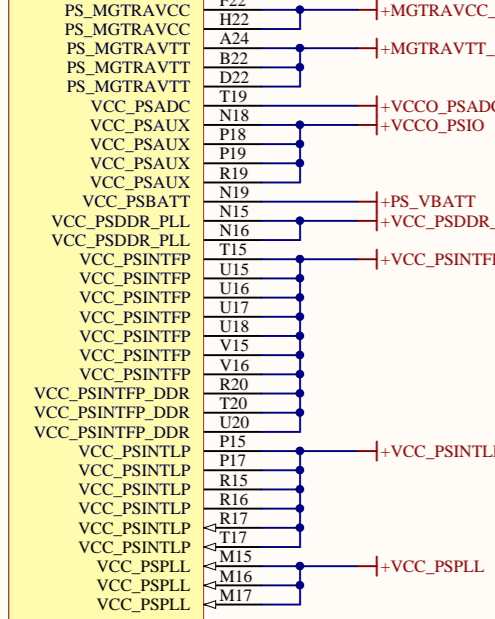
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PL CORE POWER**



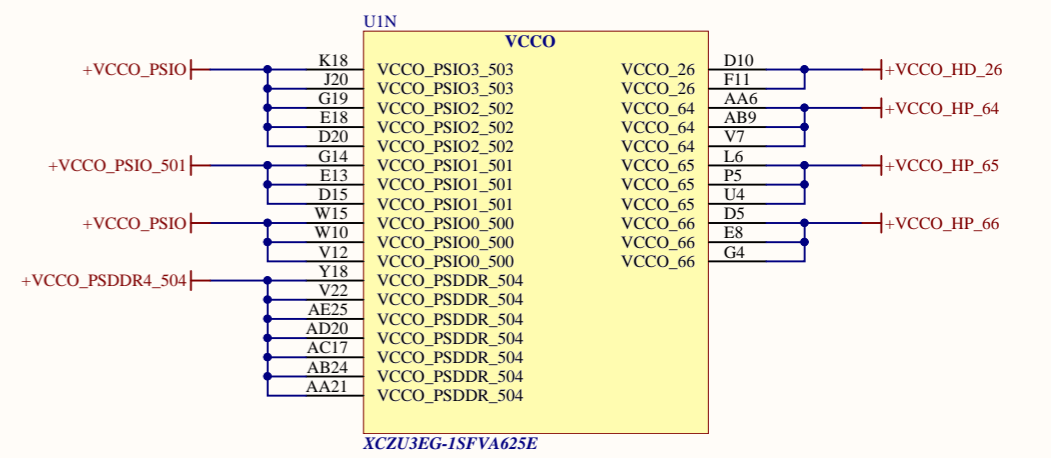
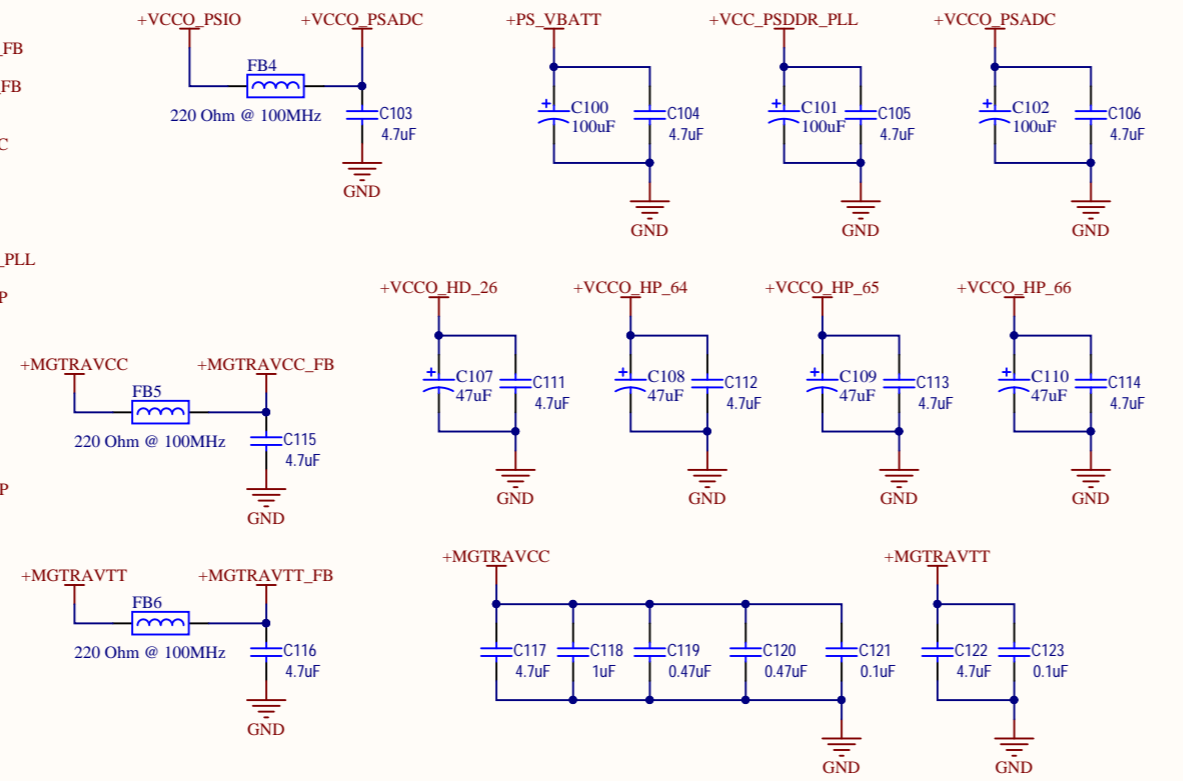
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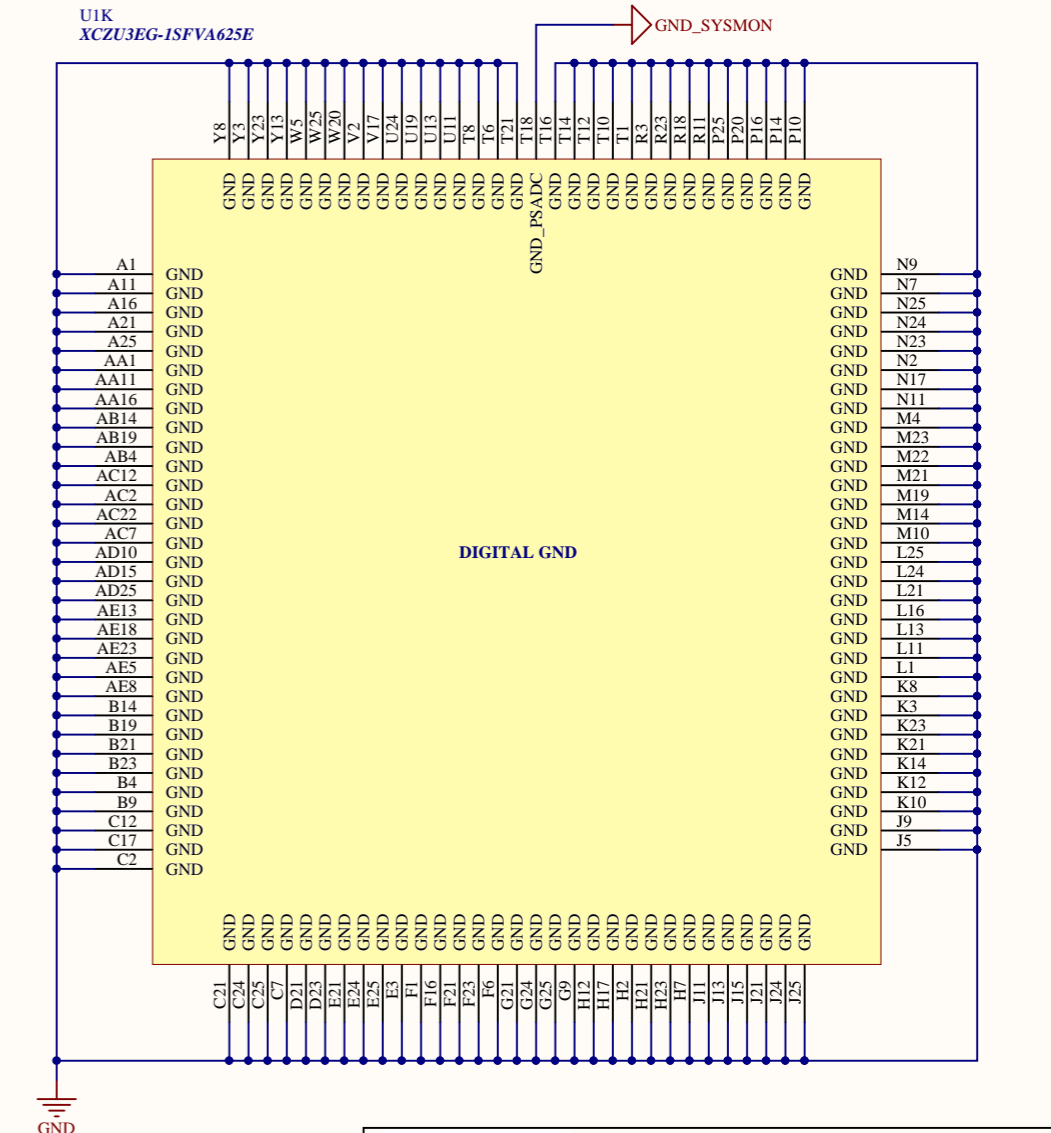
**U1M
PS CORE POWER**



XCZU3EG-1SFVA625E



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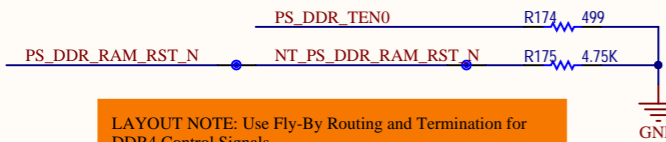
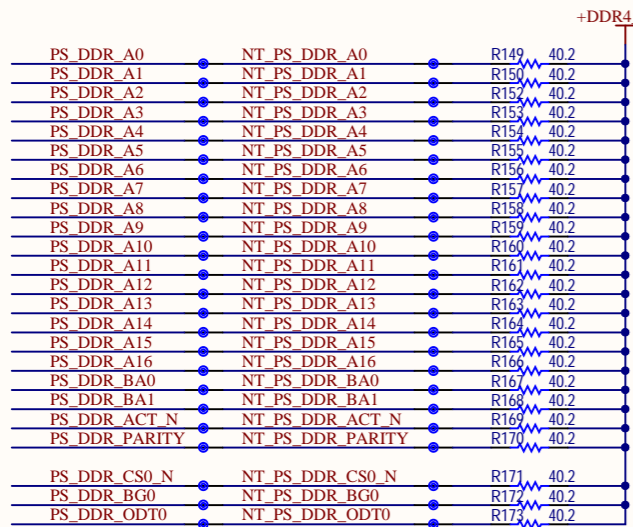
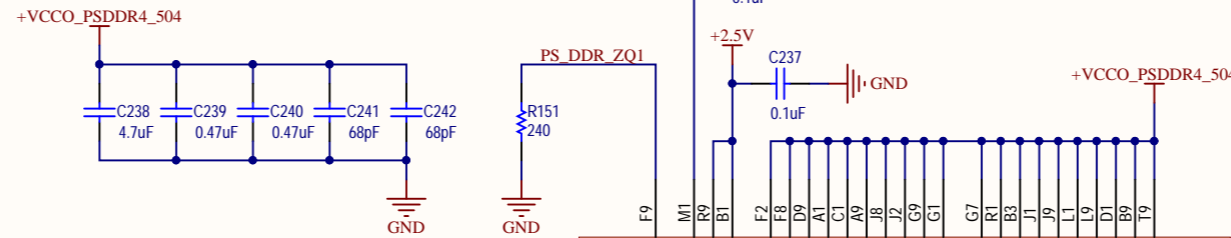


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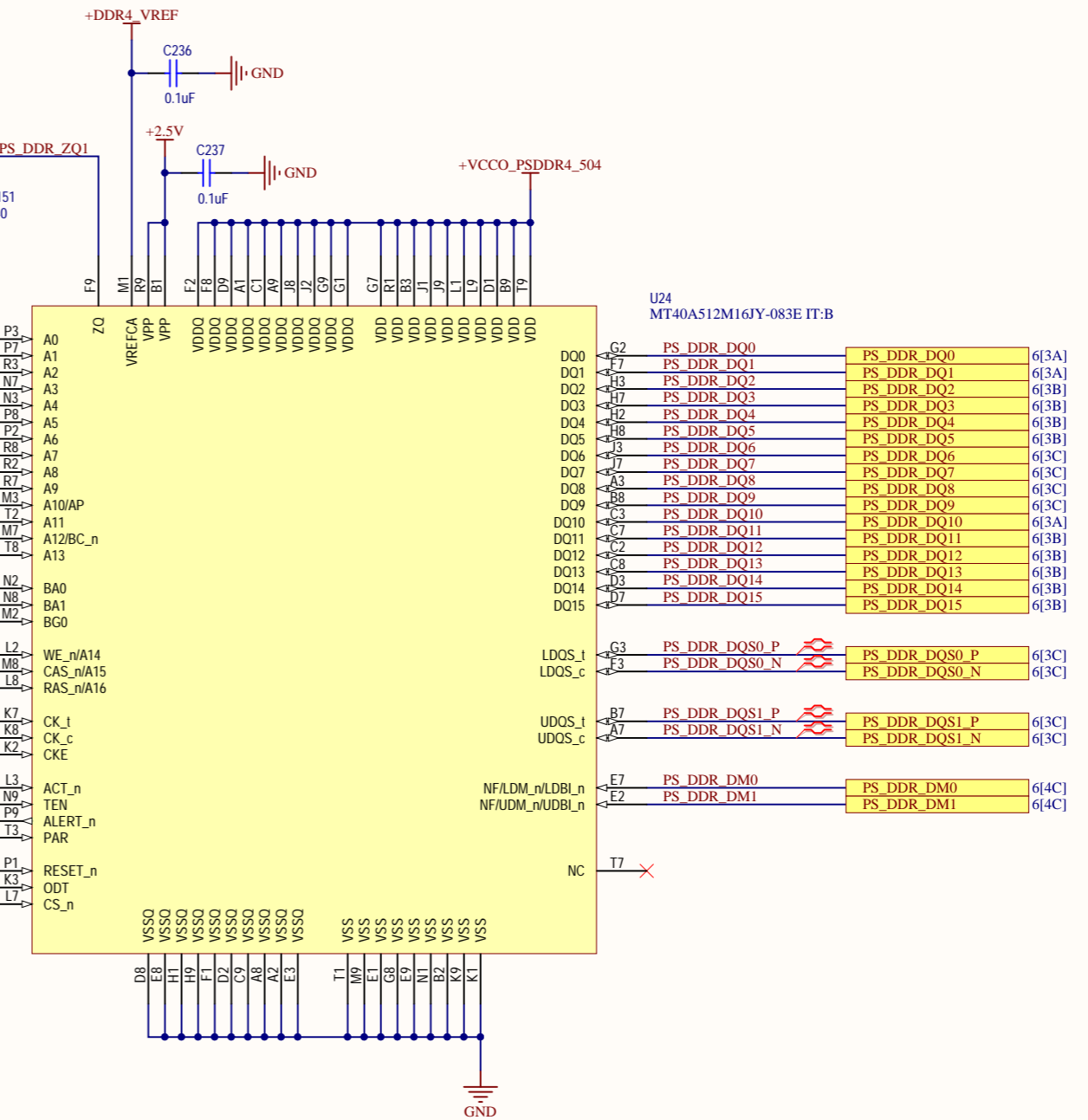
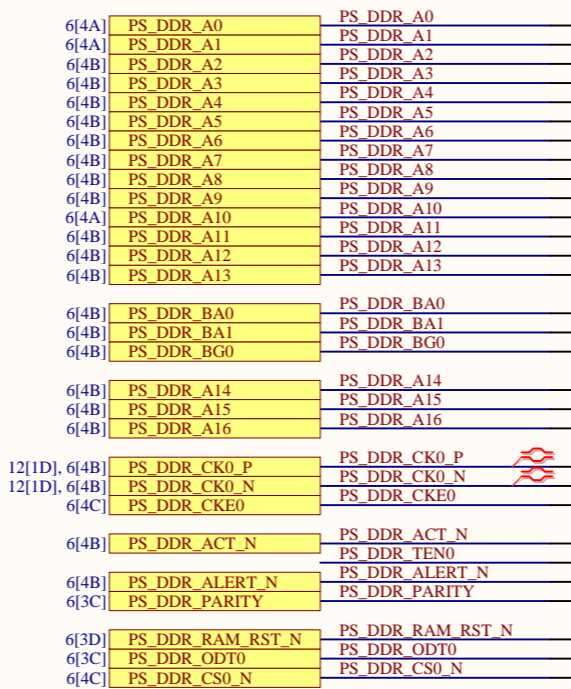
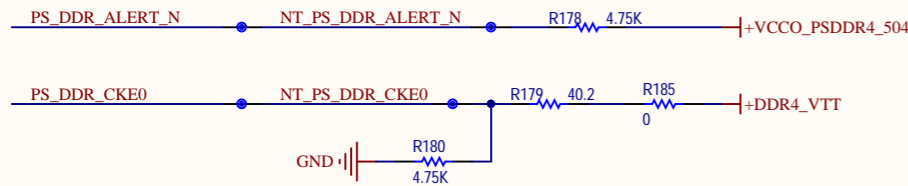
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Sheet:	B	Size:	10 of 18	

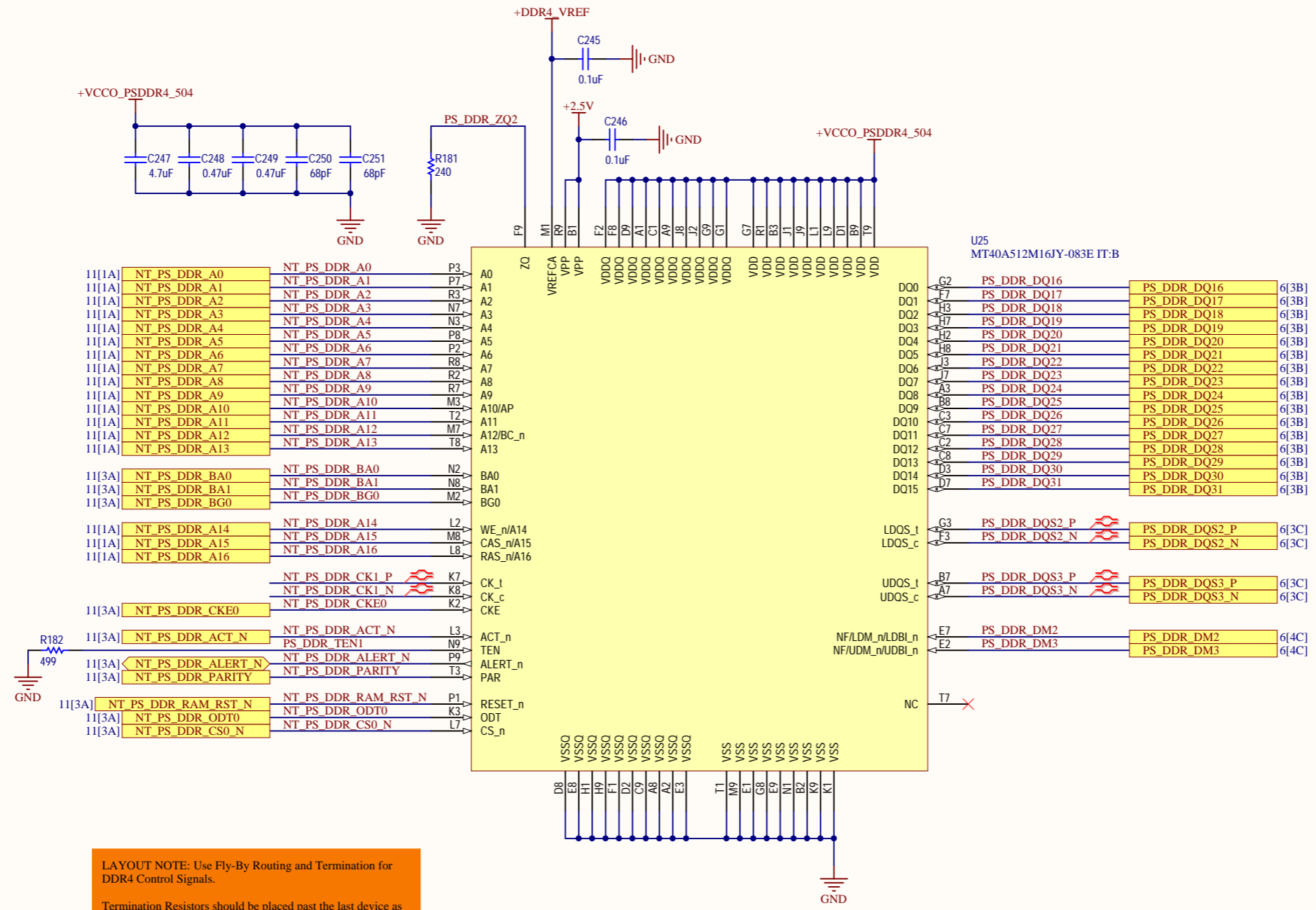
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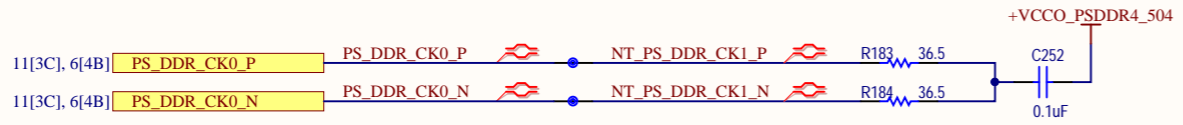


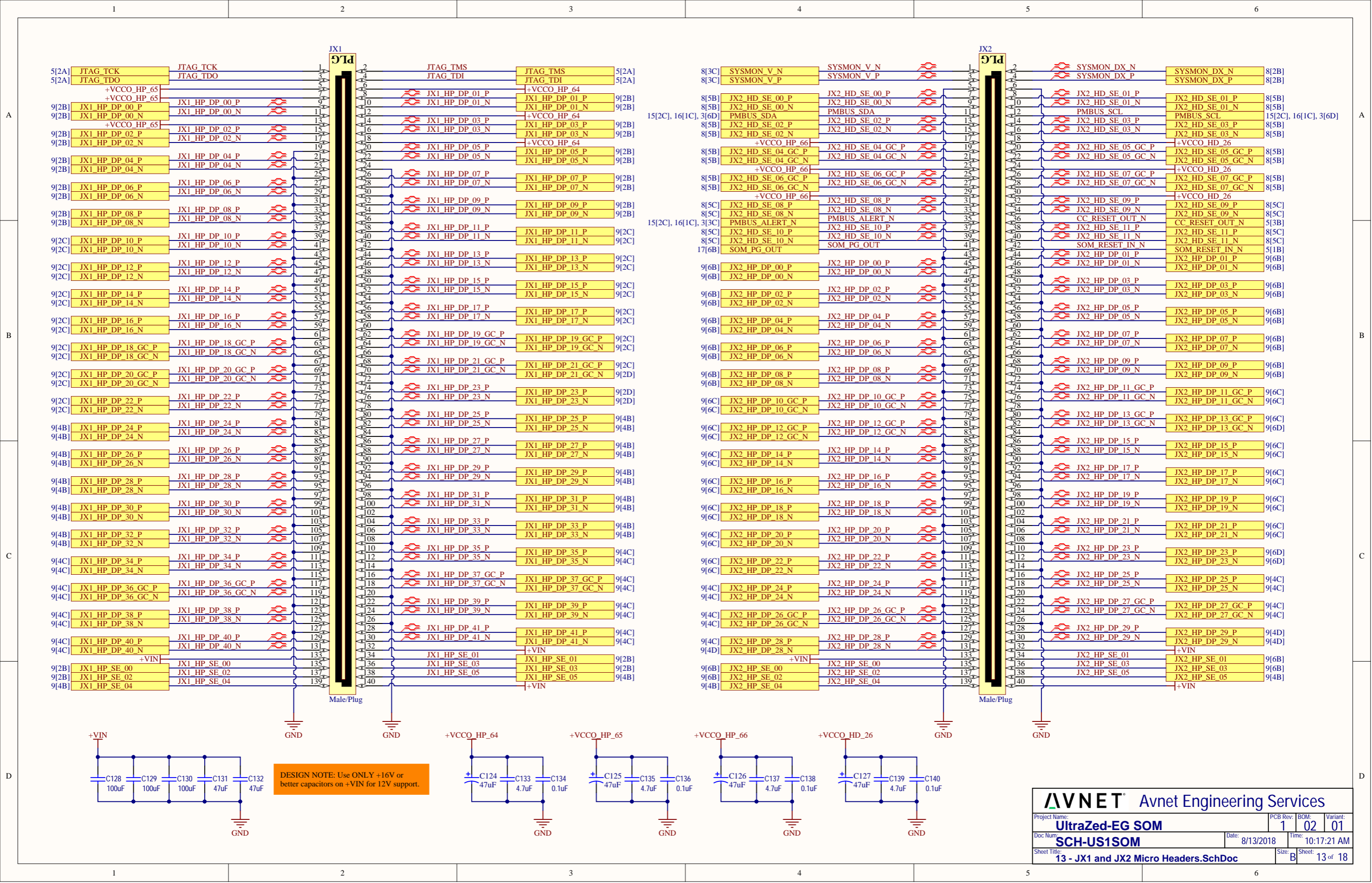
LAYOUT NOTE: Use Fly-By Routing and Termination for DDR4 Control Signals.
Termination Resistors should be placed past the last device as close to the device as possible.





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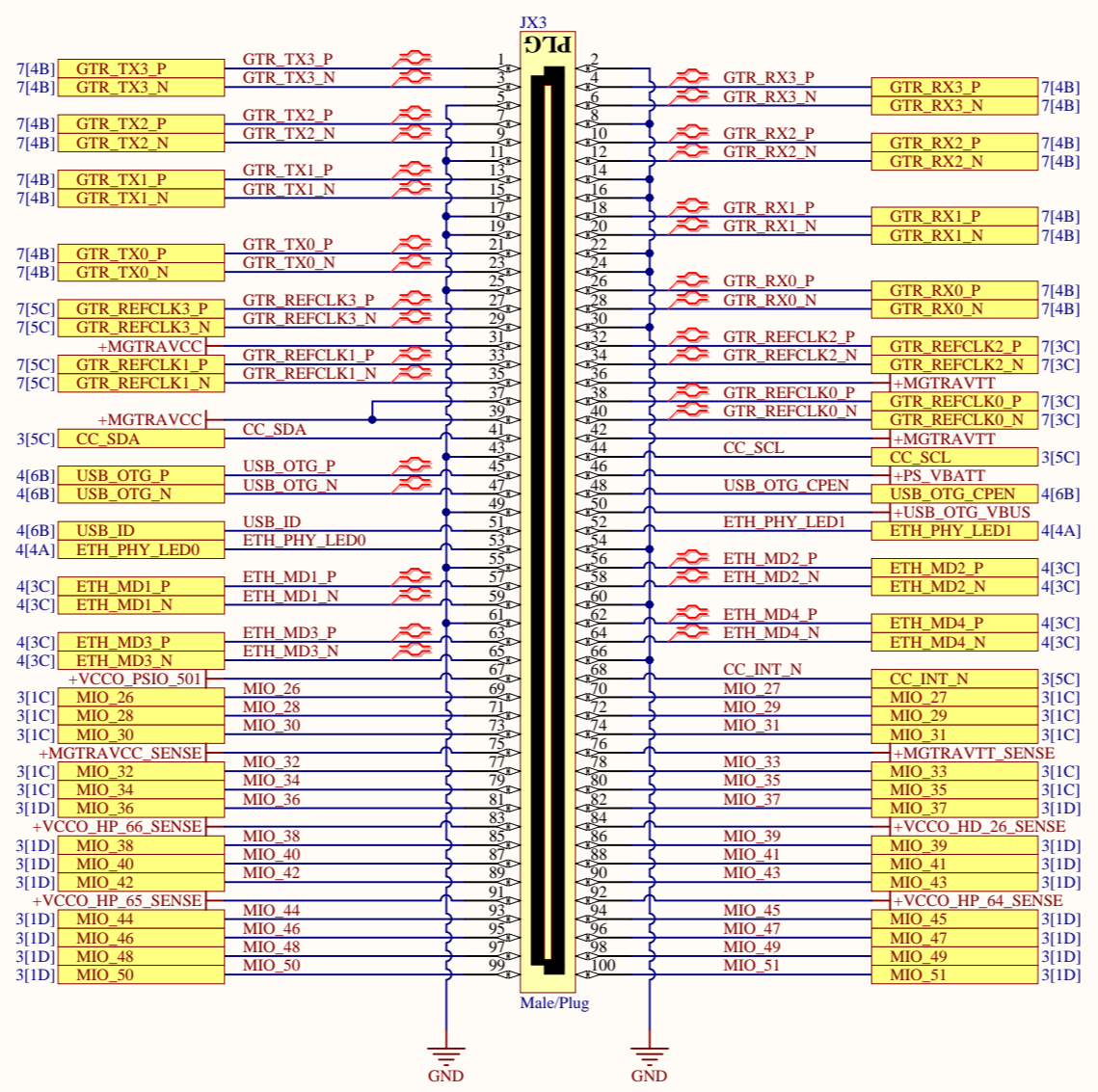
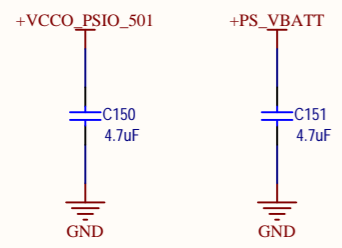
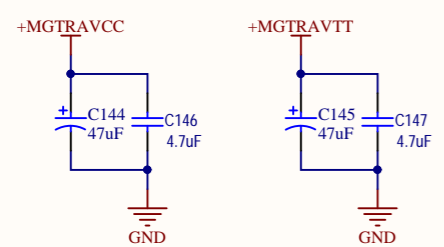
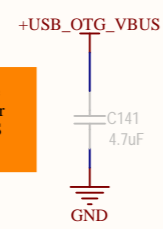




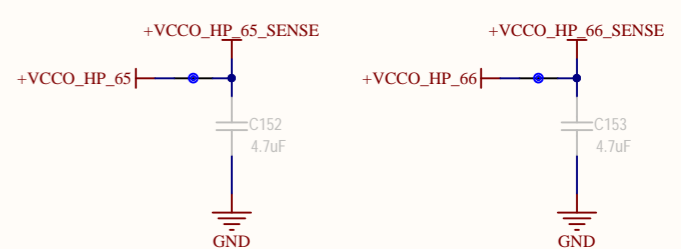
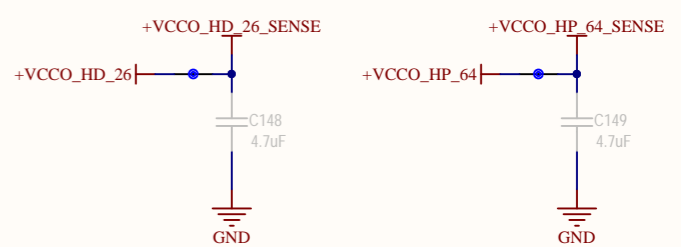
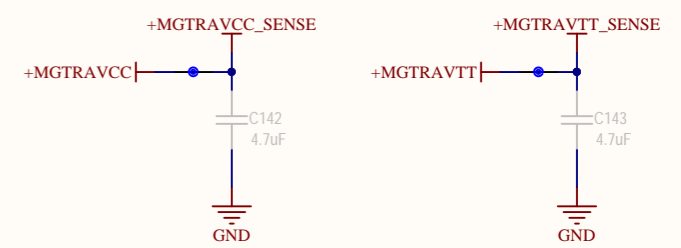
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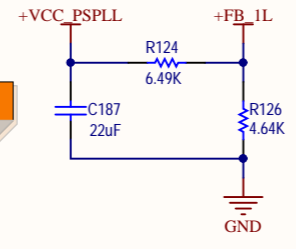
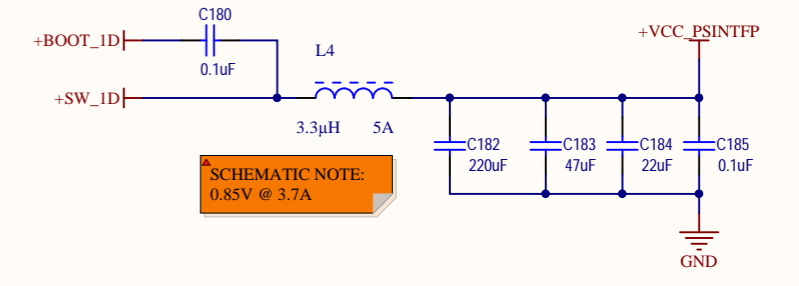
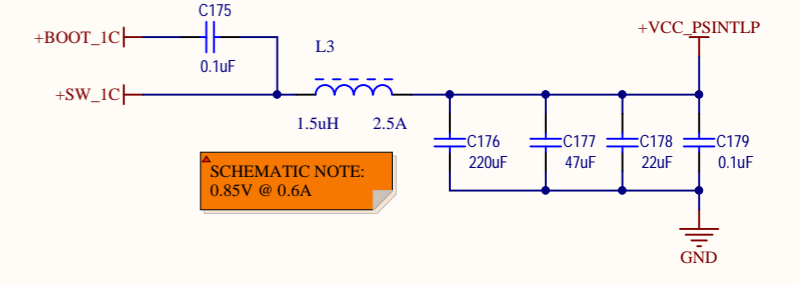
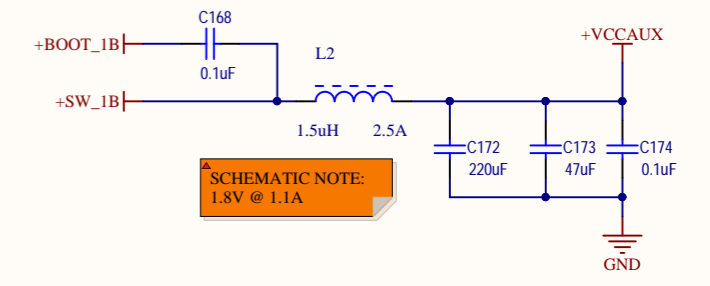
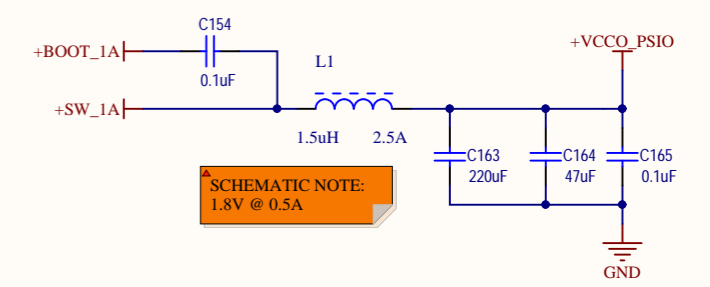
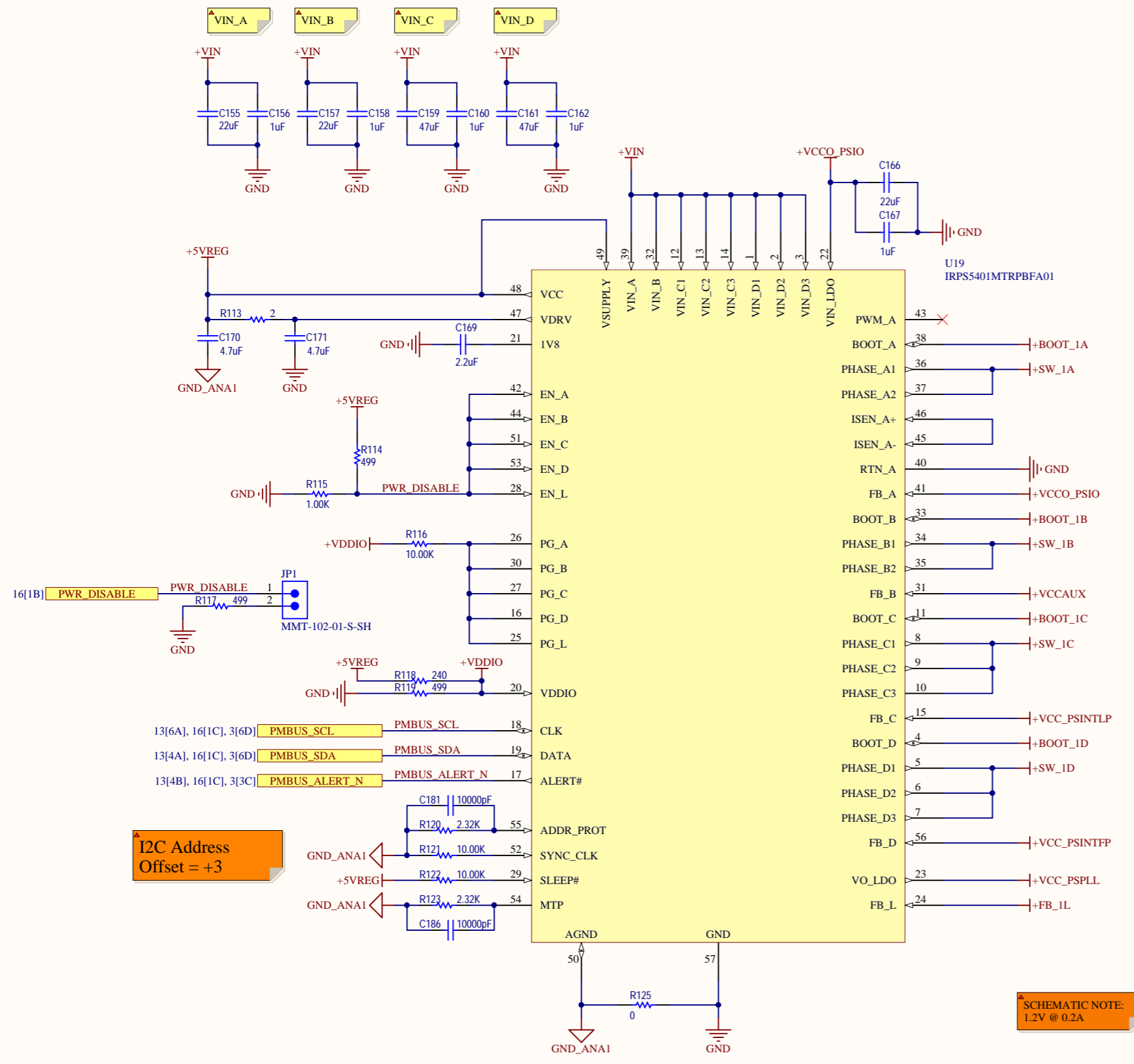
Project Name:	UltraZed-EG SOM	PCB Rev:	BOM: 1	Variant:	02	
Doc Num:	SCH-US1SOM	Date:	8/13/2018	Time:	10:17:21 AM	
Sheet Title:	13 - JX1 and JX2 Micro Headers.SchDoc		Size:	B	Sheet:	13 of 18

DESIGN NOTE: Use ONLY +10V or better capacitors on +VBUS for 5V support.



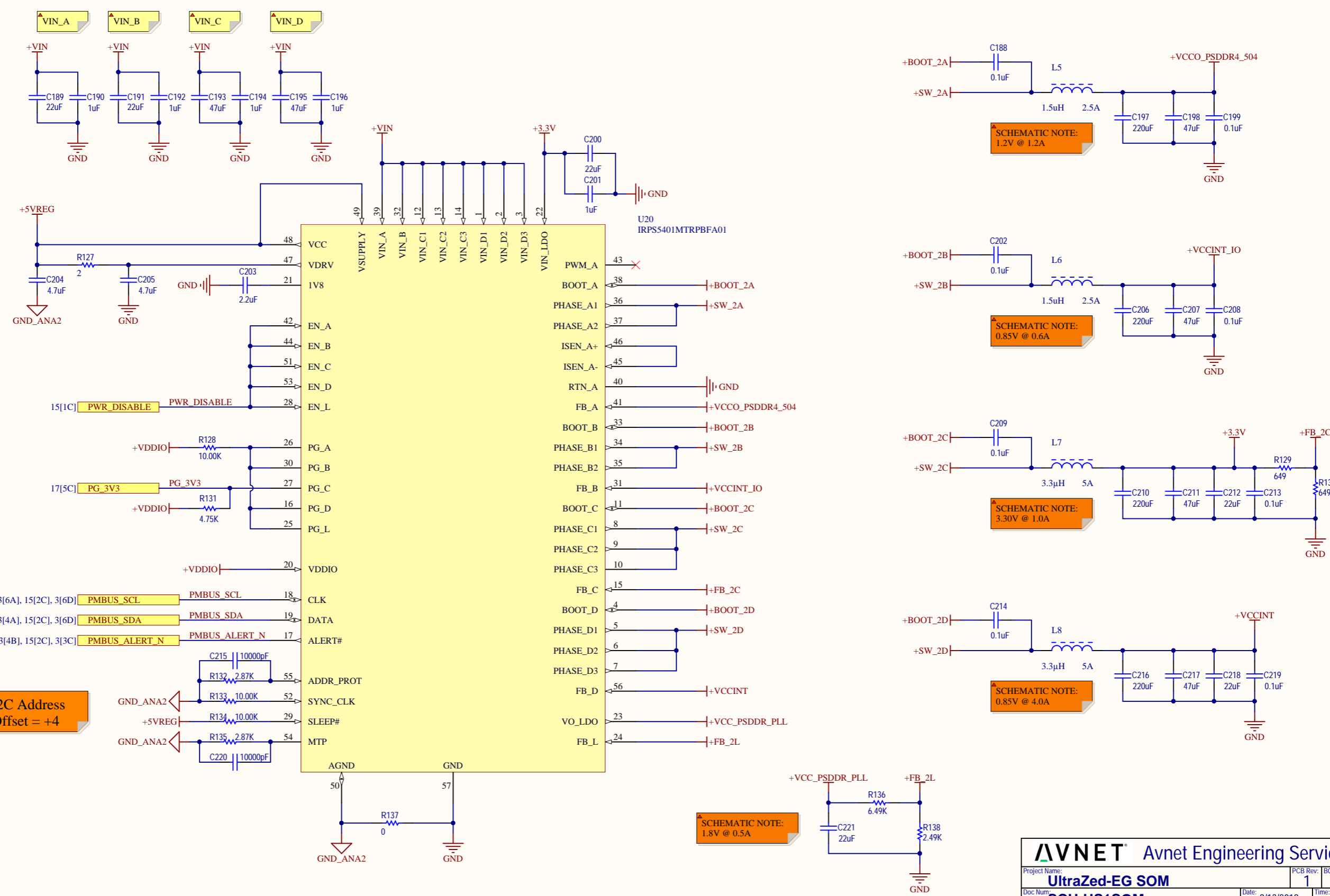
LAYOUT NOTE: ALL SENSE LINES MUST COME FROM NEAR DEVICE U1.





I2C Address Offset = +3

AVNET Avnet Engineering Services			
Project Name:	UltraZed-EG SOM	PCB Rev:	BOM: 1 02 01
Doc Num:	SCH-US1SOM	Date:	8/13/2018
Sheet Title:	15 - Rocky PMIC #1.SchDoc	Time:	10:17:22 AM
Size:	B	Sheet:	15 of 18



I2C Address Offset = +4

SCHEMATIC NOTE:
1.2V @ 1.2A

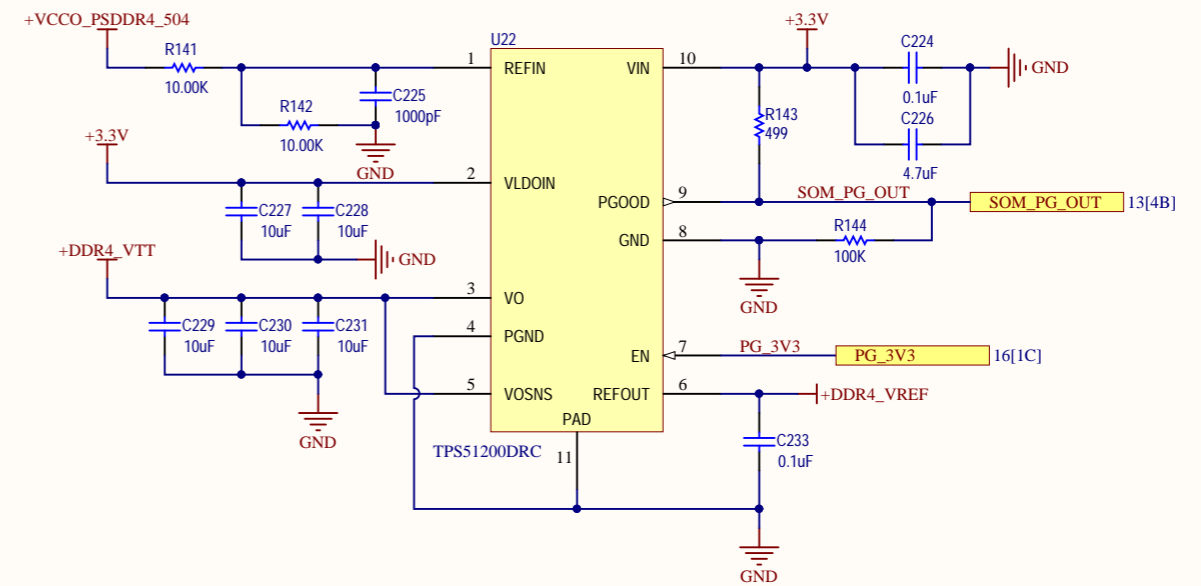
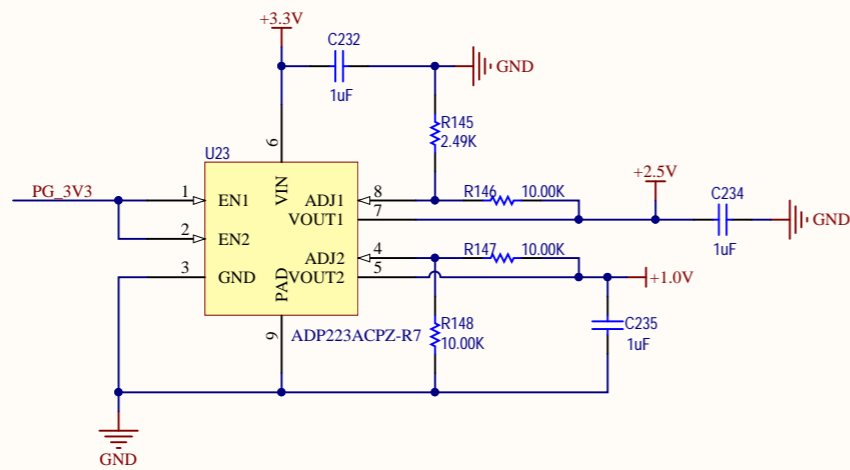
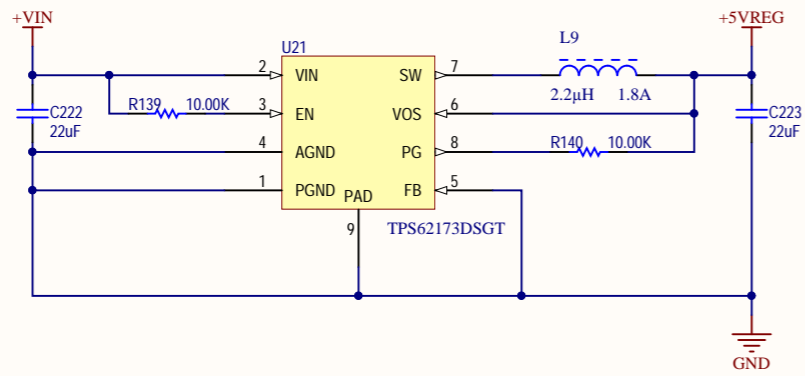
SCHEMATIC NOTE:
0.85V @ 0.6A

SCHEMATIC NOTE:
3.30V @ 1.0A

SCHEMATIC NOTE:
0.85V @ 4.0A

SCHEMATIC NOTE:
1.8V @ 0.5A

AVNET Avnet Engineering Services			
Project Name:	UltraZed-EG SOM	PCB Rev:	BOM:
Doc Num:	SCH-US1SOM	1	02
Date:	8/13/2018	Time:	10:17:23 AM
Sheet Title:	16 - Rocky PMIC #2.SchDoc	Size:	B
		Sheet:	16 of 18



Assembly:

Label1
BD-XXXX-XXXX-G
Label, Product

Label2
XXXXXXXX
Label, Serial Number



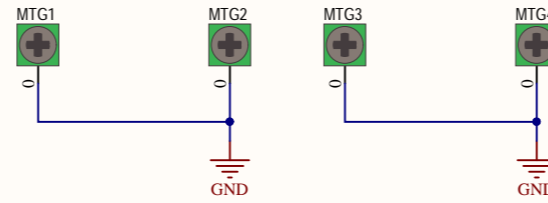
Label_ESD1
Label, ESD

Mechanicals:

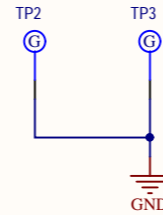


XXX-XXX-PCB-X
PCB PN (In Copper)

Mounting Holes:



GND Test Points:



Jumper Shunts:



AVNET Avnet Engineering Services			
Project Name:	UltraZed-EG SOM	PCB Rev:	1
		BOM:	02
		Variant:	01
Doc Num:	SCH-US1SOM	Date:	8/13/2018
		Time:	10:17:23 AM
Sheet Title:	18 - Back Page.SchDoc	Size:	B
		Sheet:	18 of 18