Ultra96 SBC V2
Avnet Engineering Services
www.avnet.me/ultra96-v2
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01 - Avnet Lead Sheet
02 - Block Diagram
03 - Bank 500, Bank 501, Bank 502, Bank 503
04 - Bank 504, Bank 505
05 - SD Card, RADIO
06 - USB 3.0 MicroAB
07 - USB2.0 Downstream Device & Clock Gen
08 - Bank 0, Bank 26, Bank 65, Bank 66
09 - Switches, LEDs, JTAG
10 - Bank Power and Decoupling
11 - LPDDR4 Device
12 - USB 3.0 Dual Port Hub
13 - Jx_Jy Expansion Headers, Power On
14 - Display Port
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AVNET® Reach Further™

Ultra96 SBC V2

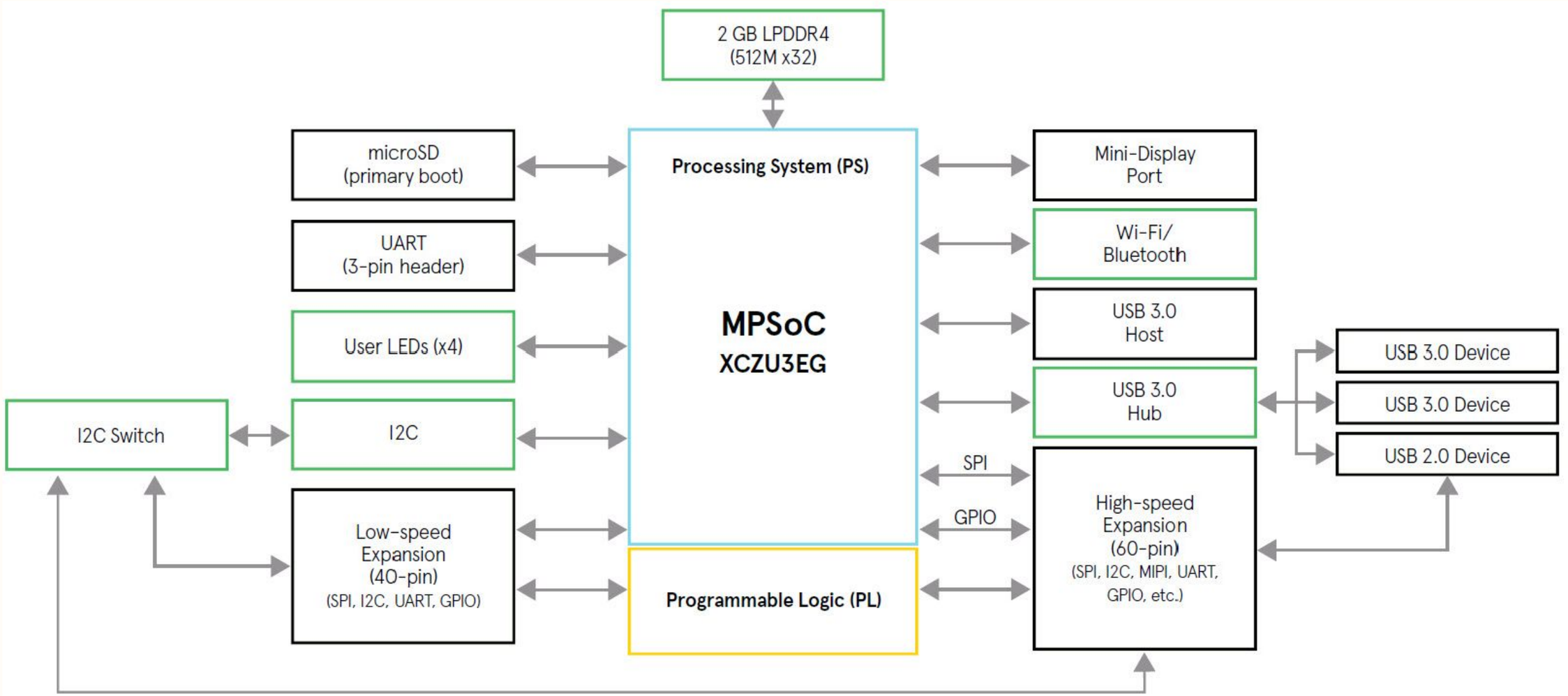
(AES-ULTRA96-V2-G)

Revision

96Boards

https://www.96boards.org/products/ce/

AVNET® Avnet Engineering Services			
Project Name: Ultra96 SBC V2	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1SBC	Date: 3/1/2019	Time: 7:57:25 AM	
Sheet Title: 01 - Avnet Lead Sheet.SchDoc	Size: B	Sheet: 1 of 18	



AVNET	Avnet Engineering Services
Project Name: Ultra96 SBC V2	PCB Rev: 1 / BOM: 01 / Variant: 00
Doc Num: SCH-US1SBC	Date: 3/1/2019 / Time: 7:57:25 AM
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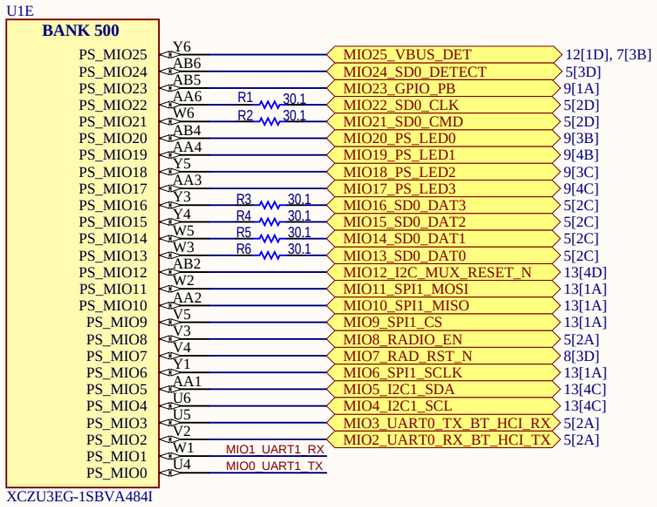
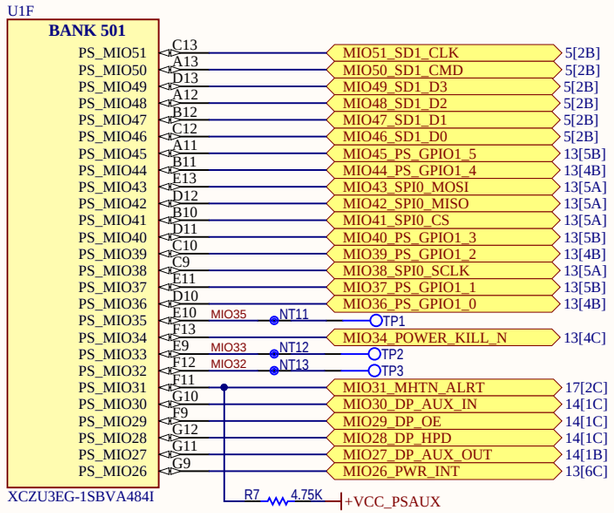
BANK 500, BANK 501, BANK 502, BANK 503

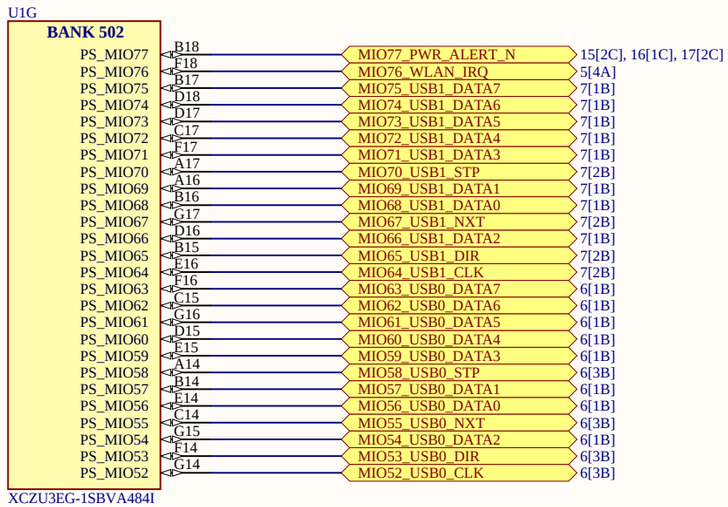
BANK 500



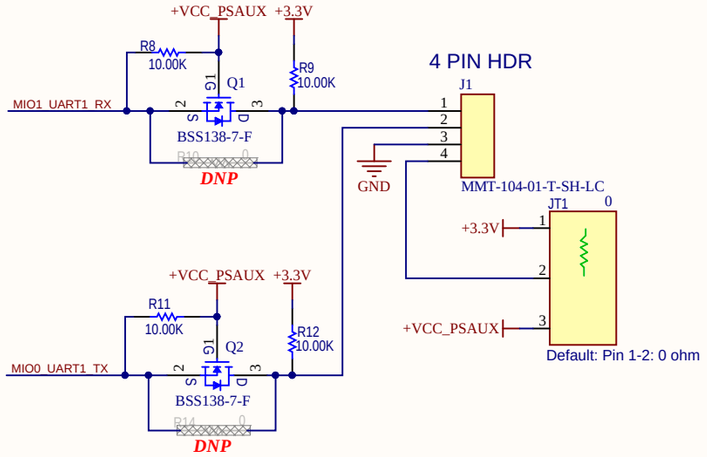
BANK 501



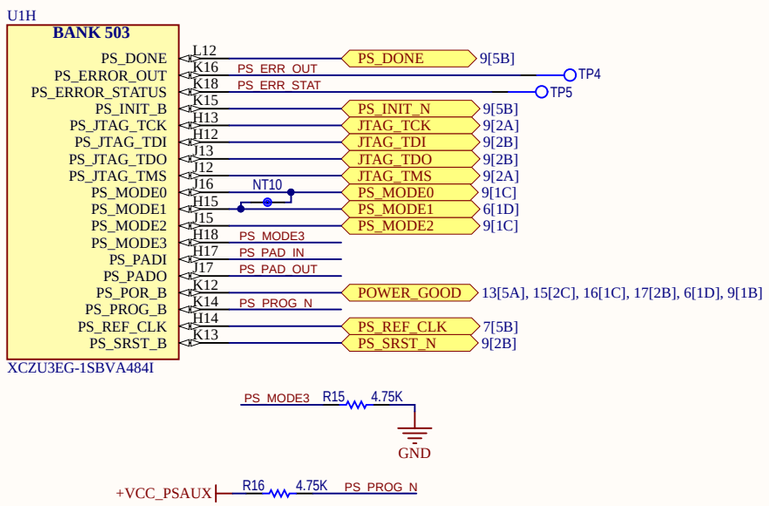
BANK 502



OFF BOARD UART & XNSLTR

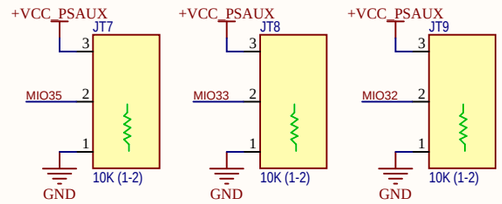


BANK 503

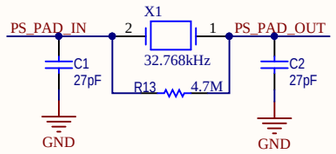


BOARD ID STRAPPING OPTIONS

(Refer to User's Guide for information)



32KHz RTC XTAL



Avnet Engineering Services	
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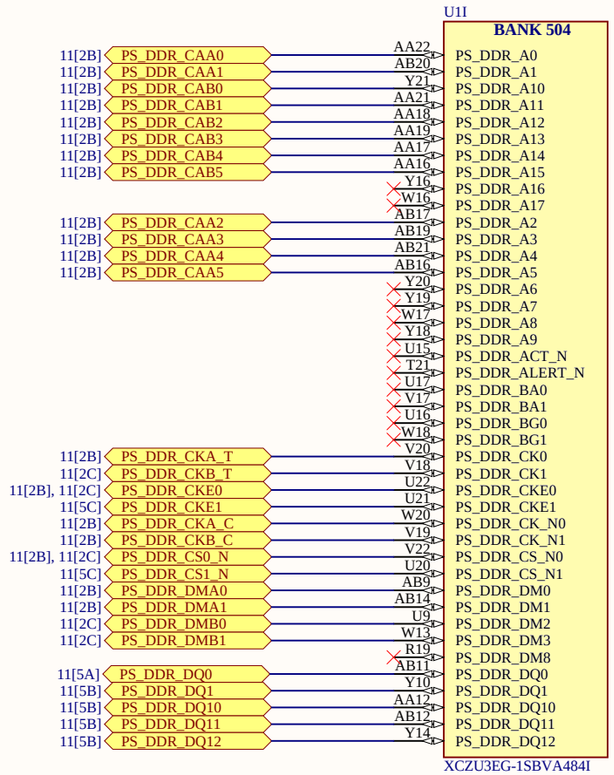
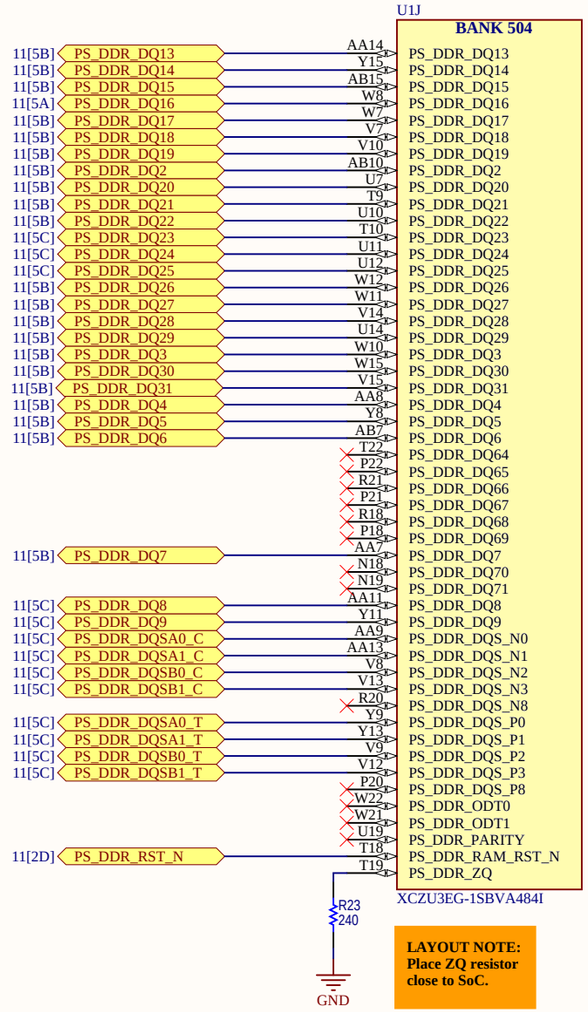
BANK 504, BANK 505

BANK 504 - DDR

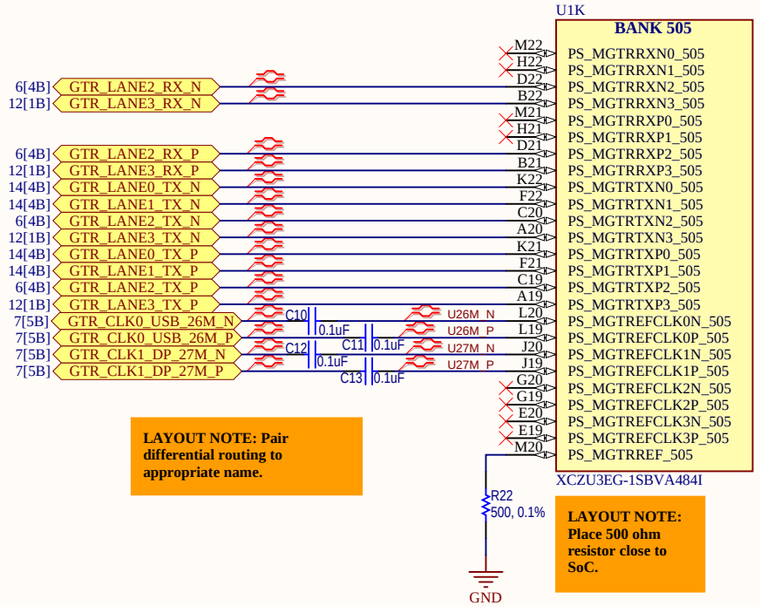


BANK 504 - DDR



LAYOUT NOTE: Place ZQ resistor close to SoC.

BANK 505 - GTR



LAYOUT NOTE: Pair differential routing to appropriate name.

LAYOUT NOTE: Place 500 ohm resistor close to SoC.

AVNET Avnet Engineering Services

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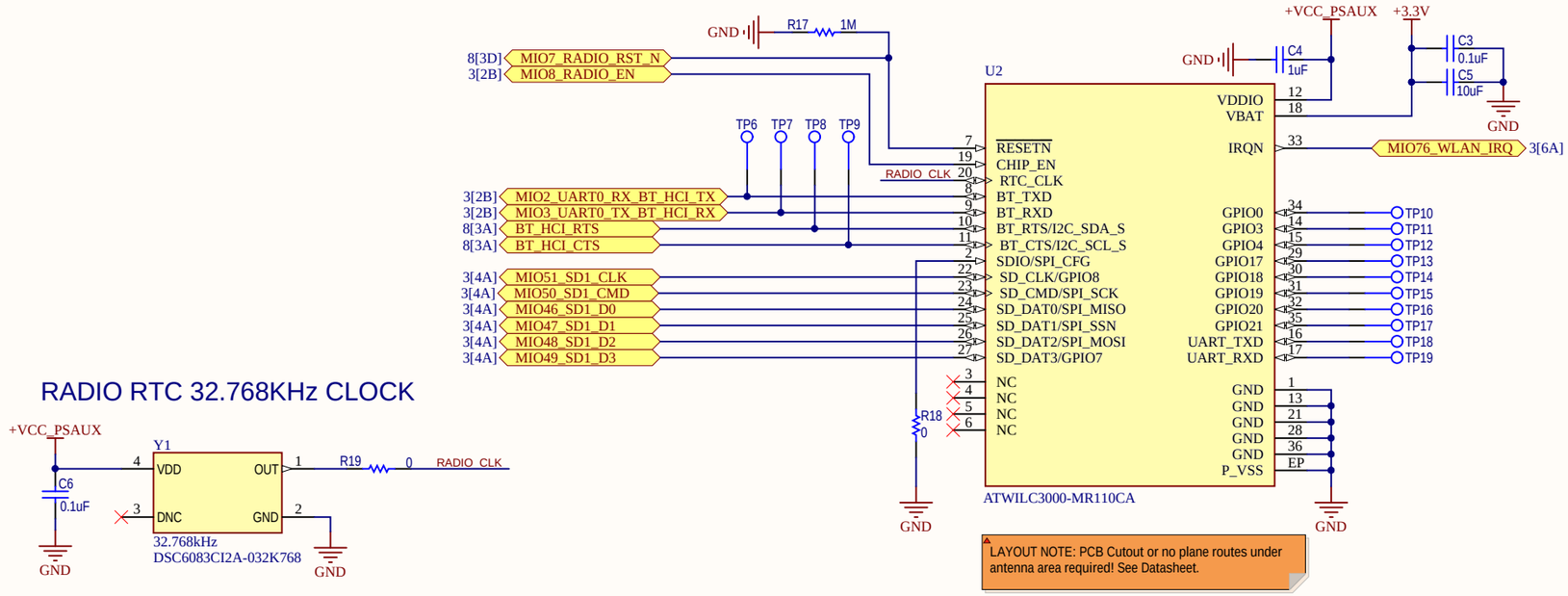
Sheet Title: 04 - Bank 504, BANK 505.SchDoc	Size: B	Sheet: 4 of 18	

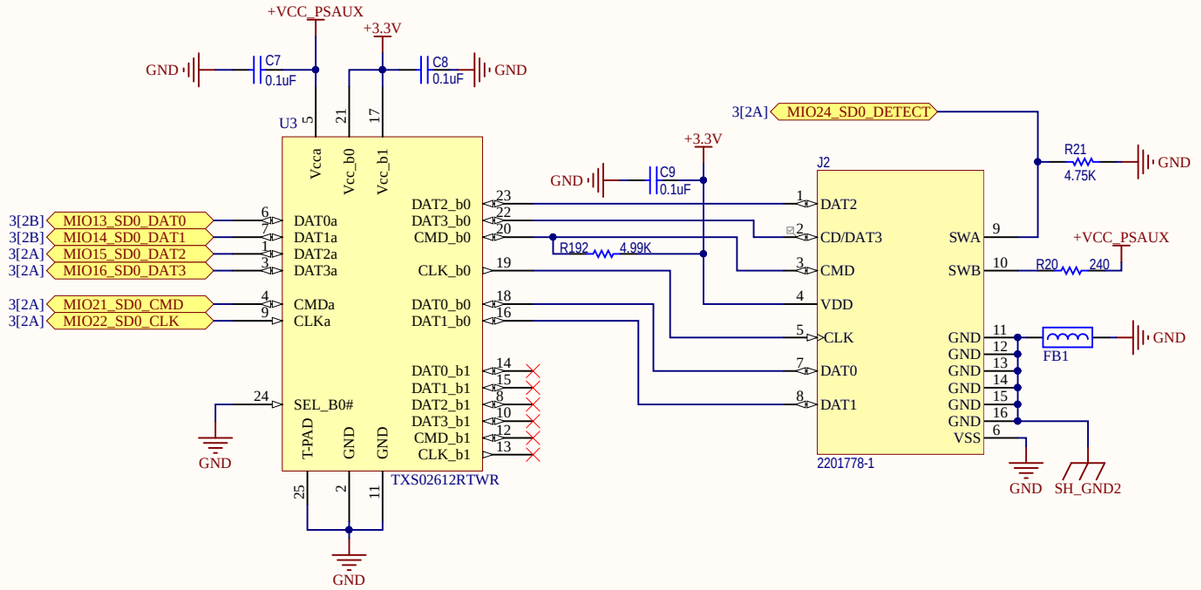
SD CARD, ATWILC3000 WiFi & BT RADIO

RADIO: BLUETOOTH, WiFi (SDIO Mode)



RADIO RTC 32.768KHz CLOCK

uSD CARD INTERFACE



AVNET Avnet Engineering Services			
Project Name: Ultra96 SBC V2	PCB Rev: 1	BOM: 01	Variant: 00
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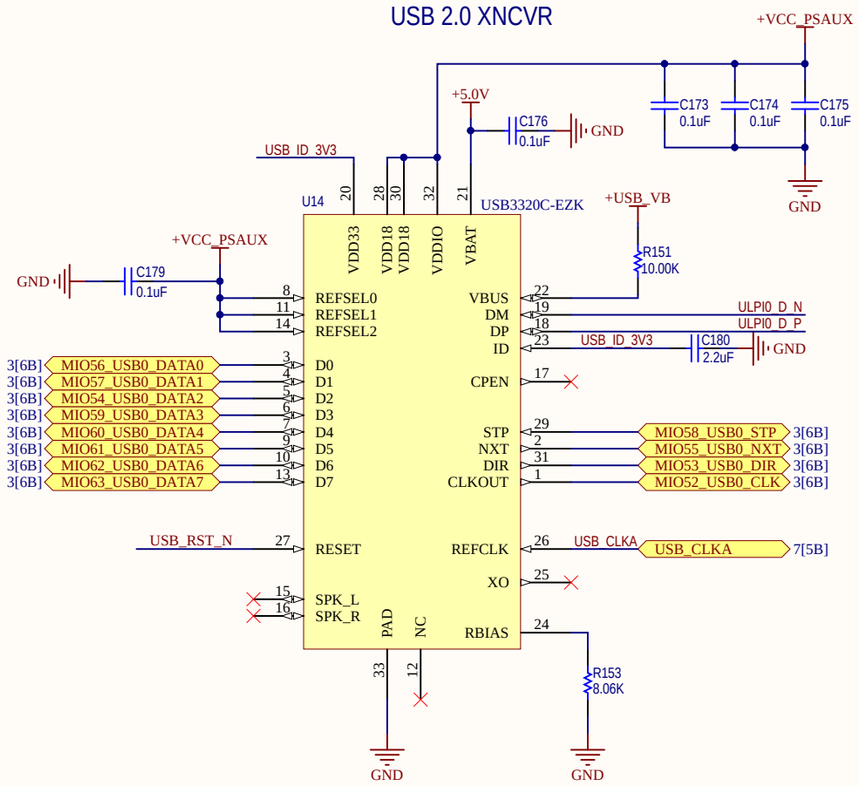
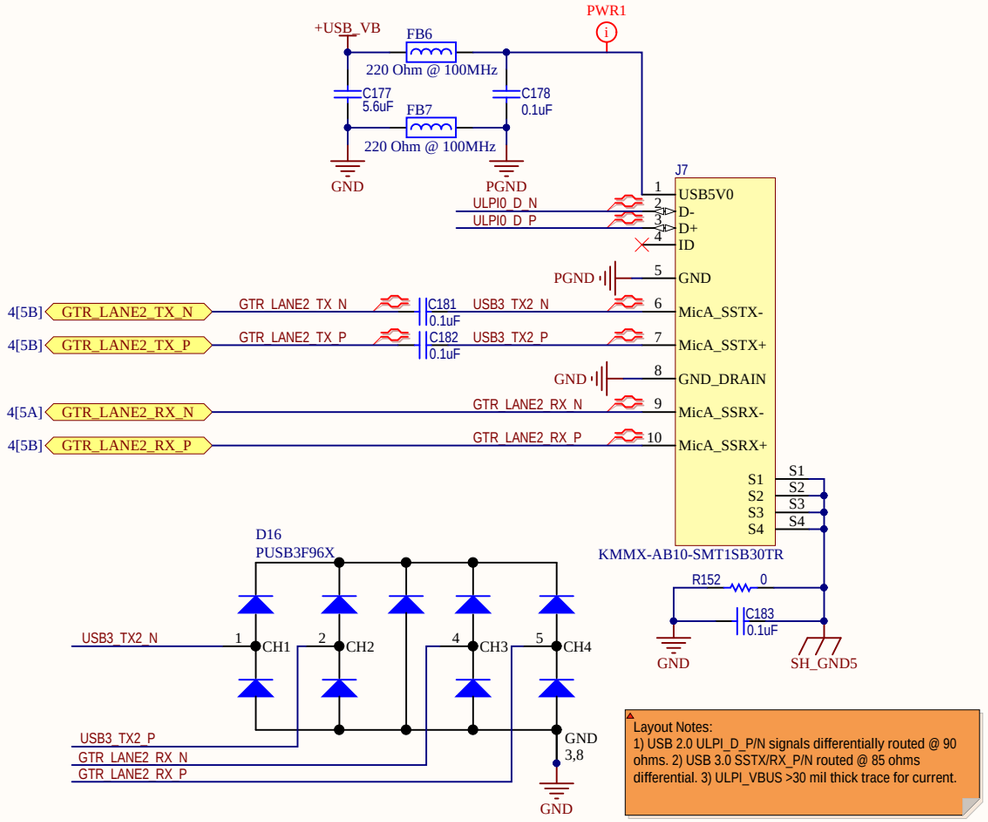
Sheet Title: 05 - SD Card, RADIO.SchDoc	Size: B	Sheet: 5 of 18	

USB 3.0 MicroAB UPSTREAM INTERFACE

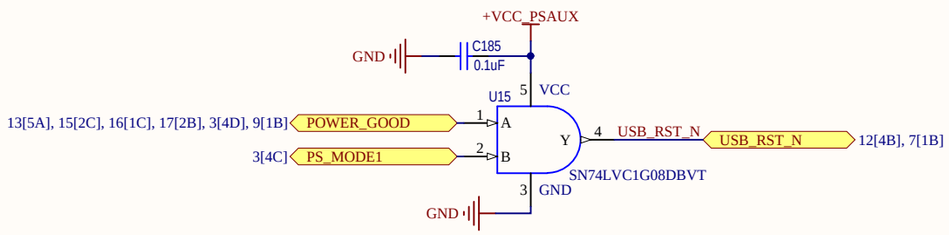
USB 2.0 XNCVR

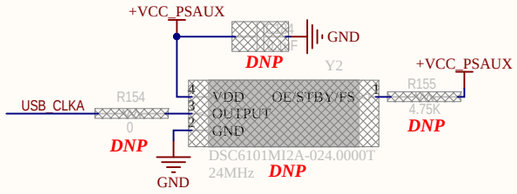


USB 3.0 Micro A/B



Layout Notes:
1) USB 2.0 ULPI_D_P/N signals differentially routed @ 90 ohms. 2) USB 3.0 SSTX/RX_P/N routed @ 85 ohms differential. 3) ULPI_VBUS >30 mil thick trace for current.





Layout Note: Place R154 pin 2 pad directly on clock trace to U14.

Avnet Engineering Services	
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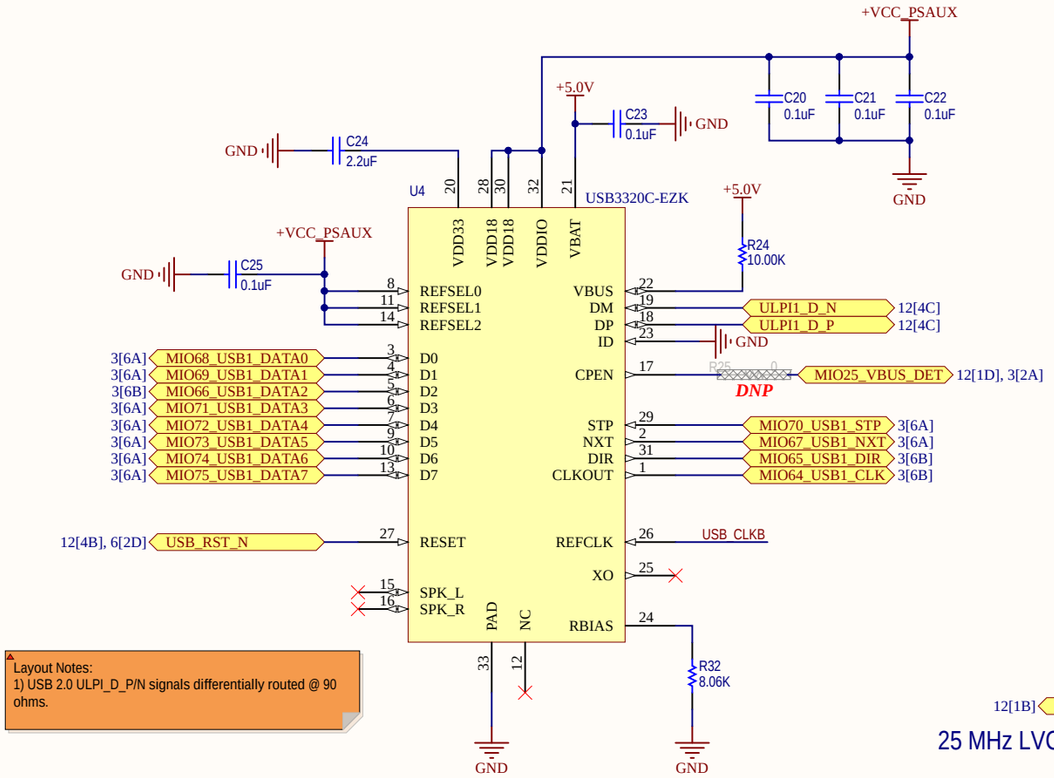
Sheet Title: 06 - USB 3.0 MicroAB.SchDoc	Size: B / Sheet: 6 of 18

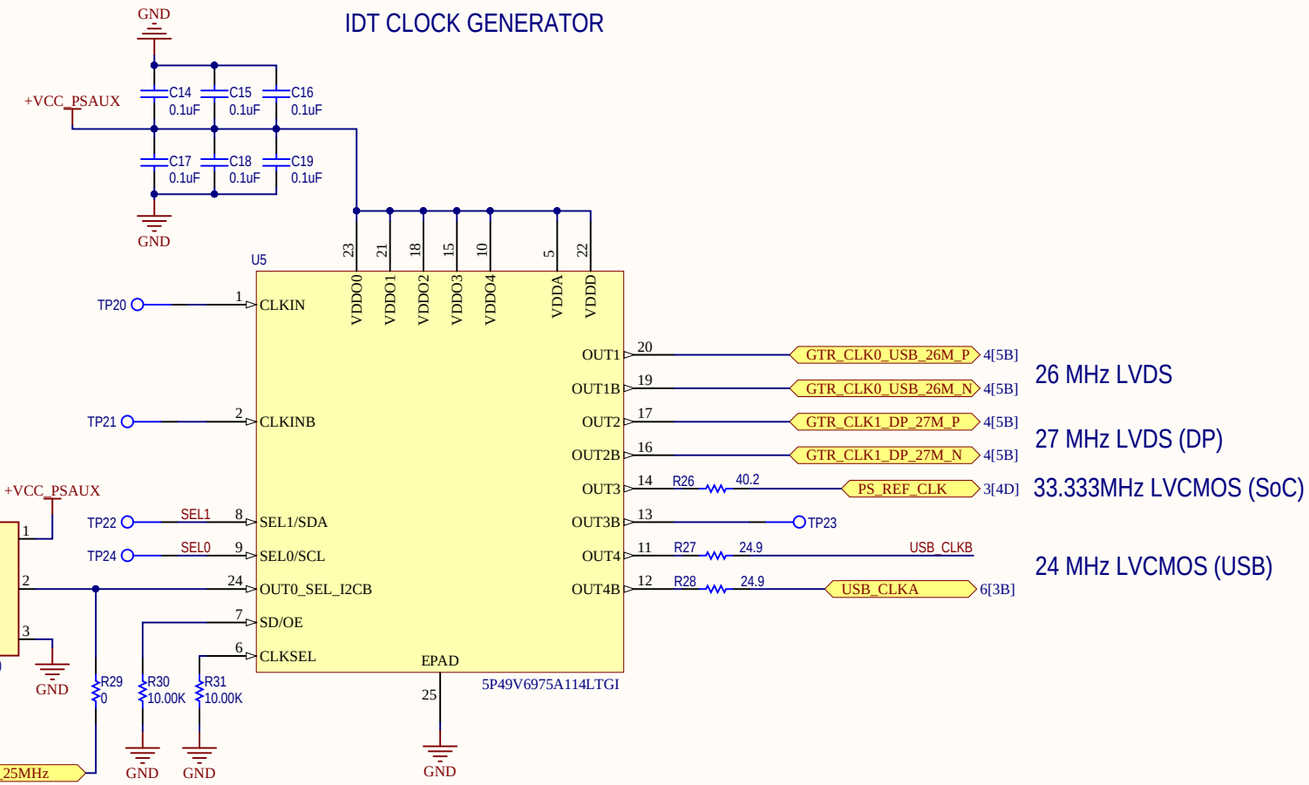
USB 2.0 DOWNSTREAM DEVICE & IDT CLOCK GENERATOR

USB 2.0 XNCVR



Layout Notes:
1) USB 2.0 ULPI_D_P/N signals differentially routed @ 90 ohms.

IDT CLOCK GENERATOR



26 MHz LVDS

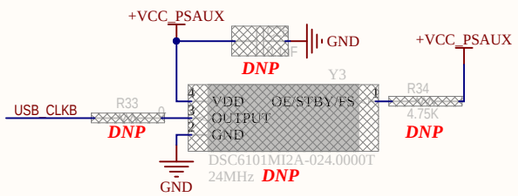
27 MHz LVDS (DP)

33.333MHz LVCMOS (SoC)

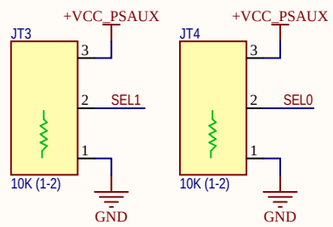
24 MHz LVCMOS (USB)

25 MHz LVCMOS (USB HUB)

24MHz CLOCK



Layout Note: Place R33 pin 2 pad directly on clock trace to U4.



Avnet Engineering Services			
Project Name: Ultra96 SBC V2	PCB Rev: 1	BOM: 01	Variant: 00
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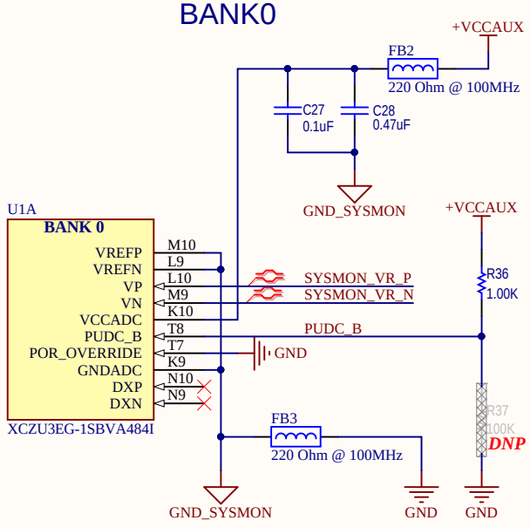
Sheet Title: 07 - USB2.0 Downstream Device & Clock Gen.SchDoc	Size: B	Sheet: 7 of 18	

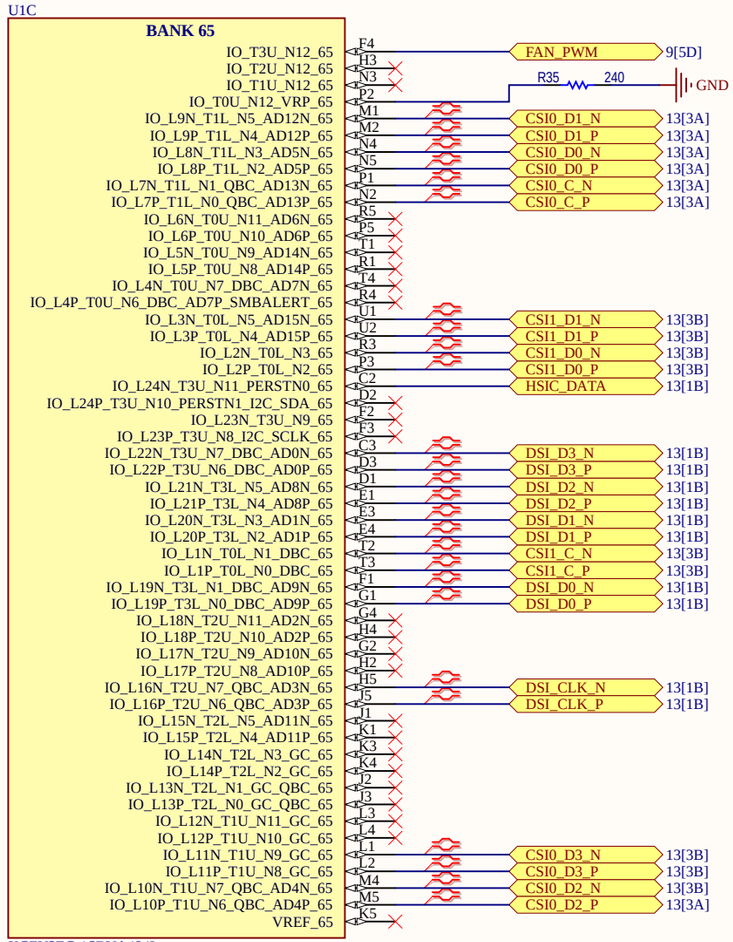
BANK0, BANK26, BANK65, BANK66

BANK0

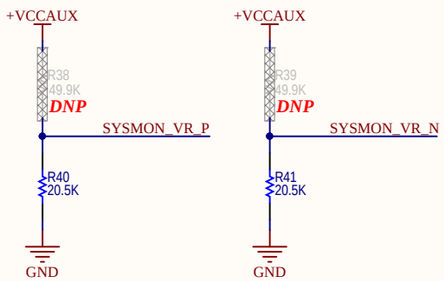


BANK26

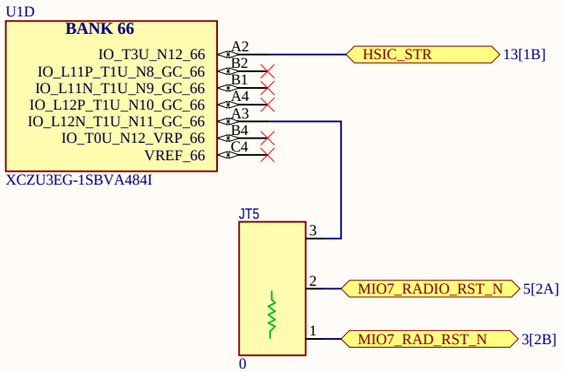
BANK65



SYSMON I2C ADDRESS SELECT



BANK66



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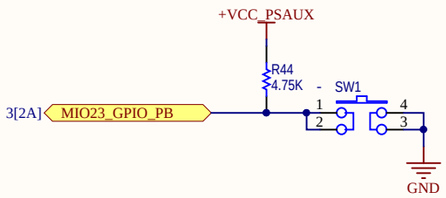
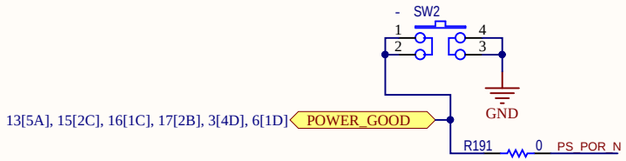
USER SWITCHES, LEDs, JTAG I/F, FAN DRIVER

SWITCHES

MIO23_GPIO_PB

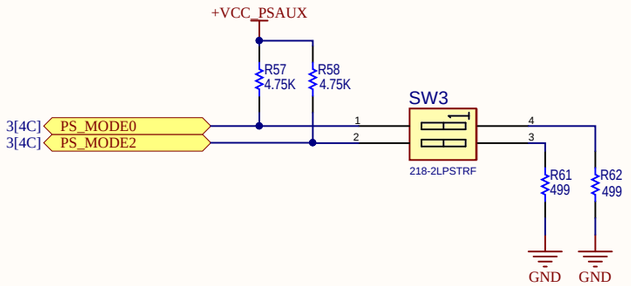


PS_POR_PB



BOOT MODE:

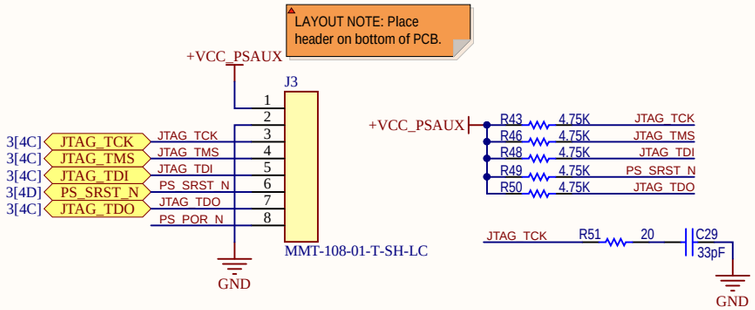
JTAG: 1,1
SD: 0,1



PMIC I2C CONNECTIONS

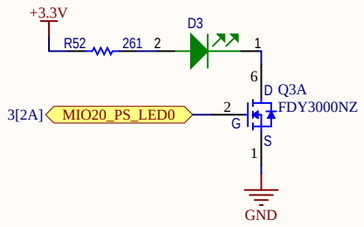
LAYOUT NOTE: Order these TPs as follows: SCL, SDA, GND in a 100 mil center-to- center line. Add silkscreen (SDA, SCL, GND) by appropriate test point.

JTAG HEADER (BOTTOM OF PCB)

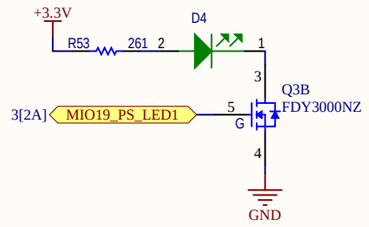


MIO/USER LEDs

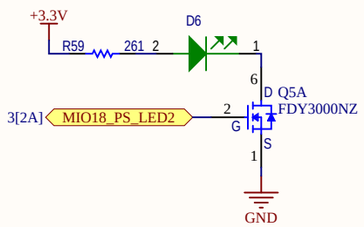
MIO20_PS_LED0



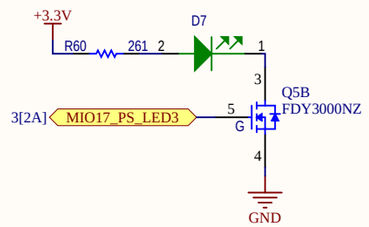
MIO19_PS_LED1



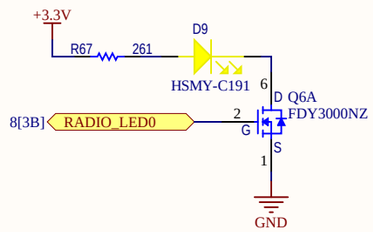
MIO18_PS_LED2

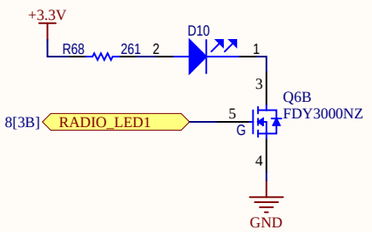


MIO17_PS_LED3

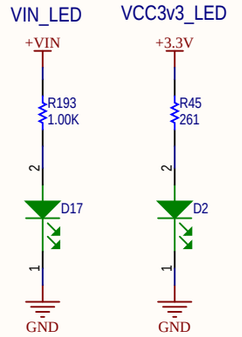


RADIO/USER LEDs

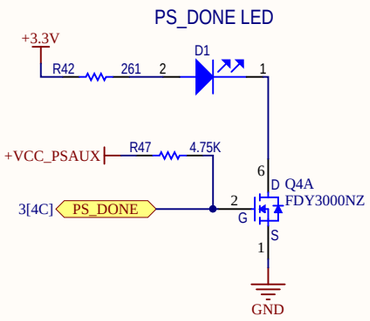




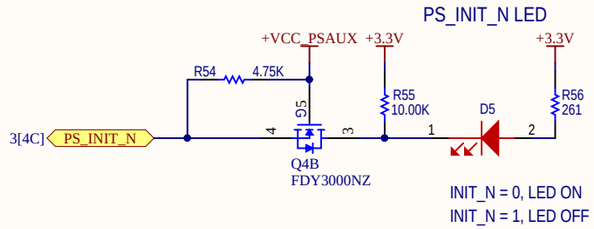
LED INDICATORS:



PS_DONE LED

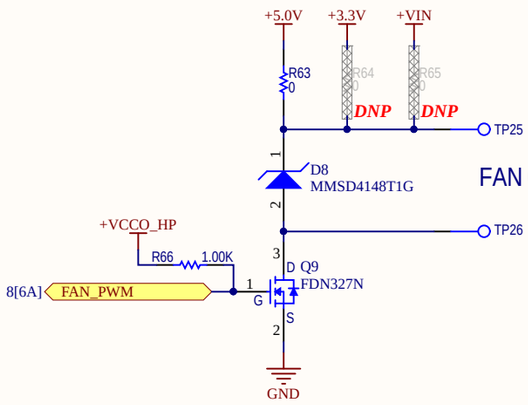


PS_INIT_N LED



INIT_N = 0, LED ON
INIT_N = 1, LED OFF

FAN DRIVER:



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BANK POWER & DECOUPLING

U1L
PL CORE POWER
VCCAUX M6
VCCAUX P6
VCCAUX_IO J6
VCCAUX_IO K6
VCCAUX_IO L6
VCCBRAM N7
VCCBRAM R6
VCCBRAM R7
VCCBRAM T6
VCCBRAM H10
VCCINT H8
VCCINT J11
VCCINT J9
VCCINT K8
VCCINT L11
VCCINT M8
VCCINT N11
VCCINT P10
VCCINT P8
VCCINT R11
VCCINT R9
VCCINT H7
VCCINT_IO J7
VCCINT_IO L7
VCCINT_IO M7
XCZU3EG-1SBVA484I
+VCCAUX
+VCCINT

+VCCINT
C30 0.47uF
C32 0.47uF
GND

+VCCAUX
C31 4.7uF
C33 0.47uF
C34 0.47uF
GND

+VCC_PSINTFP
C43 0.47uF
C45 0.47uF
GND

+VCC_PSINTLP
C42 4.7uF
C44 0.47uF
C46 0.47uF
GND

+MGTRAVTT
C57 4.7uF
C58 0.47uF
C59 0.1uF
GND

+MGTRAVCC
C60 4.7uF
C61 0.47uF
C62 0.1uF
GND

+VCC_PSAUX
C35 0.47uF
C36 0.47uF
C37 0.47uF
C38 0.47uF
C39 0.47uF
C40 0.47uF
C41 1000pF
GND

+VCCO_PSDDR
C47 10uF
C48 0.47uF
C49 4.7uF
C50 0.047uF
C51 1000pF
C52 1000pF
C53 1000pF
GND

U1M
VCCO
VCCO_PSIO0_500 AA5
VCCO_PSIO0_500 V6
VCCO_PSIO1_501 C11
VCCO_PSIO1_501 F10
VCCO_PSIO2_502 C16
VCCO_PSIO2_502 D14
VCCO_PSIO3_503 G13
VCCO_PSIO3_503 H16
VCCO_PSDDR_504 AB18
VCCO_PSDDR_504 P19
VCCO_PSDDR_504 T20
VCCO_PSDDR_504 V16
VCCO_PSDDR_504 V21
VCCO_PSDDR_504 Y17
VCCO_PSDDR_504 Y22
VCCO_26 B8
VCCO_26 E7
VCCO_65 B3
VCCO_65 G3
VCCO_65 K2
VCCO_65 P4
XCZU3EG-1SBVA484I
+VCC_PSAUX
+VCCO_PSDDR
+VCCAUX
+VCCO_HP
C54 10000pF
C55 10000pF
C56 10000pF
GND
NOTE: Bank 66 HP I/Os are attached to VCCO 65 internally.
Layout Note: Place direct pin connect CAPs under Zynq.

U1O
XCZU3EG-1SBVA484I
GND_SYSMON
Y7 Y2 Y12 W9 W4 W19 W14 V11 V1 U8 U3 U18 P16 U13 T5 T15 T11 R8 R22 R2 R17 R12 R10 P9
GND_PSADC
DIGITAL GND
A1 A10 A15 A18 A22 A5 AA10 AA15 AA20 AB1 AB13 AB22 AB3 AB8 B13 B20 C1 C18 C21 C22 C6 D20 D4 D9 E12
P7 P14 P11 N8 N6 N22 N21 N20 N16 N1 M3 M19 M18 M13 M11 L8 L5 L22 L21 L18 L15 K7 K20 K17
E17 E18 F2 E21 E22 F15 F20 F5 G18 G21 G22 G8 H1 H11 H20 H6 H9 J10 J14 J18 J21 J22 J4 J8 K11
GND

U1N
PS CORE POWER
PS_MGTRAVCC F19
PS_MGTRAVCC H19
PS_MGTRAVCC K19
PS_MGTRAVTT A21
PS_MGTRAVTT B19
PS_MGTRAVTT D19
VCC_PSADC P15
VCC_PSAUX L16
VCC_PSAUX L17
VCC_PSAUX M16
VCC_PSAUX M17
VCC_PSAUX N15
VCC_PSBATT M14
VCC_PSDDR_PLL M15
VCC_PSDDR_PLL N14
VCC_PSINTFP R15
VCC_PSINTFP R16
VCC_PSINTFP T12
VCC_PSINTFP T13
VCC_PSINTFP T14
VCC_PSINTFP T16
VCC_PSINTFP N17
VCC_PSINTFP_DDR P17
VCC_PSINTFP_DDR T17
VCC_PSINTFP_DDR N12
VCC_PSINTLP N13
VCC_PSINTLP P12
VCC_PSINTLP P13
VCC_PSINTLP R13
VCC_PSINTLP R14
VCC_PSINTLP L13
VCC_PSPLL L14
VCC_PSPLL M12
VCC_PSPLL
XCZU3EG-1SBVA484I
+MGTRAVCC
+MGTRAVTT
+VCC_PSAUX
+VCC_PSINTFP
+VCC_PSINTLP
+VCC_PSPLL
R69 0
TP30 TP31
GND
C63 0.47uF
C64 0.1uF
GND_SYSMON
FB4
FB5
GND
+VCC_PSAUX
LAYOUT NOTE: TP30/31 within 100 mils of each other. TP30 silk: +VB, TP31 silk: GND. Add silk battery symbol if possible.

AVNET Avnet Engineering Services	
Project Name: Ultra96 SBC V2	PCB Rev: 1 / BOM: 01 / Variant: 00
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Sheet Title: 10 - Bank Power and Decoupling.SchDoc	Size: B / Sheet: 10 of 18

LPDDR4 16Gb (2GB) RAM

POINT-TO-POINT: NO DDR TERM RESISTORS

40 OHM INTERFACE IMPEDANCE

LAYOUT NOTE: Place ZQ resistor close to DDR IC.

+VCCO_PSDDR R146 240

+VCCO_PSDDR R147 4.75K DDR_ODT

U13 A5 ZQ0

+VCCO_PSDDR: AA10 AA8 AA5 AA3 W12 W8 W5 W1 U10 U3 F10 F3 D12 D8 D5 D1 B10 B8 B5 B3

+VCC_PSAUX: U12 U1 T9 T4 G9 G4 F12 F1

+VCCO_PSDDR: F8 F5 A9 A4 AB9 AB4 U8 U5 R12 R8 R5 R1 N12 N10 N3 N1 K12 K10 K3 K1 H12 H8 H5 H1

VDDQ: AA10 AA8 AA5 AA3 W12 W8 W5 W1 U10 U3 F10 F3 D12 D8 D5 D1 B10 B8 B5 B3

VDD1: U12 U1 T9 T4 G9 G4 F12 F1

VDD2: F8 F5 A9 A4 AB9 AB4 U8 U5 R12 R8 R5 R1 N12 N10 N3 N1 K12 K10 K3 K1 H12 H8 H5 H1

4[1A]	PS_DDR_CAA0	H2	CA0_A
4[1A]	PS_DDR_CAA1	J2	CA1_A
4[1B]	PS_DDR_CAA2	H9	CA2_A
4[1B]	PS_DDR_CAA3	H10	CA3_A
4[1B]	PS_DDR_CAA4	H11	CA4_A
4[1B]	PS_DDR_CAA5	J11	CA5_A
4[1B]	PS_DDR_CKA_T	J8	CK_t_A
4[1B]	PS_DDR_CKA_C	J9	CK_c_A
11[2C], 4[1B]	PS_DDR_CKE0	J4	CKE0_A
11[2C], 4[1C]	PS_DDR_CS0_N	H4	CS0_A
DDR_ODT		G2	ODT_CA_A
		C3	DMI0_A
4[1C]	PS_DDR_DMA0	C10	DMI1_A
4[1C]	PS_DDR_DMA1		

4[1A]	PS_DDR_CAB0	R2	CA0_B
4[1A]	PS_DDR_CAB1	P2	CA1_B
4[1B]	PS_DDR_CAB2	R9	CA2_B
4[1B]	PS_DDR_CAB3	R10	CA3_B
4[1B]	PS_DDR_CAB4	R11	CA4_B
4[1B]	PS_DDR_CAB5	P11	CA5_B
4[1C]	PS_DDR_CKB_C	P9	CK_c_B
4[1B]	PS_DDR_CKB_T	P8	CK_t_B
11[2B], 4[1B]	PS_DDR_CKE0	P4	CKE0_B
11[2B], 4[1C]	PS_DDR_CS0_N	R4	CS0_B
DDR_ODT		T2	ODT_CA_B
		Y3	DMI0_B
4[1C]	PS_DDR_DMB0	Y10	DMI1_B
4[1C]	PS_DDR_DMB1		

LAYOUT NOTEs: 1) 40 Ohm Interface impedance. 2) Place DDR within 1 inch of Zynq device. 3) Place decoupling capacitors as close as possible to DDR device.

MT53D512M32D2DS-053 AIT:D

DQ0_A	B2	PS_DDR_DQ0	4[1C]
DQ0_B	AA2	PS_DDR_DQ16	4[3A]
DQ1_A	C2	PS_DDR_DQ1	4[1C]
DQ1_B	Y2	PS_DDR_DQ17	4[3B]
DQ10_A	E11	PS_DDR_DQ10	4[1C]
DQ10_B	V11	PS_DDR_DQ26	4[3B]
DQ11_A	F11	PS_DDR_DQ11	4[1C]
DQ11_B	U11	PS_DDR_DQ27	4[3B]
DQ12_A	F9	PS_DDR_DQ12	4[1C]
DQ12_B	U9	PS_DDR_DQ28	4[3B]
DQ13_A	E9	PS_DDR_DQ13	4[3A]
DQ13_B	V9	PS_DDR_DQ29	4[3B]
DQ14_A	C9	PS_DDR_DQ14	4[3A]
DQ14_B	Y9	PS_DDR_DQ30	4[3B]
DQ15_A	B9	PS_DDR_DQ15	4[3A]
DQ15_B	AA9	PS_DDR_DQ31	4[3B]
DQ2_A	E2	PS_DDR_DQ2	4[3B]
DQ2_B	V2	PS_DDR_DQ18	4[3B]
DQ3_A	F2	PS_DDR_DQ3	4[3B]
DQ3_B	U2	PS_DDR_DQ19	4[3B]
DQ4_A	F4	PS_DDR_DQ4	4[3B]
DQ4_B	U4	PS_DDR_DQ20	4[3B]
DQ5_A	E4	PS_DDR_DQ5	4[3B]
DQ5_B	V4	PS_DDR_DQ21	4[3B]
DQ6_A	C4	PS_DDR_DQ6	4[3B]
DQ6_B	Y4	PS_DDR_DQ22	4[3B]
DQ7_A	B4	PS_DDR_DQ7	4[3C]
DQ7_B	AA4	PS_DDR_DQ23	4[3B]
DQ8_A	B11	PS_DDR_DQ8	4[3C]
DQ8_B	AA11	PS_DDR_DQ24	4[3B]
DQ9_A	C11	PS_DDR_DQ9	4[3C]
DQ9_B	Y11	PS_DDR_DQ25	4[3B]
DQS0_c_A	E3	PS_DDR_DQSA0_C	4[3C]
DQS0_c_B	V3	PS_DDR_DQSB0_C	4[3C]
DQS0_t_A	D3	PS_DDR_DQSA0_T	4[3C]
DQS0_t_B	W3	PS_DDR_DQSB0_T	4[3C]
DQS1_c_A	E10	PS_DDR_DQSA1_C	4[3C]
DQS1_c_B	V10	PS_DDR_DQSB1_C	4[3C]
DQS1_t_A	D10	PS_DDR_DQSA1_T	4[3C]
DQS1_t_B	W10	PS_DDR_DQSB1_T	4[3C]

NC	R3	PS_DDR_CS1_N	4[1C]
NC	A8		
NC	N8		
NC	N5		
NC	K8		
NC	K5		
NC	G11		
NC	H3		
NC	P5	PS_DDR_CKE1	4[1B]
NC	J5		

R148 240 +VCCO_PSDDR

R149 0

4[3C] PS_DDR_RST_N T11 RESET_n

R150 4.75K GND

VSS: E1 E5 E8 E12 G1 G3 G5 G8 G10 G12 J1 J3 J10 J12 K2 K4 K9 K11 N2 N4 N9 N11 P1 P3 P10 P12 T1 T3 T5 T8 T10 T12 V1 V5 V8 V12 W2 W4 W9 W11 Y1 Y5 Y8 Y12 AB3 AB5 AB8 AB10 A3 A10 C1 C5 C8 C12 D2 D4 D9 D11

GND

PS_DDR_CS and CKE signals connected to maintain backwards DDR compatibility.

+VCCO_PSDDR: C161 10uF, C162 0.47uF, C163 4.7uF, C164 0.047uF, C165 1000pF, C166 1000pF, C167 1000pF

+VCCO_PSDDR: C168 0.47uF, C169 0.047uF, C170 1000pF, C171 1000pF, C172 1000pF

+VCC_PSAUX: C160 0.1uF

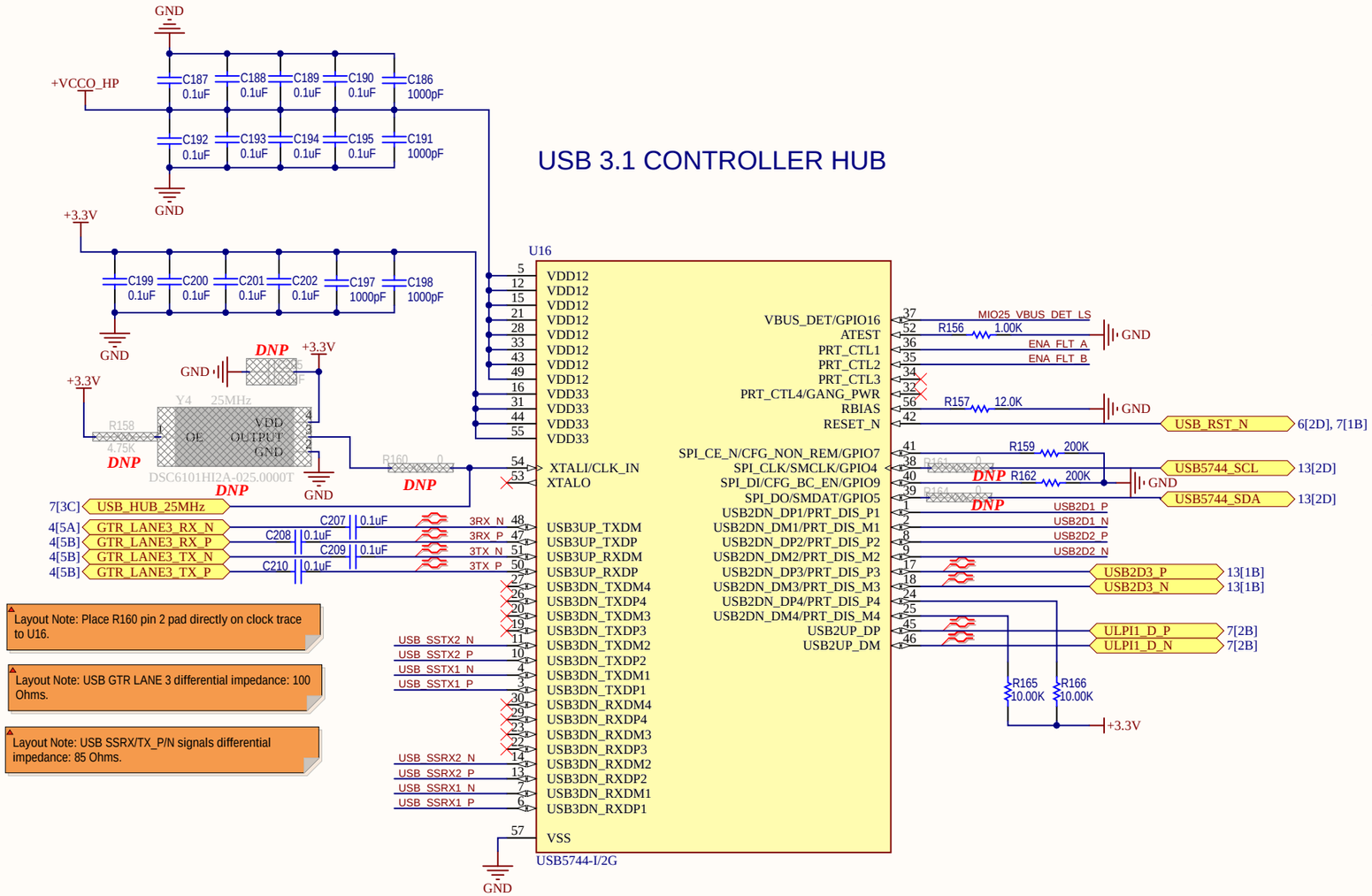
GND

AVNET Avnet Engineering Services

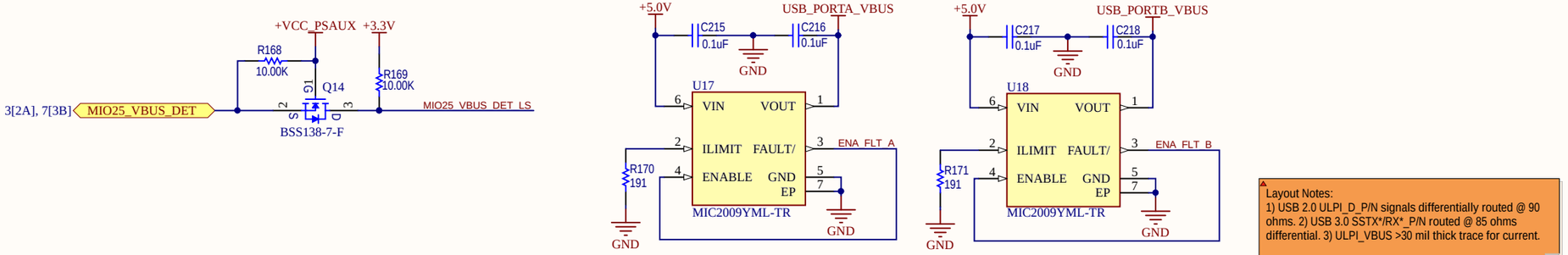
Project Name: Ultra96 SBC V2		PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1SBC	Date: 3/1/2019	Time: 7:57:27 AM		
Sheet Title: 11 - LPDDR4 Device #1.SchDoc		Size: B	Sheet: 11 of 18	

USB 3.0 DUAL PORT HUB

USB 3.1 CONTROLLER HUB



USB PORT POWER SWITCHES

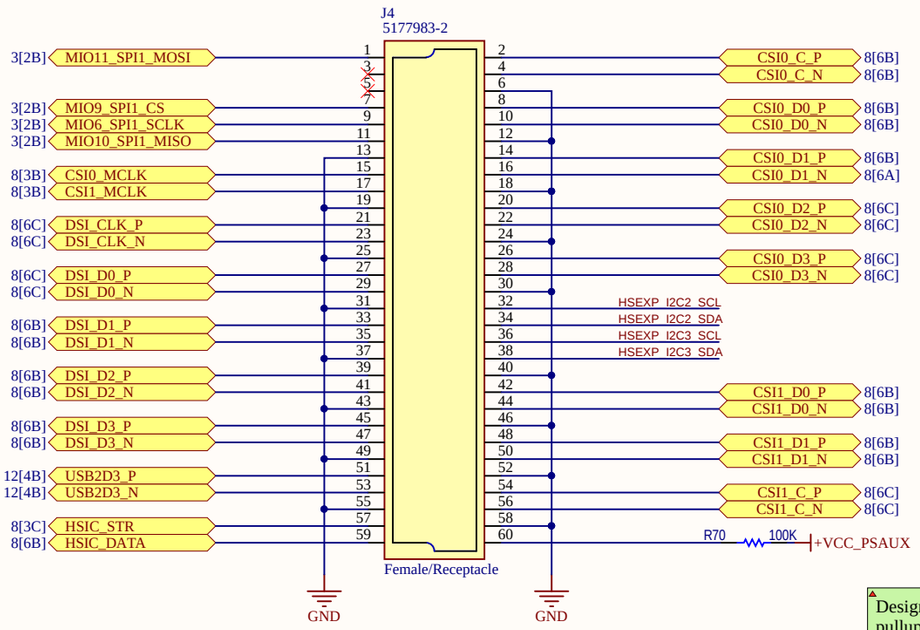


Layout Notes:
1) USB 2.0 ULPI_D_P/N signals differentially routed @ 90 ohms. 2) USB 3.0 SSTX*/RX*_P/N routed @ 85 ohms differential. 3) ULPI_VBUS >30 mil thick trace for current.

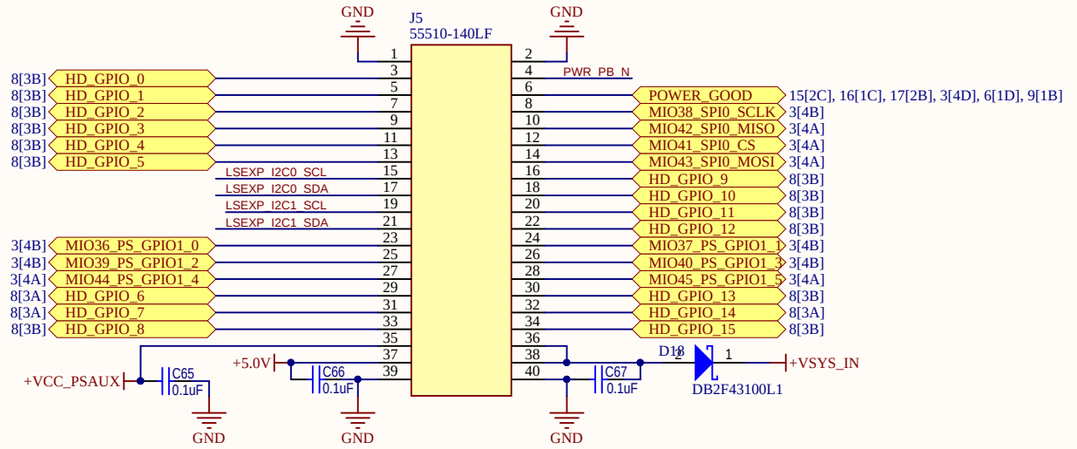
Avnet Engineering Services			
Project Name: Ultra96 SBC V2	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1SBC	Date: 3/1/2019	Time: 7:57:27 AM	
Sheet Title: 12 - USB 3.0 Dual Port Hub.SchDoc	Size: B	Sheet: 12 of 18	

I/O EXPANSION HEADERS, ON/OFF CONTROLLER

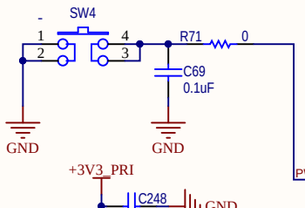
60 PIN HS EXP HDR



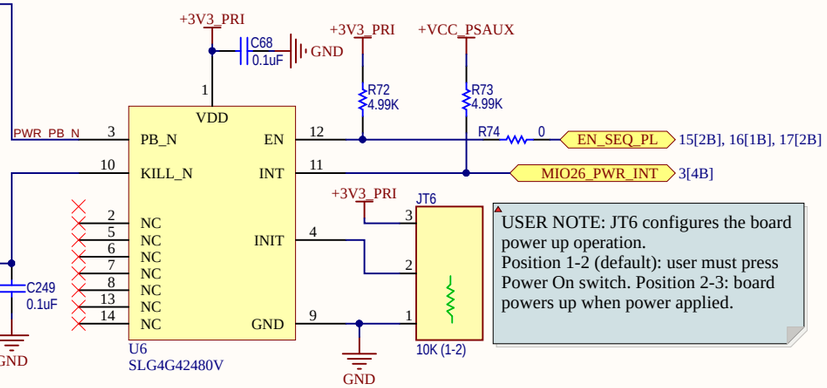
40 PIN LS EXP HDR



POWER BUTTON



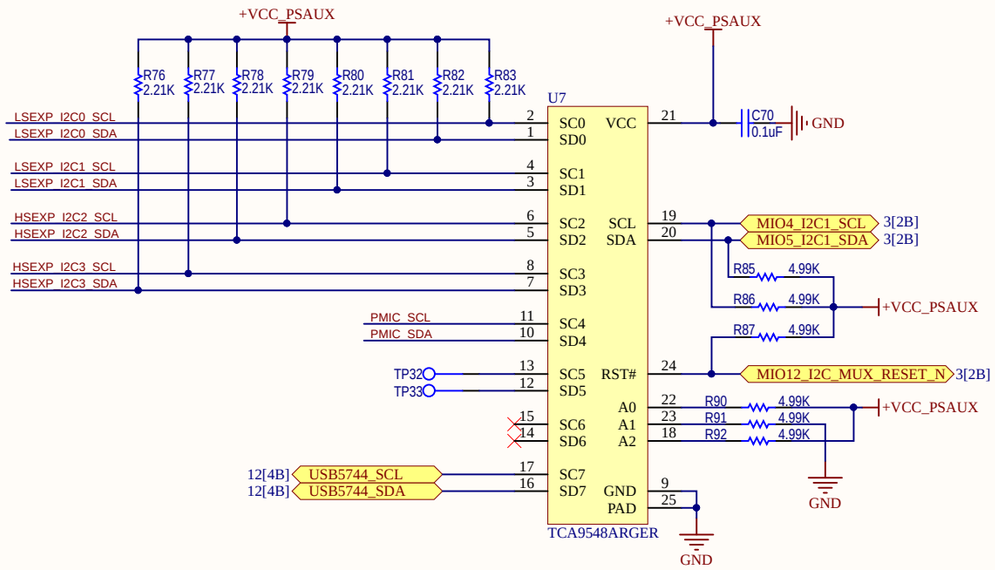
ON/OFF CONTROLLER

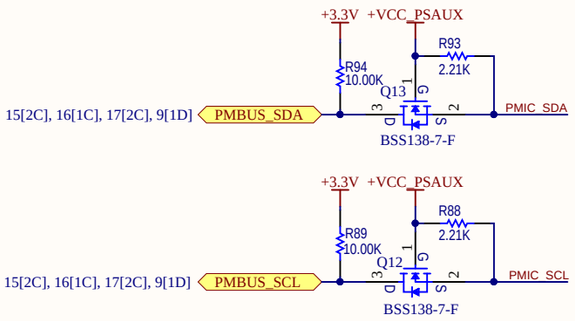


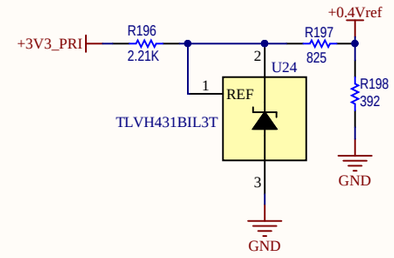
USER NOTE: JT6 configures the board power up operation.
Position 1-2 (default): user must press Power On switch. Position 2-3: board powers up when power applied.

Design Note: PB_N has 100K internal pullup to VCC. KILL_N is floating and must be pulled up to Vccio +1.8V value (as shown).

I2C EXPANDER



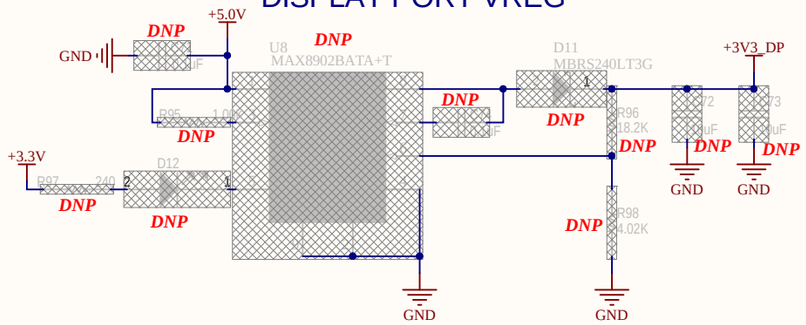




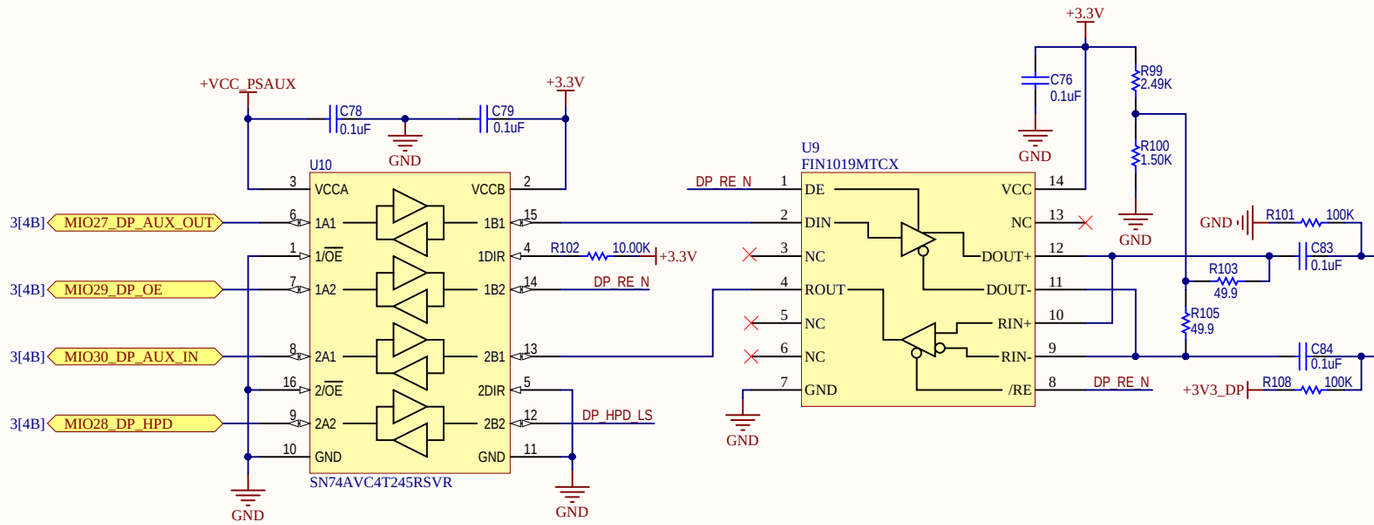
AVNET Avnet Engineering Services			
Project Name: Ultra96 SBC V2	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1SBC	Date: 3/1/2019	Time: 7:57:27 AM	
Sheet Title: 13 - Jx_Jy Expansion Headers, Power On.SchDoc	Size: B	Sheet: 13 of 18	

Mini DISPLAY PORT

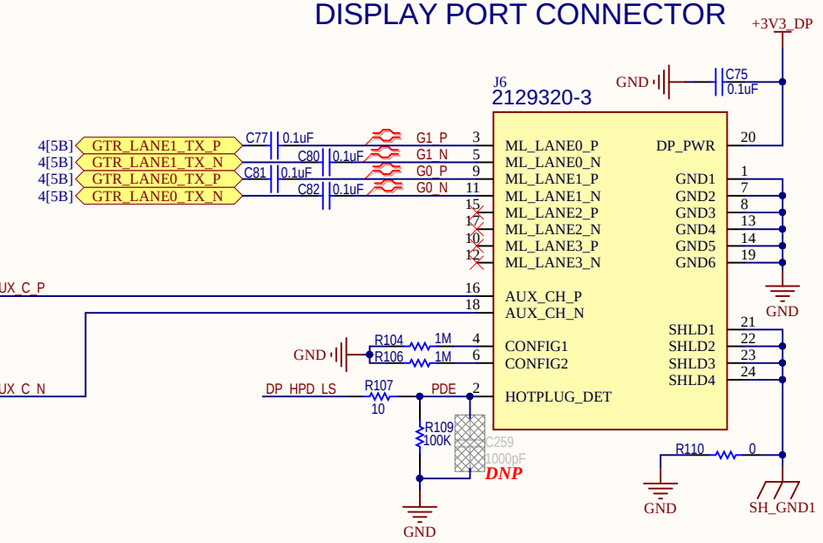
DISPLAY PORT VREG



DISPLAY PORT DPAUX GENERATOR



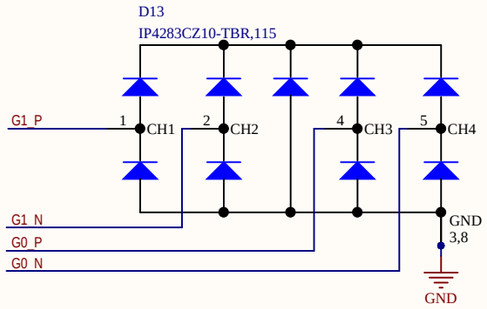
DISPLAY PORT CONNECTOR

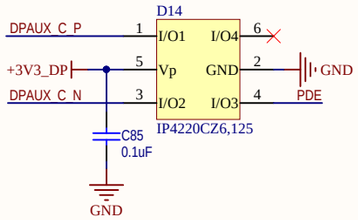


Layout Note:
All Display Port data signals (GTR_LANE0,1_TX_P/N, G0,1_P/N) differentially routed to @ 100 ohms. Trace length match to within 5 mils.

Layout Note: Board edge PCB cut-out under this device! See datasheet.

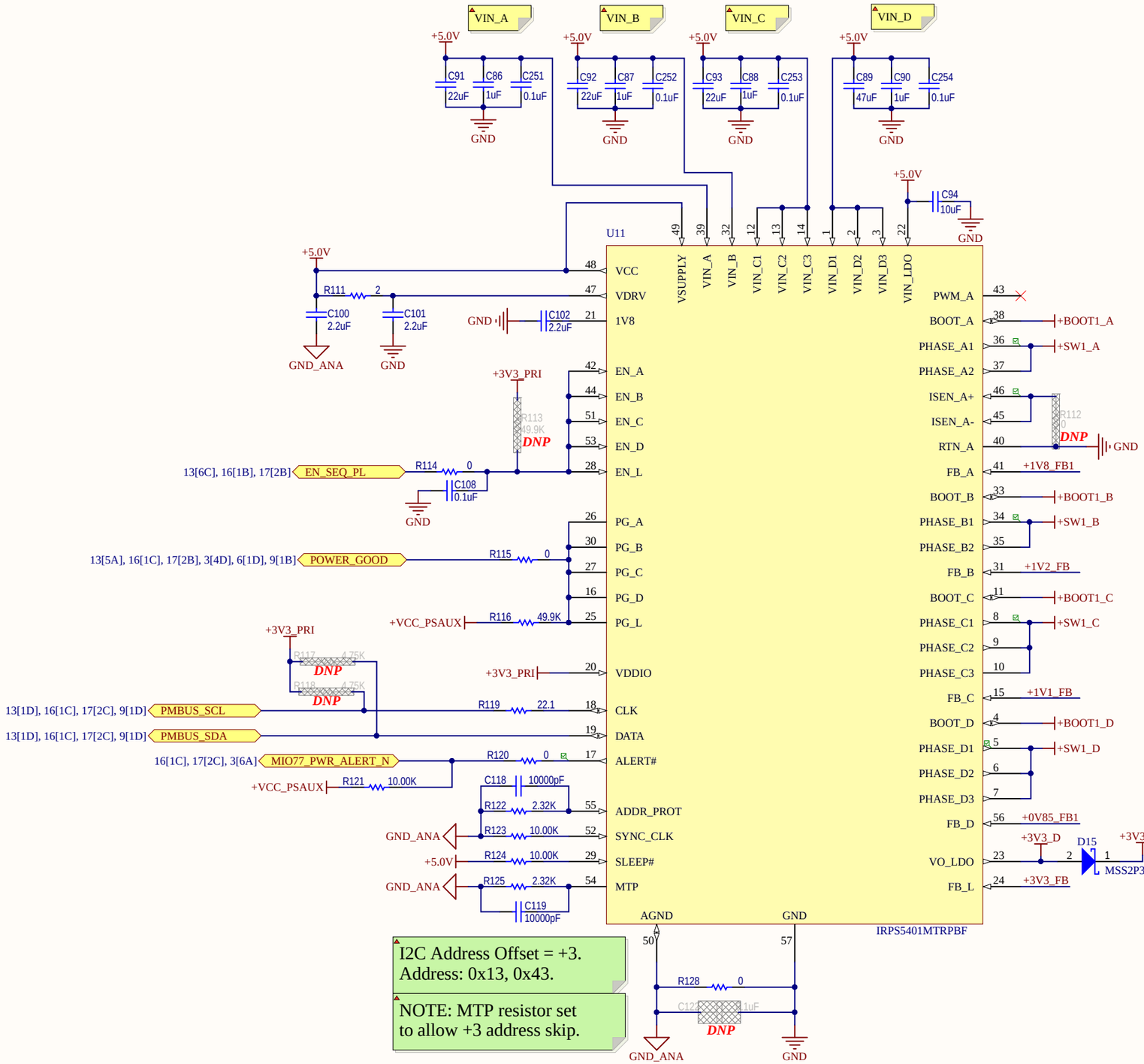
ESD PROTECTION DEVICES





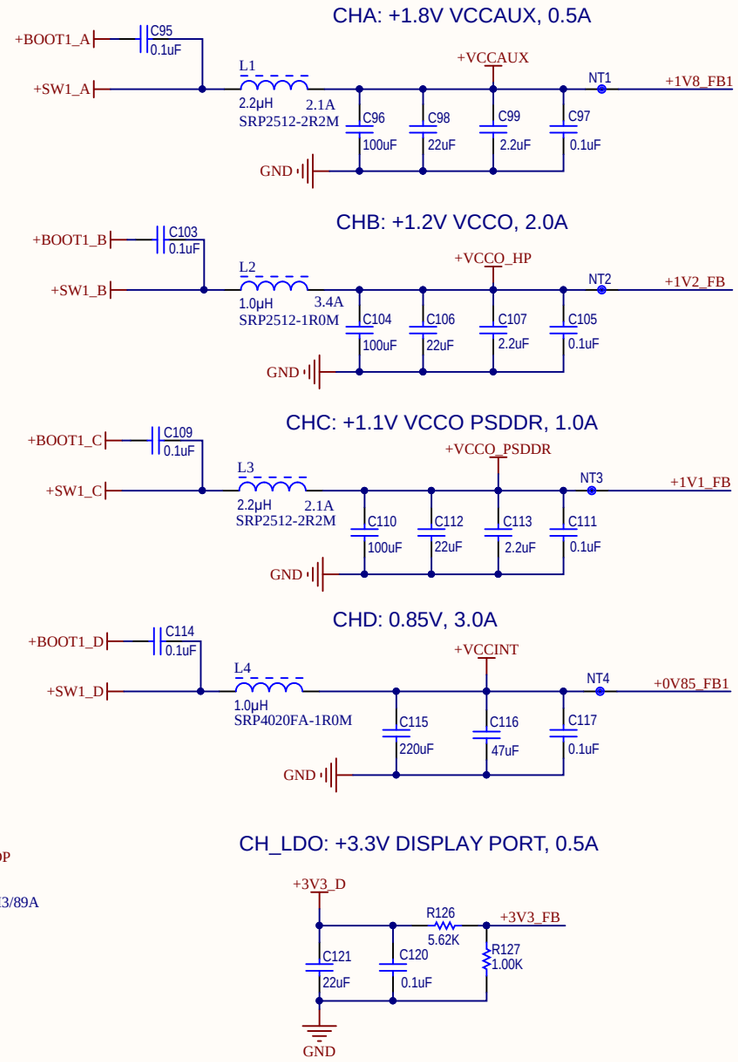
AVNET Avnet Engineering Services			
Project Name: Ultra96 SBC V2	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1SBC	Date: 3/1/2019	Time: 7:57:27 AM	
Sheet Title: 14 - Display Port.SchDoc	Size: B	Sheet: 14 of 18	

ROCKY PMIC #1



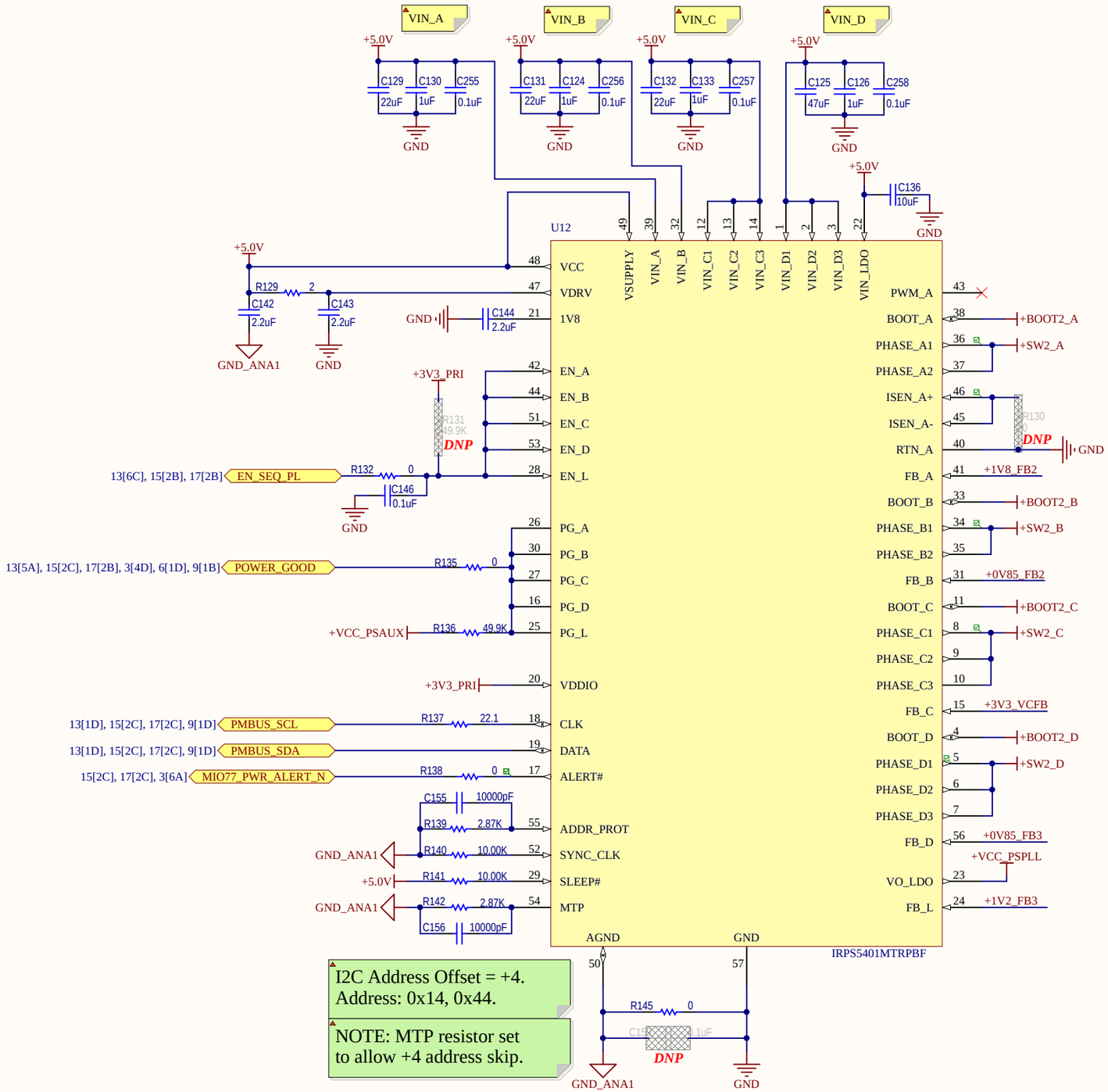
I2C Address Offset = +3.
Address: 0x13, 0x43.

NOTE: MTP resistor set to allow +3 address skip.



AVNET Avnet Engineering Services			
Project Name: Ultra96 SBC V2	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1SBC	Date: 3/1/2019	Time: 7:57:28 AM	
Sheet Title: 15 - Rocky PMIC #1.SchDoc	Size: B	Sheet: 15 of 18	

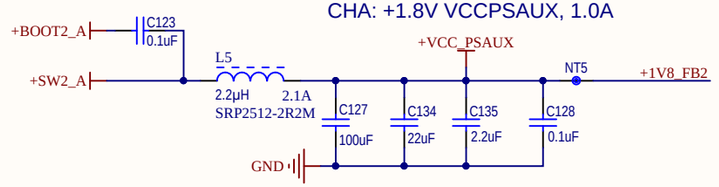
ROCKY PMIC #2



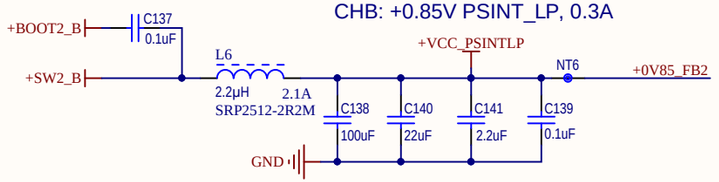
I2C Address Offset = +4.
Address: 0x14, 0x44.

NOTE: MTP resistor set to allow +4 address skip.

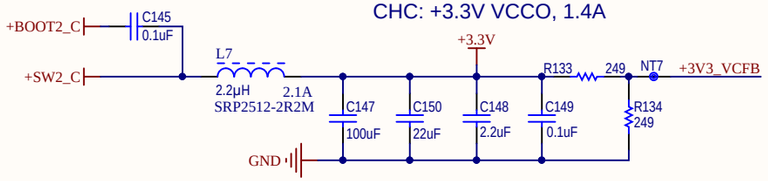
CHA: +1.8V VCCPSAUX, 1.0A



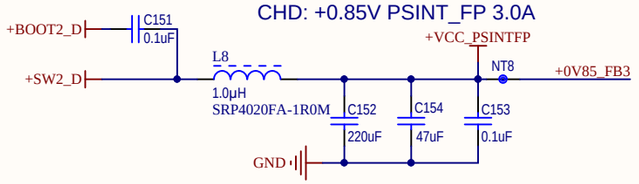
CHB: +0.85V PSINT_LP, 0.3A



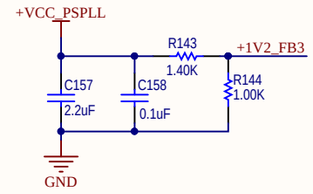
CHC: +3.3V VCCO, 1.4A



CHD: +0.85V PSINT_FP 3.0A



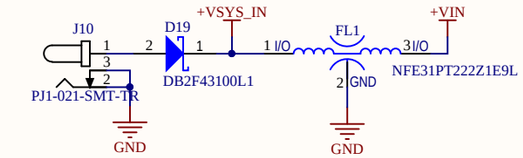
CH_LDO: +1.2V PSPLL, 0.5A



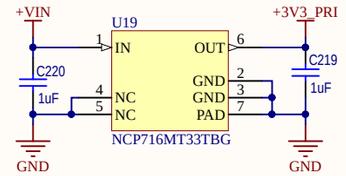
AVNET Avnet Engineering Services			
Project Name: Ultra96 SBC V2	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1SBC	Date: 3/1/2019	Time: 7:57:28 AM	
Sheet Title: 16 - Rocky PMIC #2.SchDoc	Size: B	Sheet: 16 of 18	

MANHATTAN PMIC #3

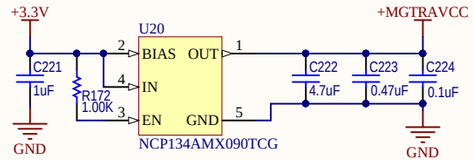
MAIN POWER +8v - 16 VIN



+3.3V_PRIMARY

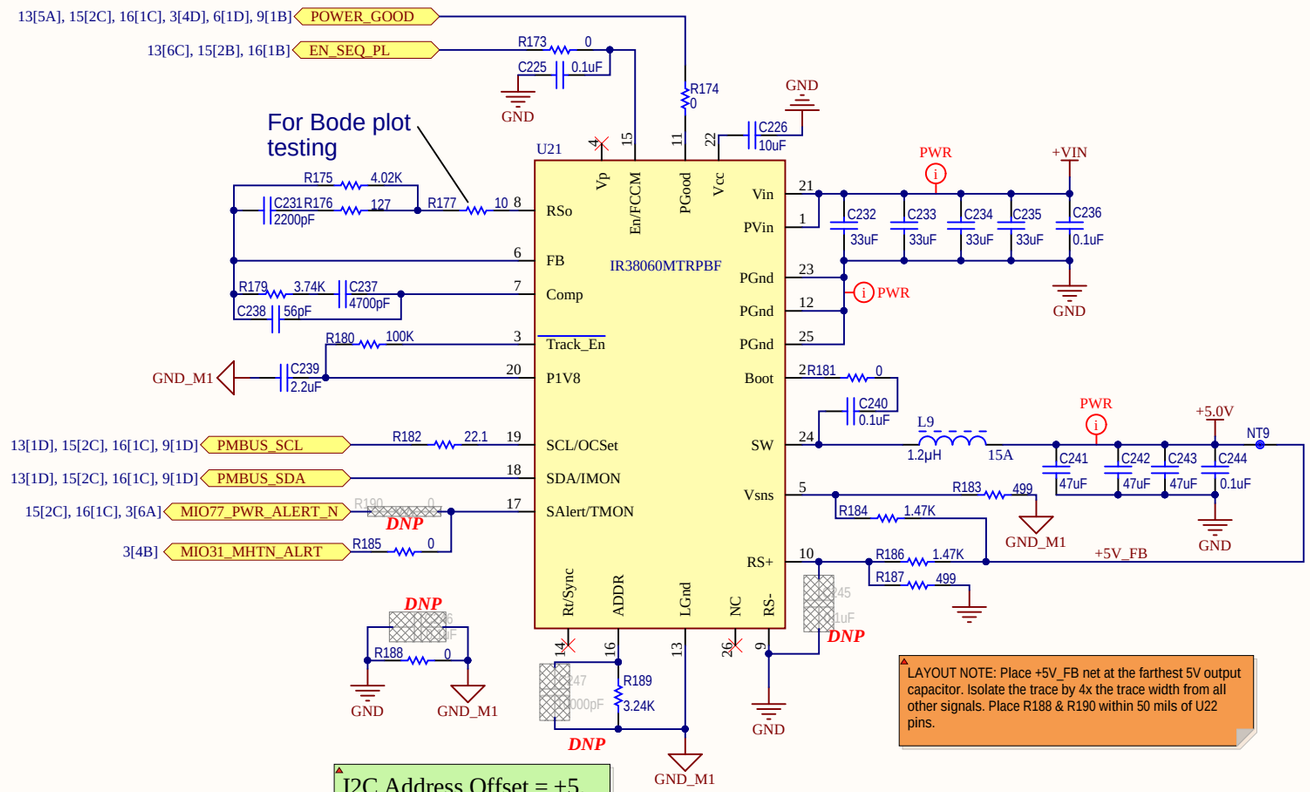


CHC: +0.9V PSMGTAVCC, 0.3A



CH_LDO: +1.8V MGTRAVTT, 0.05A

BOARD +5.0V MAIN, 6A Max



I2C Address Offset = +5.
Addresses: 0x15, 0x45.

NOTE: MTP resistor set to allow +5 address skip.

Avnet Engineering Services	
Project Name: Ultra96 SBC V2	PCB Rev: 1 / BOM: 01 / Variant: 00
Doc Num: SCH-US1SBC	Date: 3/1/2019 / Time: 7:57:28 AM
Sheet Title: 17 - Manhattan PMIC #3.SchDoc	Size: B / Sheet: 17 of 18

Assembly:

Label1
BD-XXXX-XXXXX-G
Label, Product

Label2
XXXXXXX
Label, Serial Number

ESD1

ESD Bag

Label_ESD1

Label, ESD

Mechanicals:

PCB

XXX-XXX-PCB-X
PCB PN (In Copper)

SS1

Trash Can-Silk Screen

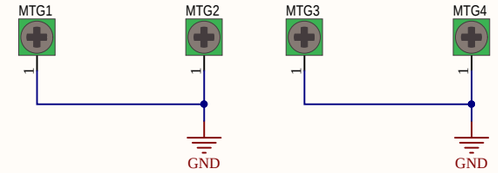
SS2

RoHS 2-Silk Screen

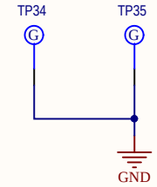
SS3

FCC - Silk Screen

Mounting Holes:



GND Test Points:



AVNET Avnet Engineering Services			
Project Name: Ultra96 SBC V2	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1SBC	Date: 3/1/2019	Time: 7:57:28 AM	
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