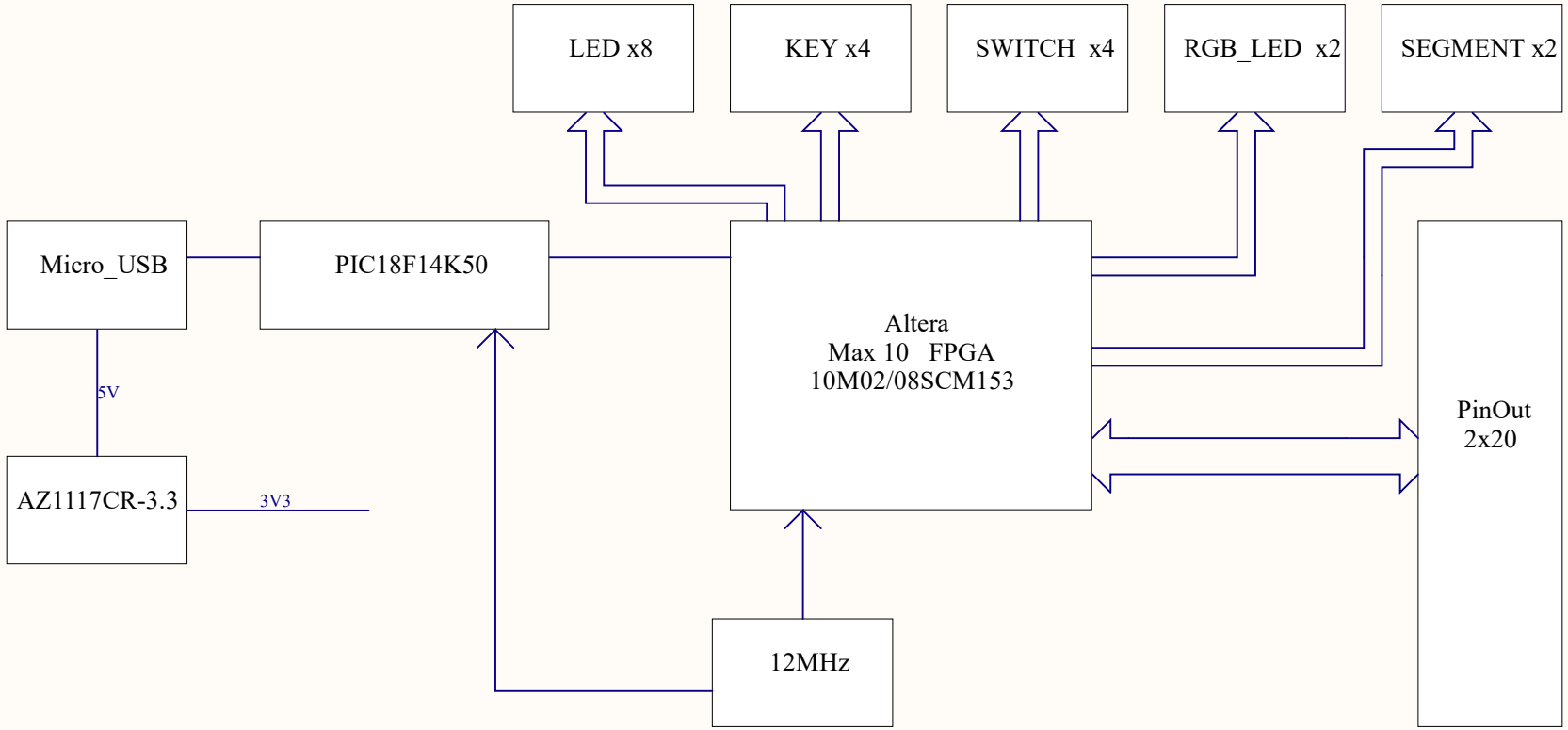

工程名称： STEP-MAX10 FPGA Board		
图纸大小： A4	版本号： V2.0	制图：
日期： 2019/8/17	页码： 第 1 共 2	审核：
Block Diagram		

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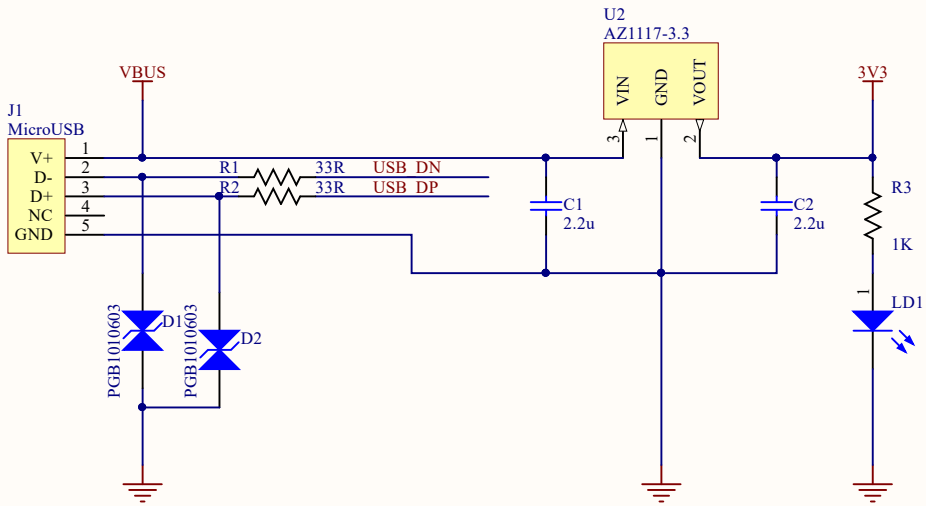

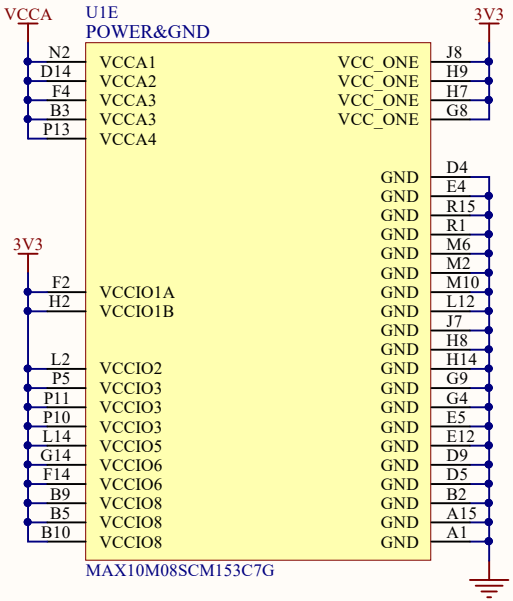

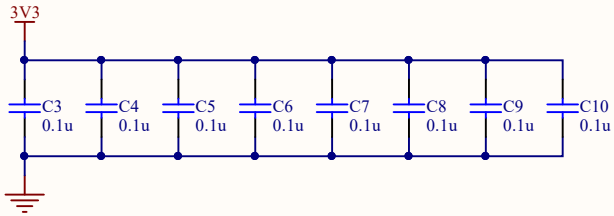

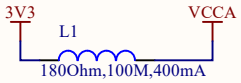

工程名称： STEP-MAX10 FPGA Board			
图纸大小： A4	版本号： V2.0	制图：	
日期： 2019/8/17	页码： 第 2 共 5	审核：	
Power			

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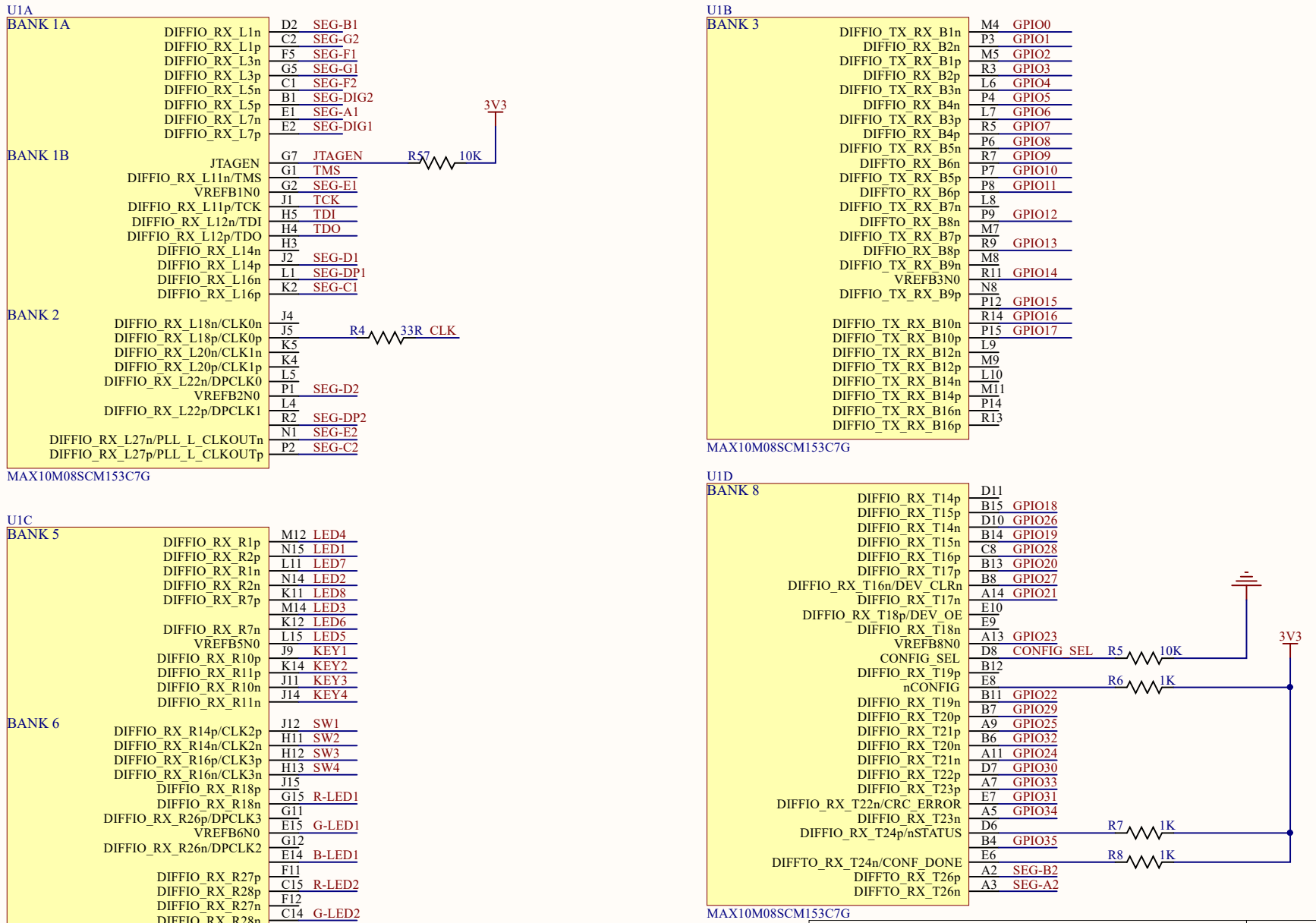
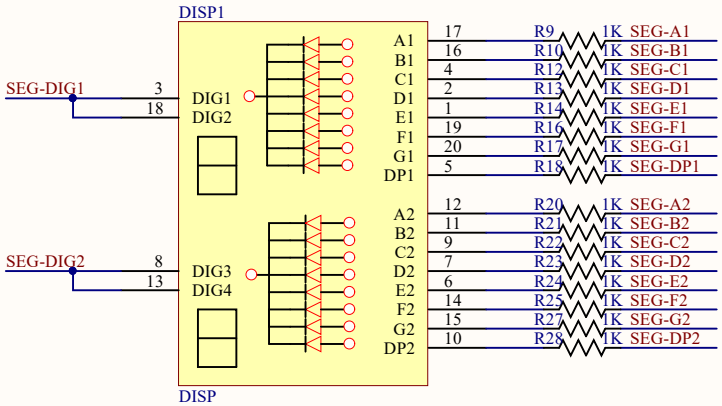
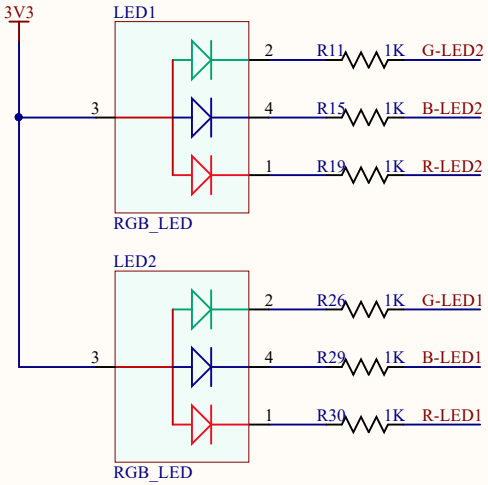
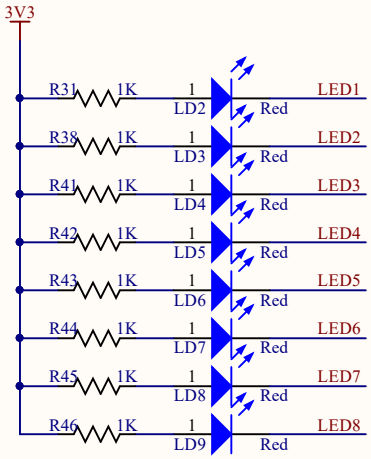
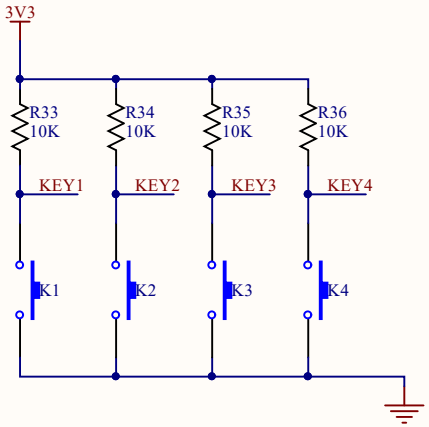
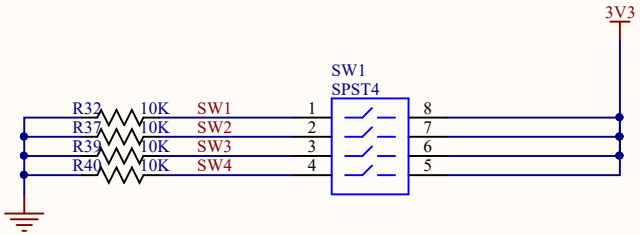

U1A
BANK 1A
DIFFIO_RX_L1n
DIFFIO_RX_L1p
DIFFIO_RX_L3n
DIFFIO_RX_L3p
DIFFIO_RX_L5n
DIFFIO_RX_L5p
DIFFIO_RX_L7n
DIFFIO_RX_L7p
D2 SEG-B1
C2 SEG-G2
F5 SEG-F1
G5 SEG-G1
C1 SEG-F2
B1 SEG-DIG2
E1 SEG-A1
E2 SEG-DIG1
3V3
BANK 1B
JTAGEN
DIFFIO_RX_L11n/TMS
VREFB1N0
DIFFIO_RX_L11p/TCK
DIFFIO_RX_L12n/TDI
DIFFIO_RX_L12p/TDO
DIFFIO_RX_L14n
DIFFIO_RX_L14p
DIFFIO_RX_L16n
DIFFIO_RX_L16p
G7 JTAGEN
G1 TMS
G2 SEG-E1
J1 TCK
H5 TDI
H4 TDO
H3
J2 SEG-D1
L1 SEG-DP1
K2 SEG-C1
R57 10K
BANK 2
DIFFIO_RX_L18n/CLK0n
DIFFIO_RX_L18p/CLK0p
DIFFIO_RX_L20n/CLK1n
DIFFIO_RX_L20p/CLK1p
DIFFIO_RX_L22n/DPCLK0
VREFB2N0
DIFFIO_RX_L22p/DPCLK1
DIFFIO_RX_L27n/PLL_L_CLKOUTn
DIFFIO_RX_L27p/PLL_L_CLKOUTp
J4
J5
K5
K4
L5
P1 SEG-D2
L4
R2 SEG-DP2
N1 SEG-E2
P2 SEG-C2
R4 33R CLK
MAX10M08SCM153C7G
U1C
BANK 5
DIFFIO_RX_R1p
DIFFIO_RX_R2p
DIFFIO_RX_R1n
DIFFIO_RX_R2n
DIFFIO_RX_R7p
DIFFIO_RX_R7n
VREFB5N0
DIFFIO_RX_R10p
DIFFIO_RX_R11p
DIFFIO_RX_R10n
DIFFIO_RX_R11n
M12 LED4
N15 LED1
L11 LED7
N14 LED2
K11 LED8
M14 LED3
K12 LED6
L15 LED5
J9 KEY1
K14 KEY2
J11 KEY3
J14 KEY4
BANK 6
DIFFIO_RX_R14p/CLK2p
DIFFIO_RX_R14n/CLK2n
DIFFIO_RX_R16p/CLK3p
DIFFIO_RX_R16n/CLK3n
DIFFIO_RX_R18p
DIFFIO_RX_R18n
DIFFIO_RX_R26p/DPCLK3
VREFB6N0
DIFFIO_RX_R26n/DPCLK2
DIFFIO_RX_R27p
DIFFIO_RX_R28p
DIFFIO_RX_R27n
DIFFIO_RX_R28n
DIFFIO_RX_R33p
DIFFIO_RX_R33n
J12 SW1
H11 SW2
H12 SW3
H13 SW4
J15
G15 R-LED1
G11
E15 G-LED1
G12
E14 B-LED1
F11
C15 R-LED2
F12
C14 G-LED2
E11
D12 B-LED2
MAX10M08SCM153C7G
U1B
BANK 3
DIFFIO_TX_RX_B1n
DIFFIO_RX_B2n
DIFFIO_TX_RX_B1p
DIFFIO_RX_B2p
DIFFIO_TX_RX_B3n
DIFFIO_RX_B4n
DIFFIO_TX_RX_B3p
DIFFIO_RX_B4p
DIFFIO_TX_RX_B5n
DIFFTO_RX_B6n
DIFFIO_TX_RX_B5p
DIFFTO_RX_B6p
DIFFIO_TX_RX_B7n
DIFFTO_RX_B8n
DIFFIO_TX_RX_B7p
DIFFIO_RX_B8p
DIFFIO_TX_RX_B9n
VREFB3N0
DIFFIO_TX_RX_B9p
DIFFIO_TX_RX_B10n
DIFFIO_TX_RX_B10p
DIFFIO_TX_RX_B12n
DIFFIO_TX_RX_B12p
DIFFIO_TX_RX_B14n
DIFFIO_TX_RX_B14p
DIFFIO_TX_RX_B16n
DIFFIO_TX_RX_B16p
M4 GPIO0
P3 GPIO1
M5 GPIO2
R3 GPIO3
L6 GPIO4
P4 GPIO5
L7 GPIO6
R5 GPIO7
P6 GPIO8
R7 GPIO9
P7 GPIO10
P8 GPIO11
L8
P9 GPIO12
M7
R9 GPIO13
M8
R11 GPIO14
N8
P12 GPIO15
R14 GPIO16
P15 GPIO17
L9
M9
L10
M11
P14
R13
MAX10M08SCM153C7G
U1D
BANK 8
DIFFIO_RX_T14p
DIFFIO_RX_T15p
DIFFIO_RX_T14n
DIFFIO_RX_T15n
DIFFIO_RX_T16p
DIFFIO_RX_T17p
DIFFIO_RX_T16n/DEV_CLRn
DIFFIO_RX_T17n
DIFFIO_RX_T18p/DEV_OE
DIFFIO_RX_T18n
VREFB8N0
CONFIG_SEL
DIFFIO_RX_T19p
nCONFIG
DIFFIO_RX_T19n
DIFFIO_RX_T20p
DIFFIO_RX_T21p
DIFFIO_RX_T20n
DIFFIO_RX_T21n
DIFFIO_RX_T22p
DIFFIO_RX_T23p
DIFFIO_RX_T22n/CRC_ERROR
DIFFIO_RX_T23n
DIFFIO_RX_T24p/nSTATUS
DIFFTO_RX_T24n/CONF_DONE
DIFFTO_RX_T26p
DIFFTO_RX_T26n
D11
B15 GPIO18
D10 GPIO26
B14 GPIO19
C8 GPIO28
B13 GPIO20
B8 GPIO27
A14 GPIO21
E10
E9
A13 GPIO23
D8 CONFIG_SEL
B12
E8
B11 GPIO22
B7 GPIO29
A9 GPIO25
B6 GPIO32
A11 GPIO24
D7 GPIO30
A7 GPIO33
E7 GPIO31
A5 GPIO34
D6
B4 GPIO35
E6
A2 SEG-B2
A3 SEG-A2
R5 10K
R6 1K
R7 1K
R8 1K
3V3
MAX10M08SCM153C7G
工程名称： STEP-MAX10 FPGA Board
图纸大小： A4
版本号： V2.0
制图：
日期： 2019/8/17
页码： 第 3 共 5
审核：
FPGA
STEP
www.stepfpga.com











工程名称： STEP-MAX10 FPGA Board			
图纸大小： A4	版本号： V2.0	制图：	
日期： 2019/8/17	页码： 第 4 共 5	审核：	
LEDs,Buttons,Switchs,RGB LEDs,Segments			

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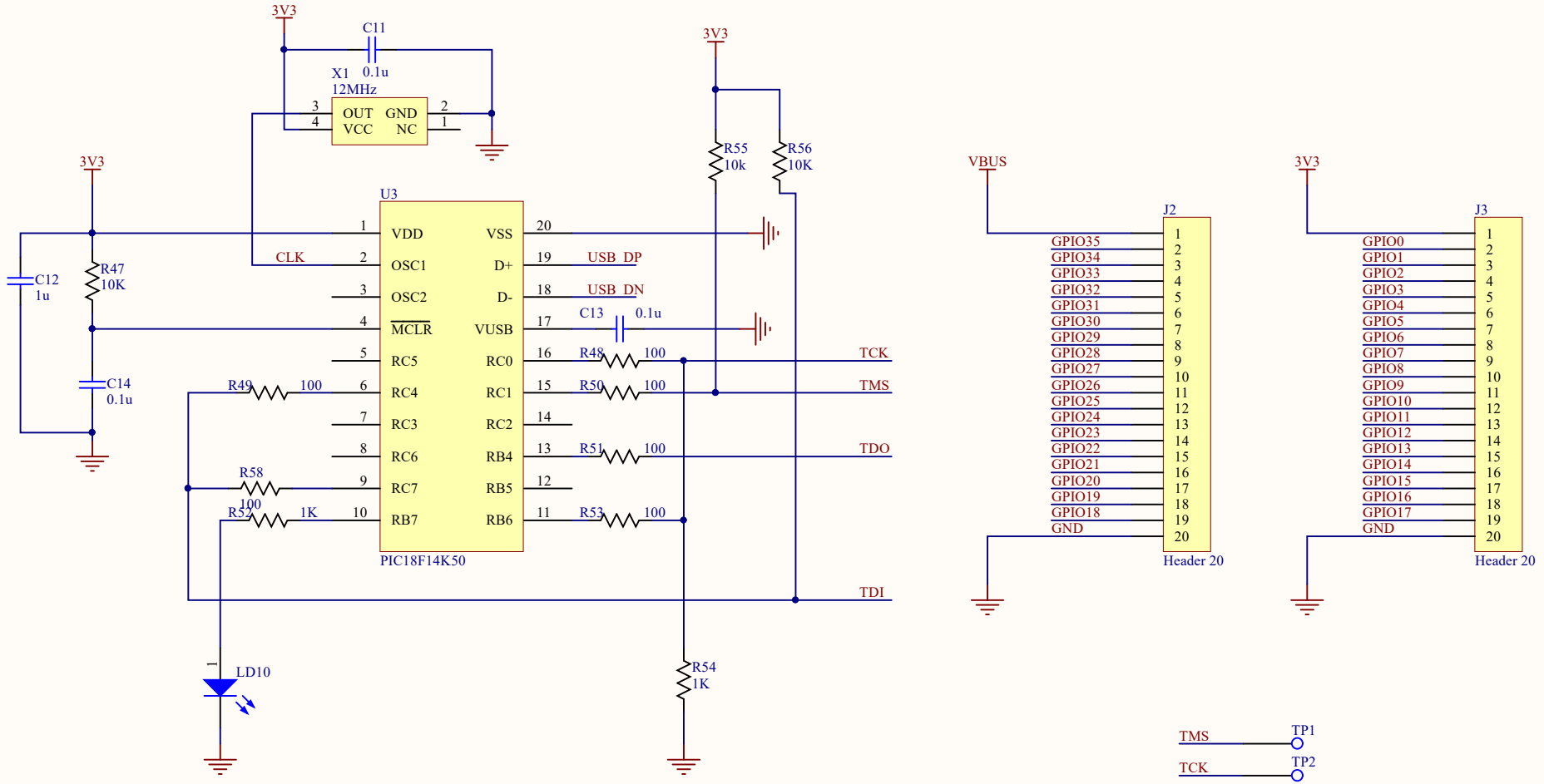

工程名称： STEP-MAX10 FPGA Board		
图纸大小： A4	版本号： V2.0	制图：
日期： 2019/8/17	页码： 第 5 共 5	审核：
Programmer,Connectors		

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