PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	TITLE, NOTE	21	RESET
2	Cyclone V ST SoC Bank 3	22	Cyclone V ST SoC POWER
3	Cyclone V ST SoC Bank 4	23	Cyclone V ST SoC GND
4	Cyclone V ST SoC Bank 5	24	Cyclone V ST SoC Decoupling
5	Cyclone V ST SoC Bank 6	25	LED & SW
6	Cyclone V ST SoC Bank 7	26	POWER LED
7	Cyclone V ST SoC Bank 8	27	Power_IN/FAN CON
8	Cyclone V ST SoC Transceiver	28	Power : 5.0V / 3.3V
9	CLK BLOCK	29	Power : 1.1V
10	Cyclone V ST SoC CONFIG	30	Power : 1.2V
11	DDR3 (FPGA)	31	Power : 2.5V
12	DDR3 (HPS)	32	Power : 3.3V
13	Gib ETH / EEPROM	33	Power : 1.5V for DDR_FPGA
14	SD CARD / QSPI FLASH	34	Power : 1.5V for DDR_HPS
15	USB_UART / RTC	35	Power : 1.2V for Gib ETH
16	HSMC POAT A	36	History
17	HSMC POAT B		
18	USB_2.0		
19	AUDIO		
20	DVI		

mPRESSION
The Solutions by Macnica Group

Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 1 of 36	

Cyclone V ST SoC Bank 3

IC4-2

CYCLONE V ST SoC BANK 3

Bank 3A = 2.5v
Bank 3B = 2.5v

HSMA

16	FPGA_HSMA_RX_D_p16	AB15	IO_3B_AB15/DIFFIO_RX_B27P/DQS4B	IO_3B_AK12/DIFFIO_TX_B36P	AK12	FPGA_HSMA_TX_D_p16	16
16	FPGA_HSMA_RX_D_n16	AC14	IO_3B_AC14/DIFFIO_RX_B27N/DQSN4B	IO_3B_AK13/DIFFIO_TX_B36N/DQ5B	AK13	FPGA_HSMA_TX_D_n16	16
16	FPGA_HSMA_RX_D_p15	AA13	IO_3B_AA13/DIFFIO_RX_B19P/DQS3B	IO_3B_AH10/DIFFIO_TX_B33P/DQ5B	AH10	FPGA_HSMA_TX_D_p15	16
16	FPGA_HSMA_RX_D_n15	AB13	IO_3B_AB13/DIFFIO_RX_B19N/DQSN3B	IO_3B_AJ10/DIFFIO_TX_B33N	AJ10	FPGA_HSMA_TX_D_n15	16
16	FPGA_HSMA_RX_D_p14	AD14	IO_3B_AD14/DIFFIO_RX_B23P	IO_3B_AJ9/DIFFIO_TX_B29P/DQ4B	AJ9	FPGA_HSMA_TX_D_p14	16
16	FPGA_HSMA_RX_D_n14	AE14	IO_3B_AE14/DIFFIO_RX_B23N	IO_3B_AK9/DIFFIO_TX_B29N/DQ4B	AK9	FPGA_HSMA_TX_D_n14	16
16	FPGA_HSMA_RX_D_p13	AE13	IO_3B_AE13/DIFFIO_RX_B22P/DQ3B	IO_3B_AH7/DIFFIO_TX_B32P/DQ4B	AH7	FPGA_HSMA_TX_D_p13	16
16	FPGA_HSMA_RX_D_n13	AF13	IO_3B_AF13/DIFFIO_RX_B22N/DQ3B	IO_3B_AH8/DIFFIO_TX_B32N/DQ4B	AH8	FPGA_HSMA_TX_D_n13	16
16	FPGA_HSMA_RX_D_p12	AG15	IO_3B_AG15/DIFFIO_RX_B38P/DQ5B	IO_3B_AJ6/DIFFIO_TX_B25P/DQ4B	AJ6	FPGA_HSMA_TX_D_p12	16
16	FPGA_HSMA_RX_D_n12	AH15	IO_3B_AH15/DIFFIO_RX_B38N/DQ5B	IO_3B_AJ7/DIFFIO_TX_B25N	AJ7	FPGA_HSMA_TX_D_n12	16
16	FPGA_HSMA_RX_D_p11	AF11	IO_3B_AF11/DIFFIO_RX_B18P/DQ3B	IO_3B_AK2/DIFFIO_TX_B20P	AK2	FPGA_HSMA_TX_D_p11	16
16	FPGA_HSMA_RX_D_n11	AG11	IO_3B_AG11/DIFFIO_RX_B18N/DQ3B	IO_3B_AK3/DIFFIO_TX_B20N/DQ3B	AK3	FPGA_HSMA_TX_D_n11	16
16	FPGA_HSMA_RX_D_p10	AJ11	IO_3B_AJ11/DIFFIO_RX_B34P/DQ5B	IO_3B_AJ4/DIFFIO_TX_B21P/DQ3B	AJ4	FPGA_HSMA_TX_D_p10	16
16	FPGA_HSMA_RX_D_n10	AK11	IO_3B_AK11/DIFFIO_RX_B34N/DQ5B	IO_3B_AK4/DIFFIO_TX_B21N/DQ3B	AK4	FPGA_HSMA_TX_D_n10	16
16	FPGA_HSMA_RX_D_p9	AH13	IO_3B_AH13/DIFFIO_RX_B30P/DQ4B	IO_3B_AJ5/DIFFIO_TX_B24P/DQ3B	AJ5	FPGA_HSMA_TX_D_p9	16
16	FPGA_HSMA_RX_D_n9	AH14	IO_3B_AH14/DIFFIO_RX_B30N/DQ4B	IO_3B_AK6/DIFFIO_TX_B24N/DQ3B	AK6	FPGA_HSMA_TX_D_n9	16
16	FPGA_HSMA_RX_D_p8	AG12	IO_3B_AG12/DIFFIO_RX_B26P/DQ4B	IO_3B_AK7/DIFFIO_TX_B28P	AK7	FPGA_HSMA_TX_D_p8	16
16	FPGA_HSMA_RX_D_n8	AG13	IO_3B_AG13/DIFFIO_RX_B26N/DQ4B	IO_3B_AK8/DIFFIO_TX_B28N/DQ4B	AK8	FPGA_HSMA_TX_D_n8	16
16	FPGA_HSMA_RX_D_p7	AD11	IO_3A_AD11/DATA8/DIFFIO_RX_B1P/DQ1B	IO_3A_AD9/DATA7/DIFFIO_TX_B2P/DQ1B	AD9	FPGA_HSMA_TX_D_p7	16
16	FPGA_HSMA_RX_D_n7	AE12	IO_3A_AE12/DATA6/DIFFIO_RX_B1N/DQ1B	IO_3A_AE9/DATA5/DIFFIO_TX_B2N	AE9	FPGA_HSMA_TX_D_n7	16
16	FPGA_HSMA_RX_D_p6	AC12	IO_3A_AC12/DIFFIO_RX_B15P	IO_3A_AG3/DATA15/DIFFIO_TX_B6P/DQ1B	AG3	FPGA_HSMA_TX_D_p6	16
16	FPGA_HSMA_RX_D_n6	AD12	IO_3A_AD12/DIFFIO_RX_B15N	IO_3A_AH4/DATA13/DIFFIO_TX_B6N/DQ1B	AH4	FPGA_HSMA_TX_D_n6	16
16	FPGA_HSMA_RX_D_p5	AA12	IO_3A_AA12/DIFFIO_RX_B11P/DQS2B	IO_3A_AG2/DIFFIO_TX_B16P/DQ2B	AG2	FPGA_HSMA_TX_D_p5	16
16	FPGA_HSMA_RX_D_n5	AB12	IO_3A_AB12/DIFFIO_RX_B11N/DQSN2B	IO_3A_AH3/DIFFIO_TX_B16N/DQ2B	AH3	FPGA_HSMA_TX_D_n5	16
16	FPGA_HSMA_RX_D_p4	AC9	IO_3A_AC9/DATA12/DIFFIO_RX_B3P/DQS1B	IO_3A_AG5/DIFFIO_TX_B13P/DQ2B	AG5	FPGA_HSMA_TX_D_p4	16
16	FPGA_HSMA_RX_D_n4	AD10	IO_3A_AD10/DATA10/DIFFIO_RX_B3N/DQSN1B	IO_3A_AH5/DIFFIO_TX_B13N/DQ2B	AH5	FPGA_HSMA_TX_D_n4	16
16	FPGA_HSMA_RX_D_p3	AD7	IO_3A_AD7/CLKUSR/DIFFIO_RX_B5P/DQ1B	IO_3A_AF6/DIFFIO_TX_B12P	AF6	FPGA_HSMA_TX_D_p3	16
16	FPGA_HSMA_RX_D_n3	AE7	IO_3A_AE7/DATA14/DIFFIO_RX_B5N/DQ1B	IO_3A_AG6/DIFFIO_TX_B12N/DQ2B	AG6	FPGA_HSMA_TX_D_n3	16
16	FPGA_HSMA_RX_D_p2	AF4	IO_3A_AF4/PR_ERROR/DIFFIO_RX_B7P	IO_3A_AF8/DIFFIO_TX_B9P/DQ2B	AF8	FPGA_HSMA_TX_D_p2	16
16	FPGA_HSMA_RX_D_n2	AF5	IO_3A_AF5/PR_DONE/DIFFIO_RX_B7N	IO_3A_AG7/DIFFIO_TX_B9N	AG7	FPGA_HSMA_TX_D_n2	16
16	FPGA_HSMA_RX_D_p1	AG1	IO_3A_AG1/DIFFIO_RX_B10P/DQ2B	IO_3A_AF9/DIFFIO_TX_B8P/DQ1B	AF9	FPGA_HSMA_TX_D_p1	16
16	FPGA_HSMA_RX_D_n1	AH2	IO_3A_AH2/DIFFIO_RX_B10N/DQ2B	IO_3A_AG8/PR_READY/DIFFIO_TX_B8N/DQ1B	AG8	FPGA_HSMA_TX_D_n1	16
16	FPGA_HSMA_RX_D_p0	AJ1	IO_3A_AJ1/DIFFIO_RX_B14P/DQ2B	IO_3A_AE11/DATA11/DIFFIO_TX_B4P	AE11	FPGA_HSMA_TX_D_p0	16
16	FPGA_HSMA_RX_D_n0	AJ2	IO_3A_AJ2/DIFFIO_RX_B14N/DQ2B	IO_3A_AF10/DATA9/DIFFIO_TX_B4N/DQ1B	AF10	FPGA_HSMA_TX_D_n0	16

HSMA

16	FPGA_HSMA_CLK_IN_p2	W15	IO_3B_W15/CLK1P/DIFFIO_RX_B39P	IO_3B_AH12/FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTP,FPLL_BL_FB/DIFFIO_TX_B37P/DQ5B	AH12	FPGA_HSMA_CLK_OUT_p2	16
16	FPGA_HSMA_CLK_IN_n2	Y16	IO_3B_Y16/CLK1N/DIFFIO_RX_B39N	IO_3B_AJ12/FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTN/DIFFIO_TX_B37N/DQ5B	AJ12	FPGA_HSMA_CLK_OUT_n2	16
16	FPGA_HSMA_CLK_IN_p1	AF14	IO_3B_AF14/CLK0P,FPLL_BL_FBP/DIFFIO_RX_B31P	IO_3B_AJ14/DIFFIO_TX_B40P/DQ5B	AJ14	FPGA_HSMA_CLK_OUT_p1	16
16	FPGA_HSMA_CLK_IN_n1	AF15	IO_3B_AF15/CLK0N,FPLL_BL_FBN/DIFFIO_RX_B31N	IO_3B_AK14/DIFFIO_TX_B40N/DQ5B	AK14	FPGA_HSMA_CLK_OUT_n1	16
				IO_3B_AG10/DIFFIO_TX_B17P/DQ3B	AG10	FPGA_HSMA_SCL	16
				IO_3B_AH9/DIFFIO_TX_B17N	AH9	FPGA_HSMA_SDA	16

FPGA_USER_IO

Bank 3B = 2.5v

25	FPGA_USER_DIP1	AA14	IO_3B_AA14/DIFFIO_RX_B35P/DQS5B

5CSTFD6D5F31I7

mPRESSION
The Solutions by Macnica Group

Title	Sodia		
Size A3	Document Number ASC001		Rev C
Date: Wednesday, November 21, 2018	Sheet 2 of 36		

Cyclone V ST SoC Bank 4

IC4-3

CYCLONE V ST SoC BANK 4

Bank 4A = 1.5v

FPGA_DDR3

11	FPGA_DDR3_x32_DQ31	AG18	IO_4A_AG18/DIFFIO_TX_B49P/DQ7B	IO_4A_AG22/DIFFIO_TX_B57P/DQ8B	AG22	FPGA_DDR3_x32_A12	11
11	FPGA_DDR3_x32_DQ30	AJ21	IO_4A_AJ21/DIFFIO_TX_B53N/DQ7B	IO_4A_AK24/DIFFIO_TX_B64N/DQ8B	AK24	FPGA_DDR3_x32_A11	11
11	FPGA_DDR3_x32_DQ29	AF19	IO_4A_AF19/DIFFIO_RX_B54P/DQ7B	IO_4A_AB21/DIFFIO_RX_B79N	AB21	FPGA_DDR3_x32_A10	11
11	FPGA_DDR3_x32_DQ28	AJ20	IO_4A_AJ20/DIFFIO_TX_B53P/DQ7B	IO_4A_AJ26/DIFFIO_TX_B68P	AJ26	FPGA_DDR3_x32_A9	11
11	FPGA_DDR3_x32_DQ27	AJ17	IO_4A_AJ17/DIFFIO_RX_B50P/DQ7B	IO_4A_AK29/DIFFIO_TX_B73N	AK29	FPGA_DDR3_x32_A8	11
11	FPGA_DDR3_x32_DQ26	AG23	IO_4A_AG23/DIFFIO_TX_B56P/DQ7B	IO_4A_AJ19/DIFFIO_TX_B52P	AJ19	FPGA_DDR3_x32_A7	11
11	FPGA_DDR3_x32_DQ25	AK18	IO_4A_AK18/DIFFIO_RX_B50N/DQ7B	IO_4A_AJ25/DIFFIO_TX_B65N	AJ25	FPGA_DDR3_x32_A6	11
11	FPGA_DDR3_x32_DQ24	AH24	IO_4A_AH24/DIFFIO_TX_B56N/DQ7B	IO_4A_AK21/DIFFIO_TX_B60P	AK21	FPGA_DDR3_x32_A5	11
11	FPGA_DDR3_x32_DQ23	AH17	IO_4A_AH17/DIFFIO_TX_B48P/DQ6B	IO_4A_AH23/DIFFIO_TX_B61P/DQ8B	AH23	FPGA_DDR3_x32_A4	11
11	FPGA_DDR3_x32_DQ22	AJ16	IO_4A_AJ16/DIFFIO_TX_B45P/DQ6B	IO_4A_AH22/DIFFIO_TX_B57N	AH22	FPGA_DDR3_x32_A3	11
11	FPGA_DDR3_x32_DQ21	AG21	IO_4A_AG21/DIFFIO_RX_B46P/DQ6B	IO_4A_AJ22/DIFFIO_TX_B61N/DQ8B	AJ22	FPGA_DDR3_x32_A2	11
11	FPGA_DDR3_x32_DQ20	AK16	IO_4A_AK16/DIFFIO_TX_B45N/DQ6B	IO_4A_AK23/DIFFIO_TX_B64P/DQ8B	AK23	FPGA_DDR3_x32_A1	11
11	FPGA_DDR3_x32_DQ19	AH18	IO_4A_AH18/DIFFIO_TX_B48N/DQ6B	IO_4A_AK22/DIFFIO_TX_B60N/DQ8B	AK22	FPGA_DDR3_x32_A0	11
11	FPGA_DDR3_x32_DQ18	AG16	IO_4A_AG16/DIFFIO_TX_B41P/DQ6B				
11	FPGA_DDR3_x32_DQ17	AH20	IO_4A_AH20/DIFFIO_RX_B46N/DQ6B				
11	FPGA_DDR3_x32_DQ16	AF16	IO_4A_AF16/DIFFIO_TX_B44N/DQ6B				
11	FPGA_DDR3_x32_DQ15	AJ24	IO_4A_AJ24/DIFFIO_TX_B65P/DQ9B	IO_4A_AG20/DIFFIO_RX_B54N/DQ7B	AG20	FPGA_DDR3_x32_BA2	11
11	FPGA_DDR3_x32_DQ14	AK27	IO_4A_AK27/DIFFIO_TX_B72N/DQ9B	IO_4A_AA21/DIFFIO_RX_B79P	AA21	FPGA_DDR3_x32_BA1	11
11	FPGA_DDR3_x32_DQ13	AE23	IO_4A_AE23/DIFFIO_RX_B70N/DQ9B	IO_4A_AE16/DIFFIO_TX_B44P	AE16	FPGA_DDR3_x32_BA0	11
11	FPGA_DDR3_x32_DQ12	AK26	IO_4A_AK26/DIFFIO_TX_B68N/DQ9B				
11	FPGA_DDR3_x32_DQ11	AF23	IO_4A_AF23/DIFFIO_RX_B66P/DQ9B	IO_4A_Y18/DIFFIO_RX_B63P	Y18	FPGA_DDR3_x32_CSn	11
11	FPGA_DDR3_x32_DQ10	AJ27	IO_4A_AJ27/DIFFIO_TX_B72P/DQ9B	IO_4A_AA19/DIFFIO_RX_B63N	AA19	FPGA_DDR3_x32_CASn	11
11	FPGA_DDR3_x32_DQ9	AG25	IO_4A_AG25/DIFFIO_TX_B69P/DQ9B	IO_4A_AD20/DIFFIO_RX_B74P/DQ10B	AD20	FPGA_DDR3_x32_RASn	11
11	FPGA_DDR3_x32_DQ8	AH25	IO_4A_AH25/DIFFIO_TX_B69N/DQ9B	IO_4A_AE17/DIFFIO_RX_B42P/DQ6B	AE17	FPGA_DDR3_x32_ODT	11
11	FPGA_DDR3_x32_DQ7	AD24	IO_4A_AD24/DIFFIO_TX_B80P/DQ10B	IO_4A_AH19/DIFFIO_TX_B49N	AH19	FPGA_DDR3_x32_WEn	11
11	FPGA_DDR3_x32_DQ6	AD21	IO_4A_AD21/DIFFIO_RX_B74N/DQ10B				
11	FPGA_DDR3_x32_DQ5	AK28	IO_4A_AK28/DIFFIO_TX_B73P/DQ10B	IO_4A_AK19/DIFFIO_TX_B52N/DQ7B	AK19	FPGA_DDR3_x32_DM3	11
11	FPGA_DDR3_x32_DQ4	AE24	IO_4A_AE24/DIFFIO_TX_B80N/DQ10B	IO_4A_AF18/DIFFIO_RX_B42N/DQ6B	AF18	FPGA_DDR3_x32_DM2	11
11	FPGA_DDR3_x32_DQ3	AH27	IO_4A_AH27/DIFFIO_TX_B76N/DQ10B	IO_4A_AE22/DIFFIO_RX_B70P/DQ9B	AE22	FPGA_DDR3_x32_DM1	11
11	FPGA_DDR3_x32_DQ2	AC22	IO_4A_AC22/DIFFIO_RX_B78P/DQ10B	IO_4A_AF26/DIFFIO_TX_B77N/DQ10B	AF26	FPGA_DDR3_x32_DM0	11
11	FPGA_DDR3_x32_DQ1	AF25	IO_4A_AF25/DIFFIO_TX_B77P/DQ10B				
11	FPGA_DDR3_x32_DQ0	AC23	IO_4A_AC23/DIFFIO_RX_B78N/DQ10B				

11	FPGA_DDR3_x32_DQS3	V17	IO_4A_V17/DIFFIO_RX_B51P/DQS7B	IO_4A_AF21/DIFFIO_RX_B62N/DQ8B	AF21	FPGA_DDR3_x32_CKE	11
11	FPGA_DDR3_x32_DQSn3	W17	IO_4A_W17/DIFFIO_RX_B51N/DQSN7B	IO_4A_V18/DIFFIO_RX_B71P	V18	FPGA_DDR3_x32_CK	11
				IO_4A_W19/DIFFIO_RX_B71N	W19	FPGA_DDR3_x32_CKn	11
11	FPGA_DDR3_x32_DQS2	V16	IO_4A_V16/DIFFIO_RX_B43P/DQS6B				
11	FPGA_DDR3_x32_DQSn2	W16	IO_4A_W16/DIFFIO_RX_B43N/DQSN6B				
11	FPGA_DDR3_x32_DQS1	AC20	IO_4A_AC20/DIFFIO_RX_B67P/DQS9B				
11	FPGA_DDR3_x32_DQSn1	AD19	IO_4A_AD19/DIFFIO_RX_B67N/DQSN9B				
11	FPGA_DDR3_x32_DQS0	Y19	IO_4A_Y19/DIFFIO_RX_B75P/DQS10B	IO_4A_AG26/DIFFIO_TX_B76P	AG26	FPGA_DDR3_x32_RESETn	11
11	FPGA_DDR3_x32_DQSn0	AA20	IO_4A_AA20/DIFFIO_RX_B75N/DQSN10B				
				IO_4A_AG17/RZQ_0/DIFFIO_TX_B41N	AG17		

R234
100/1%(1005)

FPGA_USER_IO

25	FPGA_USER_DIP0	AB17	IO_4A_AB17/CLK2N/DIFFIO_RX_B47N	
25	FPGA_USER_PB1	AF20	IO_4A_AF20/DIFFIO_RX_B62P/DQ8B	
25	FPGA_USER_PB0	AF24	IO_4A_AF24/DIFFIO_RX_B66N/DQ9B	
25	FPGA_USER_LED3	AE19	IO_4A_AE19/DIFFIO_RX_B58N/DQ8B	
25	FPGA_USER_LED2	AE18	IO_4A_AE18/DIFFIO_RX_B58P/DQ8B	
25	FPGA_USER_LED1	AA18	IO_4A_AA18/DIFFIO_RX_B59N/DQSN8B	
25	FPGA_USER_LED0	Y17	IO_4A_Y17/DIFFIO_RX_B59P/DQS8B	

CLK_IN

9	FPGA_CLKIN_DDR3_50M	AA16	IO_4A_AA16/CLK2P/DIFFIO_RX_B47P	
9	FPGA_CLKIN_100M	AC18	IO_4A_AC18/CLK3P/DIFFIO_RX_B55P	
		AD17	IO_4A_AD17/CLK3N/DIFFIO_RX_B55N	

R21
0(1005)

5CSTFD6D5F31I7

mPRESSION
The Solutions by Macnica Group

Title	Sodia		
Size A3	Document Number ASC001		Rev C
Date: Wednesday, November 21, 2018	Sheet 3 of 36		

Cyclone V ST SoC Bank 5

IC4-4

CYCLONE V ST SoC BANK 5

Bank 5A = 2.5v

FPGA_AUDIO

19	FPGA_AUDIO_BCLK	AB23	IO_5A_AB23/DIFFIO_RX_R8N/DQ1R
19	FPGA_AUDIO_DACDAT	AB22	IO_5A_AB22/DIFFIO_RX_R8P/DQ1R
19	FPGA_AUDIO_DACLRCK	Y21	IO_5A_Y21/DIFFIO_RX_R4N/DQ1R
19	FPGA_AUDIO_MCLK	W20	IO_5A_W20/DIFFIO_RX_R4P/DQ1R

HSMA

16	FPGA_HSMA_CLK_IN0	Y26	IO_5B_Y26/CLK4P,FPLL_BR_FBP/DIFFIO_RX_R23P/DQ3R
16	FPGA_HSMA_CLK_OUT0	AE29	IO_5B_AE29/FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTP,FPLL_BR_FB/DIFFIO_TX_R22P
16	FPGA_HSMA_D3	AG30	IO_5A_AG30/DIFFIO_TX_R16N
16	FPGA_HSMA_D2	W22	IO_5A_W22/NPERSTL1/DIFFIO_RX_R6N/DQSN1R
16	FPGA_HSMA_D1	AE27	IO_5A_AE27/DIFFIO_TX_R10P/DQ2R
16	FPGA_HSMA_D0	AH30	IO_5A_AH30/DIFFIO_TX_R16P/DQ2R

Bank 5B = 2.5v

CLK_IN

9	FPGA_CLKIN_27M	R20 0(1005)	AA26	IO_5B_AA26/CLK5P/DIFFIO_RX_R21P/DQS3R
			AB27	IO_5B_AB27/CLK5N/DIFFIO_RX_R21N/DQSN3R

HSMB

17	FPGA_HSMB_CLK_IN0	Y27	IO_5B_Y27/CLK4N,FPLL_BR_FBN/DIFFIO_RX_R23N/DQ3R
17	FPGA_HSMB_D3	AA25	IO_5A_AA25/DIFFIO_TX_R7P/DQ1R
17	FPGA_HSMB_D2	W21	IO_5A_W21/NPERSTL0/DIFFIO_RX_R6P/DQS1R
17	FPGA_HSMB_D1	AE28	IO_5A_AE28/DIFFIO_TX_R10N/DQ2R
17	FPGA_HSMB_D0	AF28	IO_5A_AF28/DIFFIO_TX_R12N/DQ2R

5CSTFD6D5F31I7

AA24	IO_5A_AA24/DIFFIO_RX_R9P	FPGA_DVI_DATA23	20
Y23	IO_5A_Y23/DIFFIO_RX_R11P/DQ2R	FPGA_DVI_DATA22	20
Y24	IO_5A_Y24/DIFFIO_RX_R11N/DQ2R	FPGA_DVI_DATA21	20
AD26	IO_5A_AD26/DIFFIO_RX_R15P/DQ2R	FPGA_DVI_DATA20	20
AC27	IO_5A_AC27/DIFFIO_RX_R15N/DQ2R	FPGA_DVI_DATA19	20
AH28	IO_5A_AH28/PR_REQUEST/DIFFIO_TX_R1N/DQ1R	FPGA_DVI_DATA18	20
AH29	IO_5A_AH29/CVP_CONFDONE/DIFFIO_TX_R3N/DQ1R	FPGA_DVI_DATA17	20
AJ29	IO_5A_AJ29/NCEO/DIFFIO_TX_R3P/DQ1R	FPGA_DVI_DATA16	20
AE26	IO_5A_AE26/DEV_OE/DIFFIO_TX_R5P	FPGA_DVI_DATA15	20
AG27	IO_5A_AG27/RZQ_1/DIFFIO_TX_R1P/DQ1R	FPGA_DVI_DATA14	20
AF30	IO_5A_AF30/DIFFIO_TX_R14N/DQ2R	FPGA_DVI_DATA13	20
AF29	IO_5A_AF29/DIFFIO_TX_R14P	FPGA_DVI_DATA12	20
AB26	IO_5A_AB26/DIFFIO_TX_R7N	FPGA_DVI_DATA11	20
AG28	IO_5A_AG28/DIFFIO_TX_R12P/DQ2R	FPGA_DVI_DATA10	20
AC25	IO_5A_AC25/CRC_ERROR/DIFFIO_RX_R2N	FPGA_DVI_DATA9	20
W24	IO_5A_W24/DIFFIO_RX_R13N/DQSN2R	FPGA_DVI_DE	20
AB25	IO_5A_AB25/DIFFIO_RX_R9N	FPGA_DVI_HS	20
V23	IO_5A_V23/DIFFIO_RX_R13P/DQS2R	FPGA_DVI_VS	20

V25	IO_5B_V25/DIFFIO_RX_R17N	FPGA_DVI_DATA8	20
AB30	IO_5B_AB30/DIFFIO_RX_R19P/DQ3R	FPGA_DVI_DATA7	20
W25	IO_5B_W25/DIFFIO_RX_R17P	FPGA_DVI_DATA6	20
AA30	IO_5B_AA30/DIFFIO_RX_R19N/DQ3R	FPGA_DVI_DATA5	20
AC30	IO_5B_AC30/RZQ_2/DIFFIO_TX_R24N	FPGA_DVI_DATA4	20
AB28	IO_5B_AB28/DIFFIO_TX_R20P/DQ3R	FPGA_DVI_DATA3	20
AD29	IO_5B_AD29/FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTN/DIFFIO_TX_R22N/DQ3R	FPGA_DVI_DATA2	20
AD30	IO_5B_AD30/DIFFIO_TX_R24P/DQ3R	FPGA_DVI_DATA1	20
AA28	IO_5B_AA28/DIFFIO_TX_R20N/DQ3R	FPGA_DVI_DATA0	20
AC29	IO_5B_AC29/DIFFIO_TX_R18N/DQ3R	FPGA_DVI_CLK	20
AC28	IO_5B_AC28/DIFFIO_TX_R18P/DQ3R	FPGA_DVI_RESETn	20

FPGA_DVI

mPRESSION The Solutions by Macnica Group

Title	Sodia		
Size A3	Document Number ASC001		Rev C
Date: Wednesday, November 21, 2018	Sheet 4 of 36		

Cyclone V ST SoC Bank 6

HPS_DDR3

IC4-5

CYCLONE V ST SoC BANK 6

Bank 6A = 1.5v
Bank 6B = 1.5v

12	HPS_DDR3_x32_DQ39	Y29	HPS_DDR_6B_Y29		
12	HPS_DDR3_x32_DQ38	V27	HPS_DDR_6B_V27		
12	HPS_DDR3_x32_DQ37	U25	HPS_DDR_6B_U25		
12	HPS_DDR3_x32_DQ36	T25	HPS_DDR_6B_T25		
12	HPS_DDR3_x32_DQ35	V28	HPS_DDR_6B_V28		
12	HPS_DDR3_x32_DQ34	U27	HPS_DDR_6B_U27		
12	HPS_DDR3_x32_DQ33	R24	HPS_DDR_6B_R24		
12	HPS_DDR3_x32_DQ32	W26	HPS_DDR_6B_W26		
12	HPS_DDR3_x32_DQ31	W29	HPS_DDR_6B_W29		
12	HPS_DDR3_x32_DQ30	V30	HPS_DDR_6B_V30		
12	HPS_DDR3_x32_DQ29	R26	HPS_DDR_6B_R26		
12	HPS_DDR3_x32_DQ28	R27	HPS_DDR_6B_R27		
12	HPS_DDR3_x32_DQ27	T28	HPS_DDR_6B_T28		
12	HPS_DDR3_x32_DQ26	T29	HPS_DDR_6B_T29		
12	HPS_DDR3_x32_DQ25	P25	HPS_DDR_6B_P25		
12	HPS_DDR3_x32_DQ24	P24	HPS_DDR_6B_P24		
12	HPS_DDR3_x32_DQ23	R29	HPS_DDR_6B_R29		
12	HPS_DDR3_x32_DQ22	N27	HPS_DDR_6B_N27		
12	HPS_DDR3_x32_DQ21	P27	HPS_DDR_6B_P27		
12	HPS_DDR3_x32_DQ20	P26	HPS_DDR_6B_P26		
12	HPS_DDR3_x32_DQ19	N28	HPS_DDR_6B_N28		
12	HPS_DDR3_x32_DQ18	N29	HPS_DDR_6B_N29		
12	HPS_DDR3_x32_DQ17	T26	HPS_DDR_6B_T26		
12	HPS_DDR3_x32_DQ16	U26	HPS_DDR_6B_U26		
12	HPS_DDR3_x32_DQ15	M30	HPS_DDR_6A_M30		
12	HPS_DDR3_x32_DQ14	L28	HPS_DDR_6A_L28		
12	HPS_DDR3_x32_DQ13	M27	HPS_DDR_6A_M27		
12	HPS_DDR3_x32_DQ12	M26	HPS_DDR_6A_M26		
12	HPS_DDR3_x32_DQ11	K27	HPS_DDR_6A_K27		
12	HPS_DDR3_x32_DQ10	K29	HPS_DDR_6A_K29		
12	HPS_DDR3_x32_DQ9	L26	HPS_DDR_6A_L26		
12	HPS_DDR3_x32_DQ8	K26	HPS_DDR_6A_K26		
12	HPS_DDR3_x32_DQ7	J29	HPS_DDR_6A_J29		
12	HPS_DDR3_x32_DQ6	J30	HPS_DDR_6A_J30		
12	HPS_DDR3_x32_DQ5	L24	HPS_DDR_6A_L24		
12	HPS_DDR3_x32_DQ4	L25	HPS_DDR_6A_L25		
12	HPS_DDR3_x32_DQ3	G28	HPS_DDR_6A_G28		
12	HPS_DDR3_x32_DQ2	H30	HPS_DDR_6A_H30		
12	HPS_DDR3_x32_DQ1	K22	HPS_DDR_6A_K22		
12	HPS_DDR3_x32_DQ0	K23	HPS_DDR_6A_K23		
12	HPS_DDR3_x32_DQS4	T24	HPS_DDR_6B_T24		
12	HPS_DDR3_x32_DQSn4	T23	HPS_DDR_6B_T23		
12	HPS_DDR3_x32_DQS3	R22	HPS_DDR_6B_R22		
12	HPS_DDR3_x32_DQSn3	R21	HPS_DDR_6B_R21		
12	HPS_DDR3_x32_DQS2	R19	HPS_DDR_6B_R19		
12	HPS_DDR3_x32_DQSn2	R18	HPS_DDR_6B_R18		
12	HPS_DDR3_x32_DQS1	N25	HPS_DDR_6A_N25		
12	HPS_DDR3_x32_DQSn1	N24	HPS_DDR_6A_N24		
12	HPS_DDR3_x32_DQS0	N18	HPS_DDR_6A_N18		
12	HPS_DDR3_x32_DQSn0	M19	HPS_DDR_6A_M19		
		K21	HPS_DDR_6A_K21		
		G25	HPS_DDR_6A_G25		
		H29	HPS_DDR_6A_H29		
		L30	HPS_DDR_6A_L30		
		M25	HPS_GPI0_6A_M25		
		J26	HPS_GPI1_6A_J26		
		N23	HPS_GPI2_6A_N23		
		M22	HPS_GPI3_6A_M22		

Bank 6B = 1.5v

		Y28	HPS_GPI13_6B_Y28		
		V29	HPS_GPI12_6B_V29		
		U20	HPS_GPI11_6B_U20		
		T21	HPS_GPI10_6B_T21		
		U28	HPS_GPI9_6B_U28		
		T30	HPS_GPI8_6B_T30		
		V20	HPS_GPI7_6B_V20		
		P22	HPS_GPI6_6B_P22		
		P29	HPS_GPI5_6B_P29		
		N30	HPS_GPI4_6B_N30		

5CSTFD6D5F31I7

			HPS_DDR_6A_H25	H25	
			HPS_DDR_6A_C29	C29	
			HPS_DDR_6A_B30	B30	
			HPS_DDR_6A_C30	C30	
			HPS_DDR_6A_D29	D29	
			HPS_DDR_6A_G26	G26	
			HPS_DDR_6A_H27	H27	
			HPS_DDR_6A_E28	E28	
			HPS_DDR_6A_F29	F29	
			HPS_DDR_6A_J27	J27	
			HPS_DDR_6A_J25	J25	
			HPS_DDR_6A_F30	F30	
			HPS_DDR_6A_F28	F28	
			HPS_DDR_6A_G30	G30	
			HPS_DDR_6A_F26	F26	
HPS_DDR3_x32_A14	12				
HPS_DDR3_x32_A13	12				
HPS_DDR3_x32_A12	12				
HPS_DDR3_x32_A11	12				
HPS_DDR3_x32_A10	12				
HPS_DDR3_x32_A9	12				
HPS_DDR3_x32_A8	12				
HPS_DDR3_x32_A7	12				
HPS_DDR3_x32_A6	12				
HPS_DDR3_x32_A5	12				
HPS_DDR3_x32_A4	12				
HPS_DDR3_x32_A3	12				
HPS_DDR3_x32_A2	12				
HPS_DDR3_x32_A1	12				
HPS_DDR3_x32_A0	12				
			HPS_DDR_6A_J23	J23	
			HPS_DDR_6A_J24	J24	
			HPS_DDR_6A_E29	E29	
HPS_DDR3_x32_BA2	12				
HPS_DDR3_x32_BA1	12				
HPS_DDR3_x32_BA0	12				
			HPS_DDR_6A_H24	H24	
			HPS_DDR_6A_E27	E27	
			HPS_DDR_6A_D30	D30	
			HPS_DDR_6A_H28	H28	
			HPS_DDR_6A_C28	C28	
HPS_DDR3_x32_CSn	12				
HPS_DDR3_x32_CASn	12				
HPS_DDR3_x32_RASn	12				
HPS_DDR3_x32_ODT	12				
HPS_DDR3_x32_WEn	12				
			HPS_DDR_6B_W27	W27	
			HPS_DDR_6B_W30	W30	
			HPS_DDR_6B_R28	R28	
			HPS_DDR_6A_M28	M28	
			HPS_DDR_6A_K28	K28	
HPS_DDR3_x32_DM4	12				
HPS_DDR3_x32_DM3	12				
HPS_DDR3_x32_DM2	12				
HPS_DDR3_x32_DM1	12				
HPS_DDR3_x32_DM0	12				
			HPS_DDR_6A_L29	L29	
			HPS_DDR_6A_M23	M23	
			HPS_DDR_6A_L23	L23	
HPS_DDR3_x32_CKE	12				
HPS_DDR3_x32_CK	12				
HPS_DDR3_x32_CKn	12				
			HPS_DDR_6B_P30	P30	
HPS_DDR3_x32_RESETn	12				
			HPS_RZQ_0_6A_D27	D27	

R211
100/1%(1005)

HPS_DDR3

S13
SKQMASE010
HPS PB3

S12
SKQMASE010
HPS PB2

S11
SKQMASE010
HPS PB1

S10
SKQMASE010
HPS PB0

DDR_1p5v_HPS

R242 10k(1005)
R239 10k(1005)
R240 10k(1005)
R241 10k(1005)

DDR_1p5v_HPS

R237 10k(1005)
R183 10k(1005)
R236 10k(1005)
R238 10k(1005)

HPS DIP

S9

TDA04H0SB1

mPRESSION
The Solutions by Macnica Group

Title	Sodia		
Size A3	Document Number ASC001		Rev C
Date: Wednesday, November 21, 2018	Sheet 5 of 36		

Cyclone V ST SoC Bank 7

i2c 2pin hader

J15
XG8S-0231

19,6,9 HPS_I2C1_SCL
19,6,9 HPS_I2C1_SDA

3p3v 3p3v

4.7k(1005) 4.7k(1005) 4.7k(1005) 4.7k(1005)
R33 R34 R35 R36

IC4-6

CYCLONE V ST SoC BANK 7

HPS_I2C

13,15 HPS_I2C0_SCL — D22 — I2C0_SCL_7A_D22/UART1_TX/SPIM1_MOSI/HPS_GPIO64
13,15 HPS_I2C0_SDA — C23 — I2C0_SDA_7A_C23/UART1_RX/SPIM1_CLK/HPS_GIPO63
19,6,9 HPS_I2C1_SCL — C22 — SPIM0_MOSI_7A_C22/I2C1_SCL/UART0_RTS/HPS_GPIO58
19,6,9 HPS_I2C1_SDA — A23 — SPIM0_CLK_7A_A23/I2C1_SDA/UART0_CTS/HPS_GPIO57

HPS_CLKIN

9 HPS_CLKIN1_25M — D25 — HPS_CLK1_7A_D25
9 HPS_CLKIN2_25M — F25 — HPS_CLK2_7A_F25

Bank 7A = 3.3v

B23 SPIM0_MISO_7A_B23/CAN1_RX/UART1_CTS/HPS_GPIO59
E23 TRACE_D7_7A_E23/SPIS1_MISO/I2C0_SCL/HPS_GPIO56
C24 TRACE_D6_7A_C24/SPIS1_SS0/I2C0_SDA/HPS_GPIO55
G21 TRACE_D5_7A_G21/SPIS1_MOSI/CAN1_TX/HPS_GPIO54
A24 TRACE_D4_7A_A24/SPIS1_CLK/CAN1_RX/HPS_GPIO53
H23 TRACE_D3_7A_H23/SPIS0_SS0/I2C1_SCL/HPS_GPIO52
A25 TRACE_D2_7A_A25/SPIS0_MISO/I2C1_SDA/HPS_GPIO51
C25 TRACE_D1_7A_C25/SPIS0_MOSI/UART0_TX/HPS_GPIO50
B25 TRACE_D0_7A_B25/SPIS0_CLK/UART0_RX/HPS_GPIO49
B26 TRACE_CLK_7A_B26

boot_sel0 — H20 — SPIM0_SS0,BOOTSEL0_7A_H20/CAN1_TX/UART1_RTS/HPS_GPIO60
boot_sel2 — D20 — NAND_WE,BOOTSEL2_7B_D20/QSPI_SS1/HPS_GPIO28

Bank 7B = 3.3v

Bank 7C = 3.3v

Bank 7D = 3.3v

5CSTFD6D5F31I7

XJ2 XJ8A-0211 BOOTSEL[0]
VCCHPS_3p3v
1 R23 10k(1005)
2
3 R24 1k(1005)
boot_sel0
J2 XG8S-0331

XJ3 XJ8A-0211 BOOTSEL[1]
VCCHPS_3p3v
1 R25 10k(1005)
2
3 R26 1k(1005)
HPS_QSPI_SS
J3 XG8S-0331

XJ4 XJ8A-0211 BOOTSEL[2]
VCCHPS_3p3v
1 R27 10k(1005)
2
3 R28 1k(1005)
boot_sel2
J4 XG8S-0331

VCCHPS_3p3v
R29 10k(1005)
HPS_UART_TX
1 2 3
J5 XG8S-0331
R30 1k(1005)
CLKSEL[0]

VCCHPS_3p3v
R31 10k(1005)
clk_sel1
1 2 3
J6 XG8S-0331
R32 1k(1005)
CLKSEL[1]

XJ5 XJ8A-0211
XJ6 XJ8A-0211

HPS_QSPI

14 HPS_QSPI_CLK — D19 — QSPI_CLK_7B_D19/HPS_GPIO34
14 HPS_QSPI_SS — A18 — QSPI_SS0,BOOTSEL1_7B_A18/HPS_GPIO33
14 HPS_QSPI_IO3 — E19 — QSPI_IO3_7B_E19/USB1_NXT/HPS_GPIO32
14 HPS_QSPI_IO2 — A19 — QSPI_IO2_7B_A19/USB1_DIR/HPS_GPIO31
14 HPS_QSPI_IO1 — H18 — QSPI_IO1_7B_H18/USB1_STP/HPS_GPIO30
14 HPS_QSPI_IO0 — C20 — QSPI_IO0_7B_C20/USB1_CLK/HPS_GPIO29

HPS_USER_IO

25 HPS_USER_LED3 — C18 — SDMMC_D5_7C_C18/USB0_D5/HPS_GPIO41
25 HPS_USER_LED2 — G17 — SDMMC_D6_7C_G17/USB0_D6/HPS_GPIO42
25 HPS_USER_LED1 — E18 — SDMMC_D7_7C_E18/USB0_D7/HPS_GPIO43
25 HPS_USER_LED0 — E17 — SDMMC_FB_CLK_IN_7C_E17/USB0_CLK/HPS_GPIO44

HPS_UART

E24 HPS_UART_RX — 15
D24 HPS_UART_TX — 15
CAN0_RX_7A_E24/UART0_RX/SPIM1_MISO/HPS_GPIO65
CAN0_TX,CLKSEL0_7A_D24/UART0_TX/SPIM1_SS0/HPS_GPIO66
G22 clk_sel1
B22
UART0_TX,CLKSEL1_7A_G22/CAN0_TX/SPIM1_SS1/HPS_GPIO62
UART0_RX_7A_B22/CAN0_RX/SPIM0_SS1/HPS_GPIO61

HPS_JTAG

H22 HPS_TCK — 10
B28 HPS_TDO — 10
B27 HPS_TDI — 10
A29 HPS_TMS — 10
HPS_TCK_7A_H22
HPS_TDO_7A_B28
HPS_TDI_7A_B27
HPS_TMS_7A_A29

HPS_RST

C27 HPS_nRST — 10,21
F23 HPS_RESETn — 21
A28 JTAG_TRST — 10
F24 R273 0(1005) VCCHPS_3p3v
HPS_NRST_7A_C27
HPS_NPOR_7A_F23
HPS_TRST_7A_A28
HPS_PORSEL_7A_F24

HPS_ENET

H19 HPS_ENET_GTX_CLK — 13
C19 HPS_ENET_INTn — 13
NAND_ALE_7B_H19/RGMII1_TX_CLK/QSPI_SS3/HPS_GPIO14
QSPI_SS1_7B_C19/HPS_GPIO35
B21 HPS_ENET_MDC — 13
E21 HPS_ENET_MDIO — 13
NAND_DQ2_7B_B21/RGMII1_MDC/I2C3_SCL/HPS_GPIO21
NAND_DQ1_7B_E21/RGMII1_MDIO/I2C3_SDA/HPS_GPIO20
G20 HPS_ENET_RX_CLK — 13
K17 HPS_ENET_RX_DV — 13
NAND_DQ5_7B_G20/RGMII1_RX_CLK/USB1_D6/HPS_GPIO24
NAND_DQ3_7B_K17/RGMII1_RX_CTL/USB1_D4/HPS_GPIO22
D21 HPS_ENET_RX_D3 — 13
B18 HPS_ENET_RX_D2 — 13
B20 HPS_ENET_RX_D1 — 13
A21 HPS_ENET_RX_D0 — 13
NAND_WP_7B_D21/RGMII1_RXD3/QSPI_SS2/HPS_GPIO27
NAND_DQ7_7B_B18/RGMII1_RXD2/HPS_GPIO26
NAND_DQ6_7B_B20/RGMII1_RXD1/USB1_D7/HPS_GPIO25
NAND_DQ0_7B_A21/RGMII1_RXD0/HPS_GPIO19
A20 HPS_ENET_TX_EN — 13
NAND_DQ4_7B_A20/RGMII1_TX_CTL/USB1_D5/HPS_GPIO23
F19 HPS_ENET_TX_D3 — 13
F21 HPS_ENET_TX_D2 — 13
J19 HPS_ENET_TX_D1 — 13
F20 HPS_ENET_TX_D0 — 13
NAND_RB_7B_F19/RGMII1_TXD3/USB1_D3/HPS_GPIO18
NAND_RE_7B_F21/RGMII1_TXD2/USB1_D2/HPS_GPIO17
NAND_CLE_7B_J19/RGMII1_TXD1/USB1_D1/HPS_GPIO16
NAND_CE_7B_F20/RGMII1_TXD0/USB1_D0/HPS_GPIO15

HPS_SD_CARD

A16 HPS_SDIO_CLK — 14
F18 HPS_SDIO_CMD — 14
SDMMC_CCLK_OUT_7C_A16/USB0_STP/HPS_GPIO45
SDMMC_CMD_7C_F18/USB0_D0/HPS_GPIO36
B17
H17
B16 HPS_SDIO_D3 — 14
D17 HPS_SDIO_D2 — 14
C17 HPS_SDIO_D1 — 14
G18 HPS_SDIO_D0 — 14
SDMMC_PWREN_7C_B17/USB0_D1/HPS_GPIO37
SDMMC_D4_7C_H17/USB0_D4/HPS_GPIO40
SDMMC_D3_7C_B16/USB0_NXT/HPS_GPIO47
SDMMC_D2_7C_D17/USB0_DIR/HPS_GPIO46
SDMMC_D1_7C_C17/USB0_D3/HPS_GPIO39
SDMMC_D0_7C_G18/USB0_D2/HPS_GPIO38

HPS_USB2.0

N16 HPS_ULPI_CLK — 18
E14 HPS_ULPI_DIR — 18
A14 HPS_ULPI_NXT — 18
C15 HPS_ULPI_STP — 18
RGMII0_RX_CLK_7D_N16/USB1_CLK/HPS_GPIO10
RGMII0_RXD2_7D_E14/USB1_DIR/HPS_GPIO12
RGMII0_RXD3_7D_A14/USB1_NXT/HPS_GPIO13
RGMII0_RXD1_7D_C15/USB1_STP/HPS_GPIO11
M17 HPS_ULPI_D7 — 18
D15 HPS_ULPI_D6 — 18
C14 HPS_ULPI_D5 — 18
A15 HPS_ULPI_D4 — 18
D14 HPS_ULPI_D3 — 18
D16 HPS_ULPI_D2 — 18
G16 HPS_ULPI_D1 — 18
E16 HPS_ULPI_D0 — 18
RGMII0_RX_CTL_7D_M17/USB1_D7/HPS_GPIO8
RGMII0_MDC _7D_D15/USB1_D6/I2C2_SCL/HPS_GPIO7
RGMII0_MDIO_7D_C14/USB1_D5/I2C2_SDA/HPS_GPIO6
RGMII0_RXD0_7D_A15/USB1_D4/HPS_GPIO5
RGMII0_TXD3_7D_D14/USB1_D3/HPS_GPIO4
RGMII0_TXD2_7D_D16/USB1_D2/HPS_GPIO3
RGMII0_TXD1_7D_G16/USB1_D1/HPS_GPIO2
RGMII0_TXD0_7D_E16/USB1_D0/HPS_GPIO1
F16
B15
RGMII0_TX_CLK_7D_F16/HPS_GPIO0
RGMII0_TX_CTL_7D_B15/HPS_GPIO9

CLKSEL [1:0]	OSC1 CLK range	Note
0x0	10–50MHz	default
0x1	10–12.5MHz	
0x2	12.5–25MHz	
0x3	25–50MHz	

BOOTSEL [2:0]	Boot Flash device	Note
0x1	FPGA (HPS-to-FPGA bridge)	
0x5	3.3 V SD/MMC flash memory with internal transceiver	default
0x7	3.3 V SPI or quad SPI flash memory	

mPRESSION The Solutions by Macnica Group

Title: Sodia
Size: A3
Document Number: ASC001
Rev: C
Date: Wednesday, November 21, 2018
Sheet 6 of 36

Cyclone V ST SoC Bank 8

IC4-7

CYCLONE V ST SoC BANK 8

Bank 8A = 2.5v

HSMB

17	FPGA_HSMB_RX_D_p16	F15	IO_8A_F15/DIFFIO_RX_T5P/DQS1T		IO_8A_C10/DIFFIO_TX_T14P	C10	FPGA_HSMB_TX_D_p16	17
17	FPGA_HSMB_RX_D_n16	F14	IO_8A_F14/DIFFIO_RX_T5N/DQSN1T		IO_8A_C9/DIFFIO_TX_T14N/DQ2T	C9	FPGA_HSMB_TX_D_n16	17
17	FPGA_HSMB_RX_D_p15	H13	IO_8A_H13/DIFFIO_RX_T21P/DQS3T		IO_8A_C8/DIFFIO_TX_T12P/DQ2T	C8	FPGA_HSMB_TX_D_p15	17
17	FPGA_HSMB_RX_D_n15	H12	IO_8A_H12/DIFFIO_RX_T21N/DQSN3T		IO_8A_B8/DIFFIO_TX_T12N/DQ2T	B8	FPGA_HSMB_TX_D_n15	17
17	FPGA_HSMB_RX_D_p14	C13	IO_8A_C13/DIFFIO_RX_T3P/DQ1T		IO_8A_C7/DIFFIO_TX_T10P/DQ2T	C7	FPGA_HSMB_TX_D_p14	17
17	FPGA_HSMB_RX_D_n14	B12	IO_8A_B12/DIFFIO_RX_T3N/DQ1T		IO_8A_B7/DIFFIO_TX_T10N/DQ2T	B7	FPGA_HSMB_TX_D_n14	17
17	FPGA_HSMB_RX_D_p13	E12	IO_8A_E12/DIFFIO_RX_T19P/DQ3T		IO_8A_E8/DIFFIO_TX_T24P/DQ3T	E8	FPGA_HSMB_TX_D_p13	17
17	FPGA_HSMB_RX_D_n13	D12	IO_8A_D12/DIFFIO_RX_T19N/DQ3T		IO_8A_D7/DIFFIO_TX_T24N	D7	FPGA_HSMB_TX_D_n13	17
17	FPGA_HSMB_RX_D_p12	F11	IO_8A_F11/DIFFIO_RX_T23P/DQ3T		IO_8A_E7/DIFFIO_TX_T38P	E7	FPGA_HSMB_TX_D_p12	17
17	FPGA_HSMB_RX_D_n12	E11	IO_8A_E11/DIFFIO_RX_T23N/DQ3T		IO_8A_E6/DIFFIO_TX_T38N/DQ5T	E6	FPGA_HSMB_TX_D_n12	17
17	FPGA_HSMB_RX_D_p11	J10	IO_8A_J10/DIFFIO_RX_T37P/DQS5T		IO_8A_G7/DIFFIO_TX_T40P/DQ5T	G7	FPGA_HSMB_TX_D_p11	17
17	FPGA_HSMB_RX_D_n11	J9	IO_8A_J9/DIFFIO_RX_T37N/DQSN5T		IO_8A_F6/DIFFIO_TX_T40N	F6	FPGA_HSMB_TX_D_n11	17
17	FPGA_HSMB_RX_D_p10	E9	IO_8A_E9/DIFFIO_RX_T11P/DQ2T		IO_8A_C3/DIFFIO_TX_T28P/DQ4T	C3	FPGA_HSMB_TX_D_p10	17
17	FPGA_HSMB_RX_D_n10	D9	IO_8A_D9/DIFFIO_RX_T11N/DQ2T		IO_8A_B3/DIFFIO_TX_T28N/DQ4T	B3	FPGA_HSMB_TX_D_n10	17
17	FPGA_HSMB_RX_D_p9	K12	IO_8A_K12/DIFFIO_RX_T29P/DQS4T		IO_8A_B2/DIFFIO_TX_T26P/DQ4T	B2	FPGA_HSMB_TX_D_p9	17
17	FPGA_HSMB_RX_D_n9	J12	IO_8A_J12/DIFFIO_RX_T29N/DQSN4T		IO_8A_B1/DIFFIO_TX_T26N/DQ4T	B1	FPGA_HSMB_TX_D_n9	17
17	FPGA_HSMB_RX_D_p8	J7	IO_8A_J7/DIFFIO_RX_T25P		IO_8A_D2/DIFFIO_TX_T30P	D2	FPGA_HSMB_TX_D_p8	17
17	FPGA_HSMB_RX_D_n8	H7	IO_8A_H7/DIFFIO_RX_T25N		IO_8A_C2/DIFFIO_TX_T30N/DQ4T	C2	FPGA_HSMB_TX_D_n8	17
17	FPGA_HSMB_RX_D_p7	H8	IO_8A_H8/DIFFIO_RX_T17P		IO_8A_D5/DIFFIO_TX_T22P	D5	FPGA_HSMB_TX_D_p7	17
17	FPGA_HSMB_RX_D_n7	G8	IO_8A_G8/DIFFIO_RX_T17N		IO_8A_C4/DIFFIO_TX_T22N/DQ3T	C4	FPGA_HSMB_TX_D_n7	17
17	FPGA_HSMB_RX_D_p6	G12	IO_8A_G12/DIFFIO_RX_T31P/DQ4T		IO_8A_C12/DIFFIO_TX_T6P	C12	FPGA_HSMB_TX_D_p6	17
17	FPGA_HSMB_RX_D_n6	G11	IO_8A_G11/DIFFIO_RX_T31N/DQ4T		IO_8A_B11/DIFFIO_TX_T6N/DQ1T	B11	FPGA_HSMB_TX_D_n6	17
17	FPGA_HSMB_RX_D_p5	F13	IO_8A_F13/DIFFIO_RX_T15P/DQ2T		IO_8A_A9/DIFFIO_TX_T8P/DQ1T	A9	FPGA_HSMB_TX_D_p5	17
17	FPGA_HSMB_RX_D_n5	E13	IO_8A_E13/DIFFIO_RX_T15N/DQ2T		IO_8A_A8/DIFFIO_TX_T8N	A8	FPGA_HSMB_TX_D_n5	17
17	FPGA_HSMB_RX_D_p4	D11	IO_8A_D11/DIFFIO_RX_T7P/DQ1T		IO_8A_D6/DIFFIO_TX_T20P/DQ3T	D6	FPGA_HSMB_TX_D_p4	17
17	FPGA_HSMB_RX_D_n4	D10	IO_8A_D10/DIFFIO_RX_T7N/DQ1T		IO_8A_C5/DIFFIO_TX_T20N/DQ3T	C5	FPGA_HSMB_TX_D_n4	17
17	FPGA_HSMB_RX_D_p3	G10	IO_8A_G10/DIFFIO_RX_T35P/DQ5T		IO_8A_A4/DIFFIO_TX_T18P/DQ3T	A4	FPGA_HSMB_TX_D_p3	17
17	FPGA_HSMB_RX_D_n3	F10	IO_8A_F10/DIFFIO_RX_T35N/DQ5T		IO_8A_A3/DIFFIO_TX_T18N/DQ3T	A3	FPGA_HSMB_TX_D_n3	17
17	FPGA_HSMB_RX_D_p2	B6	IO_8A_B6/DIFFIO_RX_T27P/DQ4T		IO_8A_E4/DIFFIO_TX_T32P/DQ4T	E4	FPGA_HSMB_TX_D_p2	17
17	FPGA_HSMB_RX_D_n2	B5	IO_8A_B5/DIFFIO_RX_T27N/DQ4T		IO_8A_D4/DIFFIO_TX_T32N	D4	FPGA_HSMB_TX_D_n2	17
17	FPGA_HSMB_RX_D_p1	F9	IO_8A_F9/DIFFIO_RX_T39P/DQ5T		IO_8A_E1/DIFFIO_TX_T36P/DQ5T	E1	FPGA_HSMB_TX_D_p1	17
17	FPGA_HSMB_RX_D_n1	F8	IO_8A_F8/DIFFIO_RX_T39N/DQ5T		IO_8A_D1/DIFFIO_TX_T36N/DQ5T	D1	FPGA_HSMB_TX_D_n1	17
17	FPGA_HSMB_RX_D_p0	K7	IO_8A_K7/DIFFIO_RX_T33P		IO_8A_E3/DIFFIO_TX_T34P/DQ5T	E3	FPGA_HSMB_TX_D_p0	17
17	FPGA_HSMB_RX_D_n0	K8	IO_8A_K8/DIFFIO_RX_T33N		IO_8A_E2/DIFFIO_TX_T34N/DQ5T	E2	FPGA_HSMB_TX_D_n0	17
17	FPGA_HSMB_CLK_IN_p2	H15	IO_8A_H15/CLK7P/DIFFIO_RX_T1P		IO_8A_A11/FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTP,FPLL_TL_FB/DIFFIO_TX_T4P/DQ1T	A11	FPGA_HSMB_CLK_OUT_p2	17
17	FPGA_HSMB_CLK_IN_n2	G15	IO_8A_G15/CLK7N/DIFFIO_RX_T1N		IO_8A_A10/FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTN/DIFFIO_TX_T4N/DQ1T	A10	FPGA_HSMB_CLK_OUT_n2	17
17	FPGA_HSMB_CLK_IN_p1	K14	IO_8A_K14/CLK6P,FPLL_TL_FBP/DIFFIO_RX_T9P		IO_8A_A6/DIFFIO_TX_T16P/DQ2T	A6	FPGA_HSMB_CLK_OUT_p1	17
17	FPGA_HSMB_CLK_IN_n1	J14	IO_8A_J14/CLK6N,FPLL_TL_FBN/DIFFIO_RX_T9N		IO_8A_A5/DIFFIO_TX_T16N	A5	FPGA_HSMB_CLK_OUT_n1	17
					IO_8A_B13/DIFFIO_TX_T2P/DQ1T	B13	FPGA_HSMB_SCL	17
					IO_8A_A13/DIFFIO_TX_T2N/DQ1T	A13	FPGA_HSMB_SDA	17
					IO_3B_AA15/DIFFIO_RX_B35N/DQSN5B	AA15	FPGA_HSMB_CLK_OUT0	17

FPGA_AUDIO

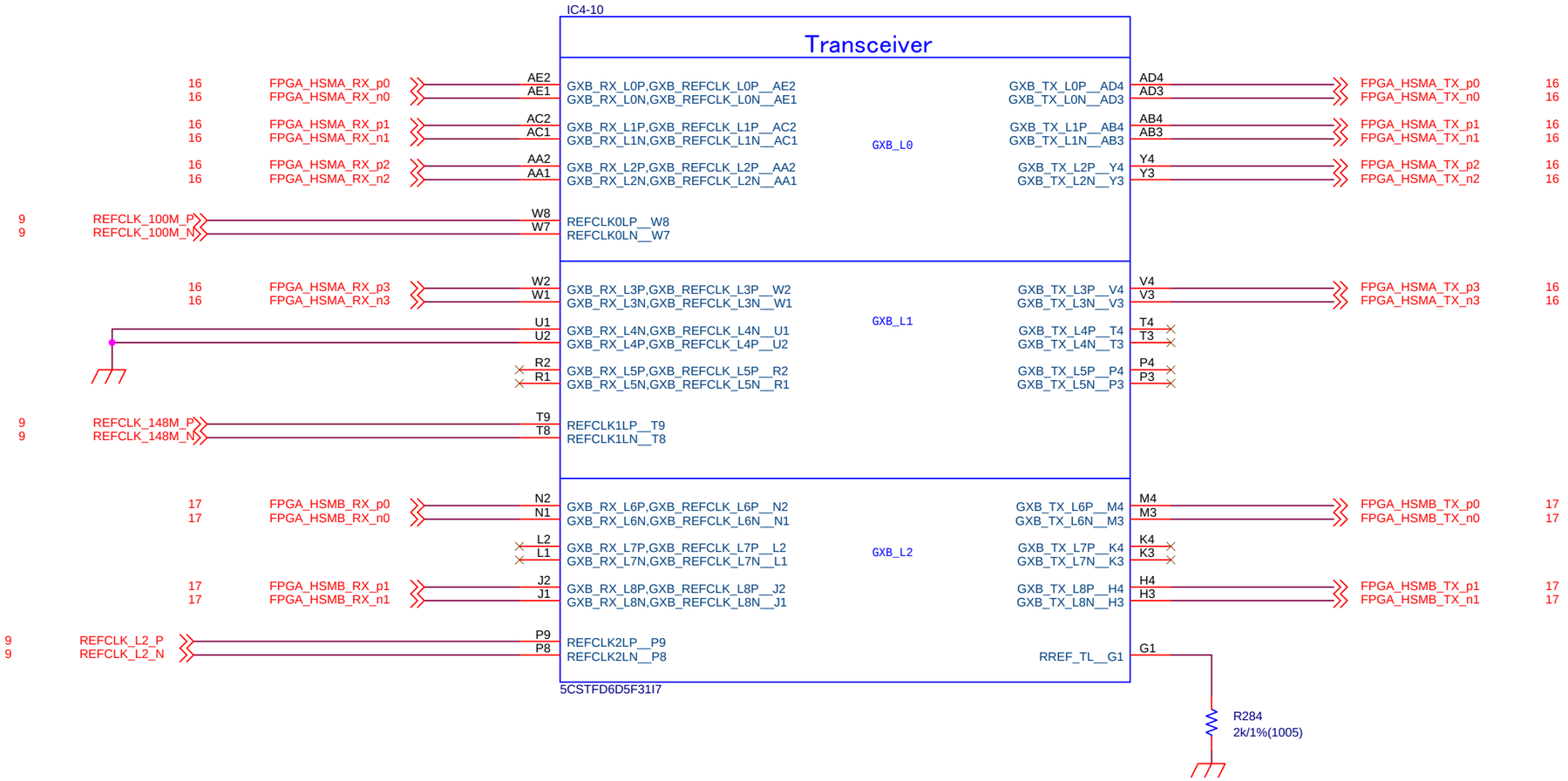
19	FPGA_AUDIO_ADCDAT	H14	IO_8A_H14/DIFFIO_RX_T13P/DQS2T						
19	FPGA_AUDIO_ADCLRCK	G13	IO_8A_G13/DIFFIO_RX_T13N/DQSN2T						

5CSTFD6D5F31I7

mPRESSION
The Solutions by Macnica Group

Title	Sodia		
Size A3	Document Number ASC001		Rev C
Date: Wednesday, November 21, 2018	Sheet 7 of 36		

Cyclone V ST SoC Transceiver



The Solutions by Macnica Group

Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 8 of 36	

CLK BLOCK

REFCLK0L p/n
f = 100MHz

2p5v L19 BLM18KG300TN1D

X8 530SC100M000DG

R1 NM(1608)

C3 0.1u(B)

C4 0.1u(B)

REFCLK_100M_P 8

REFCLK_100M_N 8

C450 0.1u(B)

R270 0(1005)

REFCLK1L p/n
f = 148.5MHz

2p5v L20 BLM18KG300TN1D

X9 530SC148M500DG

R5 NM(1608)

C8 0.1u(B)

C9 0.1u(B)

REFCLK_148M_P 8

REFCLK_148M_N 8

C451 0.1u(B)

R271 0(1005)

3p3v L17 BLM18KG300TN1D

C13 0.1u(B)

R288 0(1005)

X4 510CCB25M0000AAG

FREQ 25MHz

R203 22(1005)

3p3v

R12 NM(1608)

R14 NM(1608)

19,6,9 HPS_I2C1_SCL

19,6,9 HPS_I2C1_SDA

I2C ADDR = 0x70

X3 Si5338C-B05096-GM

2p5v

C479 0.1u(B)

C420 0.1u(B)

C421 0.1u(B)

C422 0.1u(B)

VCCHPS_3p3v

3p3v

C423 0.1u(B)

2p5v

VCCHPS_3p3v

3p3v R6 1k(1005)

R168 33(1005) FPGA_CLKIN_DDR3_50M 3

R10 33(1005) FPGA_CLKIN_100M 3

R13 0(1005) FPGA_CLKIN_27M 4

R15 0(1005) HPS_CLKIN2_25M 6

R250 82(1005)

R248 82(1005)

R251 43(1005)

R249 43(1005)

1.5 V CMOS Output (VDDOx = 2.5v)
R1 : 33Ω
R2 : 125Ω (82+43)

REFCLK2L p/n
f = 125MHz or SMA

3p3v L24 BLM18KG300TN1D

C24 0.1u(B)

C11 2.2u/16V(B)

X2 570SCC000115DG

19,6,9 HPS_I2C1_SCL

19,6,9 HPS_I2C1_SDA

I2C ADDR = 0x55

R272 0(1005)

3p3v C10 0.1u(B)

C2 0.1u(B)

IC2 Si53307-B-GM

R9 100/1%(1608)

R8 100/1%(1608)

R11 100/1%(1608)

C18 0.1u(B)

C19 0.1u(B)

REFCLK_L2_P 8

REFCLK_L2_N 8

REFCLK_125M_SEL 14

C14 0.1u(B)

C15 0.1u(B)

CN1 5-1814832-1

CN2 5-1814832-1

CLK DIF

CLK_SEL
LOW = CLK0
HIGH = CLK1

3p3v L18 BLM18KG300TN1D

C20 0.1u(B)

R289 0(1005)

X5 510CCB25M0000AAG

R204 22(1005)

CLK IN

CN3 5-1814832-1

R205 22(1005)

R269 NM(1608)

3p3v 1k(1005) R206 R207 R210 R209

3p3v

C448 0.1u(B)

IC3 Si53307-B-GM

VCCHPS_3p3v

C449 0.1u(B)

R17 33(1005) HPS_CLKIN1_25M 6

1k(1005) R19 R18

CLK_SEL
LOW = CLK0
HIGH = CLK1

S8	CLK_SEL
off	LOW = CLK0
on	HIGH = CLK1

3p3v S8 TDA02H0SB1

REFCLK_125M_SEL

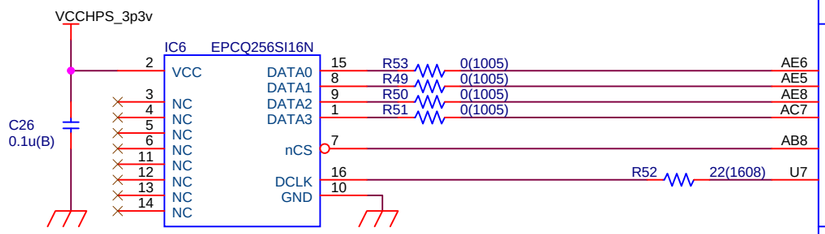
R208 10k(1005)

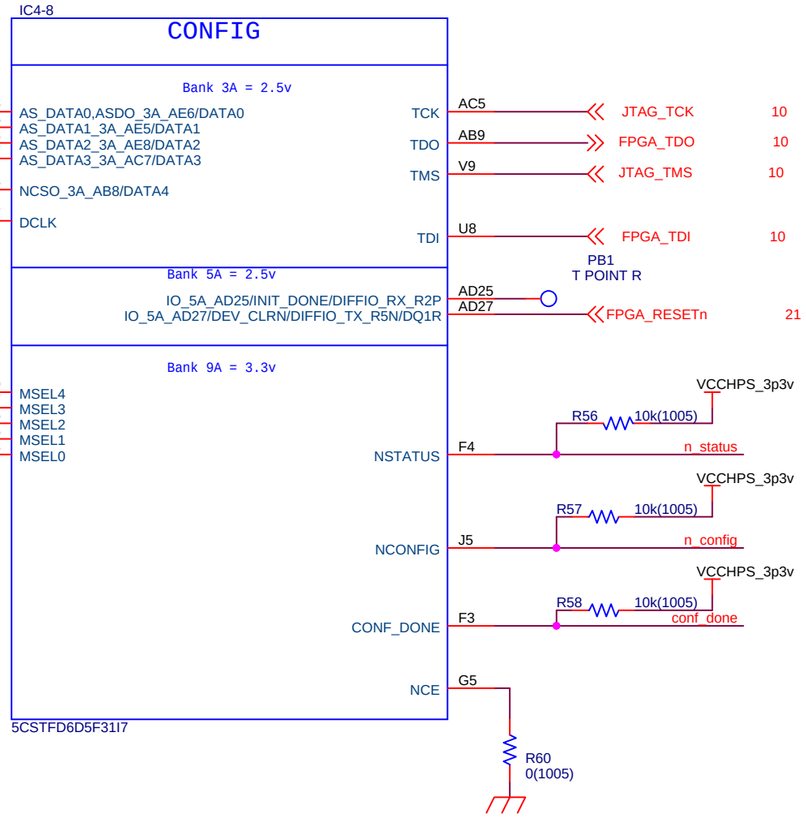
R235 10k(1005)

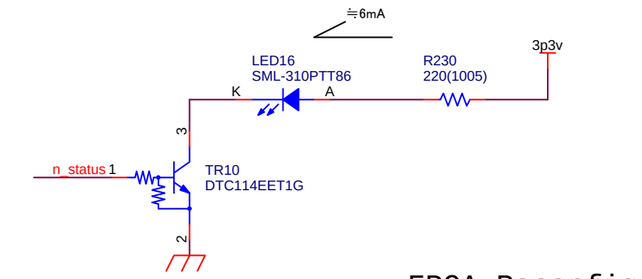
mPRESSION
The Solutions by Macnica Group

Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 9 of 36	

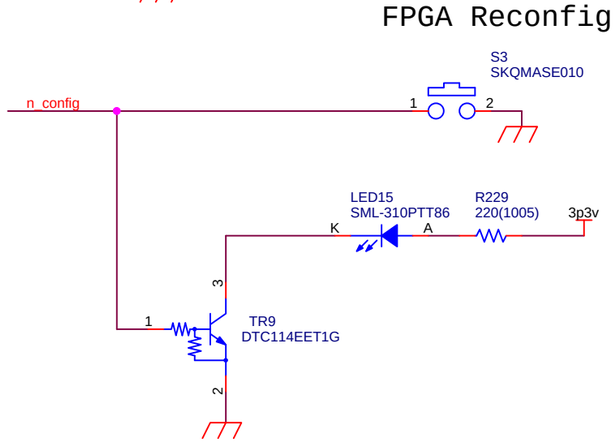
Cyclone V ST SoC CONFIG

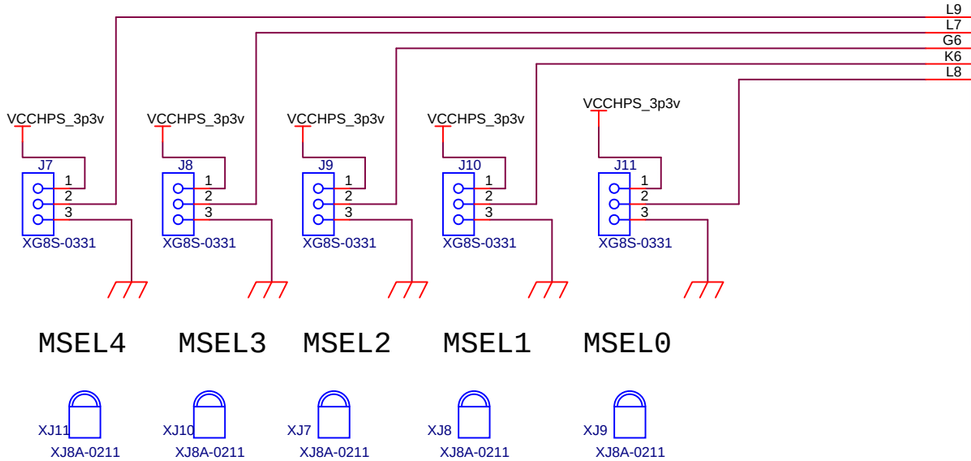




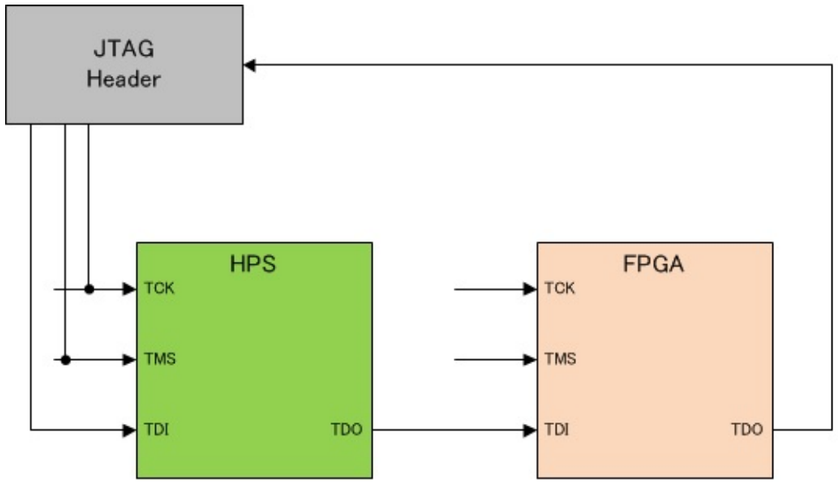


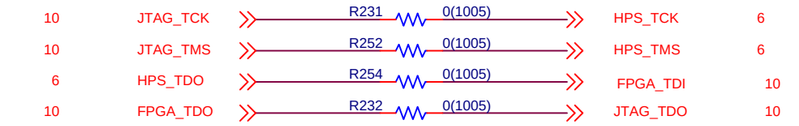
FPGA Reconfig

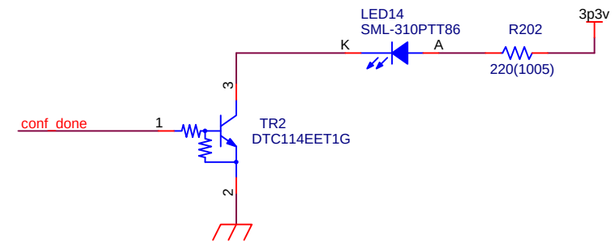


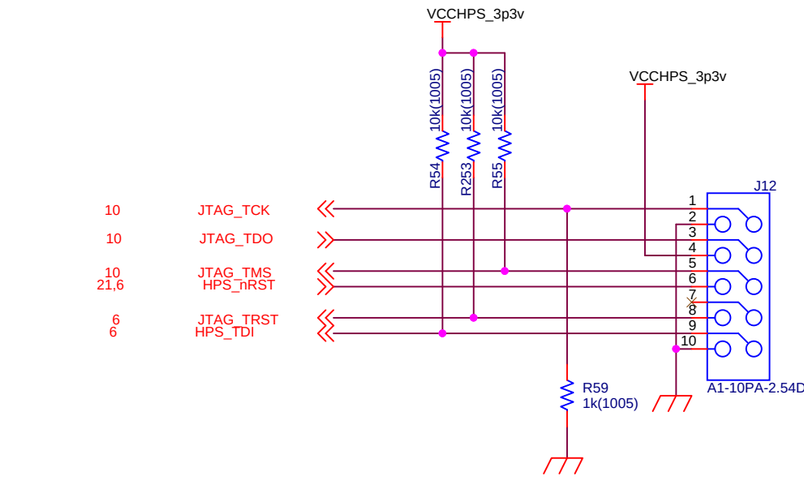


MSEL [4:0]	Configuration	Note
10010	AS (x1 and x4), Power-On Reset (POR) Delay: Fast	
10011	AS (x1 and x4), Power-On Reset (POR) Delay: Standard	
01010	FPPx32 w/ Copmression Fast	default







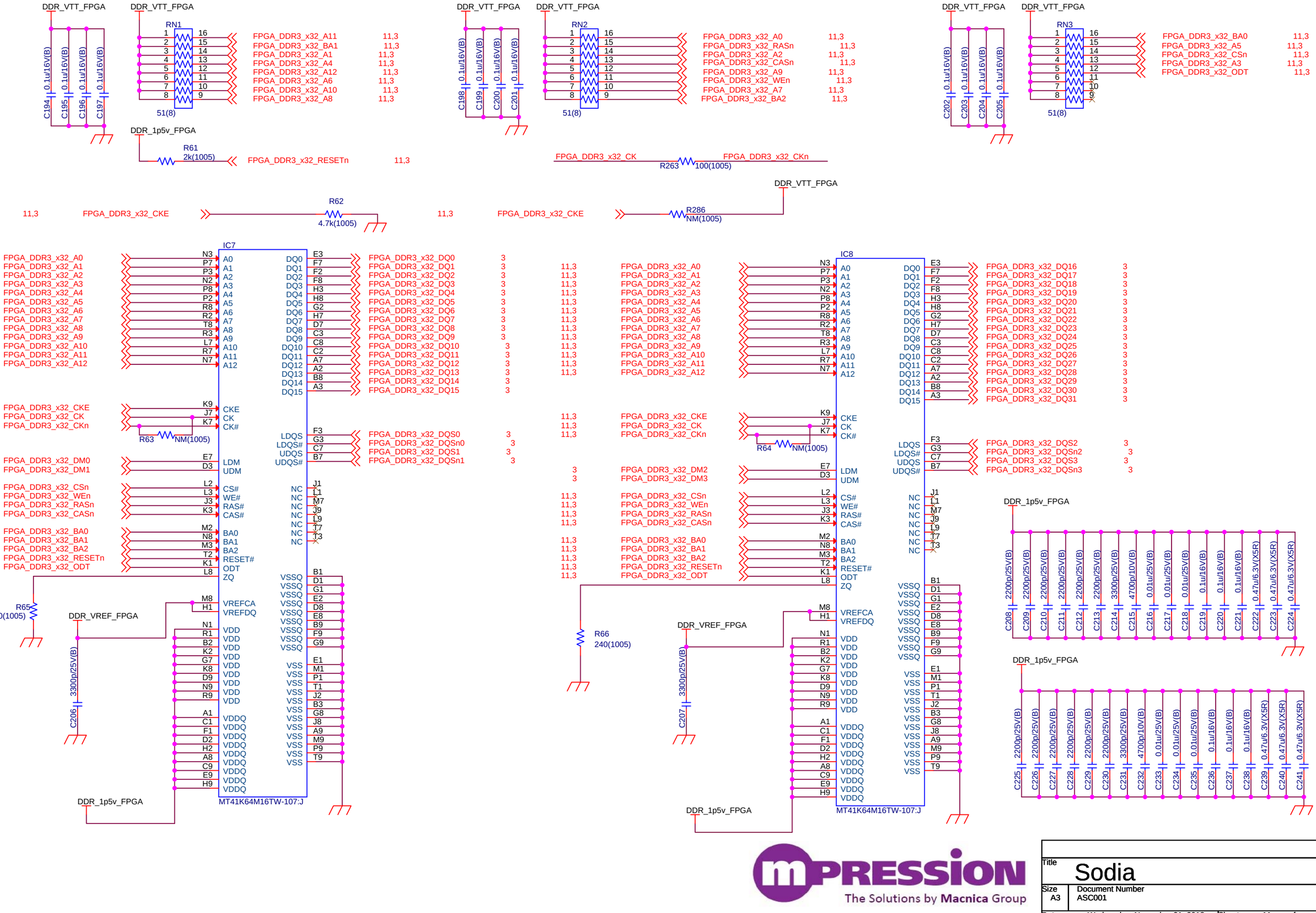


JTAG

mPRESSION
The Solutions by Macnica Group

Title: Sodia			
Size: A3	Document Number: ASC001		Rev: B
Date: Wednesday, November 21, 2018	Sheet 10 of 36		

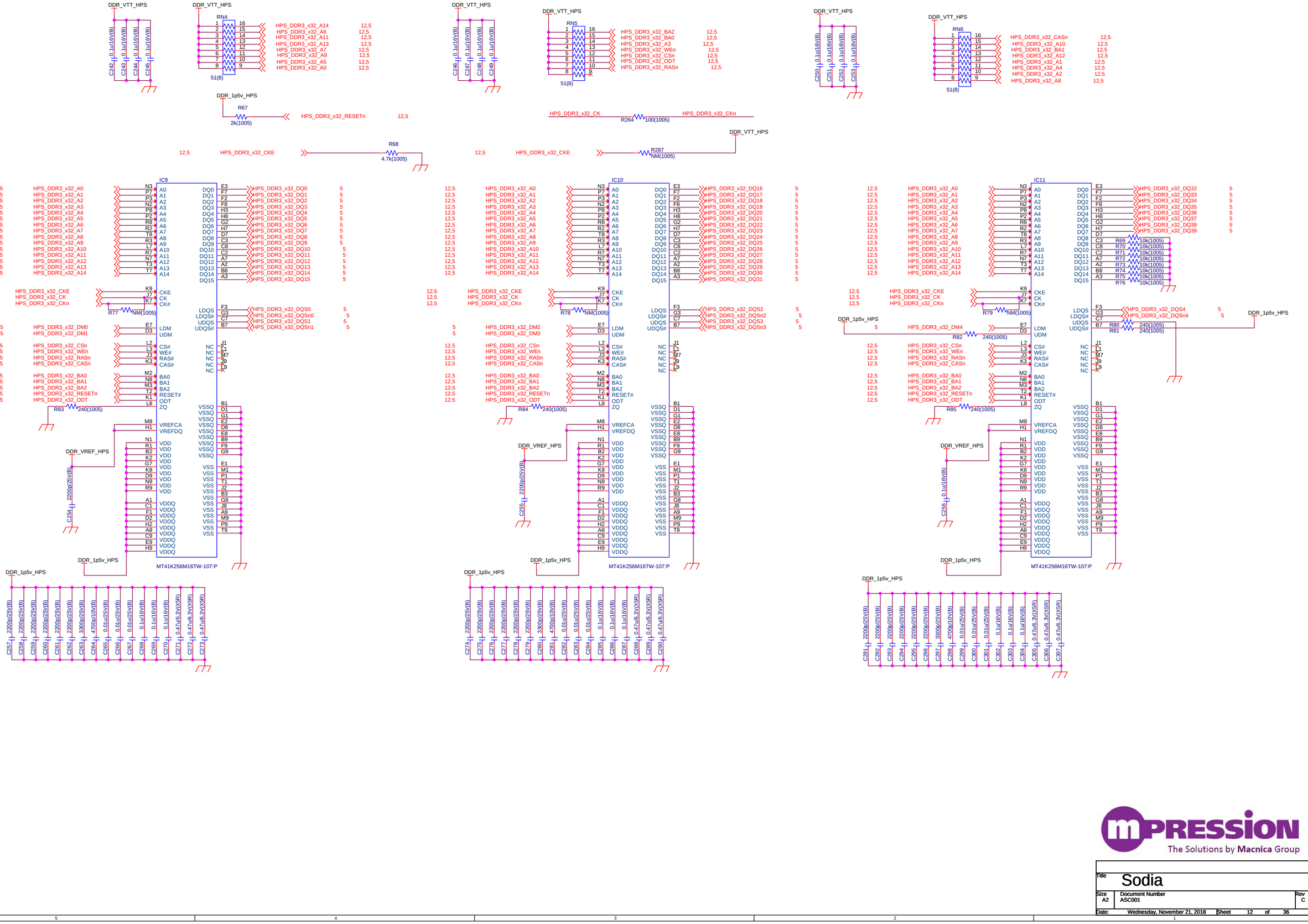
DDR3 (FPGA)



mPRESSION The Solutions by Macnica Group

Title	Sodia		
Size A3	Document Number ASC001		Rev B
Date: Wednesday, November 21, 2018	Sheet 11 of 36		

DDR3 (HPS)

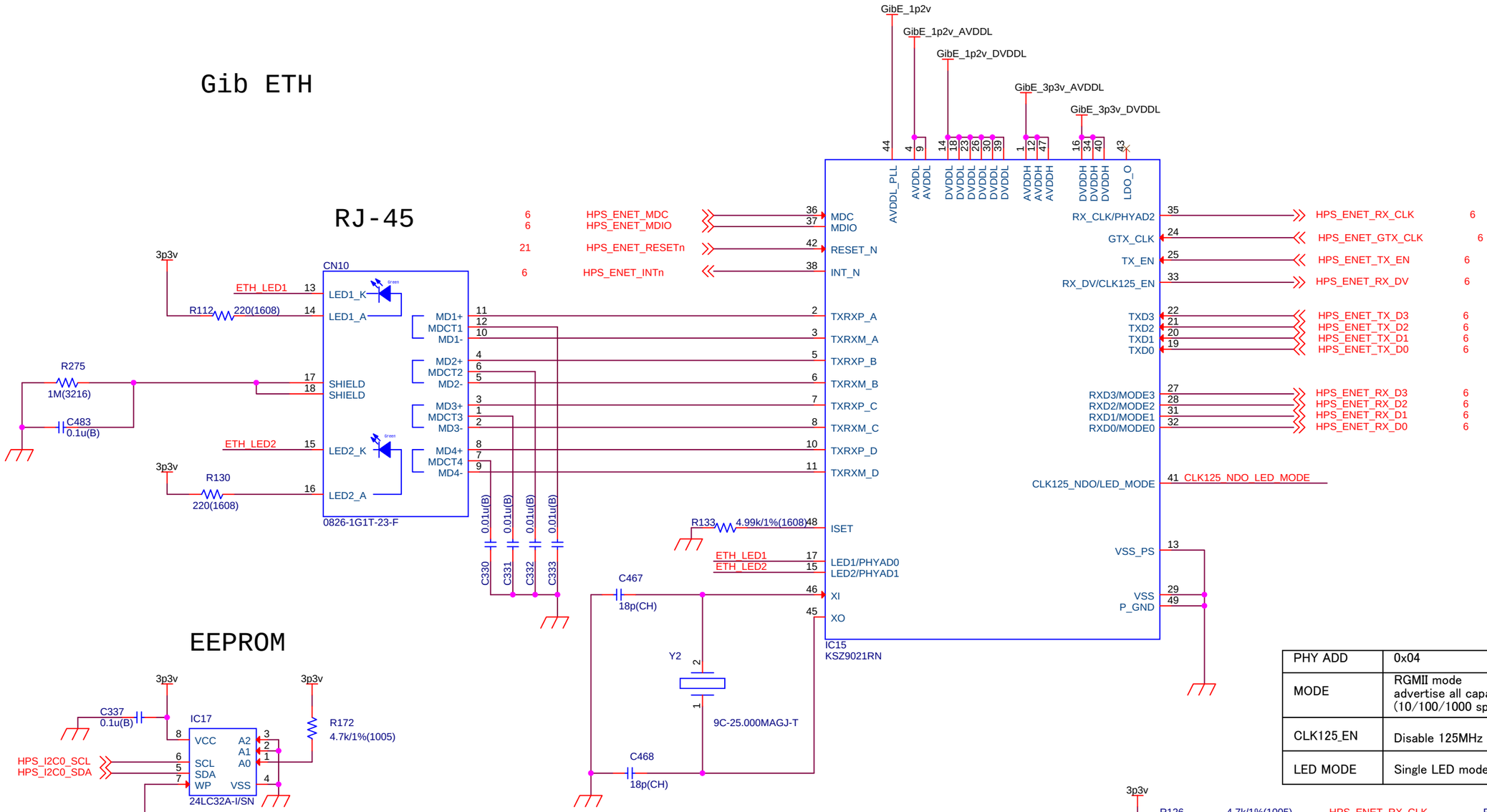


Title	Sodia		
Size A2	Document Number ASC001		Rev C
Date: Wednesday, November 21, 2018	Sheet 12	of 36	

Gib ETH / EEPROM

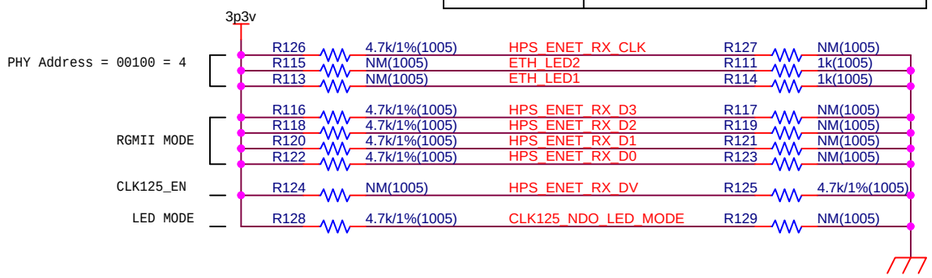
Gib ETH

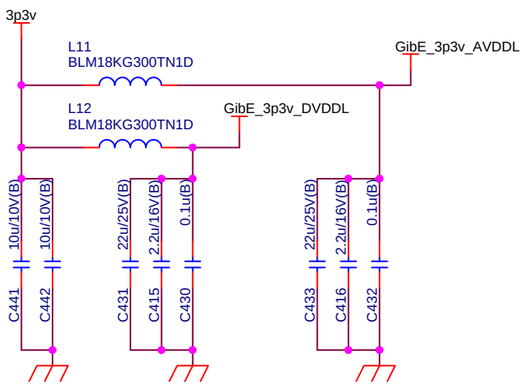
RJ-45

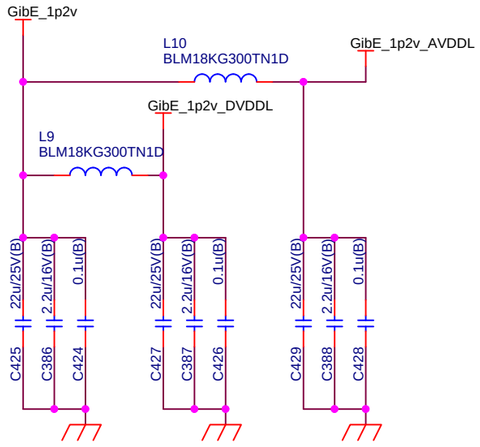


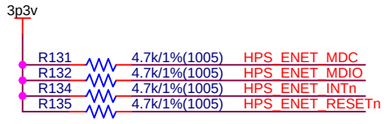
EEPROM

PHY ADD	0x04
MODE	RGMII mode advertise all capabilities (10/100/1000 speed half-/full-duplex)
CLK125_EN	Disable 125MHz clock output
LED MODE	Single LED mode







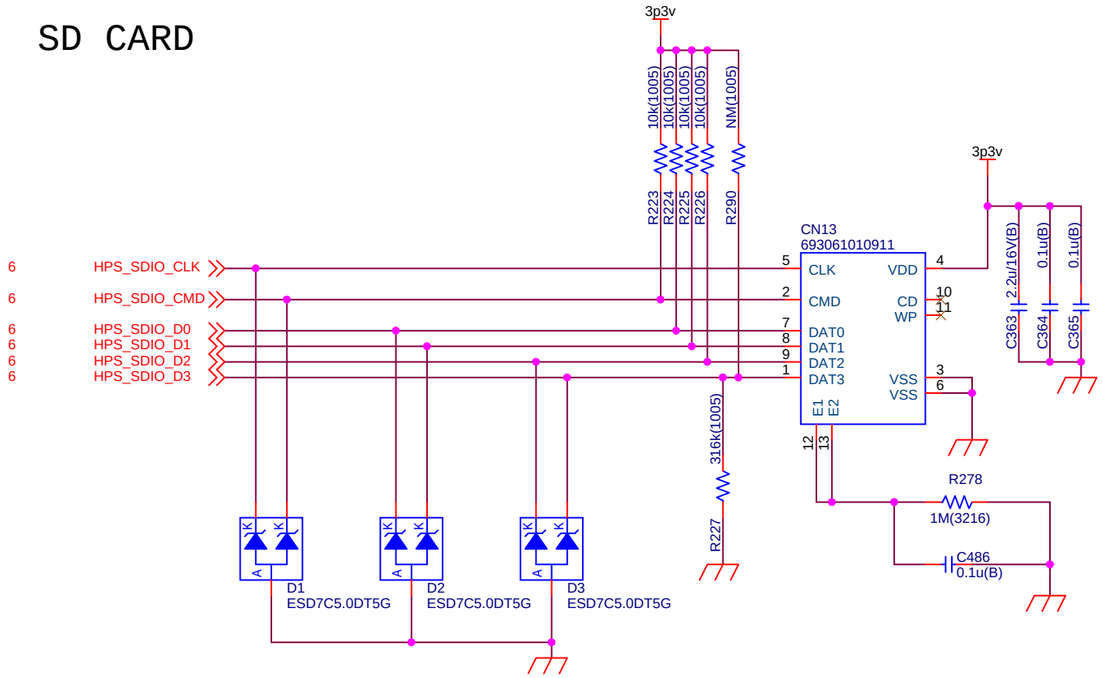


mPRESSION
The Solutions by Macnica Group

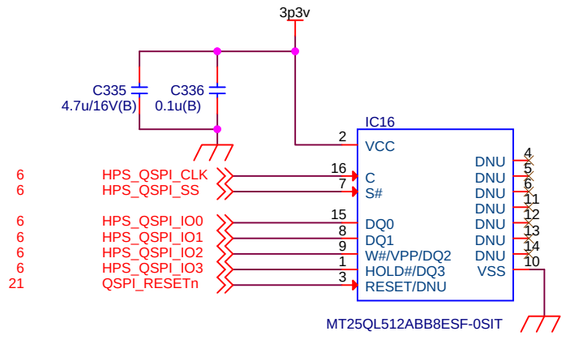
Title: Sodia			
Size: A3	Document Number: ASC001		Rev: C
Date: Wednesday, November 21, 2018	Sheet 13 of 36		

SD CARD / QSPI FLASH

SD CARD



QSPI FLASH

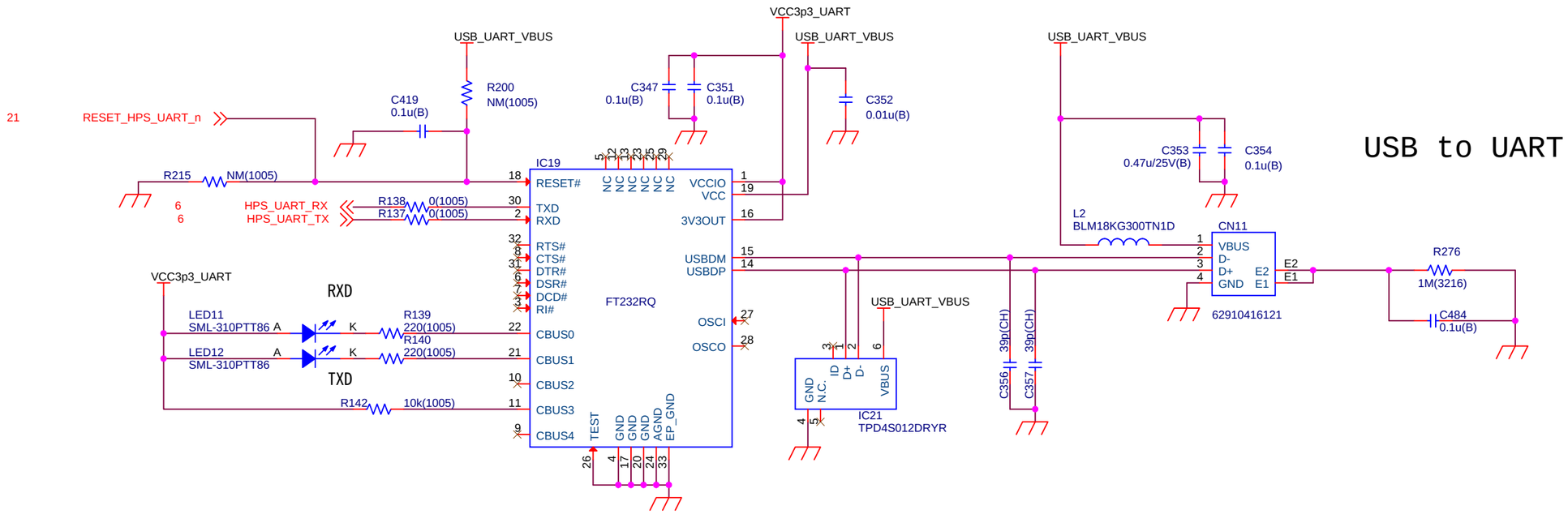


mPRESSION
The Solutions by Macnica Group

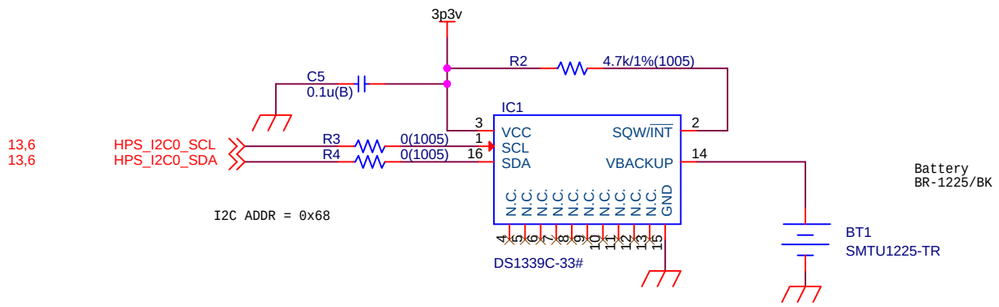
Title: Sodia		
Size: A3	Document Number: ASC001	Rev: B
Date: Wednesday, November 21, 2018	Sheet 14 of 36	

USB_UART / RTC

USB_UART

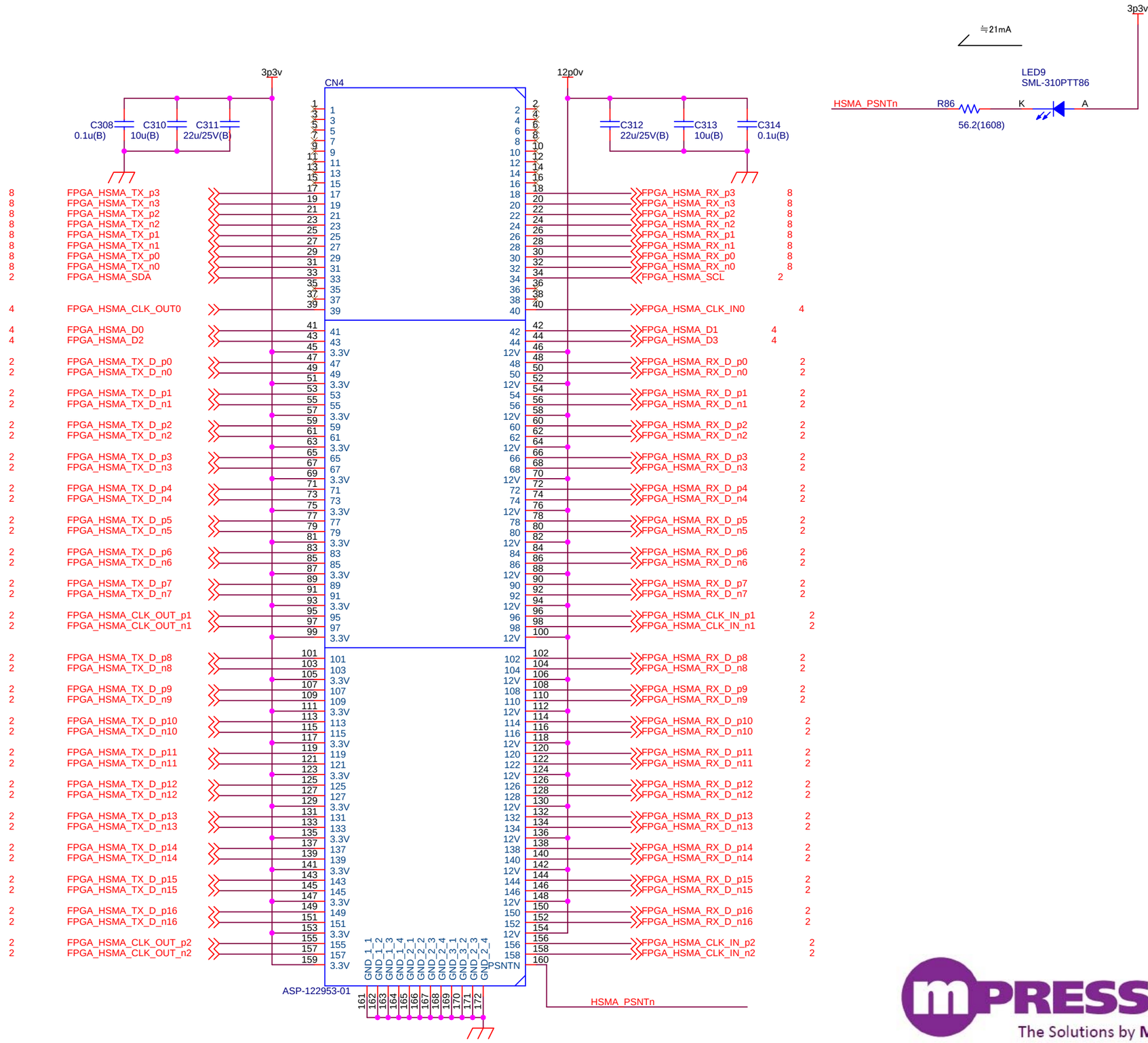


RTC



Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 15 of 36	

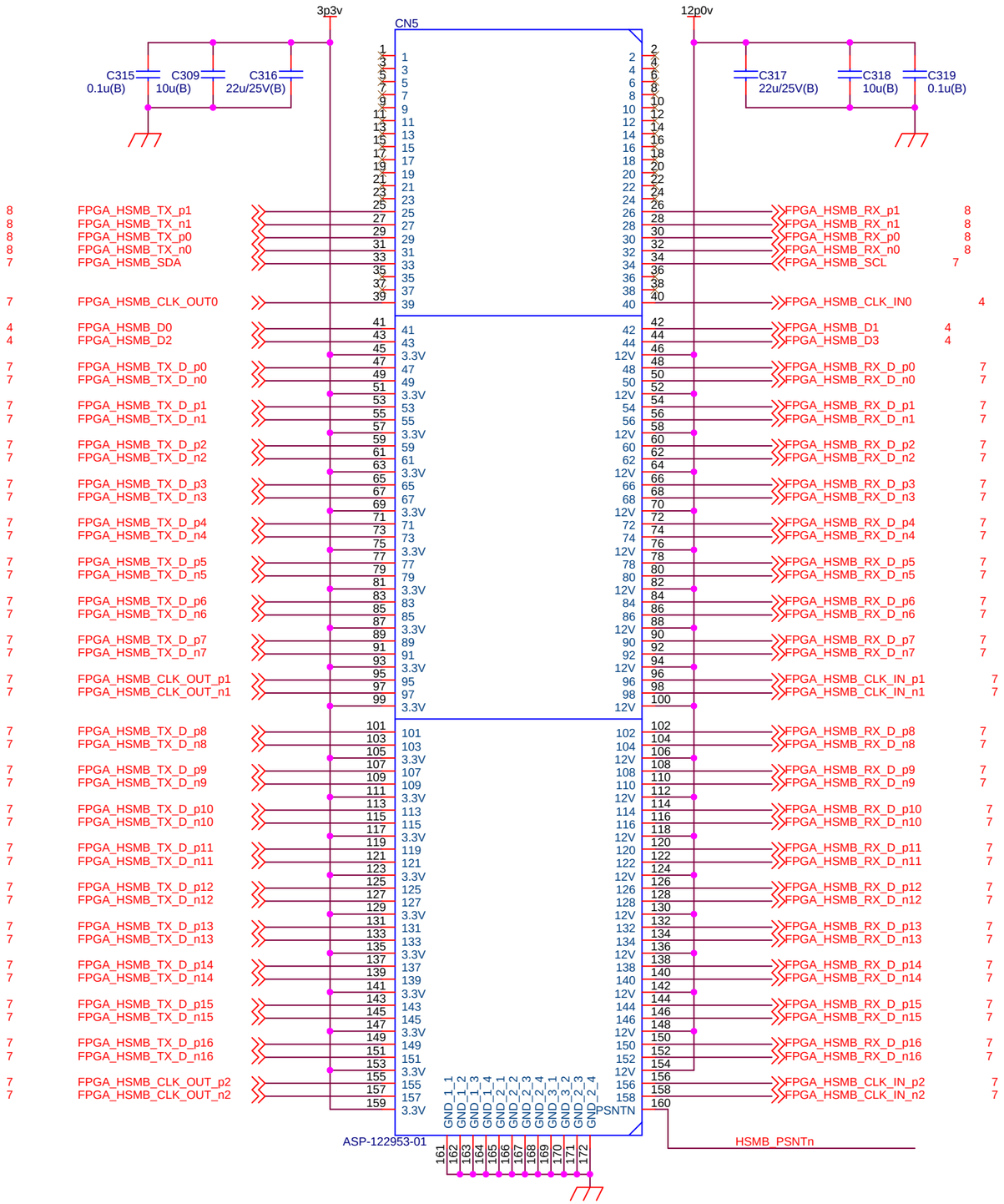
HSMC POAT A

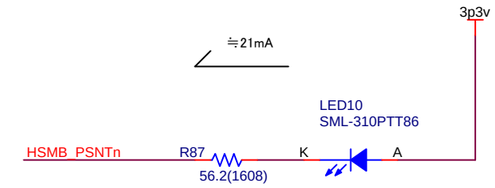


mPRESSION
The Solutions by Macnica Group

Title	Sodia	
Size A3	Document Number ASC001	Rev C
Date: Wednesday, November 21, 2018	Sheet 16 of 36	

HSMC POAT B





mPRESSION
The Solutions by Macnica Group

Title	Sodia		
Size A3	Document Number ASC001		Rev C
Date: Wednesday, November 21, 2018		Sheet 17 of 36	

USB_2.0

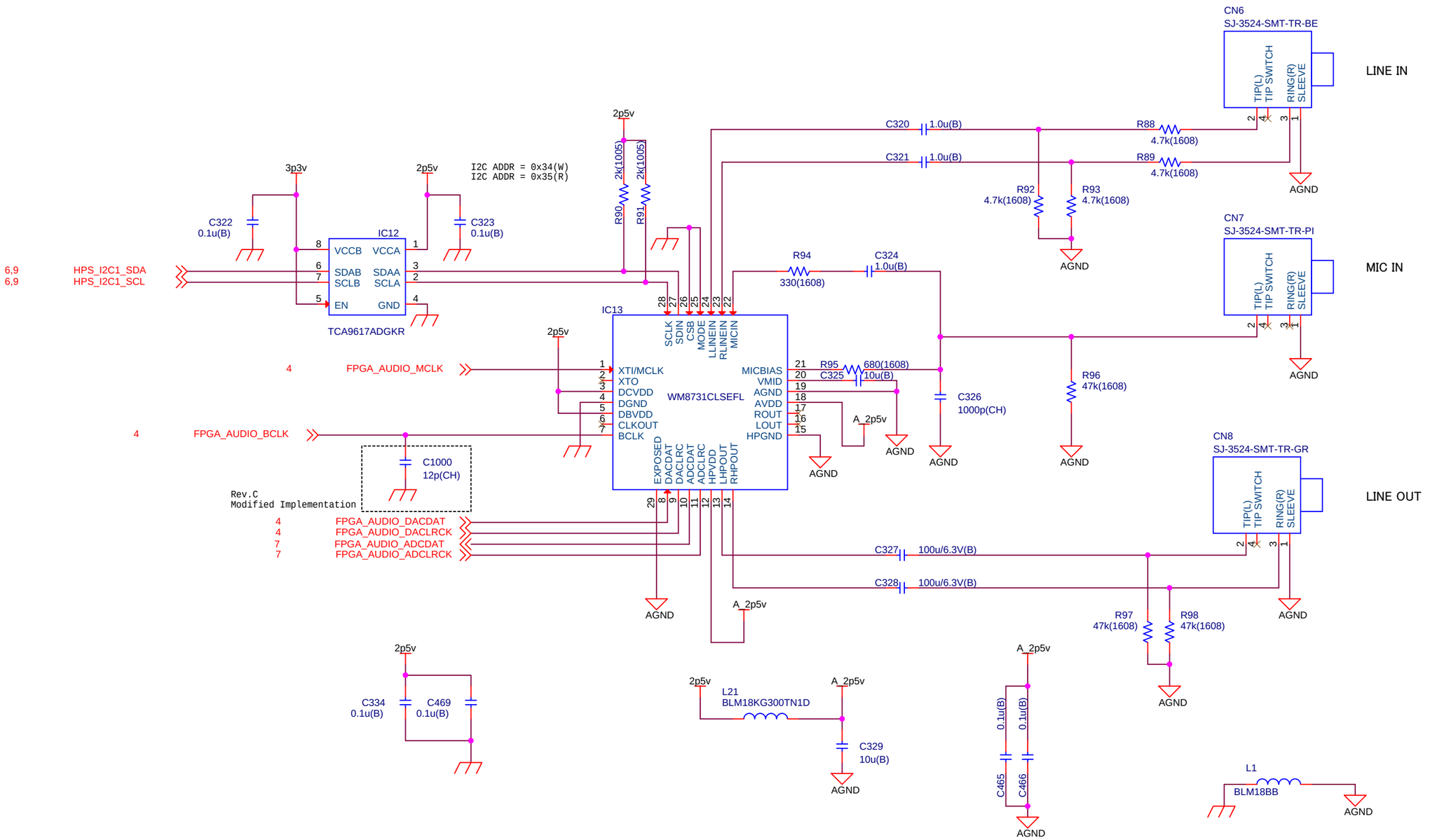
USB standard-A

USB_ID_CTL	OTG Role
OPEN	PERIPHERAL
GND	HOST

Title	Sodia
Size	A3
Document Number	ASC001
Rev	C
Date:	Wednesday, November 21, 2018
Sheet	18 of 36

The Solutions by Macnica Group

AUDIO



mPRESSION
The Solutions by Macnica Group

Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 19 of 36	

DVI

Controller Interface Options
ISEL = LOW
BSEL = HIGH
EDGE = HIGH
DSEL = LOW

IC14
TFP410PAP

TVDD_3p3v
DVDD_3p3v
PVDD_3p3v

DATA23 DATA22 DATA21 DATA20 DATA19 DATA18 DATA17 DATA16 DATA15 DATA14 DATA13 DATA12 DATA11 DATA10 DATA9 DATA8 DATA7 DATA6 DATA5 DATA4 DATA3 DATA2 DATA1 DATA0

CTL3/A3/DK3
CTL2/A2/DK2
CTL1/A1/DK1
EDGE/HTPLG
DKEN
DSEL/SDA
ISEL/RST
BSEL/SCL

DE
HSYNC
VSYNC
IDCK+
IDCK-

PD
MSEN/PO1

NC

TFADJ
VREF

R99 510(1005)
R100 4.7k(1005)
R101 NM(1005)
R102 0(1005)
R103 0(1005)
R104 0(1005)
R105 0(1005)
R106 10k(1005)
R107 5.1k(1005)
R222 100(1005)

C452 22u/25V(B)

TX2+ TX2- TX1+ TX1- TX0+ TX0- TXC+ TXC-

DVI_DATA2_p DVI_DATA2_n DVI_DATA1_p DVI_DATA1_n DVI_DATA0_p DVI_DATA0_n DVI_CLK_p DVI_CLK_n

DVI TX

CN9

DATA2+ DATA2- GND DATA1+ DATA1- GND DATA0+ DATA0- GND CLK+ CLK- GND
DDC_CLK DDC_DAT
+5V GND DETECT
VSYNC
DATA4+ DATA4-
DATA3+ DATA3-
DATA5+ DATA5-

A_RED A_GREEN A_BLUE A_HSYNC AGND

74320-1000

5p0v F1 0ZCH0020FF2E
R217 NM(1005)
R218 20k(1005)
R219 30k(1005)
HTPLG

R274 1M(3216)
C482 0.1u(B)

FPGA_DVI_DATA23 FPGA_DVI_DATA22 FPGA_DVI_DATA21 FPGA_DVI_DATA20 FPGA_DVI_DATA19 FPGA_DVI_DATA18 FPGA_DVI_DATA17 FPGA_DVI_DATA16 FPGA_DVI_DATA15 FPGA_DVI_DATA14 FPGA_DVI_DATA13 FPGA_DVI_DATA12 FPGA_DVI_DATA11 FPGA_DVI_DATA10 FPGA_DVI_DATA9 FPGA_DVI_DATA8 FPGA_DVI_DATA7 FPGA_DVI_DATA6 FPGA_DVI_DATA5 FPGA_DVI_DATA4 FPGA_DVI_DATA3 FPGA_DVI_DATA2 FPGA_DVI_DATA1 FPGA_DVI_DATA0

CTL_3 CTL_2 CTL_1 DKEN

FPGA_DVI_DE FPGA_DVI_HS FPGA_DVI_VS FPGA_DVI_CLK

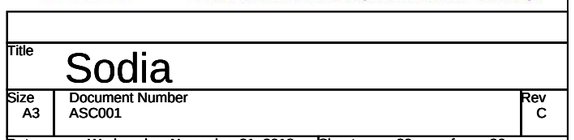
FPGA_DVI_RESETn

R108 10k(1608) R109 10k(1608) R110 10k(1608) R221 10k(1608)
R173 NM(1608) R174 NM(1608) R175 NM(1608) R220 NM(1608)

L14 BLM18KG300TN1D
L15 BLM18KG300TN1D
L16 BLM18KG300TN1D

C380 10u/10V(B)
C381 10u/10V(B)
C417 10u/10V(B)

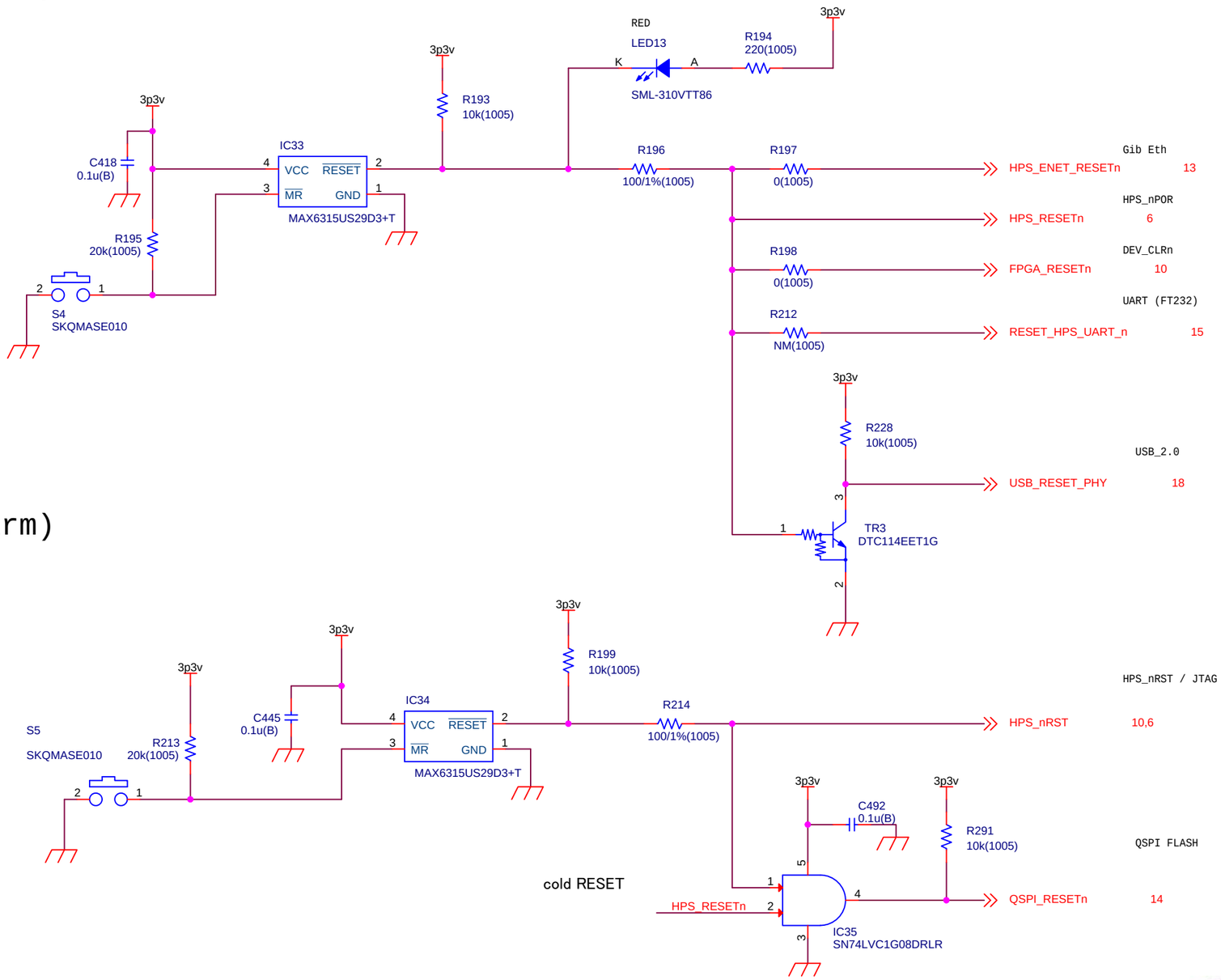
C435 C436 C434 C437 C439 C440 C438 C443 C444
22u/25V(B) 0.1u(B)



Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 20 of 36	

RESET

RESET (cold)

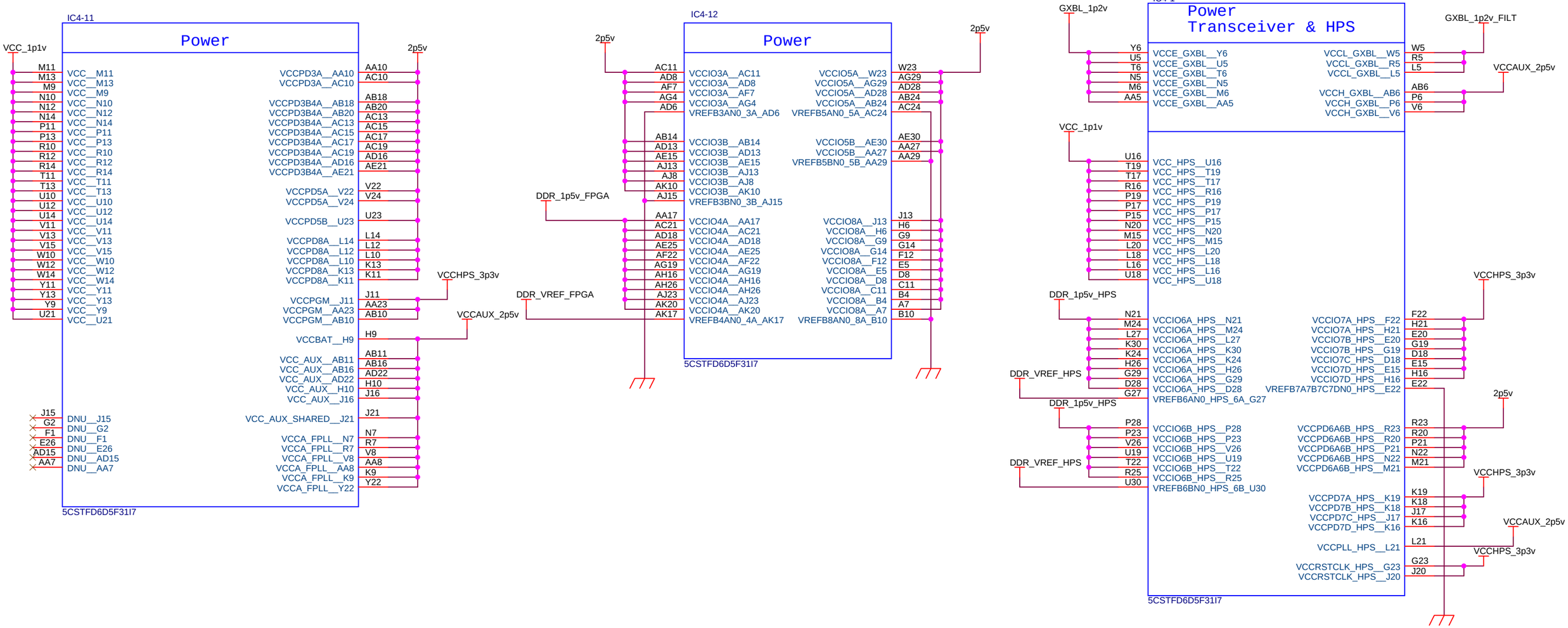


RESET (warm)

mPRESSION
The Solutions by Macnica Group

Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 21 of 36	

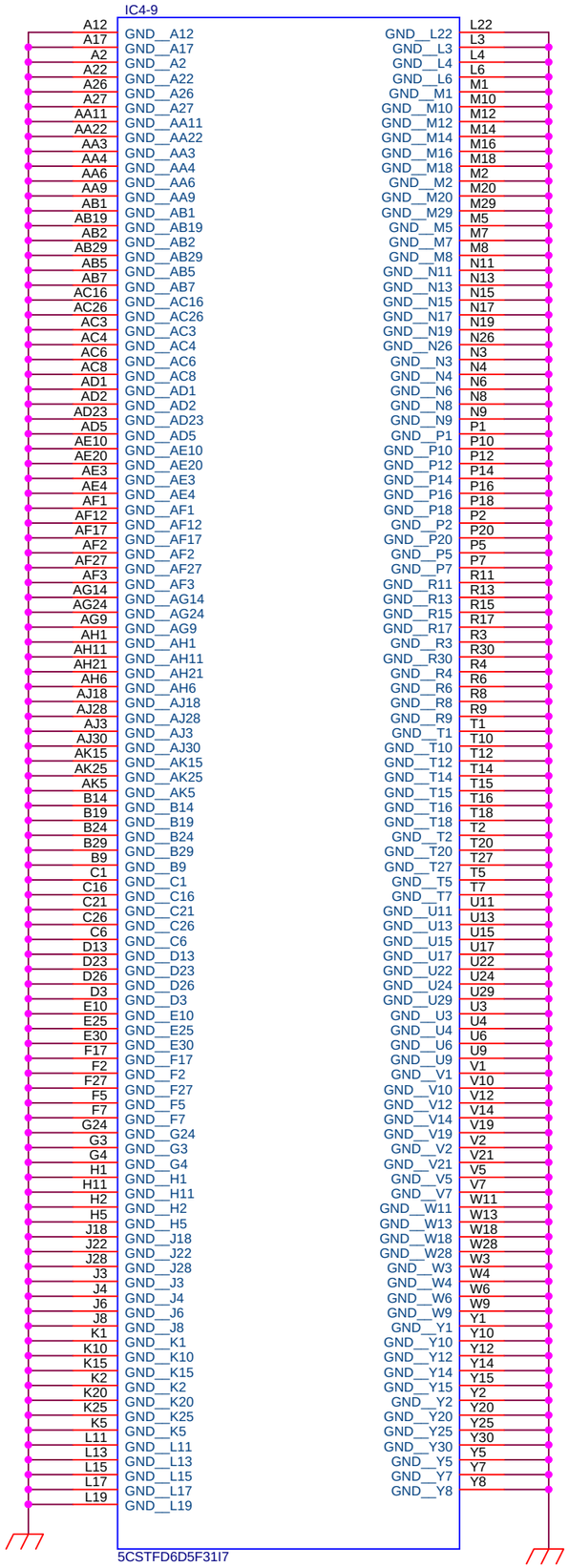
Cyclone V ST SoC POWER



mPRESSION
The Solutions by Macnica Group

Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 22 of 36	

Cyclone V ST SoC GND



mPRESSION
The Solutions by Macnica Group

Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 23 of 36	

Cyclone V ST SoC Decoupling

VCC_1p1v

C44 100u/6.3V(B)
C45 100u/6.3V(B)
C46 100u/6.3V(B)
C31 47u/16V(B)

C52 4.7u/16V(B)
C60 4.7u/16V(B)
C53 2.2u/10V(B)
C61 2.2u/10V(B)
C54 2.2u/10V(B)

C84 0.47u/10V(B)
C85 0.47u/10V(B)
C86 0.47u/10V(B)
C87 0.22u/10V(B)
C88 0.22u/10V(B)
C89 0.22u/10V(B)
C90 0.22u/10V(B)
C76 0.1u(B)
C91 0.1u(B)
C74 0.1u(B)
C92 0.1u(B)
C72 0.1u(B)

C125 0.022u(B)
C126 0.022u(B)
C127 0.022u(B)
C128 0.022u(B)
C129 0.022u(B)
C130 0.022u(B)
C131 0.022u(B)
C132 0.022u(B)
C133 0.022u(B)
C134 0.022u(B)

C145 0.01u(B)
C146 0.01u(B)
C147 0.01u(B)
C148 0.01u(B)
C149 0.01u(B)
C150 0.01u(B)
C151 0.01u(B)
C152 0.01u(B)
C153 0.01u(B)
C154 0.01u(B)

GXBL_1p2v

C48 100u/6.3V(B)
C32 100u/6.3V(B)
C49 10u/10V(B)
C56 4.7u/16V(B)

C93 0.47u/10V(B)
C77 0.22u/10V(B)
C68 0.1u(B)

C107 0.022u(B)
C108 0.022u(B)
C113 0.01u(B)

2p5v

C33 100u/6.3V(B)
C34 100u/6.3V(B)
C35 10u/10V(B)
C36 10u/10V(B)

C50 2.2u/10V(B)
C59 2.2u/10V(B)
C51 2.2u/10V(B)

C78 0.47u/10V(B)
C71 0.47u/10V(B)
C79 0.47u/10V(B)
C69 0.22u/10V(B)
C80 0.22u/10V(B)
C66 0.1u(B)
C81 0.1u(B)
C67 0.1u(B)
C82 0.1u(B)
C83 0.1u(B)

C97 0.022u(B)
C98 0.022u(B)
C99 0.022u(B)
C100 0.022u(B)
C101 0.022u(B)
C102 0.022u(B)
C103 0.022u(B)
C104 0.022u(B)
C105 0.022u(B)
C106 0.022u(B)

C135 0.01u(B)
C136 0.01u(B)
C137 0.01u(B)
C138 0.01u(B)
C139 0.01u(B)
C140 0.01u(B)
C141 0.01u(B)
C142 0.01u(B)
C143 0.01u(B)
C144 0.01u(B)

2p5v
L8
BLM18KG300TN1D
VCCAUX_2p5v

C37 100u/6.3V(B)
C39 47u/16V(B)
C40 10u/10V(B)

C63 2.2u/10V(B)
C64 2.2u/10V(B)
C65 2.2u/10V(B)

C73 0.47u/10V(B)
C75 0.47u/10V(B)
C95 0.22u/10V(B)
C96 0.22u/10V(B)

C117 0.022u(B)
C118 0.022u(B)
C119 0.022u(B)
C120 0.01u(B)
C121 0.01u(B)
C122 0.01u(B)
C123 0.01u(B)
C124 0.01u(B)

GXBL_1p2v
L23
BLM18KG300TN1D
GXBL_1p2v_FILT

C94 0.22u/10V(B)
C70 0.1u(B)
C110 0.022u(B)
C111 0.022u(B)
C116 0.01u(B)

DDR_1p5v_FPGA

C155 100u/6.3V(B)
C156 10u/10V(B)

C163 2.2u/10V(B)
C164 2.2u/10V(B)

C169 0.47u/10V(B)
C170 0.47u/10V(B)
C171 0.1u(B)
C172 0.1u(B)

C179 0.022u(B)
C180 0.022u(B)
C181 0.01u(B)
C182 0.01u(B)
C183 0.01u(B)

DDR_VREF_FPGA

C480
3300p/25V(B)

DDR_1p5v_HPS

C157 100u/6.3V(B)
C158 10u/10V(B)

C165 2.2u/10V(B)
C166 2.2u/10V(B)

C173 0.47u/10V(B)
C174 0.47u/10V(B)
C175 0.1u(B)
C176 0.1u(B)

C184 0.022u(B)
C185 0.022u(B)
C186 0.01u(B)
C187 0.01u(B)
C188 0.01u(B)

DDR_VREF_HPS

C481
2200p/25V(B)

VCCHPS_3p3v

C159 100u/6.3V(B)
C160 47u/16V(B)
C161 10u/10V(B)
C162 10u/10V(B)

C167 2.2u/10V(B)
C168 2.2u/10V(B)

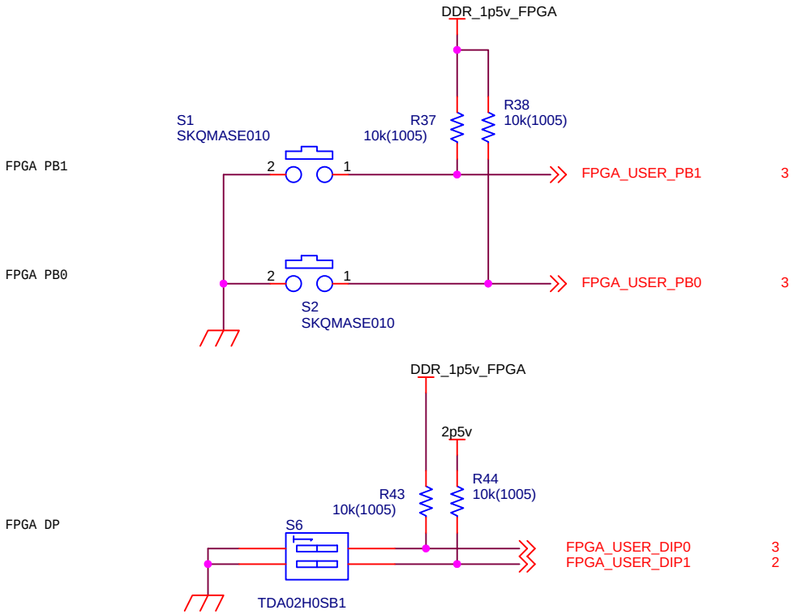
C177 0.1u(B)
C178 0.1u(B)

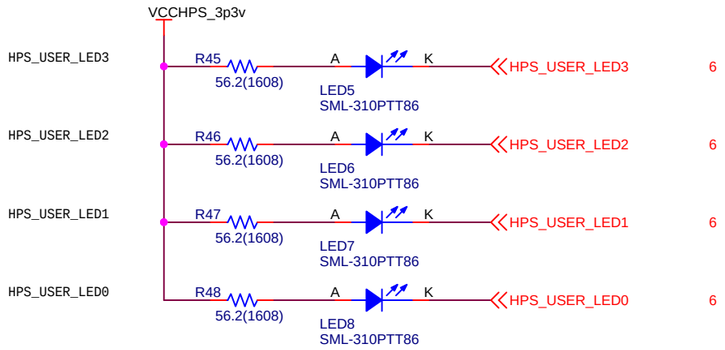
C189 0.022u(B)
C190 0.022u(B)
C191 0.01u(B)
C192 0.01u(B)
C193 0.01u(B)

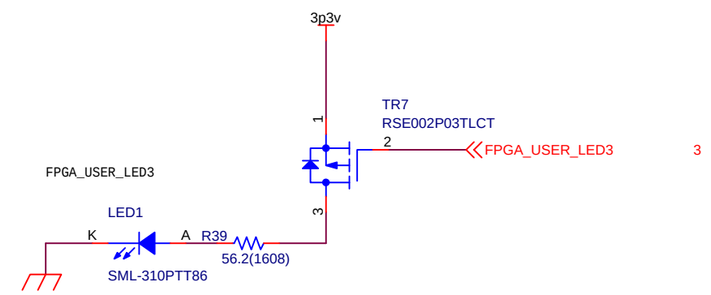
mPRESSION
The Solutions by Macnica Group

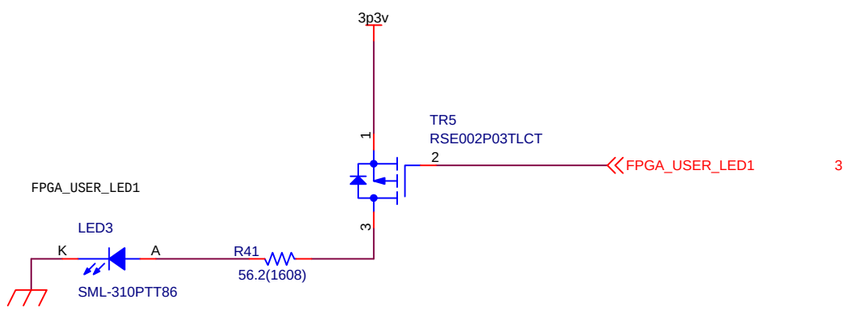
Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 24 of 36	

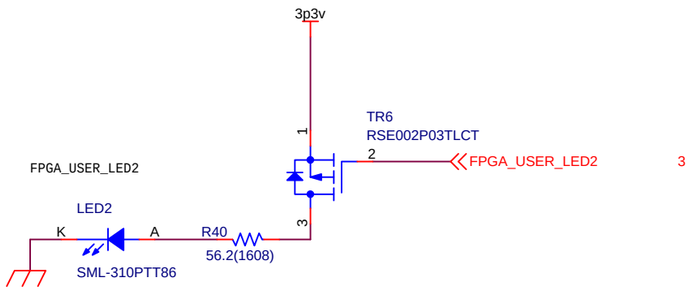
LED & SW

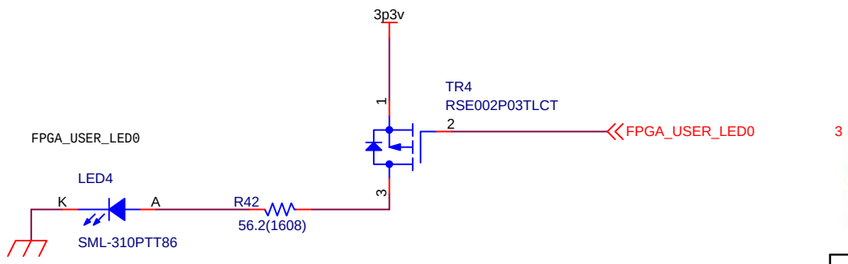










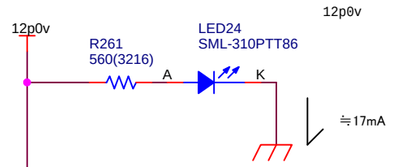


mPRESSION
The Solutions by Macnica Group

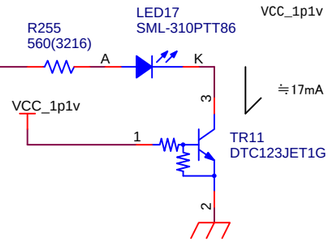
Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 25 of 36	

POWER LED

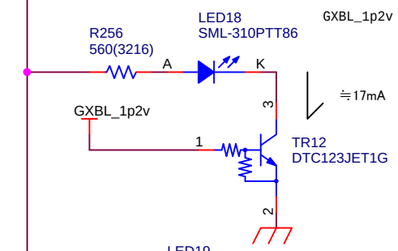
12p0v



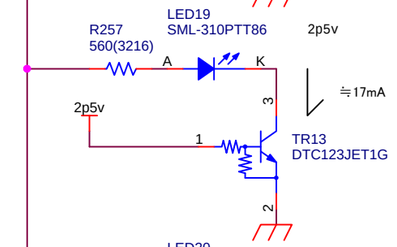
VCC_1p1v



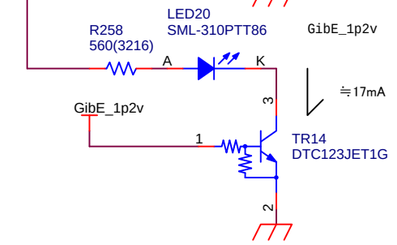
GXBL_1p2v



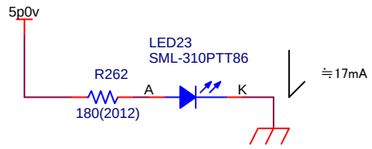
2p5v



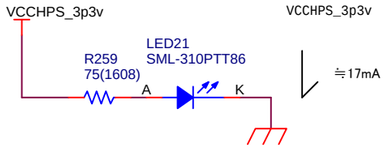
GibE_1p2v



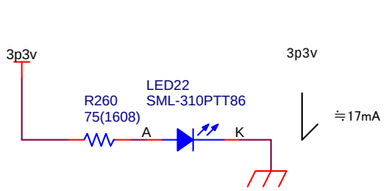
5p0v



VCCHPS_3p3v



3p3v

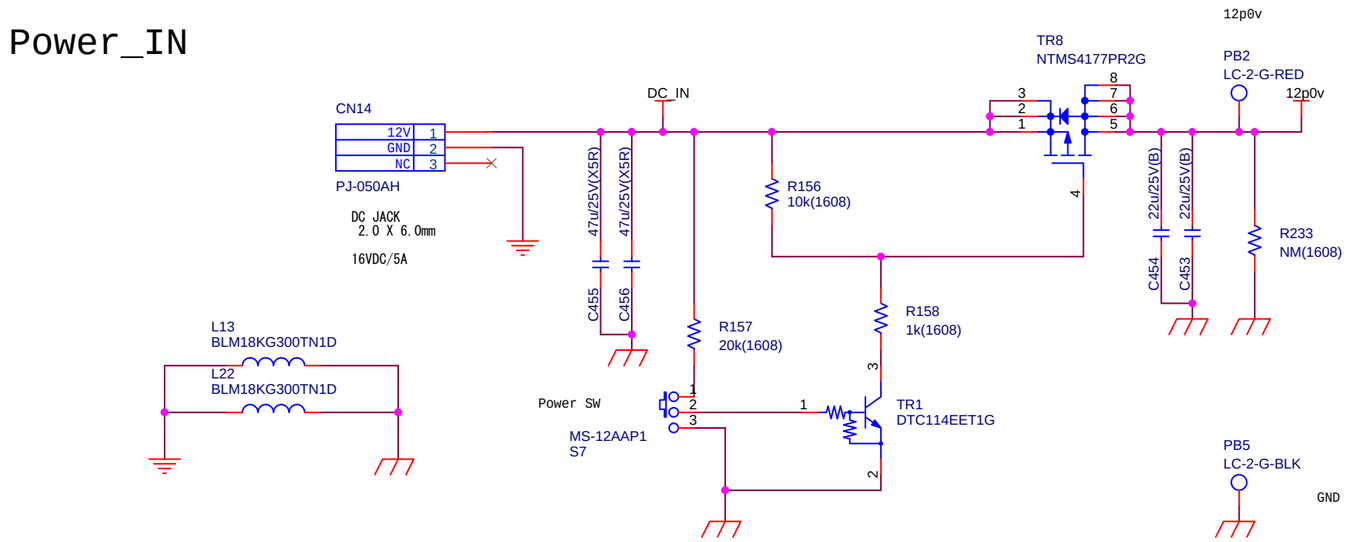


mPRESSION
The Solutions by Macnica Group

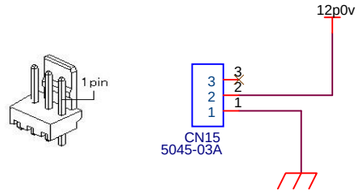
Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 26 of 36	

Power_IN/FAN CON

Power_IN



FAN



note:
HEAT SINK & FAN
->ALPHA : FSR40-8M42
push pin : S001YZ1P
spring : S001YJ0D
Thermal Pad :S001Z03F(T-PCM905C-20S)

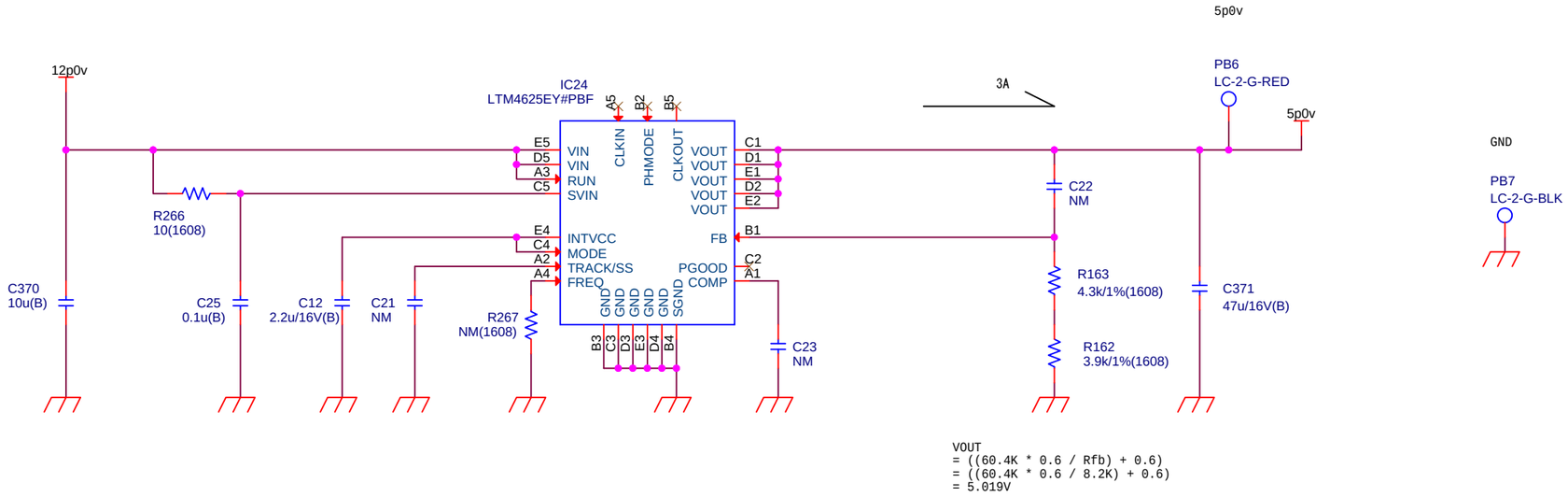
FAN CON mating
Molex : 5051-03
5159PBT

mPRESSION
The Solutions by Macnica Group

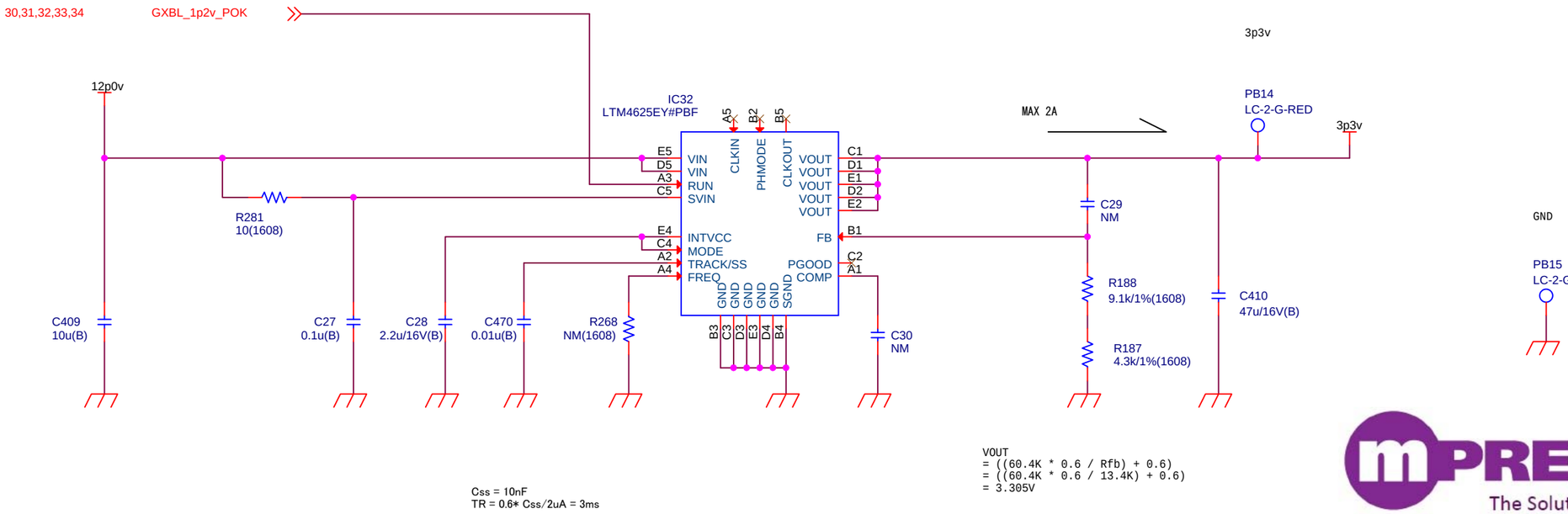
Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 27 of 36	

Power : 5.0V / 3.3V

5.0V



3.3V

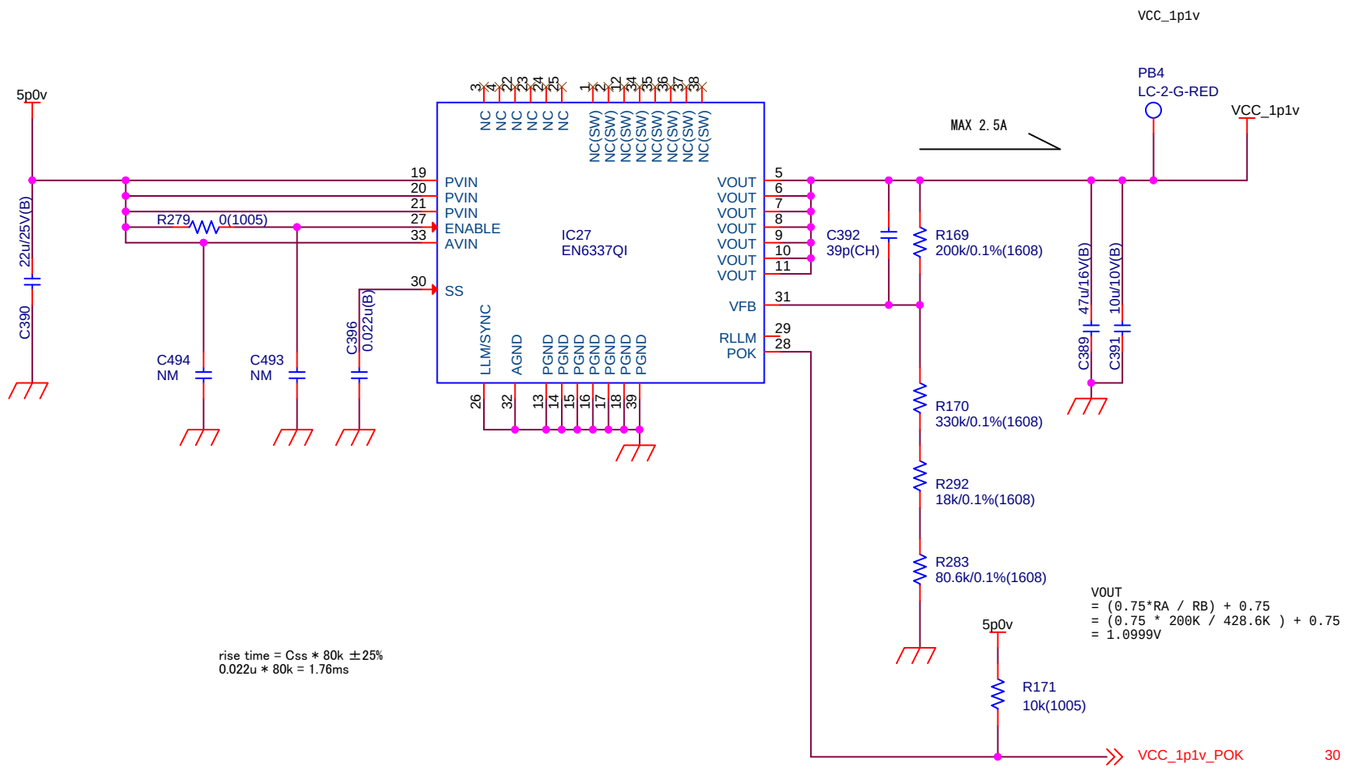


mPRESSION
The Solutions by Macnica Group

Title	Sodia	
Size A3	Document Number ASC001	Rev C
Date: Wednesday, November 21, 2018	Sheet 28 of 36	

Power : 1.1V

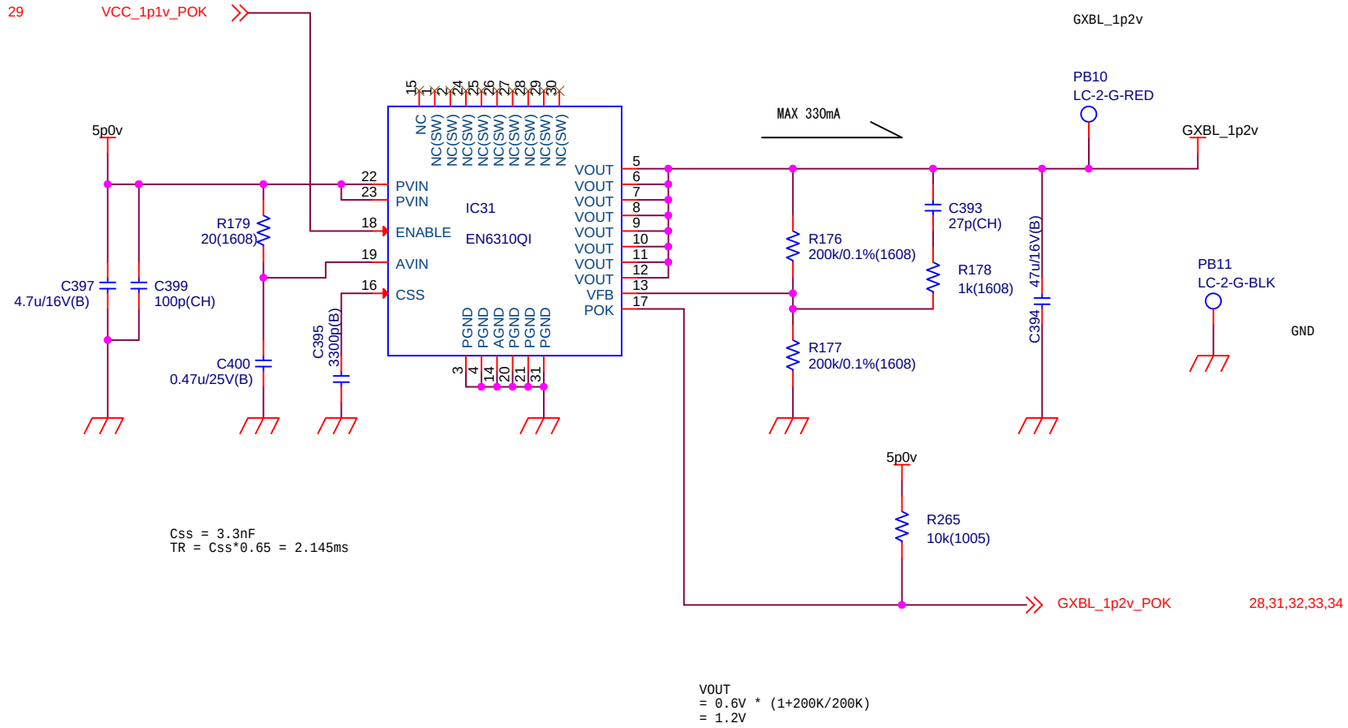
1.1V



Title	Sodia	
Size A3	Document Number ASC001	Rev C
Date: Wednesday, November 21, 2018	Sheet 29 of 36	

Power : 1.2V

1.2V

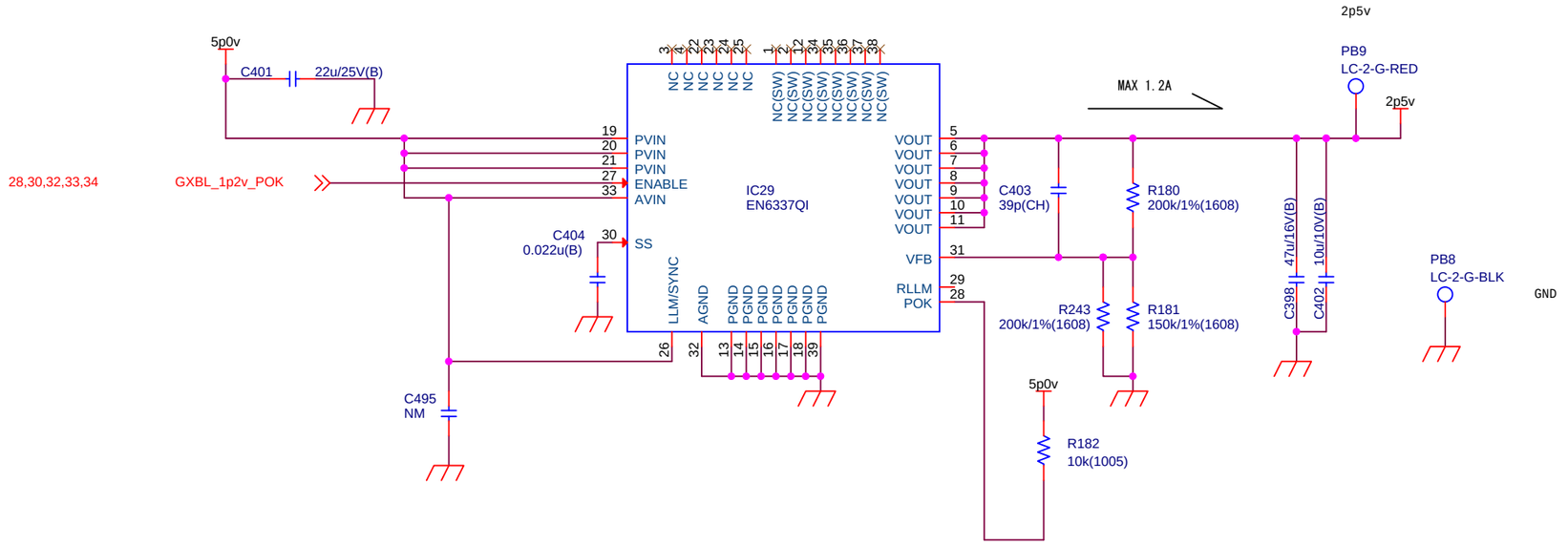


mPRESSION
The Solutions by Macnica Group

Title: Sodia			
Size: A3	Document Number: ASC001		Rev: C
Date: Wednesday, November 21, 2018	Sheet 30 of 36		

Power : 2.5V

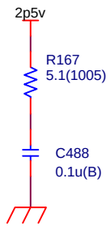
2.5V



rise time = Css * 80k ±25%
0.022u * 80k = 1.76ms

VOUT --- {RB = rb1 // rb2 = 200K // 150K = 85.714K}
= (0.75*RA / RB) + 0.75
= (0.75 * 200K / 85.7K) + 0.75
= 2.500V

Resonance measures of power plane

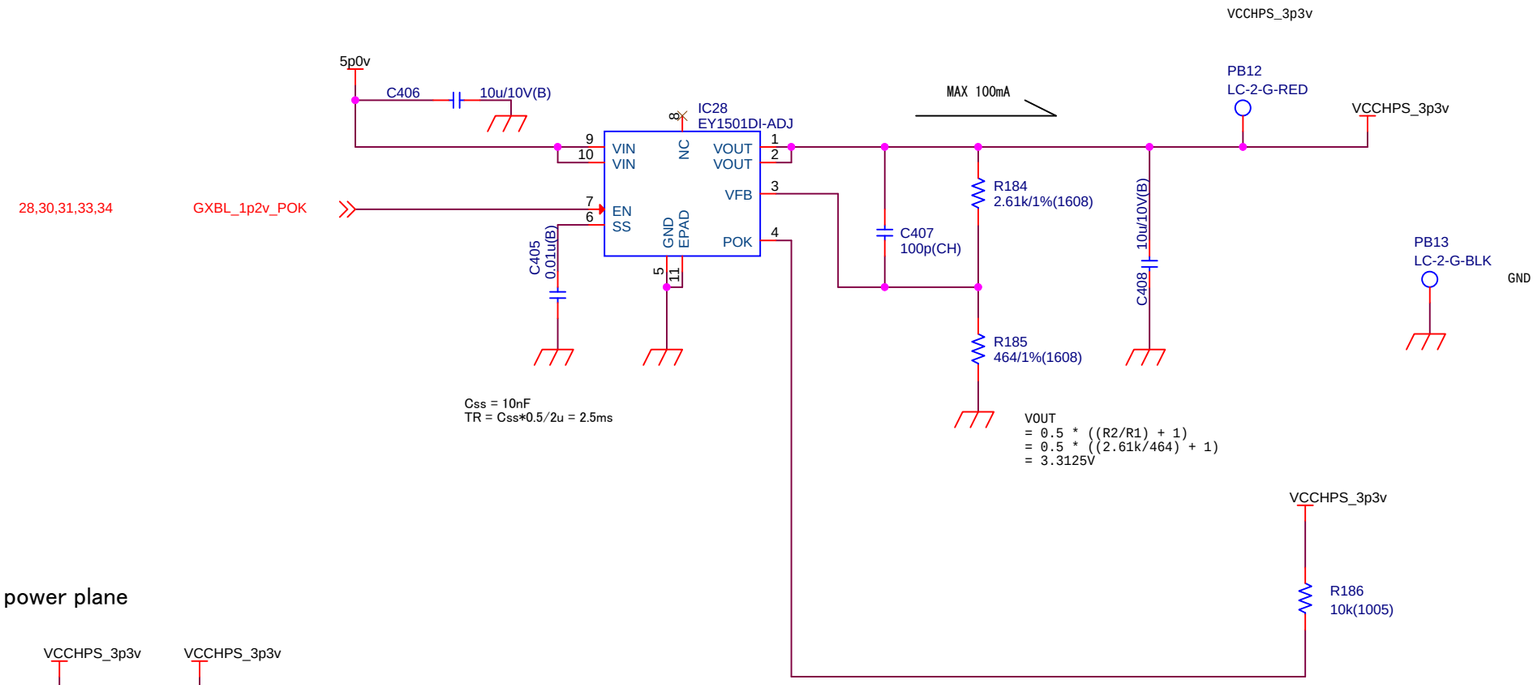


mPRESSION
The Solutions by Macnica Group

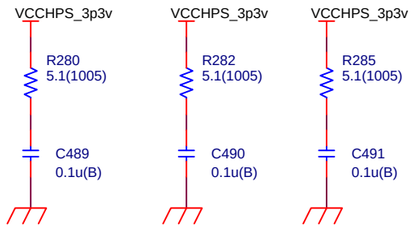
Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 31 of 36	

Power : 3.3V

3.3V



Resonance measures of power plane

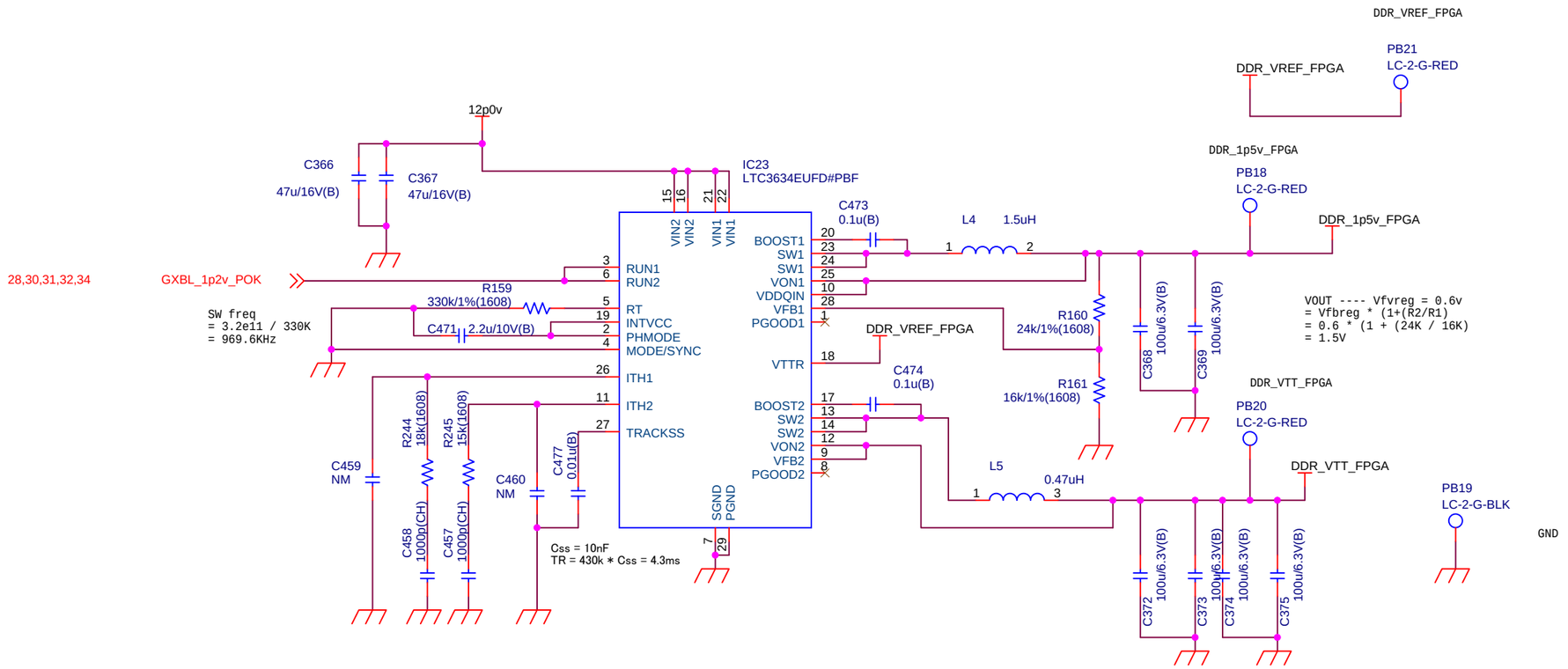


mPRESSION
The Solutions by Macnica Group

Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 32 of 36	

Power : 1.5V for DDR_FPGA

1.5V for DDR_FPGA

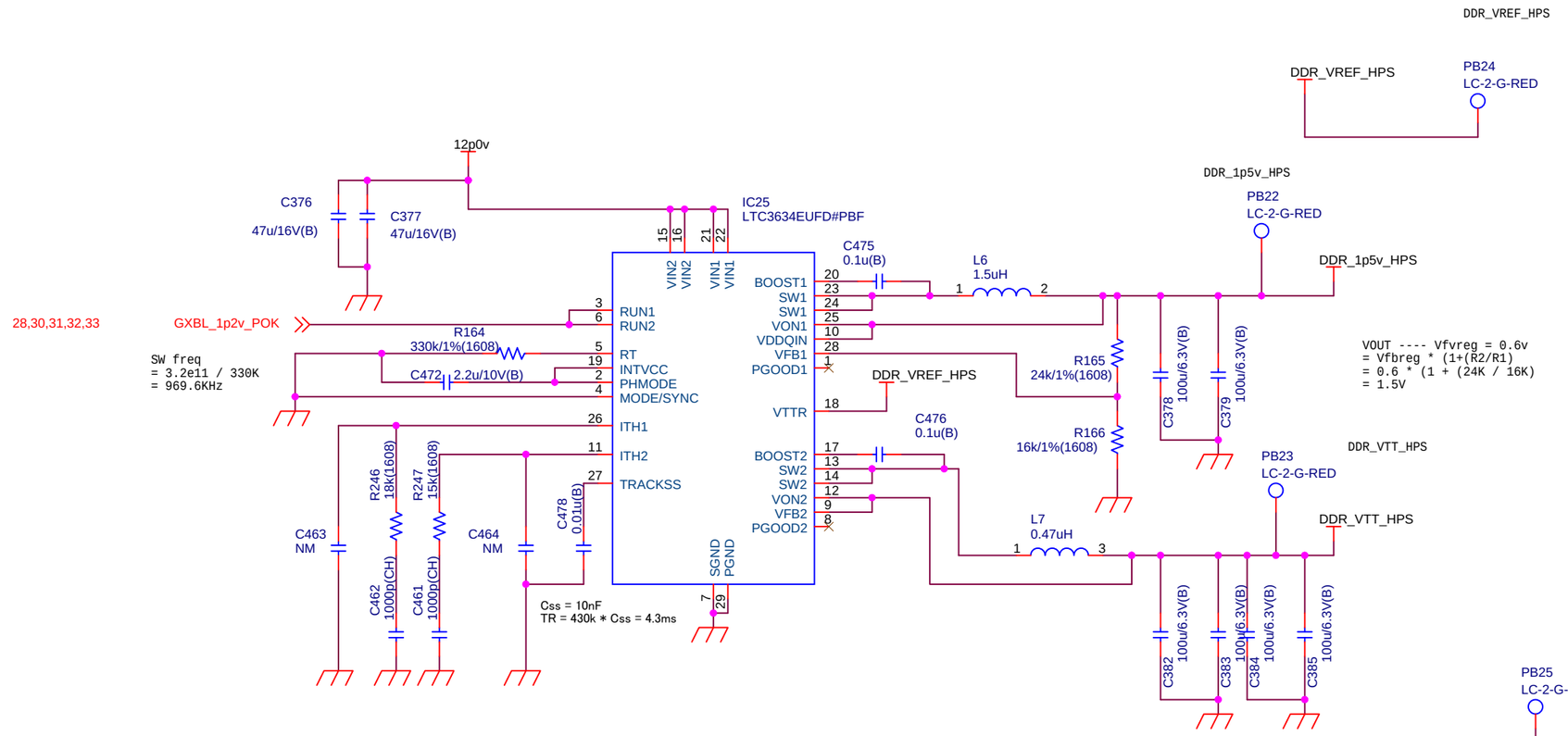


mPRESSION
The Solutions by Macnica Group

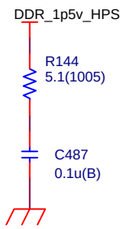
Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 33 of 36	

Power : 1.5V for DDR_HPS

1.5V for DDR_HPS



Resonance measures of power plane

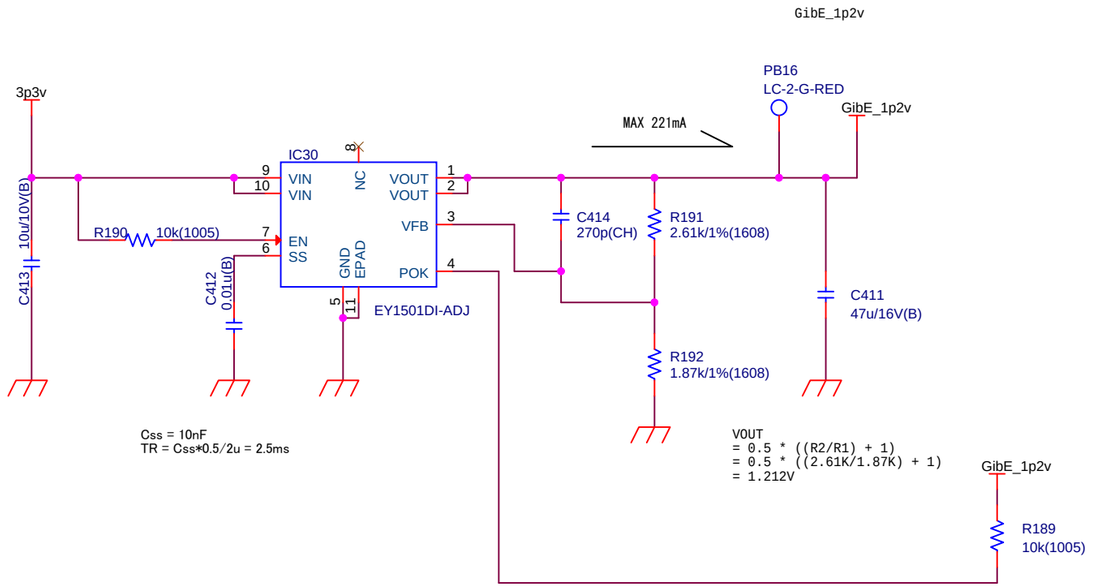


mPRESSION
The Solutions by Macnica Group

Title: Sodia		
Size: A3	Document Number: ASC001	Rev: C
Date: Wednesday, November 21, 2018	Sheet 34 of 36	

Power : 1.2V for Gib ETH

1.2V for Gib ETH



mPRESSION
The Solutions by Macnica Group

Title: Sodia			
Size: A3	Document Number: ASC001		Rev: C
Date: Wednesday, November 21, 2018		Sheet 35 of 36	

History

REV	DATE	PAGES	DESCRIPTION
A	02/03/2016	Page 15	Change Component BT1 SMTU1225-LF to SMTU1225-TR Battery CR1225 to BR-1225/BK
		Page 27	Change Component S7 MS12ANW03 to MS-12AAP1
B	06/07/2017	Page 14	Change Component IC16 N25Q512A83GSF40F to MT25QL512ABB8ESF-0SIT
C	11/21/2018	Page 12	Change Component IC9/10/11 MT41K256M16LY-107:N to MT41K256M16TW-107:P
		Page 19	Modified Implementation C1000

mPRESSION
The Solutions by Macnica Group

Title: Sodia			
Size: A3	Document Number: ASC001		Rev: C
Date: Wednesday, November 21, 2018	Sheet 36 of 36		