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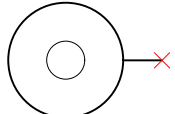
C

C

D

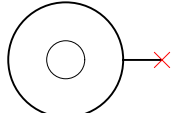
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U\_A-Headers  
A-Headers.SchDoc



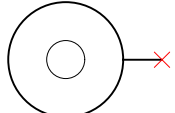
Mount.Hole 2mm (unplated)

U\_FPGA  
FPGA.SchDoc



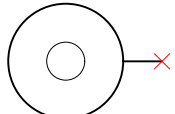
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U\_PowerSupply  
PowerSupply.SchDoc

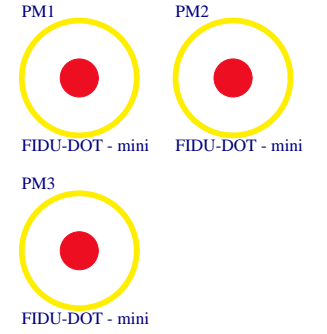


Mount.Hole 2mm (unplated)

U\_FTDI  
FTDI.SchDoc



Mount.Hole 2mm (unplated)



LOGO1

TE Logo PRINT Layer

LOGO PRINT

Serial1

Serial

Serialnumber 6,3 x 6.3mm



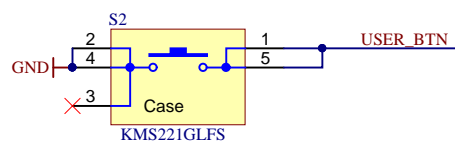
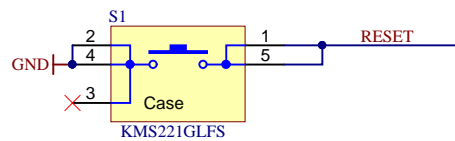
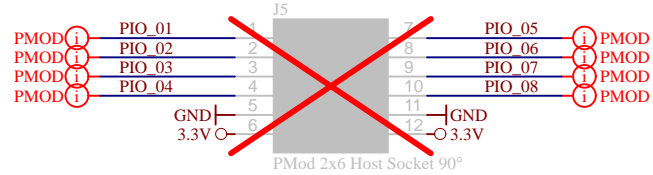
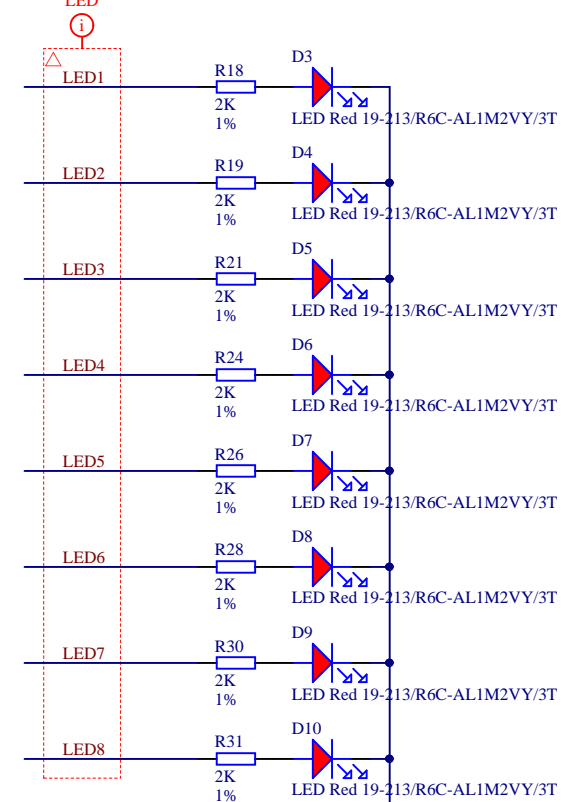
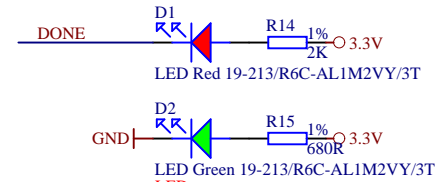
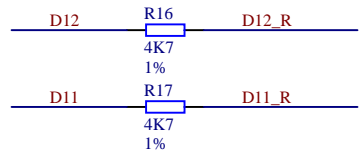
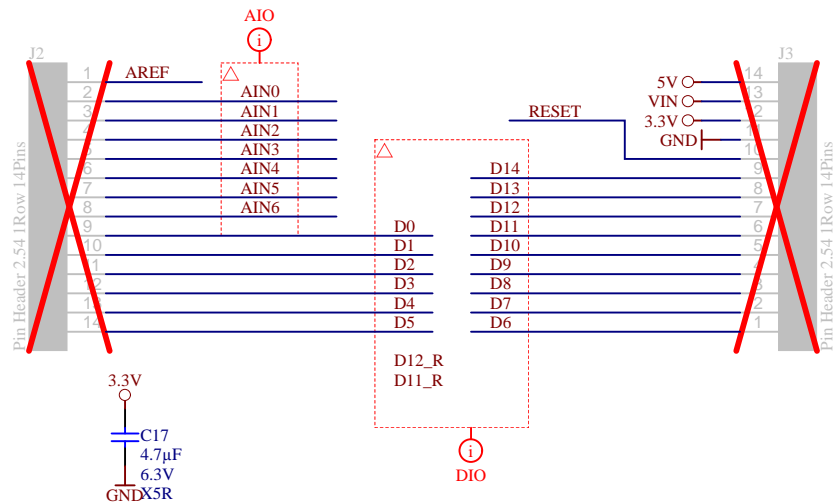
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A4	Number: TEL0001 Default	Rev. 02
Date: 2018-04-11	Copyright: Trenz Electronic GmbH	Page1 of 6
Filename: TEL0001.SchDoc		

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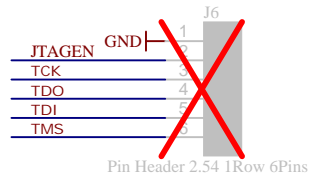
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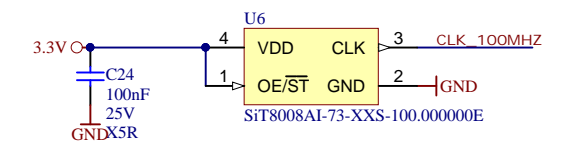
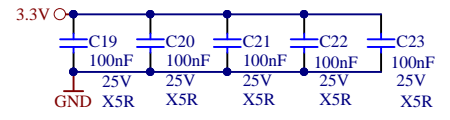
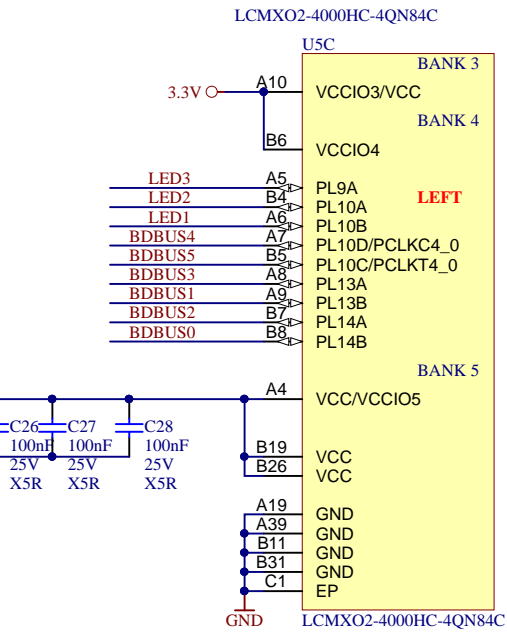
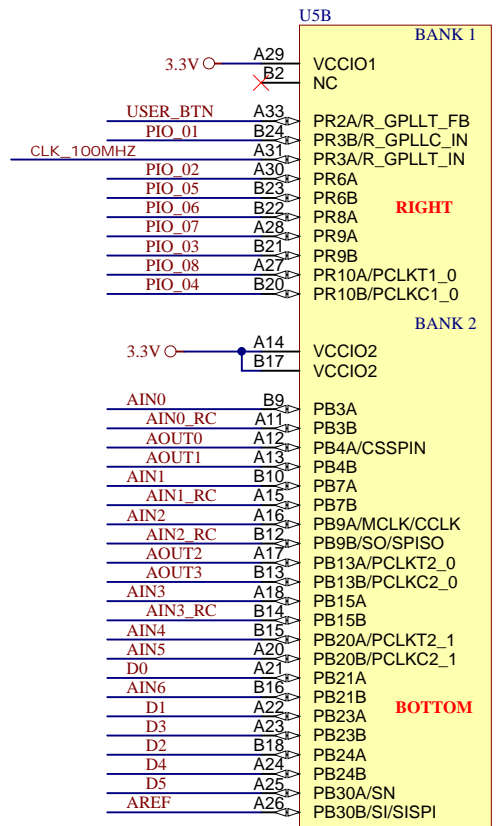
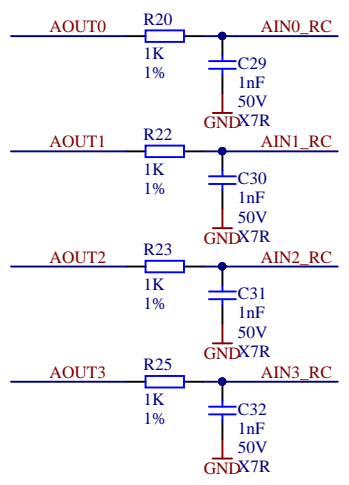
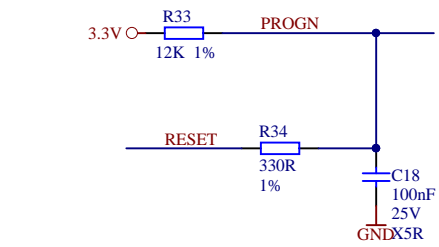
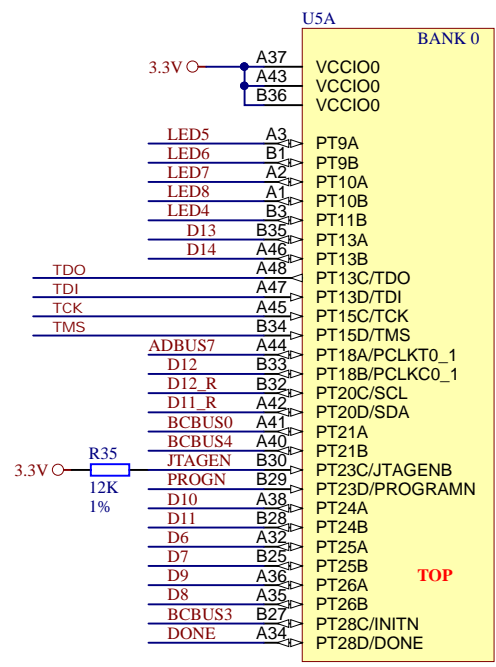
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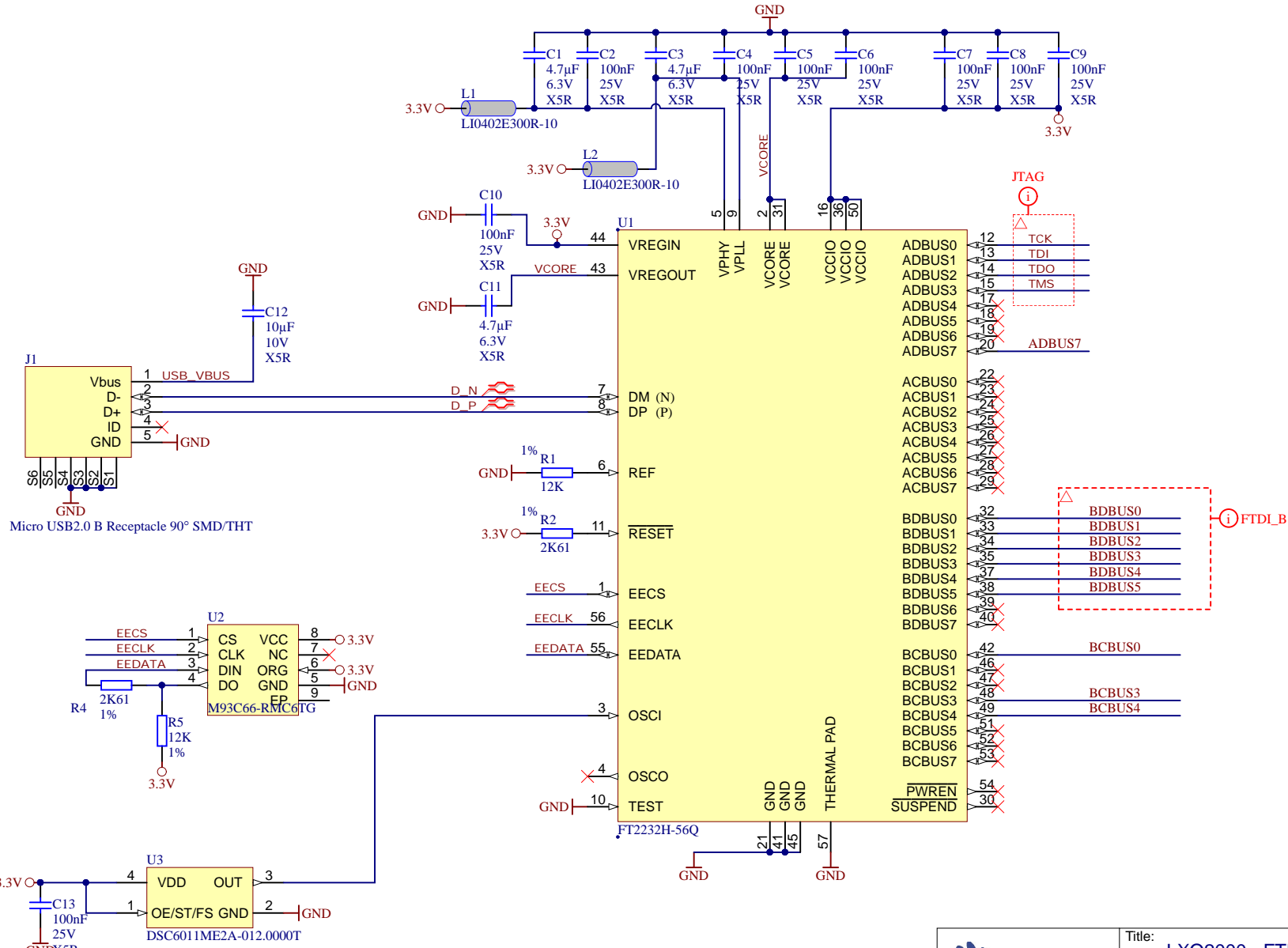
DUAL Function: JTAG or USER I/O if FT2232H not installed



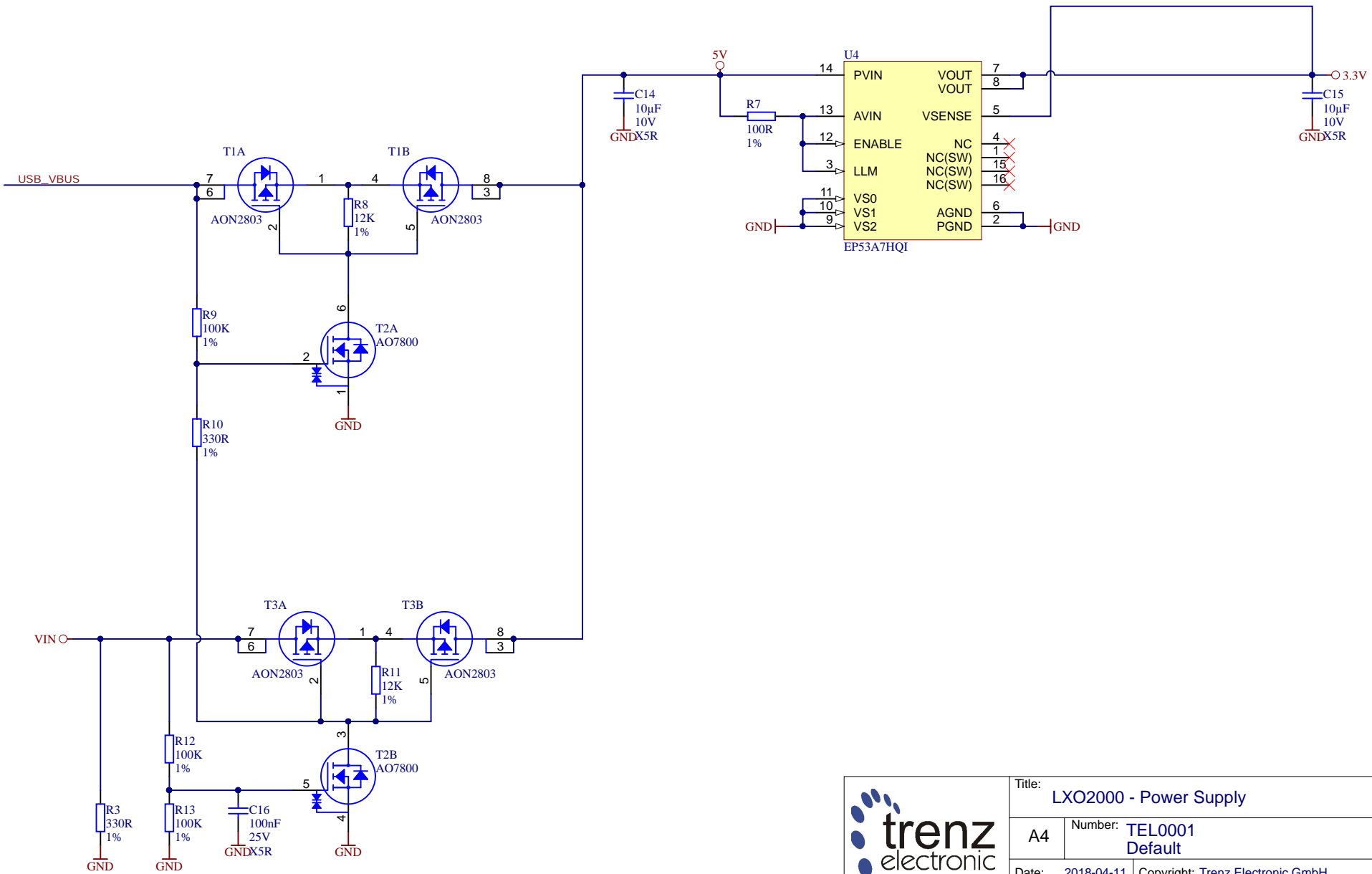
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Filename: A-Headers.SchDoc		



Title: LXO2000 - FPGA		
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Date: 2018-04-11	Copyright: Trenz Electronic GmbH	Page3 of 6
Filename: FPGA.SchDoc		



Title: LXO2000 - FTDI		
A4	Number: TEL0001 Default	Rev. 02
Date: 2018-04-11	Copyright: Trenz Electronic GmbH	Page4 of 6
Filename: FTDI.SchDoc		



Title: LXO2000 - Power Supply		
A4	Number: TEL0001 Default	Rev. 02
Date: 2018-04-11	Copyright: Trenz Electronic GmbH	Page5 of 6
Filename: PowerSupply.SchDoc		

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CHANGES REV01 to REV02

- 1) Removed LIS3DH (U7)
- 2) Changed MEMS clock oscillator (U6) 12MHz -> 100MHz
- 3) Added RC-networks
- 4) Removed connector J4
- 5) Added additional connections between FTDI and FPGA
- 6) Optimized routing & full updated library

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Title: L XO2000			
A4	Number: TEL0001 Default	Rev. 02	
Date: 2018-04-11	Copyright: Trenz Electronic GmbH	Page6 of 6	
Filename: Revision_Changes.SchDoc			

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