PicoZed 7015/7030 SOM
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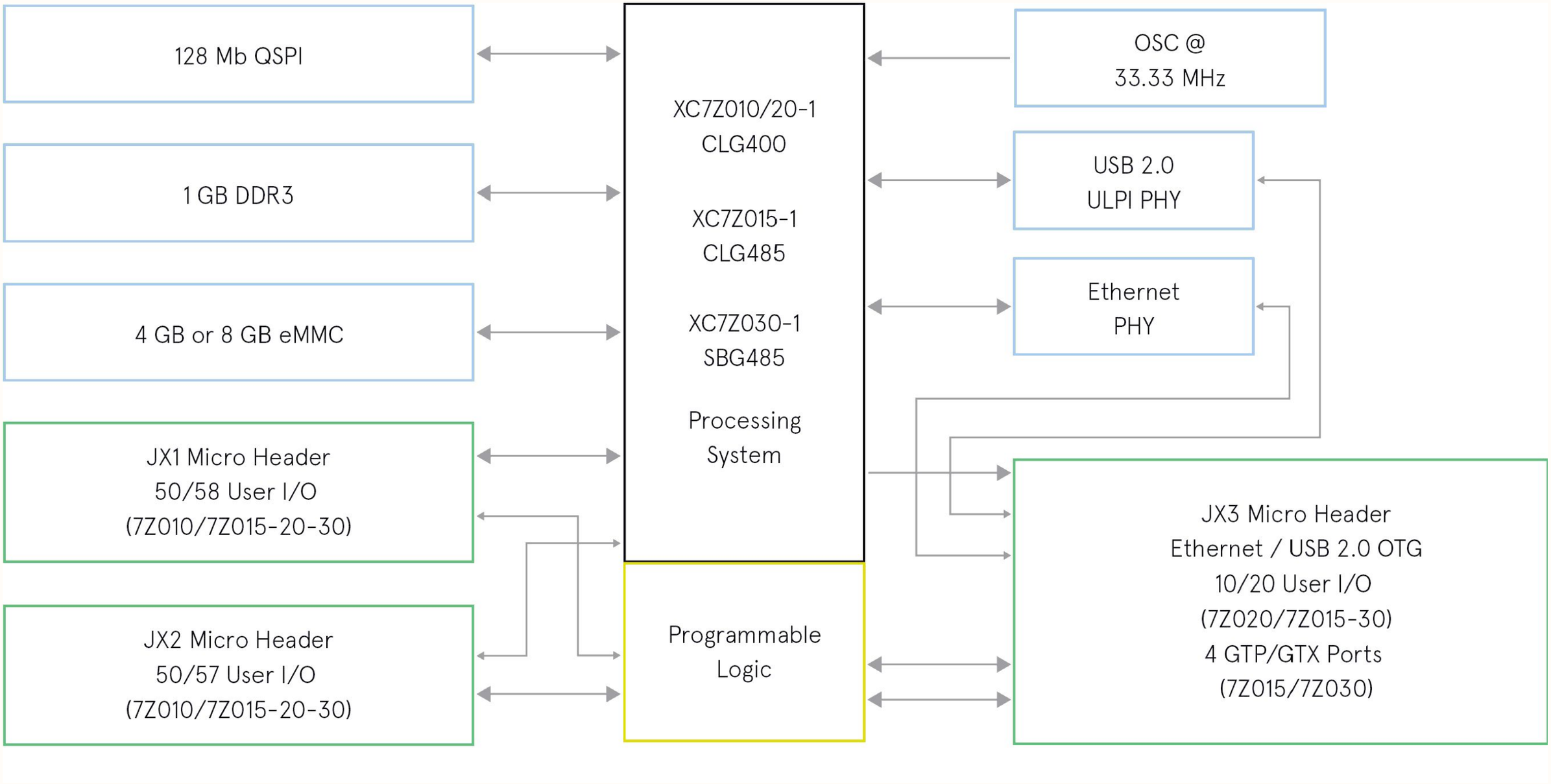
Sheet Name

AVNET® Reach Further™

PicoZed 7015/7030 SOM

Revision E

AVNET® Avnet Engineering Services				
Project Name: PicoZed 7015/7030 SOM		PCB Rev: E	BOM: 01	Variant: 01
Doc Num: SCH-PZ2SOM	Date: 12/18/2017	Time: 11:06:36 AM		
Sheet Title: 01 - Lead Sheet.SchDoc	Size: B	Sheet: 1 of 12		



AVNET Avnet Engineering Services

Project Name: PicoZed 7015/7030 SOM	PCB Rev: E	BOM: 01	Variant: 01
Doc Num: SCH-PZ2SOM	Date: 12/18/2017	Time: 11:06:36 AM	
Sheet Title: 02 - Block Diagram.SchDoc	Size: B	Sheet: 2 of 12	

Zynq PS DDR - Bank 502

U1G
XC7Z015-1CLG485C

BANK 502

PS_DDR_DQ0_502	D22	DDR3_DQ0
PS_DDR_DQ1_502	C20	DDR3_DQ1
PS_DDR_DQ2_502	B21	DDR3_DQ2
PS_DDR_DQ3_502	D20	DDR3_DQ3
PS_DDR_DQ4_502	E20	DDR3_DQ4
PS_DDR_DQ5_502	E22	DDR3_DQ5
PS_DDR_DQ6_502	F21	DDR3_DQ6
PS_DDR_DQ7_502	F22	DDR3_DQ7
PS_DDR_DQ8_502	G21	DDR3_DQ8
PS_DDR_DQ9_502	G22	DDR3_DQ9
PS_DDR_DQ10_502	J22	DDR3_DQ10
PS_DDR_DQ11_502	J21	DDR3_DQ11
PS_DDR_DQ12_502	J20	DDR3_DQ12
PS_DDR_DQ13_502	K22	DDR3_DQ13
PS_DDR_DQ14_502	J23	DDR3_DQ14
PS_DDR_DQ15_502	K20	DDR3_DQ15
PS_DDR_DQ16_502	M22	DDR3_DQ16
PS_DDR_DQ17_502	L20	DDR3_DQ17
PS_DDR_DQ18_502	N20	DDR3_DQ18
PS_DDR_DQ19_502	L22	DDR3_DQ19
PS_DDR_DQ20_502	R20	DDR3_DQ20
PS_DDR_DQ21_502	L21	DDR3_DQ21
PS_DDR_DQ22_502	M21	DDR3_DQ22
PS_DDR_DQ23_502	R22	DDR3_DQ23
PS_DDR_DQ24_502	Y20	DDR3_DQ24
PS_DDR_DQ25_502	U22	DDR3_DQ25
PS_DDR_DQ26_502	AA22	DDR3_DQ26
PS_DDR_DQ27_502	U21	DDR3_DQ27
PS_DDR_DQ28_502	W22	DDR3_DQ28
PS_DDR_DQ29_502	W20	DDR3_DQ29
PS_DDR_DQ30_502	V20	DDR3_DQ30
PS_DDR_DQ31_502	Y22	DDR3_DQ31

DDR_D

PS_DDR_A0_502	M19	DDR3_A0
PS_DDR_A1_502	M18	DDR3_A1
PS_DDR_A2_502	K19	DDR3_A2
PS_DDR_A3_502	L19	DDR3_A3
PS_DDR_A4_502	K17	DDR3_A4
PS_DDR_A5_502	K18	DDR3_A5
PS_DDR_A6_502	J16	DDR3_A6
PS_DDR_A7_502	J17	DDR3_A7
PS_DDR_A8_502	J18	DDR3_A8
PS_DDR_A9_502	H18	DDR3_A9
PS_DDR_A10_502	J20	DDR3_A10
PS_DDR_A11_502	G18	DDR3_A11
PS_DDR_A12_502	H19	DDR3_A12
PS_DDR_A13_502	F19	DDR3_A13
PS_DDR_A14_502	G19	DDR3_A14

DDR_AC

DDR_DQ

PS_DDR_DQS_P0_502	C21	DDR3_DQS0_P
PS_DDR_DQS_N0_502	D21	DDR3_DQS0_N
PS_DDR_DQS_P1_502	H21	DDR3_DQS1_P
PS_DDR_DQS_N1_502	J21	DDR3_DQS1_N
PS_DDR_DQS_P2_502	N21	DDR3_DQS2_P
PS_DDR_DQS_N2_502	P21	DDR3_DQS2_N
PS_DDR_DQS_P3_502	V21	DDR3_DQS3_P
PS_DDR_DQS_N3_502	W21	DDR3_DQS3_N

PS_DDR_CKP_502	N19	DDR3_CK0_P
PS_DDR_CKN_502	N18	DDR3_CK0_N

PS_DDR_BA0_502	L16	DDR3_BA0
PS_DDR_BA1_502	L17	DDR3_BA1
PS_DDR_BA2_502	M17	DDR3_BA2

DDR_AC

PS_DDR_DM0_502	B22	DDR3_DM0
PS_DDR_DM1_502	H20	DDR3_DM1
PS_DDR_DM2_502	P22	DDR3_DM2
PS_DDR_DM3_502	AA21	DDR3_DM3

DDR_DM

PS_DDR_CS_B_502	P17	DDR3_CS#
PS_DDR_WE_B_502	R19	DDR3_WE#
PS_DDR_CAS_B_502	P20	DDR3_CAS#
PS_DDR_RAS_B_502	R18	DDR3_RAS#
PS_DDR_CKE_502	T19	DDR3_CKE
PS_DDR_ODT_502	P18	DDR3_ODT

DDR_AC

PS_DDR_DRST_B_502	F20	DDR3_RESET#

PS_DDR_VRP_502	N16	R3	80.6	GND
PS_DDR_VRN_502	M16	R7	80.6	

VCCO_DDR3

IC SOC CORTEX-A9, Zynq-7000, 485BGA

DDR_D_BL0 — DDR3_DQ[7..0]
DDR_D_BL1 — DDR3_DQ[15..8]
DDR_D_BL2 — DDR3_DQ[23..16]
DDR_D_BL3 — DDR3_DQ[31..24]

VCCO_DDR3

C5	0.1uF	
C4	0.1uF	
C3	0.1uF	
C2	0.1uF	
C1	47uF	GND
C11	10000pF	
C12	10000pF	
C13	10000pF	
C14	10000pF	GND
C24	47uF	
C25	0.1uF	
C26	0.1uF	
C27	0.1uF	
C28	0.1uF	GND
C33	10000pF	
C34	10000pF	
C35	10000pF	
C36	10000pF	GND

DDR_PWR

VTTREF
C38 10000pF GND

U2
MT41K256M16TW-107:P

DDR3_A0	N3	A0
DDR3_A1	P7	A1
DDR3_A2	P3	A2
DDR3_A3	N2	A3
DDR3_A4	P8	A4
DDR3_A5	P2	A5
DDR3_A6	R8	A6
DDR3_A7	R2	A7
DDR3_A8	T8	A8
DDR3_A9	R3	A9
DDR3_A10	L7	A10/AP
DDR3_A11	R7	A11
DDR3_A12	N7	A12/BC#
DDR3_A13	T3	A13
DDR3_A14	T7	A14
DDR3_BA0	M2	BA0
DDR3_BA1	N8	BA1
DDR3_BA2	M3	BA2
DDR3_CS#	L2	CS#
DDR3_WE#	L3	WE#
DDR3_CAS#	K3	CAS#
DDR3_RAS#	J3	RAS#
DDR3_CKE	K9	CKE
DDR3_CK0_P	J7	CK
DDR3_CK0_N	K7	CK#
DDR3_RESET#	T2	RESET#
	L9	n/c
	L3	n/c
	J9	n/c
	J1	n/c

DQ0	E3	DDR3_DQ0
DQ1	F7	DDR3_DQ1
DQ2	F2	DDR3_DQ2
DQ3	F8	DDR3_DQ3
DQ4	H3	DDR3_DQ4
DQ5	H8	DDR3_DQ5
DQ6	G2	DDR3_DQ6
DQ7	H7	DDR3_DQ7
DQ8	D7	DDR3_DQ8
DQ9	C3	DDR3_DQ9
DQ10	C8	DDR3_DQ10
DQ11	C2	DDR3_DQ11
DQ12	A7	DDR3_DQ12
DQ13	A2	DDR3_DQ13
DQ14	B8	DDR3_DQ14
DQ15	A3	DDR3_DQ15
UDM	D3	DDR3_DM1
LDM	E7	DDR3_DM0
UDQS	C7	DDR3_DQS1_P
UDQS#	B7	DDR3_DQS1_N
LDQS	F3	DDR3_DQS0_P
LDQS#	G3	DDR3_DQS0_N
ODT	K1	DDR3_ODT
ZQ	L8	R1 240
n/c	M7	

GND

Layout Note:
Use Fly-by routing and termination for DDR3 control signals.
Resistors should be placed past the last memory IC & as close to the device as possible.

Layout Note:
DDR3 trace lengths must include Zynq package flight times.
See UG933 and Layout Guidelines.

Layout Note:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms

DDR_T

DDR3_A14	DDR3_T_A14	R4	40.2
DDR3_A13	DDR3_T_A13	R5	40.2
DDR3_A12	DDR3_T_A12	R6	40.2
DDR3_A11	DDR3_T_A11	R8	40.2
DDR3_A10	DDR3_T_A10	R9	40.2
DDR3_A9	DDR3_T_A9	R10	40.2
DDR3_A8	DDR3_T_A8	R11	40.2
DDR3_A7	DDR3_T_A7	R12	40.2
DDR3_A6	DDR3_T_A6	R13	40.2
DDR3_A5	DDR3_T_A5	R14	40.2
DDR3_A4	DDR3_T_A4	R15	40.2
DDR3_A3	DDR3_T_A3	R16	40.2
DDR3_A2	DDR3_T_A2	R17	40.2
DDR3_A1	DDR3_T_A1	R18	40.2
DDR3_A0	DDR3_T_A0	R21	40.2
DDR3_BA0	DDR3_T_BA0	R22	40.2
DDR3_BA1	DDR3_T_BA1	R23	40.2
DDR3_BA2	DDR3_T_BA2	R24	40.2
DDR3_CS#	DDR3_T_CS#	R25	40.2
DDR3_WE#	DDR3_T_WE#	R26	40.2
DDR3_CAS#	DDR3_T_CAS#	R27	40.2
DDR3_RAS#	DDR3_T_RAS#	R28	40.2
DDR3_ODT	DDR3_T_ODT	R29	40.2
DDR3_RESET#	DDR3_T_RESET#		
DDR3_CK0_P	DDR3_T_CK0_P		
DDR3_CK0_N	DDR3_T_CK0_N		
DDR3_CKE	DDR3_T_CKE		

DDR3_VTT
R95 4.99K GND
R30 80.6
R31 40.2

NOTE:
RESET# requires a Pull Down resistor through FPGA Configuration. See UG933p62 and Answer Record 55616.

DDR3

VCCO_DDR3

C6	47uF	
C7	0.1uF	
C8	0.1uF	
C9	0.1uF	
C10	0.1uF	GND
C15	10000pF	
C16	10000pF	
C17	10000pF	
C18	10000pF	GND
C19	47uF	
C20	0.1uF	
C21	0.1uF	
C22	0.1uF	
C23	0.1uF	GND
C29	10000pF	
C30	10000pF	
C31	10000pF	
C32	10000pF	GND

DDR_PWR

VTTREF
C37 10000pF GND

U3
MT41K256M16TW-107:P

DDR3_A0	N3	A0
DDR3_A1	P7	A1
DDR3_A2	P3	A2
DDR3_A3	N2	A3
DDR3_A4	P8	A4
DDR3_A5	P2	A5
DDR3_A6	R8	A6
DDR3_A7	R2	A7
DDR3_A8	T8	A8
DDR3_A9	R3	A9
DDR3_A10	L7	A10/AP
DDR3_A11	R7	A11
DDR3_A12	N7	A12/BC#
DDR3_A13	T3	A13
DDR3_A14	T7	A14
DDR3_BA0	M2	BA0
DDR3_BA1	N8	BA1
DDR3_BA2	M3	BA2
DDR3_CS#	L2	CS#
DDR3_WE#	L3	WE#
DDR3_CAS#	K3	CAS#
DDR3_RAS#	J3	RAS#
DDR3_CKE	K9	CKE
DDR3_CK0_P	J7	CK
DDR3_CK0_N	K7	CK#
DDR3_RESET#	T2	RESET#
	L9	n/c
	L3	n/c
	J9	n/c
	J1	n/c

DQ0	E3	DDR3_DQ16
DQ1	F7	DDR3_DQ17
DQ2	F2	DDR3_DQ18
DQ3	F8	DDR3_DQ19
DQ4	H3	DDR3_DQ20
DQ5	H8	DDR3_DQ21
DQ6	G2	DDR3_DQ22
DQ7	H7	DDR3_DQ23
DQ8	D7	DDR3_DQ24
DQ9	C3	DDR3_DQ25
DQ10	C8	DDR3_DQ26
DQ11	C2	DDR3_DQ27
DQ12	A7	DDR3_DQ28
DQ13	A2	DDR3_DQ29
DQ14	B8	DDR3_DQ30
DQ15	A3	DDR3_DQ31
UDM	D3	DDR3_DM3
LDM	E7	DDR3_DM2
UDQS	C7	DDR3_DQS3_P
UDQS#	B7	DDR3_DQS3_N
LDQS	F3	DDR3_DQS2_P
LDQS#	G3	DDR3_DQS2_N
ODT	K1	DDR3_ODT
ZQ	L8	R2 240
n/c	M7	

GND

DDR3 Termination Supply

VCCO_DDR3
R52 10.00K
R96 10.00K
C195 0.1uF GND

U4
NCP51400MNTXG

1	VRI	
2	PVcc	
3	VTT	
4	PGND	
5	VTTS	
10	Vcc	3.3V, C39 4.7uF GND
9	PGOOD	R19 10.00K 3.3V
8	GND	
7	EN	R20 10.00K 3.3V
6	VRO	VTTREF, C42 0.1uF GND
11	PAD	GND

3.3V, C41 10uF, C196 10uF, GND
DDR3_VTT, C199 10uF, C200 10uF, C40 10uF, GND

DDR_PWR

DDR3_VTT
C45 100uF, C46 100uF, C47 4.7uF, C48 4.7uF, C49 0.1uF, C50 0.1uF, C43 10000pF, C44 10000pF
GND

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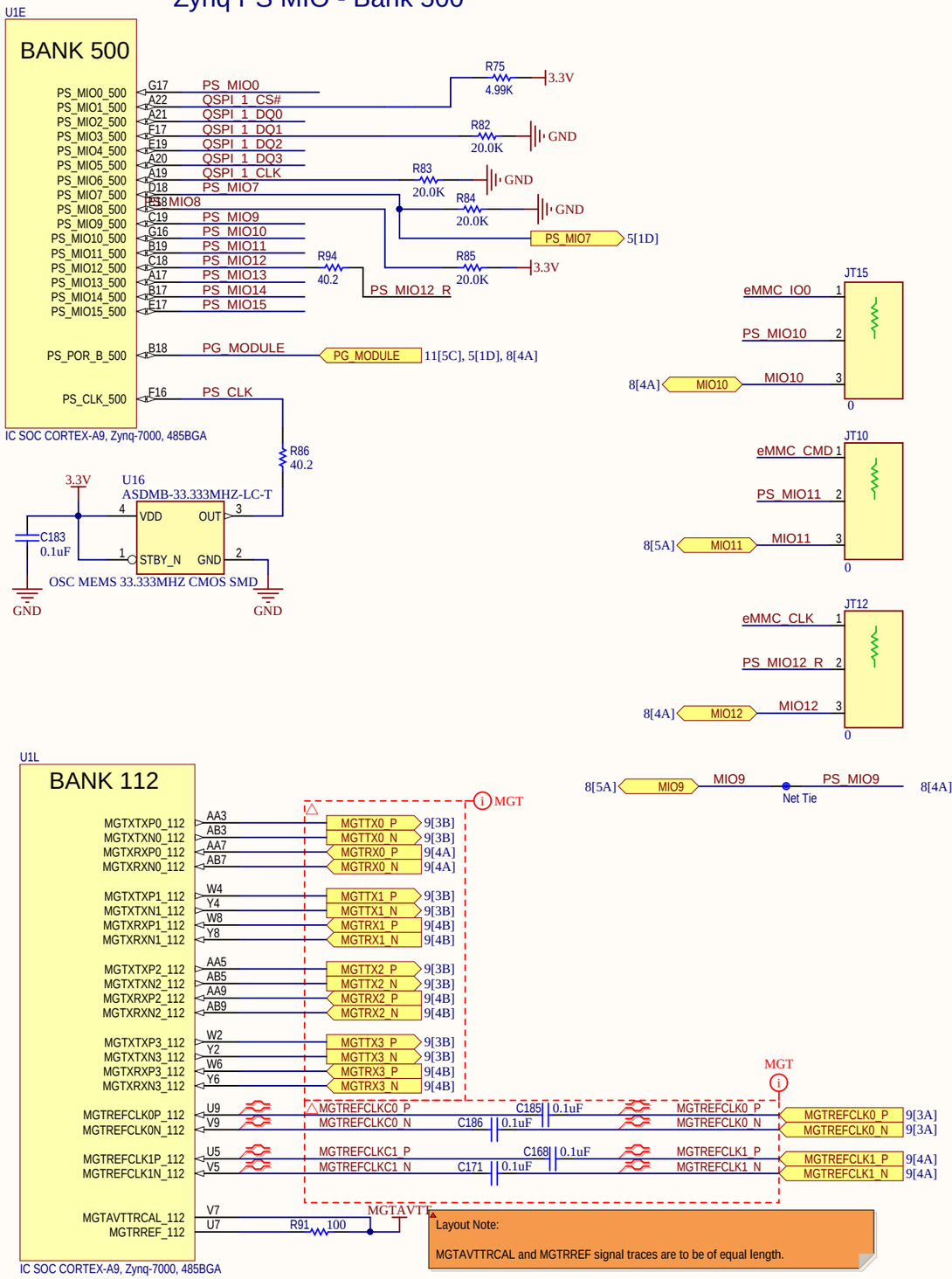
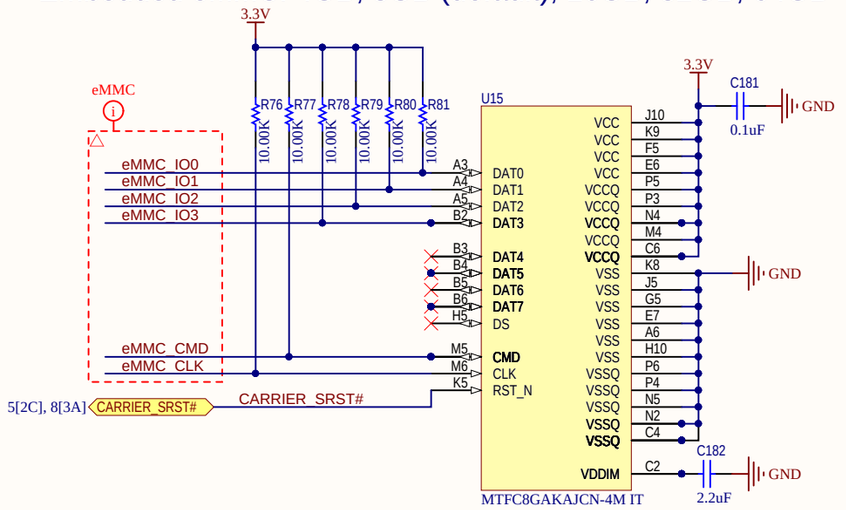
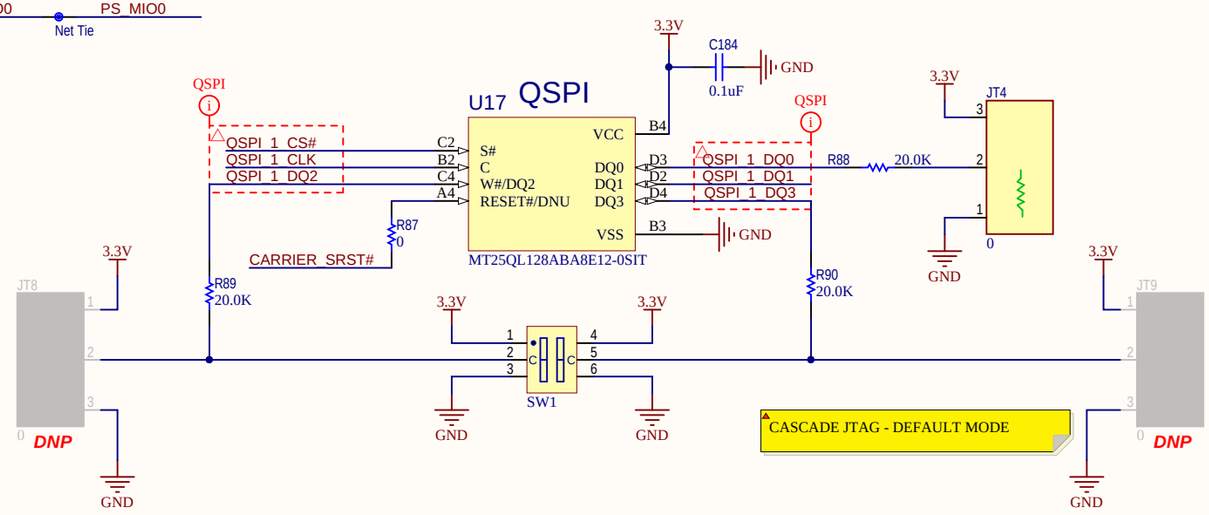
Project Name: PicoZed 7015/7030 SOM	PCB Rev: E	BOM: 01	Variant: 01
Doc Num: SCH-PZ2SOM	Date: 12/18/2017	Time: 11:06:36 AM	
Sheet Title: 03 - DDR3.SchDoc	Size: B	Sheet: 3 of 12	

Zynq PS MIO - Bank 500



Embedded eMMC: 4GB, 8GB (default), 16GB, 32GB, 64GB





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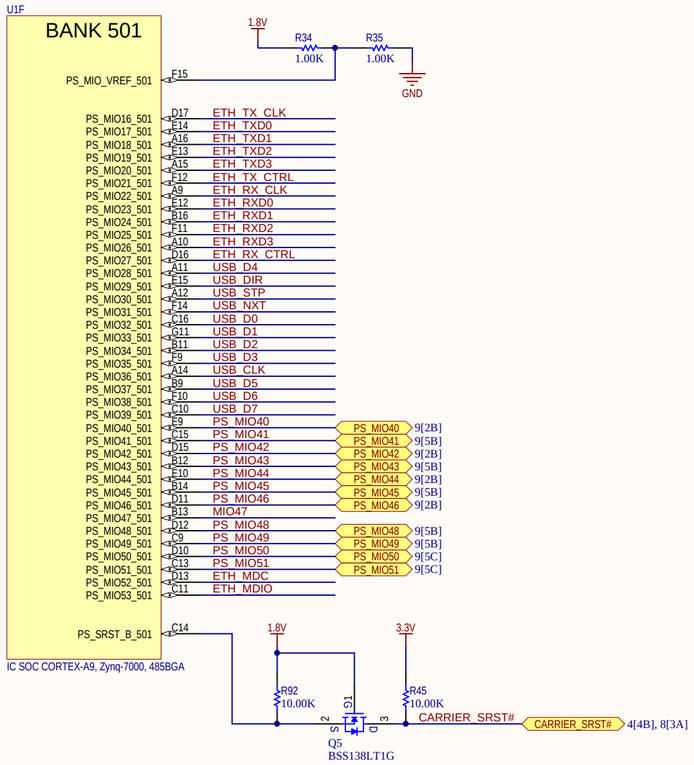
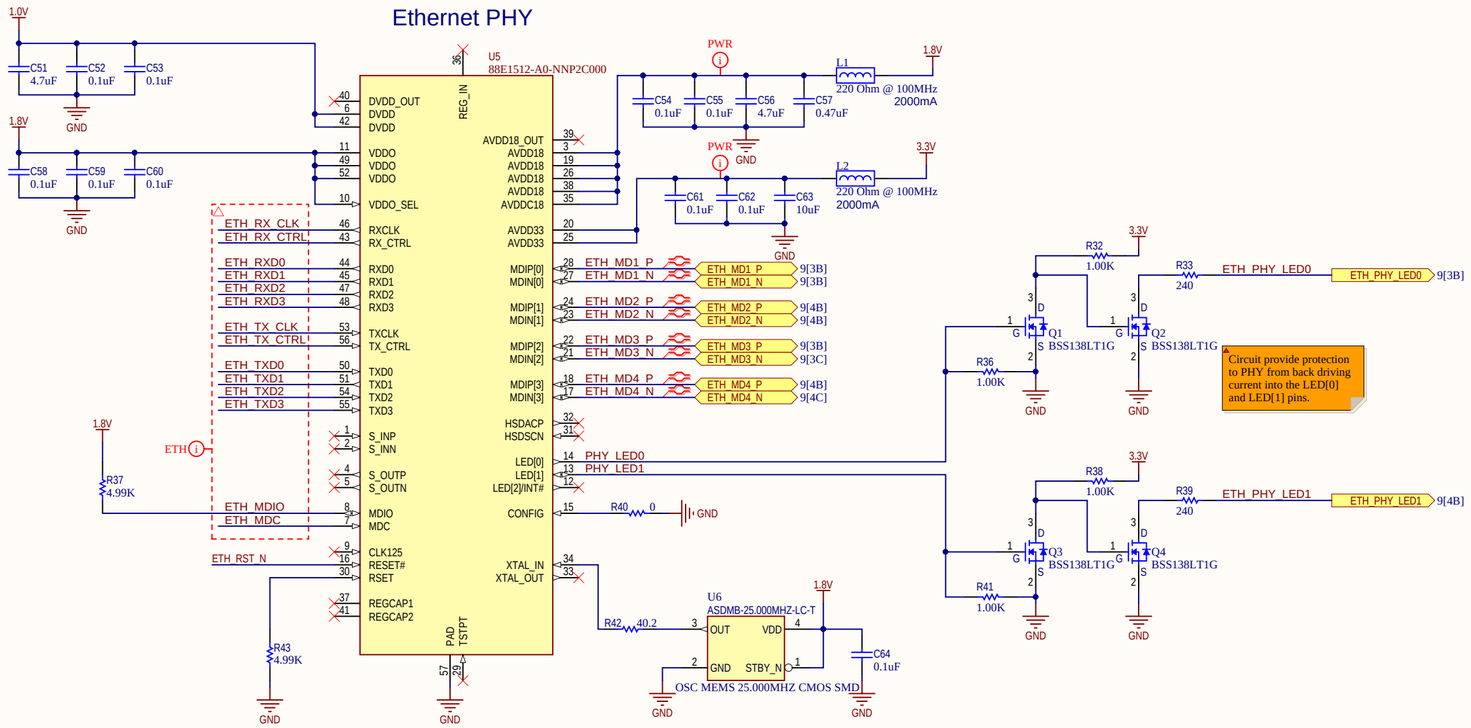
Project Name: PicoZed 7015/7030 SOM	PCB Rev: E	BOM: 01	Variant: 01
Doc Num: SCH-PZ2SOM	Date: 12/18/2017	Time: 11:06:37 AM	
Sheet Title: 04 - GTP, QSPI FLASH, eMMC.SchDoc	Size: B	Sheet: 4 of 12	

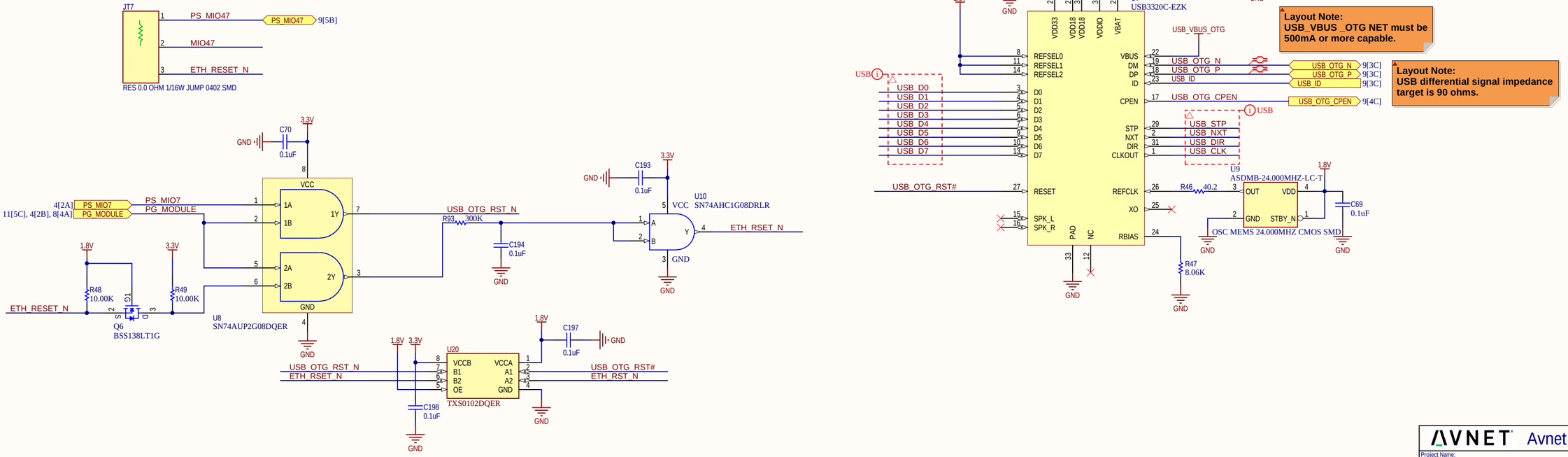
Zynq PS MIO - Bank 501



Ethernet PHY



USB 2.0 OTG



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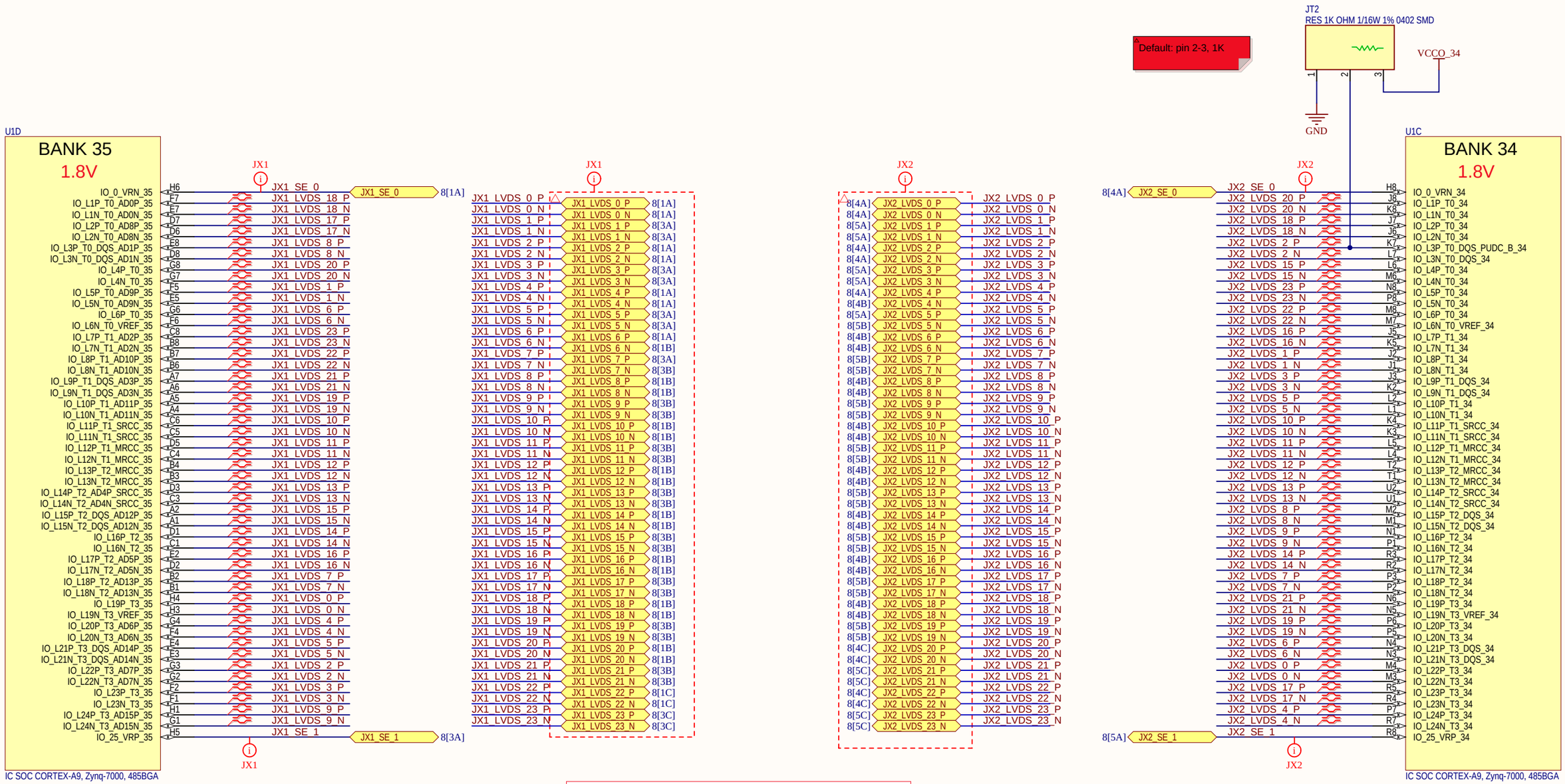
Project Name: PicoZed 7015/7030 SOM	PCB Rev: E	BOM: 01	Variant: 01
Doc Num: SCH-PZ2SOM	Date: 12/18/2017	Time: 11:06:37 AM	
Sheet Title: 05 - ETHERNET, USB.SchDoc	Size: B	Sheet: 5 of 12	



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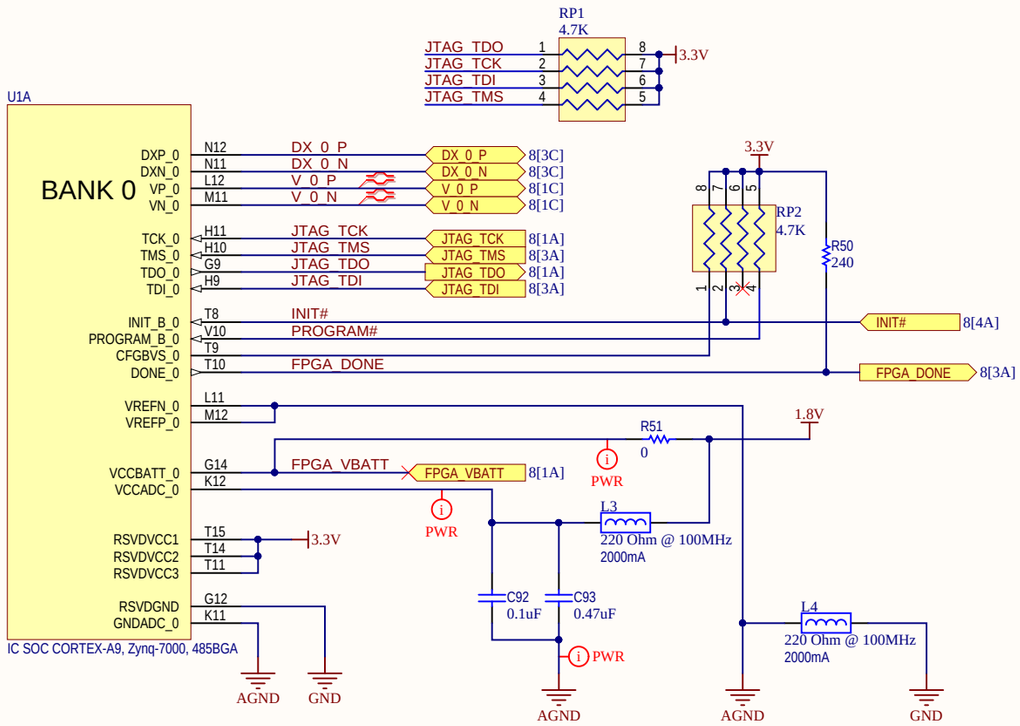
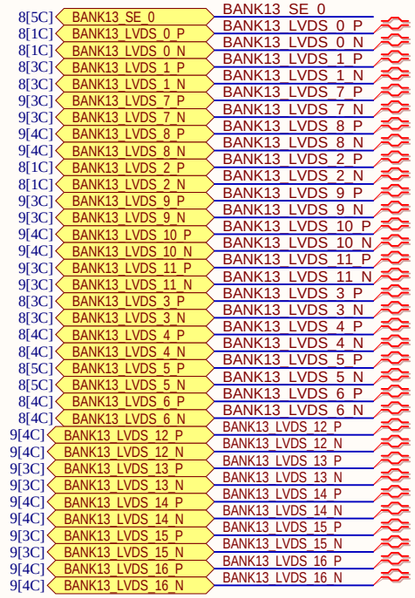
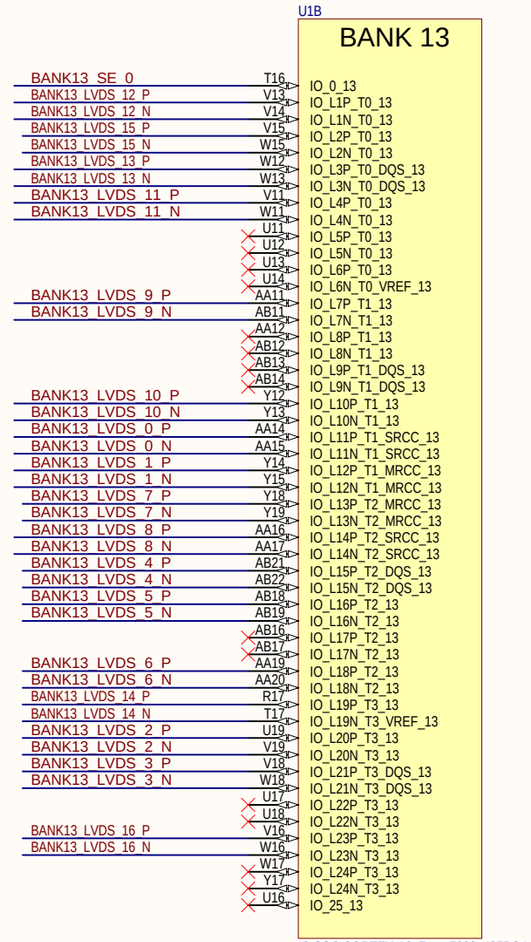
Project Name: PicoZed 7015/7030 SOM	PCB Rev: E / BOM: 01 / Variant: 01
Doc Num: SCH-PZ2SOM	Date: 12/18/2017 Time: 11:06:38 AM
Sheet Title: 06 - BANKS 34 and 35.SchDoc	Size: B Sheet: 6 of 12







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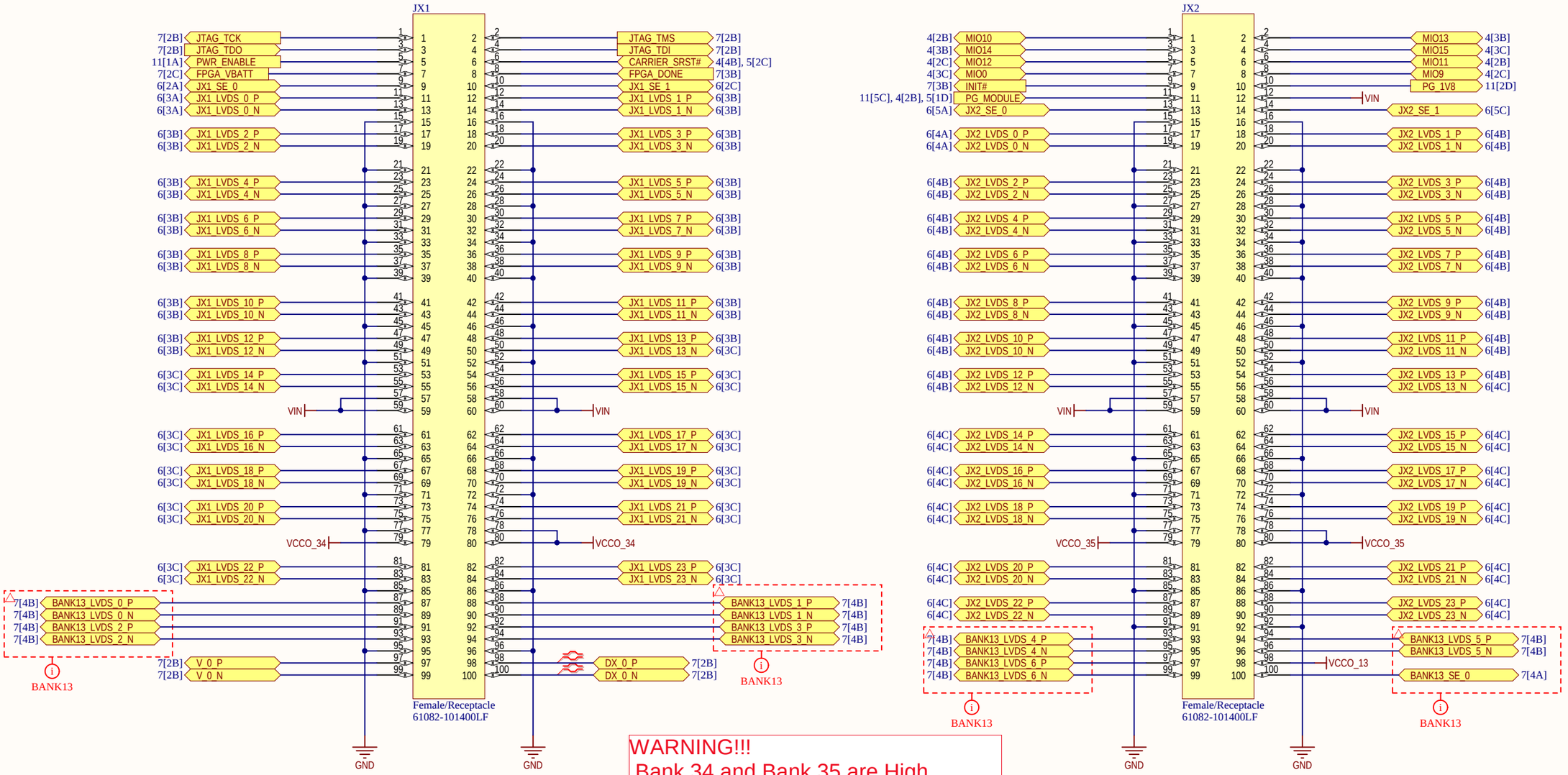
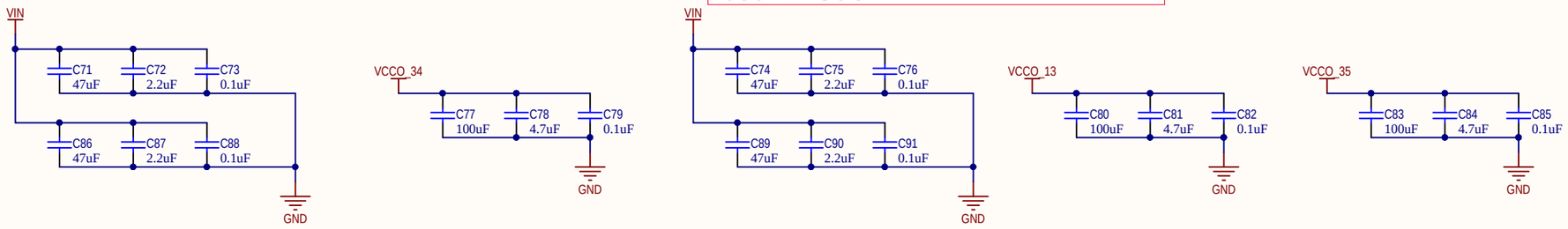
Doc Num: SCH-PZ2SOM	Date: 12/18/2017	Time: 11:06:38 AM		
Sheet Title: 07 - BANK 0, BANK13, JTAG.SchDoc		Size: B	Sheet: 7 of 12	



WARNING!!!
Bank 34 and Bank 35 are High Performance banks (7030 only) and will only accept 1.8V level signals. Failure to limit Bank 34 and 35 to 1.8V signals can damage the Zynq 7030 AP SoC.



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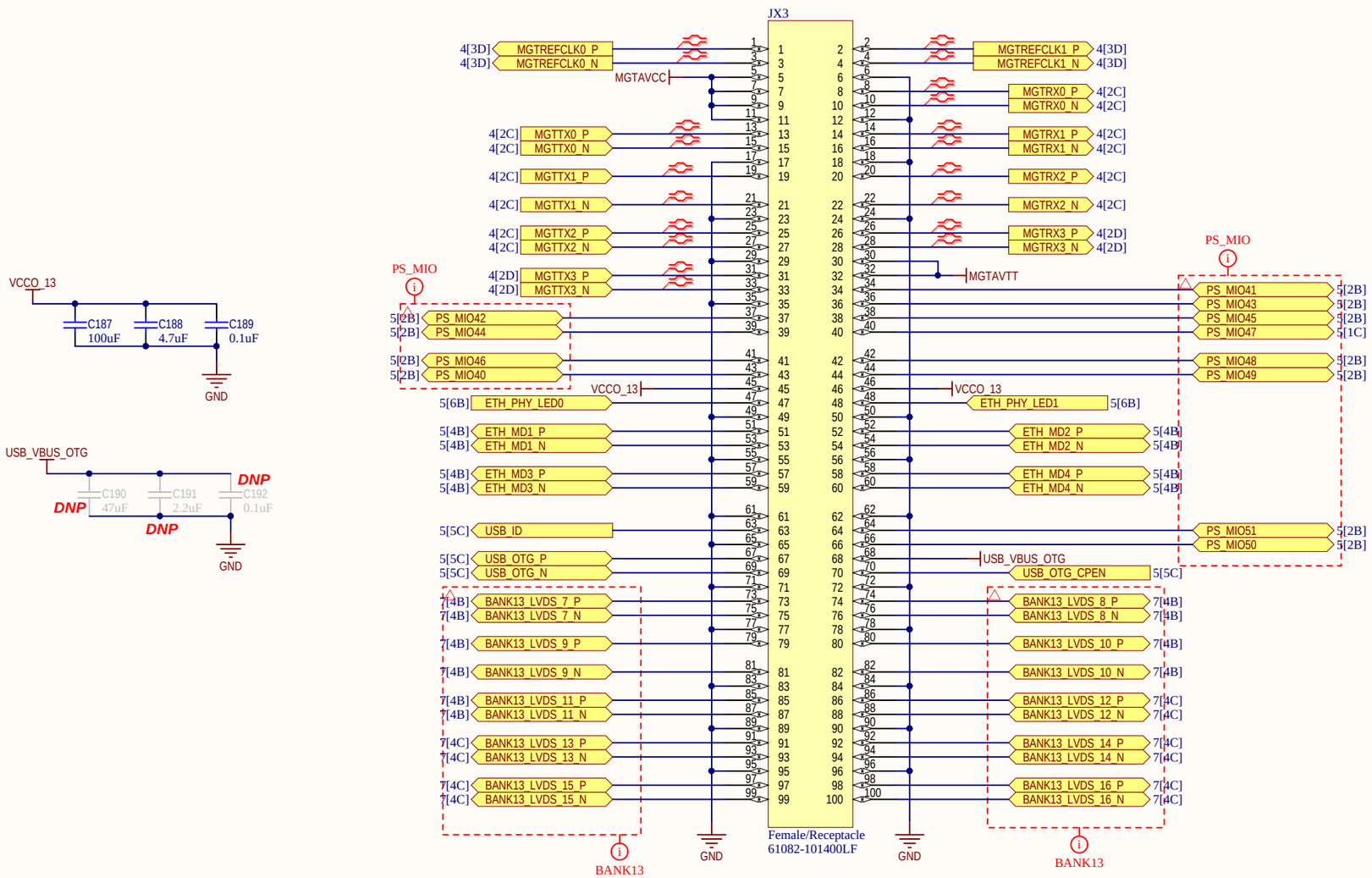
Doc Num: SCH-PZ2SOM	Date: 12/18/2017	Time: 11:06:38 AM		
Sheet Title: 08 - MICROHEADERS - JX1 and JX2.SchDoc		Size: B	Sheet: 8 of 12	



ZYNQ MIO POTENTIAL MAPPING OPTIONS:

SDIO INTERFACE
PS_MIO40 - SD_CLK through a 40.2-ohm RES
PS_MIO41 - SD_CMD
PS_MIO42 - SD_D0
PS_MIO43 - SD_D1
PS_MIO44 - SD_D2
PS_MIO45 - SD_D3
PS_MIO46 - SD_CD

UART INTERFACE
PS_MIO48 - UART_RXD (Tie to the TXD pin of a UART)
PS_MIO49 - UART TXD (Tie to the RXD pin of a UART)

USB INTERFACE
PS_MIO40 - DATA
PS_MIO41 - DIR
PS_MIO42 - STP
PS_MIO43 - NXT
PS_MIO44 - DATA
PS_MIO45 - DATA
PS_MIO46 - DATA
PS_MIO47 - DATA
PS_MIO48 - CK
PS_MIO49 - DATA
PS_MIO50 - DATA
PS_MIO51 - DATA

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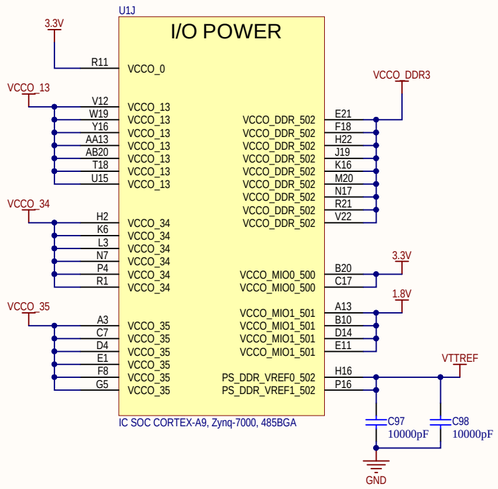
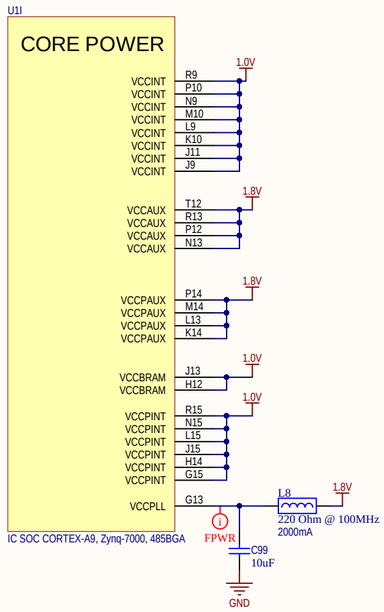
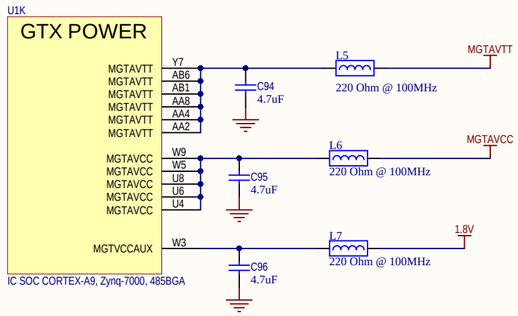
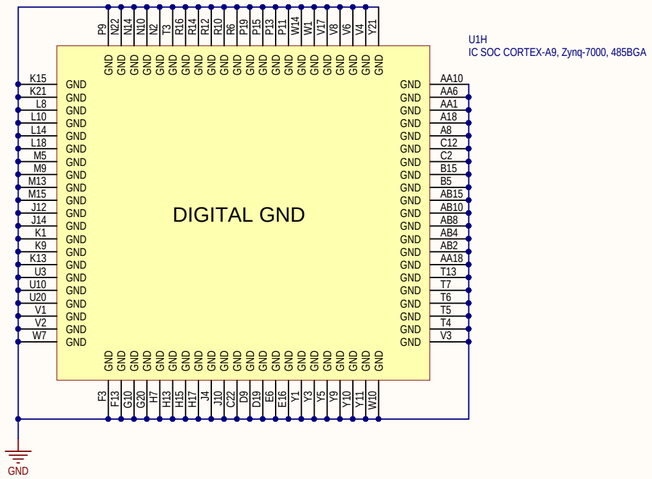
Project Name: PicoZed 7015/7030 SOM	PCB Rev: E	BOM: 01	Variant: 01
Doc Num: SCH-PZ2SOM	Date: 12/18/2017	Time: 11:06:38 AM	
Sheet Title: 09 - MICROHEADER - JX3.SchDoc	Size: B	Sheet: 9 of 12	

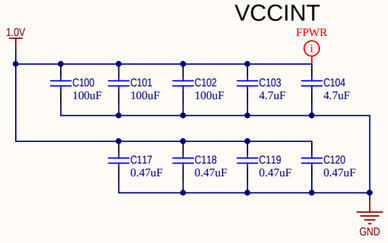








VCCINT



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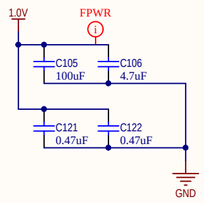

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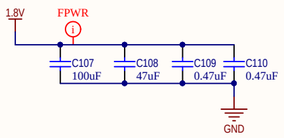

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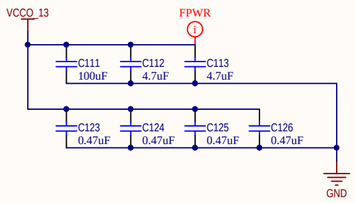

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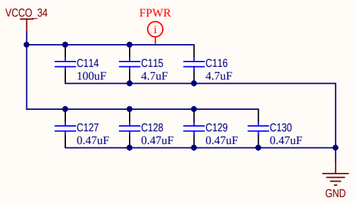

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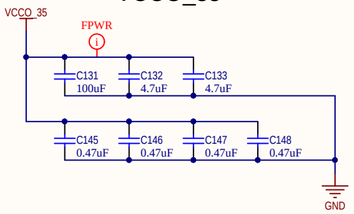
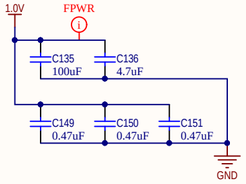


BANK 0

VCCPINT



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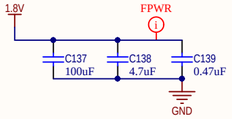

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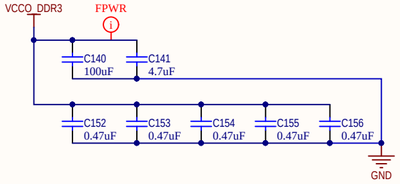

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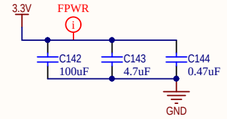

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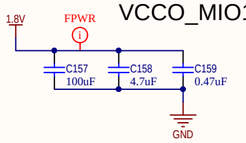
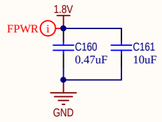
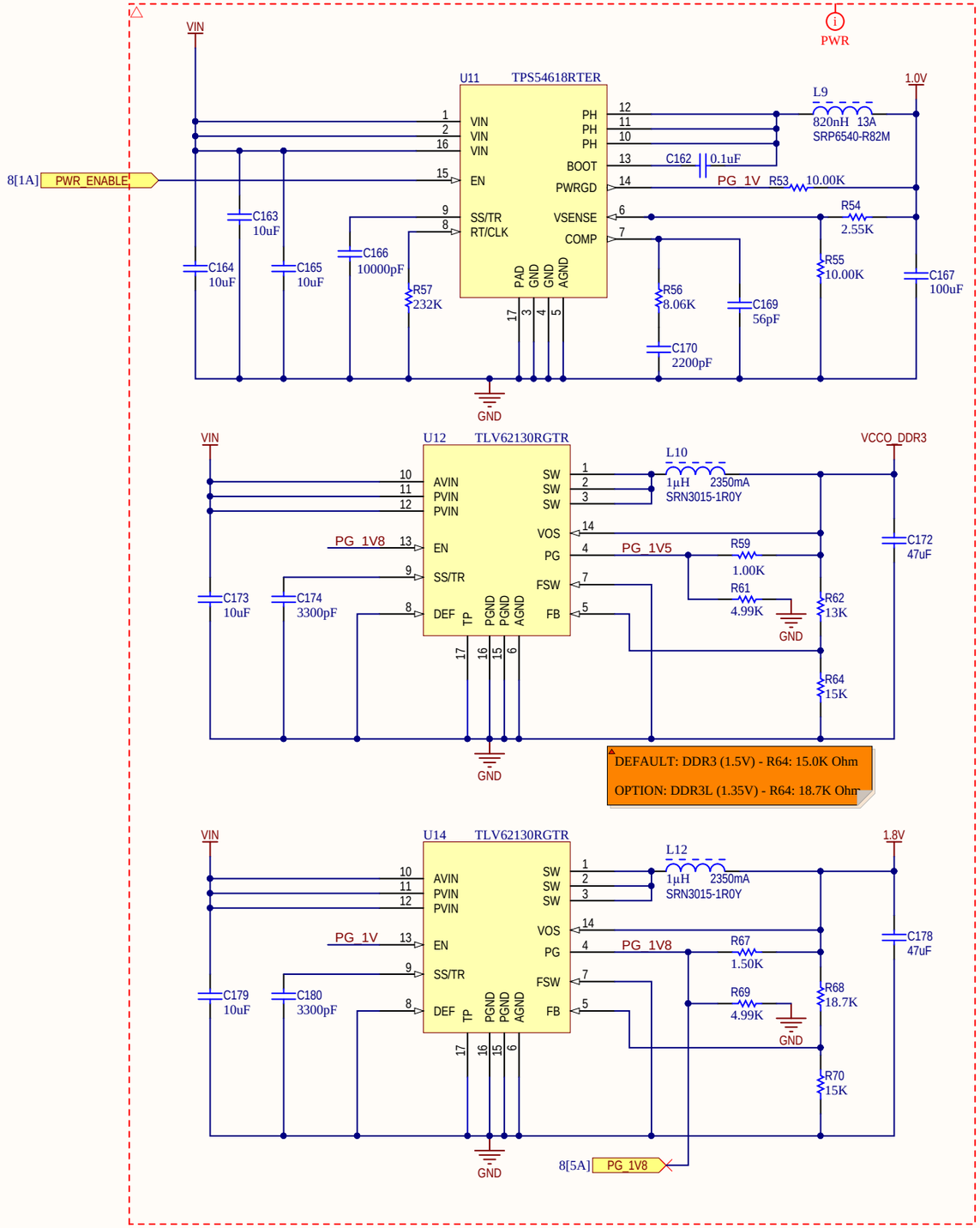
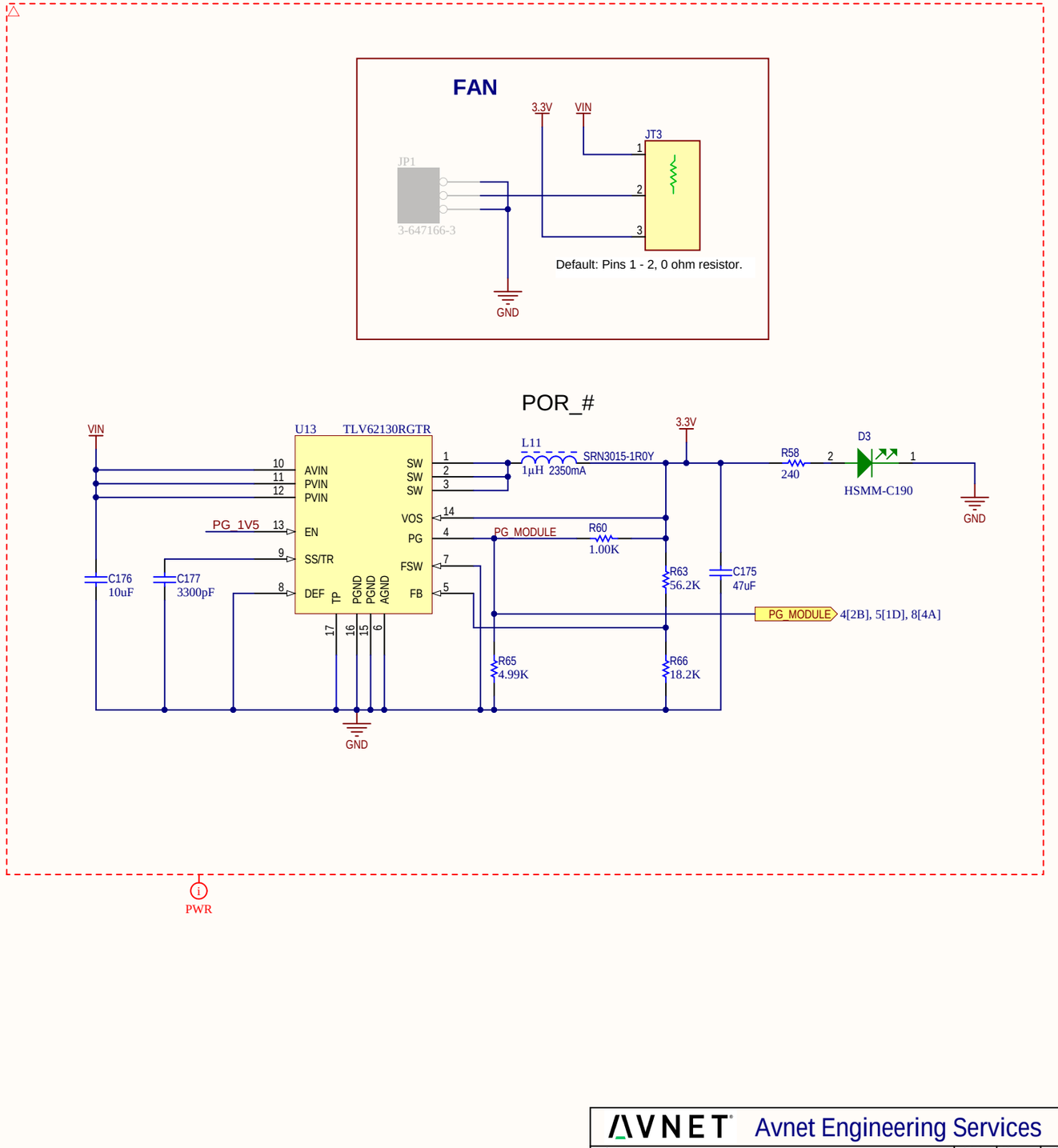


VCC_PLL



AVNET Avnet Engineering Services			
Project Name: PicoZed 7015/7030 SOM	PCB Rev: E	BOM: 01	Variant: 01
Doc Num: SCH-PZ2SOM	Date: 12/18/2017	Time: 11:06:39 AM	
Sheet Title: 10 - DEVICE POWER.SchDoc	Size: B	Sheet: 10 of 12	





AVNET Avnet Engineering Services				
Project Name: PicoZed 7015/7030 SOM		PCB Rev: E	BOM: 01	Variant: 01
Doc Num: SCH-PZ2SOM	Date: 12/18/2017	Time: 11:06:39 AM		
Sheet Title: 11 - POWER, RESET.SchDoc		Size: B	Sheet: 11 of 12	

Revision History

Rev B

Original release

Rev C

1) Updated Block Diagram
2) Added shared circuit MIO47 to JX3 and ETHERNET RESET
3) Added RC time constant to ETHERNET RESET
4) DDR3L/DDR3 option note added
5) Renamed 1.5V and DDR3_0V75 power nets
6) Changed U4.2 connection from 1.8V to 3.3V
7) Changed JX1/JX2 connections to Zynq Bank 34/35 Clock Capable Pins

Rev D

1) U18, U19, JT1, JT5, and JT6 have been removed
2) U4, U15, and U17 part numbers changed
3) Moved C84,C96,C101,C107,C111,C114,C134,C140,C142,C15,C161,C183,R86, RP2, L3,L4,L5,L6,L7,L8, and U16 away from FPGA to allow for heatsink clearance
4) JT8 and JT9 added to allow Boot Mode to be hard wired with 0 Ohm Jumpers
5) JT6 Replaced with 4.99K Pulldown resistor

Rev E

1) Connected U17 Pin B3 to GND
2) Added Voltage Divider (R52, R96) and fliter cap (C195) to U4 "VRI" pin
3) Added C199 and C200 to U15 Pin 3/5 (DDR3_VTT)
4) Added C196 to U15 Pin 2 (PVcc)
5) Changed C42 to 0.1uF Cap
6) Changed C39 to 4.7uF Cap

Mechanicals:

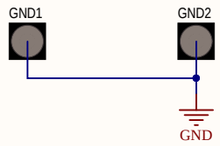
PCB

XXX-XXX-PCB-X

PCB PN (In Copper)

PCB Mounting Holes

GND Test Points



Assembly:

Label1

BD-XXXX-XXXXX-G

Label, Product

Label2

XXXXXXX

Label, Serial Number

ESD1

ESD Bag

Label_ESD1

Label, ESD

AVNET Avnet Engineering Services

Project Name: PicoZed 7015/7030 SOM	PCB Rev: E	BOM: 01	Variant: 01
Doc Num: SCH-PZ2SOM	Date: 12/18/2017	Time: 11:06:39 AM	
Sheet Title: 12 - Back Page.SchDoc	Size: B	Sheet: 12 of 12	