Reference Manual

Mpression Nitro Board

Revision 1.2

2014 / 10

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Contents

1. Read This First

1.1 Important Information

READ FIRST:

- ***READ*** this Reference Manual before using this product.
- ***KEEP*** the Reference Manual handy for future reference.
- ***Do not attempt*** to use the product until you fully understand its mechanism.

Purpose of the Product:

- The purpose of this product is to support the evaluation of a system that uses the Cyclone® V GX FPGA, manufactured by Altera® Corporation. It provides support for system development in both software and hardware.

For Users of This Product:

- This product can only be used by operators who have carefully read the "Getting Started" and "Reference Manual" manuals and understand how to use it. Use of this product requires a basic knowledge of electric circuits, logic circuits, and FPGAs.

Precautions to be taken when using This Product:

- This product is to be used for evaluation of a program, and the evaluation stage. You cannot install this Board in your product and cannot use this Board for mass-production. When mass-producing a program you have finished developing, be sure to decide at your own responsibility whether it can be put to practical use by performing integration test, evaluation, or some other experiment.
- In no event shall Macnica Inc. be liable for any consequence arising from the use of this product.
- Macnica Inc. cannot anticipate every possible circumstance that might involve a potential hazard. The warnings in this reference manual and on the product are therefore not all-inclusive. The user is therefore responsible for the safe use of the product at the user's own responsibility.
- The operation of any specific USB memories or SD cards cannot be guaranteed.
- Connection with the apparatus of any specific LAN interfaces cannot be guaranteed.
- This product does not guarantee device functionality.
- Remodeling by the customer is not guaranteed.
- This product is a lead-free mounting product.
- Generally, the brand names carried in this reference manual each constitute a maker's trademark or registered trademark.

Improvement Policy:

- Macnica Inc. pursues a policy of continuous improvement in design, performance, and safety of the product. Macnica Inc. reserves the right to change, wholly or partially, specifications, design, reference manual, and other documentation at any time without notice.

Warranty:

- Macnica Inc. offers exchange of this product free of charge only in a set range of cases of initial trouble for this product, and within 30 days from when the customer received delivery of the Board.

Macnica Inc. cannot exchange products in cases where breakdown is caused for the following reasons:
(1) Misuse, abuse of the product or use under abnormal conditions
(2) Remodeling or repair
(3) A fire, earthquake, fall or other accidents

Figures:

- Some figures in this reference manual may differ from your system as purchased.

1.2 Developer Information

The Developer of this product is:
Macnica Inc.
1-6-3 Shin-Yokohama, Kouhoku-ku, Yokohama, 222-8561 JAPAN

1.3 Inquires

In case you have any inquiries about the use this product, please contact your local Macnica company or make inquiries through the contact form in the following web site:
http://www.m-pression.com/contact

Macnica companies:

• China & HK:	Cytech Technology	http://www.cytech.com/
• ASEAN & India:	Cytech Global	http://www.cytechglobal.com/
• Taiwan:	Galaxy Far East Corp.	http://www.gfec.com.tw/
• North America:	Macnica Americas	http://www.macnica-na.com/
• Brazil:	Macnica DHW	http://www.macnicadhw.com.br/en/
• Japan:	Altima	http://www.altima.co.jp
	Elsena	http://www.elsena.co.jp

2. For Ensuring Safe Use

Be sure to follow the instructions given in this Manual which are intended to prevent harm to the user and others as well as material damage.

2.1 Legend

Danger	Indicates an imminent hazardous situation which if not avoided will result in death or serious injury.
Warning	Indicates a potentially hazardous situation which if not avoided could result in death or serious injury.
Caution	Indicates a potentially hazardous situation which if not avoided may result in minor or moderate injury or in property damage.

2.2 Cautions

Danger	If an AC adapter is required, make sure to use one that meets the specification described in this manual, or one that is included in the package. Using an AC adapter not meeting the specifications described in this Manual may cause the kit to emit heat, explode, or ignite.
Warning	Do not apply strong impacts or blows to the kit. Doing so may cause the kit to emit heat, explode, or ignite, or the equipment in the kit to fail or malfunction. This may also cause fire.
	Do not put the main unit or the AC adapter in cooking appliances such as microwave ovens, or high-pressure containers. Doing so might cause the main unit or AC adapter to emit heat, explode, ignite, or emit smoke, or its parts to break or warp.
	Do not wrap the main unit that is in use with cloth or other materials that are likely to allow heat to build up inside the wrapping. This will cause heat to build up inside the wrapping which may cause the main unit to ignite or malfunction.
	When disposing of the main unit, do not dispose of it along with general household waste. Throwing the main unit into fire may cause it to explode. Dispose of the main unit following the laws, regulations, and ordinances governing waste disposal.
	Do not pull the power supply cable with excessive force or place heavy items on it. Do not damage, break, bundle, or tamper with the power supply cable. Damaged parts of the power supply cable might cause a short circuit resulting in fire or accidents involving electrical shock.
	Do not plug or unplug the power plug with wet or moist hands. This might cause injuries or equipment malfunctions or failures due to electrical shock.

Warning (Continued from previous page)	Plug the power plug securely into the outlet. If the power plug is not securely plugged into the outlet, it may cause accidents involving electrical shock or fire due to heat emitted.
	Do not connect many electrical cords to a single socket or connect an AC adapter to an outlet that is not rated for the specified voltage. Doing so may cause the equipment to malfunction or fail, or lead to accidents involving electrical shock or fire due to heat emitted.
	Periodically remove any dust accumulated on the power plug and around the outlet (socket). Do not use a power plug with dust accumulated on it because doing so will lead to insulation failure due to moisture which may lead to fire. Remove any dust on the power plug and around the outlet with dried cloth.
	Do not place any containers such as cups or vases filled with water or other liquid on this Board. If this Board is exposed to water or other liquids it may cause the Board to malfunction or lead to accidents involving electrical shock. If you spilled water or other liquid on this Board, immediately stop using the Board, turn off the power, and unplug the power plug. If you have any requests for repairs or technical consultation, please contact the local Macnica company or Mpression inquiry URL.
	Keep this board and accessories out of reach of children. Failure to do so may lead to injuries.
Caution	Do not place the kit on unstable places such as shaky stands or tilted locations. Doing so may cause injuries or cause this Board to malfunction if the Board should fall.
	Do not attempt to use or leave the kit in places subject to strong direct sunlight or other places subject to high temperatures such as in cars in hot weather. Doing so might cause the kit to emit heat, break, ignite, run out of control, warp, or malfunction. Also, some parts of the equipment might emit heat causing burn injuries.
	Do not use the kit in places subject to extremely high or low temperatures or severe temperature changes. Doing so may cause the kit to fail or to malfunction. Always be sure to use the kit within a temperature range of 5°C to 35°C and a humidity range of 0% to 85%.
	Unplug the power supply cable when carrying out maintenance of devices in which the main unit is embedded. Failure to do so may lead to accidents involving electrical shock.
	Do not place this Board in locations where excessive force is applied to the Board. Doing so may cause the PC board to warp, leading to breakage of the PC board, missing parts or malfunctioning parts.
	When using the kit together with expansion boards or other peripheral devices, be sure to carefully read each of their manuals and to use them correctly. Developer does not guarantee the operation of specific expansion boards or peripheral devices when used in conjunction with this Board unless they are specifically mentioned in this Manual or their successful operation with this Board has been confirmed in separate documents.

Caution (Continued from previous page)	Be sure to turn off the power switch when moving this Board to connect to other devices. Failure to do so may cause this Board to fail or lead to accidents involving electrical shock.
	Do not clean this Board by using a rag containing chemicals such as benzine or thinner. Failure to do so will likely to cause this Board to deteriorate. When using a chemical cloth be sure to comply with any directions or warnings.
	Do not immediately turn on the power if you find that water or moisture had condensed onto the main unit after removing the board from the package. Condensation might occur on this Board when taking it out of the box, if the board is cool yet the room temperature is warm. Do not apply power to the Board while water or moisture has condensed on it because the moisture may cause the Board to break or may shorten the service life of the parts. When you first take this Board out of the box be sure to leave it at room temperature for a while before using it. If condensation or moisture has occurred on this Board, first wait for the moisture to fully evaporate before installing or connecting the Board to other devices.
	Do not disassemble, dismantle, modify, alter, or recycle parts unless they are clearly described as customizable in this Manual. Although this kit is customizable, if parts not specified in this Manual as customizable are modified in any way, then the overall product operation cannot be guaranteed. Please contact the local Macnica company or Mpression inquiry URL beforehand if you wish to customize or modify any parts that are not described in this Manual as customizable.

3. Unboxing

Package Components

This product consists of the Board and the parts listed in the table below. Please make sure all components listed below are included as soon as you get the Board.

<table>
<tr><td colspan="2">The Nitro Board: 1 set</td></tr>
<tr><td colspan="2">AC adaptor (Output 12 V/5 A)</td></tr>
<tr><td colspan="2">Spacer: 5 sets</td></tr>
<tr><td colspan="2">Heatsink: 1 set</td></tr>
<tr><td colspan="2">Customer Information</td></tr>
<tr><td>Reference Manual</td><td rowspan="4">Download these files from the web site given in the “Customer Information”.</td></tr>
<tr><td>The Nitro Board circuit diagram</td></tr>
<tr><td>FPGA sample design</td></tr>
<tr><td>Nitro Getting Started</td></tr>
</table>

Consider using the included heatsink if the FPGA gets hot, depending on use conditions and environments.
See the included "ASSEMBLE GUIDE" for instructions on how to install it.
Once you install it, the thermal adhesive sheet on the backside makes the heatsink stick to the FPGA. Attempting to remove it after installation may cause breakage or malfunction of the Board.
The heatsink has a cooling fan. Connect the power cable of the cooling fan to the J10 pins of this Board. See 5.7 for details.
Macnica, Inc. shall not be liable for breakage or malfunctions resulting from installation or removal of the heatsink.

4. Board Functions and Features

4.1 Overview

This Board is an FPGA development board that has DDR3-600 x 32/x64 (for soft memory controller (SMC)) and HSMC x3 interfaces, which can be used for basic circuit evaluation.
The main development target of this Board is Cyclone V GX FPGA, which is an FPGA manufactured by Altera Corporation that features Gigabit transceiver and high-speed I/O interfaces.
3 High-Speed Mezzanine Card (HSMC) connectors of this Board allow users to add various functions by connecting third-party expansion boards.

For more information and related documents, follow the links below.

- Information on the Cyclone V Devices
  Documentation: Cyclone V Devices
- High Speed Mezzanine Card (HSMC) Specification
  High Speed Mezzanine Card (HSMC) Specification.

4.2 Key Components

Table 1 shows the product specifications of this Board.

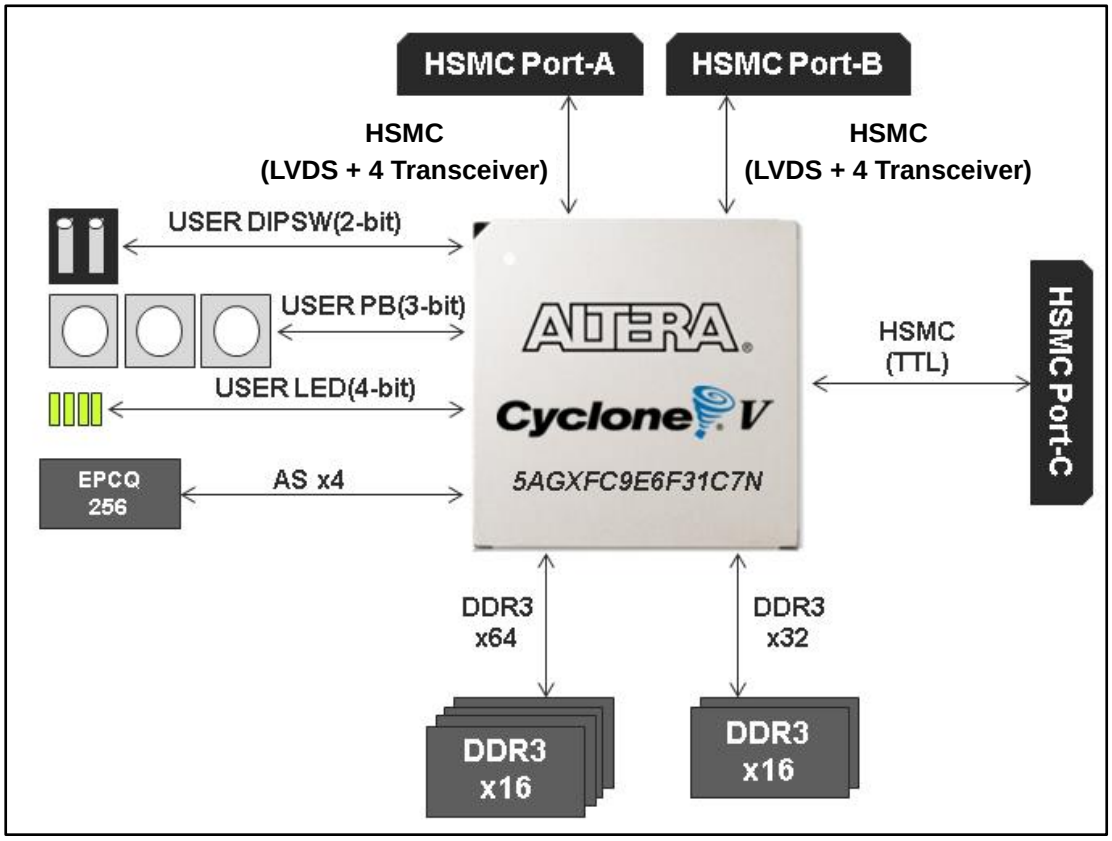
Table 1 Nitro Board Product Specifications

Product Function	ALTNITROC5GX
FPGA	5CGXFC9E6F31C7N
Power Supply	DC 12 V 5 A
Dimensions	180 mm x 125 mm
Printed Circuit Board	FR4 16-layer
Configuration	EPCQ256 (AS)
DDR-SDRAM	DDR3-300MHz, 64 bit x 1(512 MB:128 MB x 4), 32 bit x1(256 MB:128 MB x 2)
Clock	Reference clock for high-speed transceiver: • 100 MHz x 2 (LVPECL) • 125 MHz (LVDS) • 148.5 MHz (LVDS) Clock for FPGA Fabric: • 50 MHz x 2 (TTL) • 74.25 MHz (TTL) • 100 MHz (TTL)
JTAG Connector	DIP 10-pin Header, 2.54-mm pitch × 1
Status LED	5 pcs (12V_POWER, nCONFIG, nSTATUS, CONF_DONE, INIT_DONE)
FPGA Reconfiguration Push SW	1 (FPGA_Reconfig)
General-purpose LED	4
General-purpose Push SW	3
General-purpose Dip SW	1 (2-bit)
Power SW	1

4.3 Block Diagram

Figure 1 shows the block diagram of this Board. Because this Board is an evaluation board for Cyclone V GX FPGA, all of the functions are integrated in Cyclone V GX FPGA.

Figure 1 Nitro Board Block Diagram



4.4 Board Specifications

This section describes the layout of components on this Board and their specifications.
Figure 2 shows the layout of components on this Board.

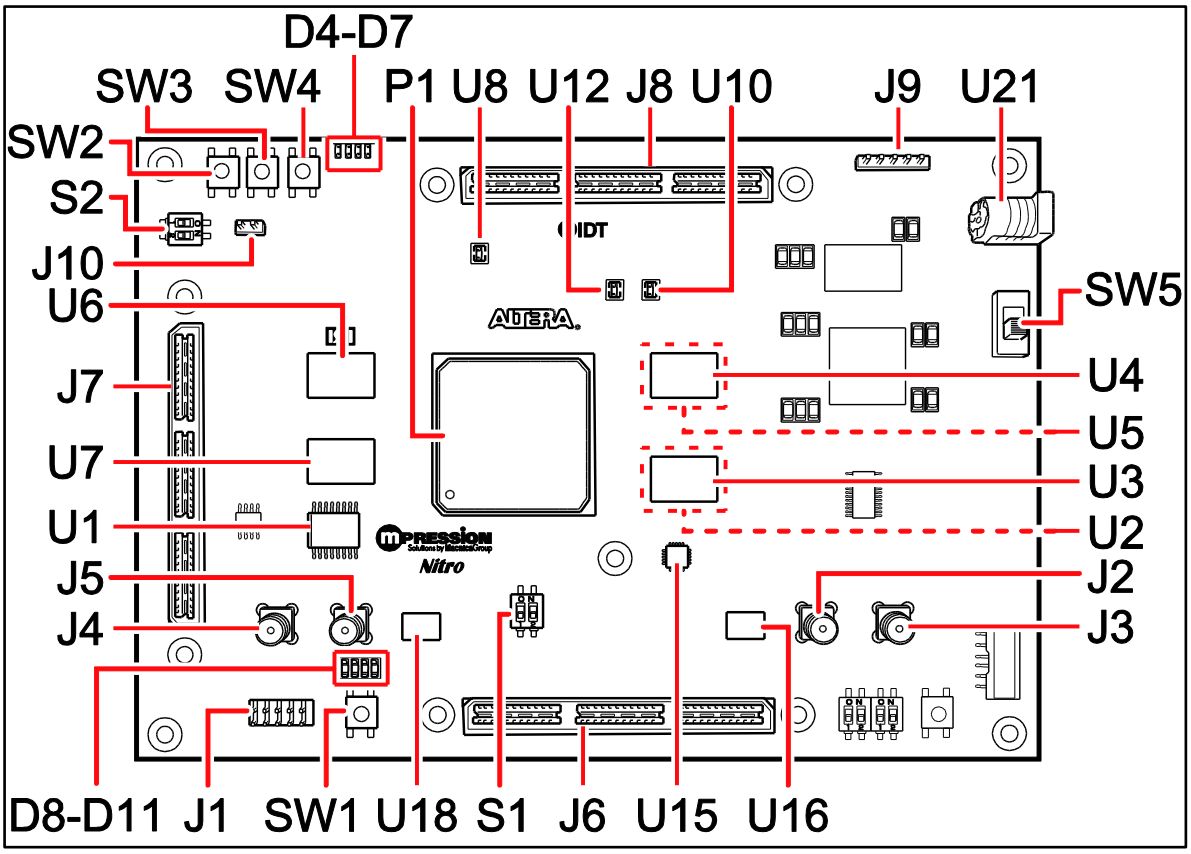


Figure 2 Layout of Components on this Board

Table 2 Main Components of this Board

Reference No.	Type	Details
Main Devices		
P1	FPGA	Cyclone V GX:5CGXFC9E6F31C7N 896-pin FPGA
U1	Configuration ROM	EPCQ256
Configuration/Status LED		
J1	JTAG 10-pin Header	Access port to the JTAG chain. Use a USB-Blaster cable for connection.
SW1	FPGA_Reconfig	Configuration Reset. Drives the nCONFIG port of the FPGA.
D8	nCONFIG	When unlit, there is abnormality in the configuration status of the FPGA. When lit, there is not abnormality.
D9	nSTATUS	When lit, FPGA configuration has been completed. When unlit, FPGA configuration has not been completed.

Continued from the previous page

Reference No.	Type	Details
D10	CONF_DONE	When lit, configuration can be done. When unlit, the FPGA configuration has been reset.
D11	INIT_DONE	When lit, configuration has been completed and the Board can operate in user mode.
Clock Circuit		
U15	Clock Generator • 148.5 MHz • 125 MHz • 74.25 MHz • 27 MHz	Generates 4 frequencies described on the left.
U16	Clock Generator • 100 MHz	Generates the frequency described on the left.
U18	Clock Generator • 100 MHz	Generates the frequency described on the left.
U8	Clock Generator • 50 MHz	Generates the frequency described on the left.
U10	Clock Generator • 50 MHz	Generates the frequency described on the left.
U12	Clock Generator • 100 MHz	Generates the frequency described on the left.
J2/J3	External clock input connector	Supplies the clock to the transceiver block via SMA.
J4/J5	External clock input connector	Supplies the clock to the transceiver block via SMA.
S1	Reference clock selector switch	DIP switch used for switching between On-board clock and clock supplied via SMA.
General-purpose user input/output		
D4, D5, D6, D7	User LED	4 low-active user LEDs.
SW2, SW3, SW4	User push-buttons	3 user push buttons. Inputs Low to the FPGA when pushed.
S2	User DIP switches	2 user DIP switches. Inputs Low to the FPGA when set to On.
J6	HSMC	HSMC Port-A
J7	HSMC	HSMC Port-B
J8	HSMC	HSMC Port-C
J9	GPIO	GPIO Pin-Header
Memory		
U2, U3, U4, U5	DDR3 SDRAM	DDR3 SDRAM 64-bit(16x4) Bottom
U6, U7	DDR3 SDRAM	DDR3 SDRAM 32-bit(16x2) Top
Power Connector and Switch		
U21	DC jack	12 V DC power can be supplied.
SW5	Power Switch	Switches on/off the power supply from the DC jack.
Power Connector for the Cooling Fan		
J10	2-pin Header	Power supply for the cooling fan

5. Board Components

This chapter describes the FPGA and various components installed on the periphery of the FPGA on this Board.

5.1 Featured Device: Cyclone V GX FPGA

This Board carries 28-nm low-cost FPGA Cyclone V GX manufactured by Altera Corporation. Table 3 shows the specifications of the Cyclone V GX FPGA.

Table 3 CGXFC9E6F31C7N Specifications

Resource	Logic Elements(K)	ALM	Register	Memory (Kb)		Variable-precision DSP Block	18 x 18 Multiplier	PLL
				M10K	MLAB			
5CGXFC9E6F31C7N	301	113,560	454,240	12,200	1,717	342	684	8

5.2 Configuration/Status LED

5.2.1 Configuration

This Board supports JTAG configuration and AS (Active Serial) configuration. The Configuration ROM for AS is EPCQ256. Programming to EPCQ256 is done via the JTAG interface.

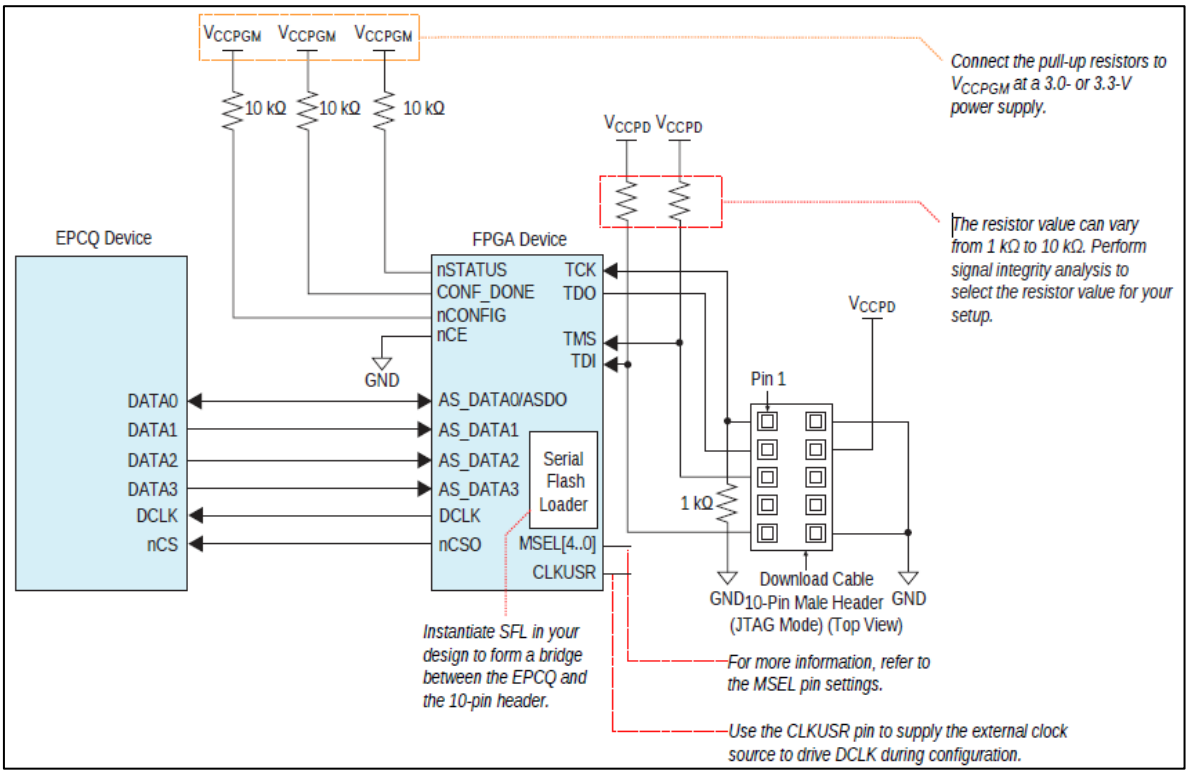


Figure 3 AS/JTAG Schematic

SW1 (FPGA_Reconfig) is connected to the “nCONFIG” pin of the FPGA. Pushing this switch starts AS configuration again.

5.2.2 Status LED

D8, D9, D10, and D11 are connected to “nCONFIG”, “uSTATUS”, “CONF_DONE”, and “INIT_DONE” of the FPGA. When all LEDs are lit, configuration has been completed correctly. Figure 4 shows the sequence of the signals.

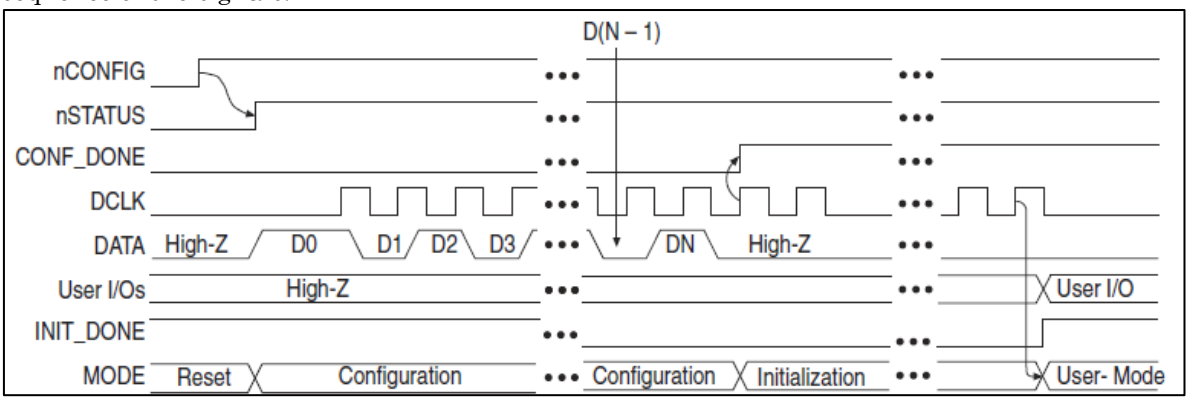


Figure 4 Configuration Sequence

5.3 Clock Circuit

This section describes clock systems.

5.3.1 Pin assignment between clock generators and the FPGA

Figure 5 shows the pin assignment between various clock generators and the FPGA. “CLKIN_100M” cannot be connected to PLL inside the FPGA because it is connected to the N channel side of the clock input pin.
“CLKIN_DDR3_50M_TOP”, “CLKIN_DDR3_50M_BOT”, “CLKIN_100M”, “CLKIN_74p25M”, and “CLKIN_27M” are output as 1.8V TTL signals from each clock generator, but the FPGA receives them as 1.5V LVTTL.

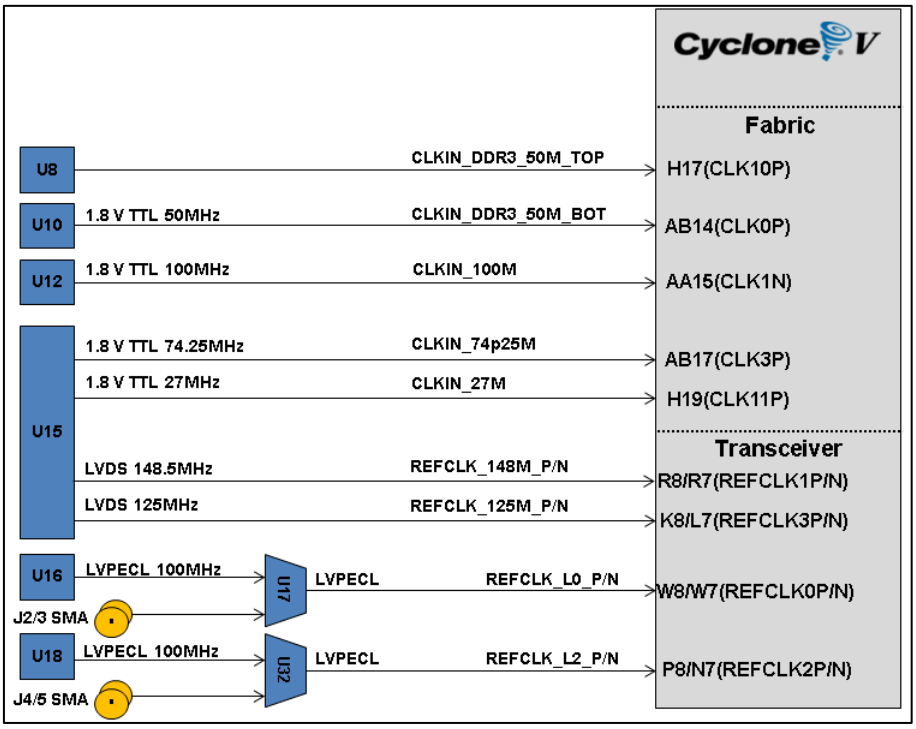


Figure 5 Pin Assignment between Clock Generators and the FPGA

5.3.2 Clock selector

The S1 “CLK_SEL” DIP switch switches the input clock source for REFCLK0P/N and REFCLK2P/N shown in Figure 5. S1-1 sets the input clock source for REFCLK0P/N and S1-2 sets the input clock source for REFCLK2P/N. When the switch is set to “OFF”, the on-board 100 MHz is selected. When the switch is set to “ON”, the input from SMA is selected.

5.4 General-purpose I/O

This section describes the general-purpose I/O interfaces of this Board.
User LED

5.4.1 User-defined LED

Table 4 shows the pin assignment between the User-defined LED and the FPGA.

Table 4 Pin assignment between User-defined LED and FPGA

Board Reference	Legend	FPGA pin assignment	Active-high/Active-low
D4	FPGA_LED0_N	V11	L (Lit when in L state)
D5	FPGA_LED1_N	U11	L (Lit when in L state)
D6	FPGA_LED2_N	T11	L (Lit when in L state)
D7	FPGA_LED3_N	U12	L (Lit when in L state)

5.4.2 User-defined Push-button

Table 5 shows the pin assignment between the User-defined push-button and the FPGA.

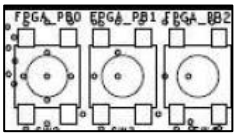


Table 5 Pin assignment between User-defined push-button and FPGA

Board Reference	Legend	FPGA pin assignment	Active-high/Active-low
SW2	FPGA_PB0	L18	L (L when pushed)
SW3	FPGA_PB1	F18	L (L when pushed)
SW4	FPGA_PB2	G17	L (L when pushed)

5.4.3 User-defined DIP switch

Table 6 shows the pin assignment between the User-defined DIP switch and the FPGA.

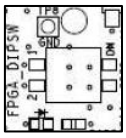


Table 6 Pin assignment between User DIP switch and FPGA

Board Reference		Legend	FPGA pin assignment	Active-high/Active-low
S2	1	FPGA_DIPSW	AF15	L (L when ON)
	2		AF21	L (L when ON)

5.4.4 HSMC Port-A

Table 7 shows the pin assignment between HSMC Port-A (J6) and the FPGA.

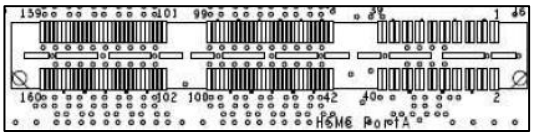


Table 7 Pin assignment between HSMC Port-A and FPGA

HSMC PIN	HSMC SIGNAL NAME	FPGA'S PIN NUM	HSMC PIN	HSMC SIGNAL NAME	FPGA'S PIN NUM
1			2		
3			4		
5			6		
7			8		
9			10		
11			12		
13			14		
15			16		
17	HSMA_TX3_P	PIN_Y4	18	HSMA_RX3_P	PIN_AA2
19	HSMA_TX3_N	PIN_Y3	20	HSMA_RX3_N	PIN_AA1
21	HSMA_TX2_P	PIN_AB4	22	HSMA_RX2_P	PIN_AC2
23	HSMA_TX2_N	PIN_AB3	24	HSMA_RX2_N	PIN_AC1
25	HSMA_TX1_P	PIN_AD4	26	HSMA_RX1_P	PIN_AE2
27	HSMA_TX1_N	PIN_AD3	28	HSMA_RX1_N	PIN_AE1
29	HSMA_TX0_P	PIN_AF4	30	HSMA_RX0_P	PIN_AG2
31	HSMA_TX0_N	PIN_AF3	32	HSMA_RX0_N	PIN_AG1
33	HSMA_SDA	PIN_AA11	34	HSMA_SCL	PIN_Y11
35			36		
37			38		
39	HSMA_CLK_OUT0	PIN_Y10	40	HSMA_CLK_IN0	PIN_Y15
41	HSMA_D0	PIN_AA8	42	HSMA_D1	PIN_AA9
43	HSMA_D2	PIN_W24	44	HSMA_D3	PIN_AA10
45	hsma_3p3v		46	12v	
47	HSMA_TX_D0_P	PIN_K10	48	HSMA_RX_D0_P	PIN_R12
49	HSMA_TX_D0_N	PIN_J10	50	HSMA_RX_D0_N	PIN_R11
51	hsma_3p3v		52	12v	
53	HSMA_TX_D1_P	PIN_J9	54	HSMA_RX_D1_P	PIN_P10
55	HSMA_TX_D1_N	PIN_H9	56	HSMA_RX_D1_N	PIN_N11
57	hsma_3p3v		58	12v	
59	HSMA_TX_D2_P	PIN_G8	60	HSMA_RX_D2_P	PIN_P12
61	HSMA_TX_D2_N	PIN_G7	62	HSMA_RX_D2_N	PIN_N12
63	hsma_3p3v		64	12v	
65	HSMA_TX_D3_P	PIN_J7	66	HSMA_RX_D3_P	PIN_N10
67	HSMA_TX_D3_N	PIN_H7	68	HSMA_RX_D3_N	PIN_N9
69	hsma_3p3v		70	12v	
71	HSMA_TX_D4_P	PIN_G6	72	HSMA_RX_D4_P	PIN_M9
73	HSMA_TX_D4_N	PIN_F6	74	HSMA_RX_D4_N	PIN_M8
75	hsma_3p3v		76	12v	
77	HSMA_TX_D5_P	PIN_F13	78	HSMA_RX_D5_P	PIN_M12

Continued from the previous page

HSMC PIN	HSMC SIGNAL NAME	FPGA'S PIN NUM	HSMC PIN	HSMC SIGNAL NAME	FPGA'S PIN NUM
79	HSMA_TX_D5_N	PIN_E13	80	HSMA_RX_D5_N	PIN_M11
81	hsma_3p3v		82	12v	
83	HSMA_TX_D6_P	PIN_C7	84	HSMA_RX_D6_P	PIN_L10
85	HSMA_TX_D6_N	PIN_C6	86	HSMA_RX_D6_N	PIN_L9
87	hsma_3p3v		88	12v	
89	HSMA_TX_D7_P	PIN_A10	90	HSMA_RX_D7_P	PIN_L11
91	HSMA_TX_D7_N	PIN_A9	92	HSMA_RX_D7_N	PIN_K11
93	hsma_3p3v		94	12v	
95	HSMA_CLK_OUT1_P	PIN_F9	96	HSMA_CLK_IN1_P	PIN_L14
97	HSMA_CLK_OUT1_N	PIN_E10	98	HSMA_CLK_IN1_N	PIN_L13
99	hsma_3p3v		100	12v	
101	HSMA_TX_D8_P	PIN_G9	102	HSMA_RX_D8_P	PIN_K12
103	HSMA_TX_D8_N	PIN_F8	104	HSMA_RX_D8_N	PIN_J12
105	hsma_3p3v		106	12v	
107	HSMA_TX_D9_P	PIN_E7	108	HSMA_RX_D9_P	PIN_J14
109	HSMA_TX_D9_N	PIN_E6	110	HSMA_RX_D9_N	PIN_H14
111	hsma_3p3v		112	12v	
113	HSMA_TX_D10_P	PIN_E8	114	HSMA_RX_D10_P	PIN_H12
115	HSMA_TX_D10_N	PIN_D8	116	HSMA_RX_D10_N	PIN_G12
117	hsma_3p3v		118	12v	
119	HSMA_TX_D11_P	PIN_D9	120	HSMA_RX_D11_P	PIN_J15
121	HSMA_TX_D11_N	PIN_C10	122	HSMA_RX_D11_N	PIN_H15
123	hsma_3p3v		124	12v	
125	HSMA_TX_D12_P	PIN_A5	126	HSMA_RX_D12_P	PIN_G14
127	HSMA_TX_D12_N	PIN_A4	128	HSMA_RX_D12_N	PIN_F14
129	hsma_3p3v		130	12v	
131	HSMA_TX_D13_P	PIN_A3	132	HSMA_RX_D13_P	PIN_E11
133	HSMA_TX_D13_N	PIN_A2	134	HSMA_RX_D13_N	PIN_D10
135	hsma_3p3v		136	12v	
137	HSMA_TX_D14_P	PIN_B6	138	HSMA_RX_D14_P	PIN_E12
139	HSMA_TX_D14_N	PIN_A6	140	HSMA_RX_D14_N	PIN_D13
141	hsma_3p3v		142	12v	
143	HSMA_TX_D15_P	PIN_B7	144	HSMA_RX_D15_P	PIN_F15
145	HSMA_TX_D15_N	PIN_A8	146	HSMA_RX_D15_N	PIN_E15
147	hsma_3p3v		148	12v	
149	HSMA_TX_D16_P	PIN_C9	150	HSMA_RX_D16_P	PIN_F16
151	HSMA_TX_D16_N	PIN_B8	152	HSMA_RX_D16_N	PIN_E16
153	hsma_3p3v		154	12v	
155	HSMA_CLK_OUT2_P	PIN_B11	156	HSMA_CLK_IN2_P	PIN_L15
157	HSMA_CLK_OUT2_N	PIN_A11	158	HSMA_CLK_IN2_N	PIN_K15
159	hsma_3p3v		160	HSMA PSNTn	

5.4.5 HSMC Port-B

Table 8 shows the pin assignment between HSMC Port-B (J7) and the FPGA.

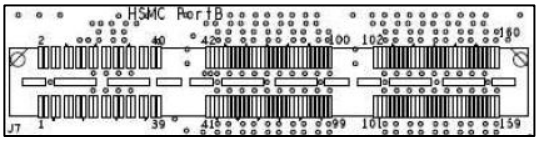


Table 8 Pin assignment between HSMC Port-B and FPGA

HSMC PIN	HSMC SIGNAL NAME	FPGA'S PIN NUM	HSMC PIN	HSMC SIGNAL NAME	FPGA'S PIN NUM
1			2		
3			4		
5			6		
7			8		
9			10		
11			12		
13			14		
15			16		
17	HSMB_TX3_P	PIN_H4	18	HSMB_RX3_P	PIN_J2
19	HSMB_TX3_N	PIN_H3	20	HSMB_RX3_N	PIN_J1
21	HSMB_TX2_P	PIN_K4	22	HSMB_RX2_P	PIN_L2
23	HSMB_TX2_N	PIN_K3	24	HSMB_RX2_N	PIN_L1
25	HSMB_TX1_P	PIN_M4	26	HSMB_RX1_P	PIN_N2
27	HSMB_TX1_N	PIN_M3	28	HSMB_RX1_N	PIN_N1
29	HSMB_TX0_P	PIN_P4	30	HSMB_RX0_P	PIN_R2
31	HSMB_TX0_N	PIN_P3	32	HSMB_RX0_N	PIN_R1
33	HSMB_SDA	PIN_U9	34	HSMB_SCL	PIN_T10
35			36		
37			38		
39	HSMB_CLK_OUT0	PIN_V9	40	HSMB_CLK_IN0	PIN_AB16
41	HSMB_D0	PIN_U8	42	HSMB_D1	PIN_T9
43	HSMB_D2	PIN_Y23	44	HSMB_D3	PIN_R10
45	HSMB_3p3v		46	12v	
47	HSMB_TX_D0_P	PIN_B28	48	HSMB_RX_D0_P	PIN_N21
49	HSMB_TX_D0_N	PIN_A29	50	HSMB_RX_D0_N	PIN_M22
51	HSMB_3p3v		52	12v	
53	HSMB_TX_D1_P	PIN_D30	54	HSMB_RX_D1_P	PIN_N22
55	HSMB_TX_D1_N	PIN_C30	56	HSMB_RX_D1_N	PIN_M23
57	HSMB_3p3v		58	12v	
59	HSMB_TX_D2_P	PIN_E27	60	HSMB_RX_D2_P	PIN_L25
61	HSMB_TX_D2_N	PIN_D27	62	HSMB_RX_D2_N	PIN_L26
63	HSMB_3p3v		64	12v	
65	HSMB_TX_D3_P	PIN_D28	66	HSMB_RX_D3_P	PIN_N24
67	HSMB_TX_D3_N	PIN_D29	68	HSMB_RX_D3_N	PIN_N25
69	HSMB_3p3v		70	12v	
71	HSMB_TX_D4_P	PIN_F30	72	HSMB_RX_D4_P	PIN_N26
73	HSMB_TX_D4_N	PIN_E30	74	HSMB_RX_D4_N	PIN_N27
75	HSMB_3p3v		76	12v	
77	HSMB_TX_D5_P	PIN_F28	78	HSMB_RX_D5_P	PIN_J22
79	HSMB_TX_D5_N	PIN_E28	80	HSMB_RX_D5_N	PIN_J23

Continued from the previous page

HSMC PIN	HSMC SIGNAL NAME	FPGA'S PIN NUM	HSMC PIN	HSMC SIGNAL NAME	FPGA'S PIN NUM
81	HSMB_3p3v		82	12v	
83	HSMB_TX_D6_P	PIN_G29	84	HSMB_RX_D6_P	PIN_K21
85	HSMB_TX_D6_N	PIN_F29	86	HSMB_RX_D6_N	PIN_K22
87	HSMB_3p3v		88	12v	
89	HSMB_TX_D7_P	PIN_G27	90	HSMB_RX_D7_P	PIN_H25
91	HSMB_TX_D7_N	PIN_G28	92	HSMB_RX_D7_N	PIN_H26
93	HSMB_3p3v		94	12v	
95	HSMB_CLK_OUT1_P	PIN_H29	96	HSMB_CLK_IN1_P	PIN_P22
97	HSMB_CLK_OUT1_N	PIN_H30	98	HSMB_CLK_IN1_N	PIN_P23
99	HSMB_3p3v		100	12v	
101	HSMB_TX_D8_P	PIN_H27	102	HSMB_RX_D8_P	PIN_L23
103	HSMB_TX_D8_N	PIN_G26	104	HSMB_RX_D8_N	PIN_L24
105	HSMB_3p3v		106	12v	
107	HSMB_TX_D9_P	PIN_K30	108	HSMB_RX_D9_P	PIN_K27
109	HSMB_TX_D9_N	PIN_J30	110	HSMB_RX_D9_N	PIN_J27
111	HSMB_3p3v		112	12v	
113	HSMB_TX_D10_P	PIN_J28	114	HSMB_RX_D10_P	PIN_M21
115	HSMB_TX_D10_N	PIN_J29	116	HSMB_RX_D10_N	PIN_L21
117	HSMB_3p3v		118	12v	
119	HSMB_TX_D11_P	PIN_H24	120	HSMB_RX_D11_P	PIN_P29
121	HSMB_TX_D11_N	PIN_J25	122	HSMB_RX_D11_N	PIN_P30
123	HSMB_3p3v		124	12v	
125	HSMB_TX_D12_P	PIN_K25	126	HSMB_RX_D12_P	PIN_P25
127	HSMB_TX_D12_N	PIN_K26	128	HSMB_RX_D12_N	PIN_R25
129	HSMB_3p3v		130	12v	
131	HSMB_TX_D13_P	PIN_L29	132	HSMB_RX_D13_P	PIN_P20
133	HSMB_TX_D13_N	PIN_L30	134	HSMB_RX_D13_N	PIN_N20
135	HSMB_3p3v		136	12v	
137	HSMB_TX_D14_P	PIN_L28	138	HSMB_RX_D14_P	PIN_R27
139	HSMB_TX_D14_N	PIN_K28	140	HSMB_RX_D14_N	PIN_R28
141	HSMB_3p3v		142	12v	
143	HSMB_TX_D15_P	PIN_M27	144	HSMB_RX_D15_P	PIN_R21
145	HSMB_TX_D15_N	PIN_M28	146	HSMB_RX_D15_N	PIN_R22
147	HSMB_3p3v		148	12v	
149	HSMB_TX_D16_P	PIN_P28	150	HSMB_RX_D16_P	PIN_R20
151	HSMB_TX_D16_N	PIN_N29	152	HSMB_RX_D16_N	PIN_T21
153	HSMB_3p3v		154	12v	
155	HSMB_CLK_OUT2_P	PIN_M29	156	HSMB_CLK_IN2_P	PIN_T23
157	HSMB_CLK_OUT2_N	PIN_N30	158	HSMB_CLK_IN2_N	PIN_R23
159	HSMB_3p3v		160	HSMB PSNTn	

5.4.6 HSMC Port-C

Table 9 shows the pin assignment between HSMC Port-C (J8) and the FPGA.

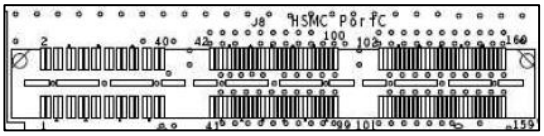


Table 9 Pin assignment between HSMC Port-C and FPGA

HSMC PIN	HSMC SIGNAL NAME	FPGA'S PIN NUM	HSMC PIN	HSMC SIGNAL NAME	FPGA'S PIN NUM
1			2		
3			4		
5			6		
7			8		
9			10		
11			12		
13			14		
15			16		
17			18		
19			20		
21			22		
23			24		
25			26		
27			28		
29			30		
31			32		
33	HSMC_SDA	PIN_R30	34	HSMC_SCL	PIN_T30
35			36		
37			38		
39	HSMC_CLK_OUT0	PIN_U29	40	HSMC_CLK_IN0	PIN_AC15
41	HSMC_D0	PIN_T29	42	HSMC_D1	PIN_T28
43	HSMC_D2	PIN_R26	44	HSMC_D3	PIN_T25
45	HSMC_3p3v		46	12v	
47	HSMC_D4	PIN_U28	48	HSMC_D5	PIN_U27
49	HSMC_D6	PIN_U26	50	HSMC_D7	PIN_V29
51	HSMC_3p3v		52	12v	
53	HSMC_D8	PIN_V27	54	HSMC_D9	PIN_V26
55	HSMC_D10	PIN_V25	56	HSMC_D11	PIN_V24
57	HSMC_3p3v		58	12v	
59	HSMC_D12	PIN_W30	60	HSMC_D13	PIN_W29
61	HSMC_D14	PIN_W28	62	HSMC_D15	PIN_W27
63	HSMC_3p3v		64	12v	
65	HSMC_D16	PIN_Y30	66	HSMC_D17	PIN_Y28
67	HSMC_D18	PIN_Y27	68	HSMC_D19	PIN_Y26
69	HSMC_3p3v		70	12v	
71	HSMC_D20	PIN_Y25	72	HSMC_D21	PIN_Y22
73	HSMC_D22	PIN_AA30	74	HSMC_D23	PIN_AA29
75	HSMC_3p3v		76	12v	
77	HSMC_D24	PIN_AA28	78	HSMC_D25	PIN_AA25
79	HSMC_D26	PIN_AA24	80	HSMC_D27	PIN_AA23

Continued from the previous page

HSMC PIN	HSMC SIGNAL NAME	FPGA'S PIN NUM	HSMC PIN	HSMC SIGNAL NAME	FPGA'S PIN NUM
81	HSMC_3p3v		82	12v	
83	HSMC_D28	PIN_AB29	84	HSMC_D29	PIN_AB28
85	HSMC_D30	PIN_AB27	86	HSMC_D31	PIN_AB26
87	HSMC_3p3v		88	12v	
89	HSMC_D32	PIN_AC30	90	HSMC_D33	PIN_AC29
91	HSMC_D34	PIN_AC27	92	HSMC_D35	PIN_AC26
93	HSMC_3p3v		94	12v	
95	HSMC_D36	PIN_AE30	96	HSMC_D37	PIN_U23
97	HSMC_D38	PIN_AD30	98	HSMC_D39	PIN_T24
99	HSMC_3p3v		100	12v	
101	HSMC_D40	PIN_AC24	102	HSMC_D41	PIN_AD29
103	HSMC_D42	PIN_AD28	104	HSMC_D43	PIN_AD27
105	HSMC_3p3v		106	12v	
107	HSMC_D44	PIN_AD24	108	HSMC_D45	PIN_AD23
109	HSMC_D46	PIN_AE28	110	HSMC_D47	PIN_AE27
111	HSMC_3p3v		112	12v	
113	HSMC_D48	PIN_AE26	114	HSMC_D49	PIN_AE25
115	HSMC_D50	PIN_AF30	116	HSMC_D51	PIN_AF29
117	HSMC_3p3v		118	12v	
119	HSMC_D52	PIN_AF28	120	HSMC_D53	PIN_AF26
121	HSMC_D54	PIN_AF25	122	HSMC_D55	PIN_AG29
123	HSMC_3p3v		124	12v	
125	HSMC_D56	PIN_AG28	126	HSMC_D57	PIN_AG27
127	HSMC_D58	PIN_AH30	128	HSMC_D59	PIN_AH29
129	HSMC_3p3v		130	12v	
131	HSMC_D60	PIN_AH27	132	HSMC_D61	PIN_AJ30
133	HSMC_D62	PIN_AG8	134	HSMC_D63	PIN_AF8
135	HSMC_3p3v		136	12v	
137	HSMC_D64	PIN_AH7	138	HSMC_D65	PIN_AG7
139	HSMC_D66	PIN_AF7	140	HSMC_D67	PIN_AH6
141	HSMC_3p3v		142	12v	
143	HSMC_D68	PIN_AG6	144	HSMC_D69	PIN_AF6
145	HSMC_D70	PIN_AH5	146	HSMC_D71	PIN_AH4
147	HSMC_3p3v		148	12v	
149	HSMC_D72	PIN_AD9	150	HSMC_D73	PIN_AC9
151	HSMC_D74	PIN_AB9	152	HSMC_D75	PIN_AB8
153	HSMC_3p3v		154	12v	
155	HSMC_D76	PIN_AJ28	156	HSMC_D77	PIN_U21
157	HSMC_D78	PIN_AJ29	158	HSMC_D79	PIN_U22
159	HSMC_3p3v		160	HSMC PSNTn	

5.4.7 GPIO

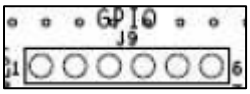


Table 10 shows the pin assignment between GPIO (J9) and the FPGA.

Table 10 Pin assignment between GPIO and FPGA

GPIO	FPGA'S PIN NUM
1	PIN_V21
2	PIN_V22
3	PIN_AE23
4	PIN_Y21
5	PIN_AF24
6	PIN_AA26

5.5 Memory

This chapter describes the memory interfaces of this Board. This Board has the following types of memory modules.

- DDR3-600 Mbps 32-bit
- DDR3-600 Mbps 64-bit

These two types are divided into Top bank and Bottom bank as shown in Figure 6.

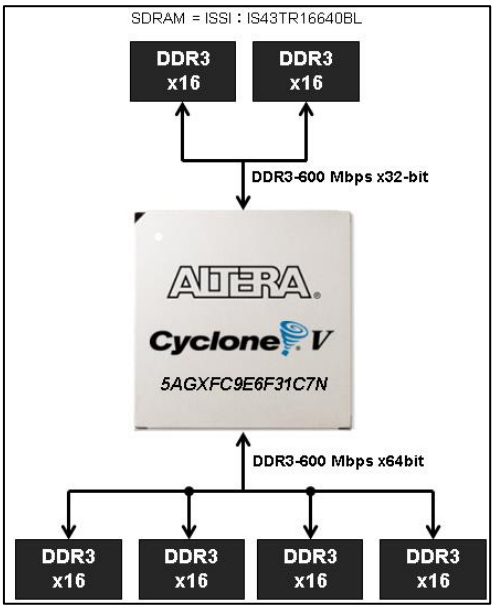


Figure 6 DDR3 configuration

5.5.1 DDR3 32-bit Top bank

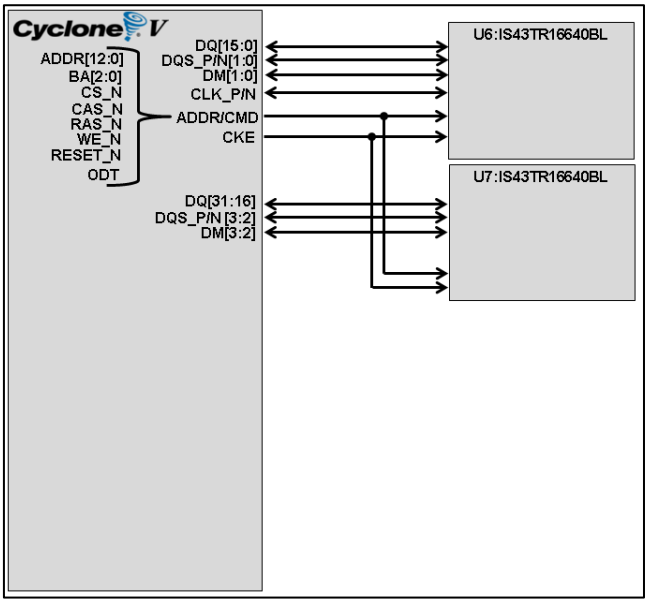


Table 11 shows the pin assignment between DDR3 32-bit (U6 and U7) and the FPGA.

Table 11 Pin assignment between DDR3 32-bit and FPGA

Signal name	SDRAM U6	SDRAM U7	FPGA'S PIN NUM
DDR3_x32_ADDR0	N3	N3	PIN_D19
DDR3_x32_ADDR1	P7	P7	PIN_A21
DDR3_x32_ADDR2	P3	P3	PIN_A23
DDR3_x32_ADDR3	N2	N2	PIN_D14
DDR3_x32_ADDR4	P8	P8	PIN_D18
DDR3_x32_ADDR5	P2	P2	PIN_A15
DDR3_x32_ADDR6	R8	R8	PIN_B27
DDR3_x32_ADDR7	R2	R2	PIN_B13
DDR3_x32_ADDR8	T8	T8	PIN_E18
DDR3_x32_ADDR9	R3	R3	PIN_E20
DDR3_x32_ADDR10	L7	L7	PIN_C24
DDR3_x32_ADDR11	R7	R7	PIN_E23
DDR3_x32_ADDR12	N7	N7	PIN_A20
DDR3_x32_BA0	M2	M2	PIN_F20
DDR3_x32_BA1	N8	N8	PIN_H21
DDR3_x32_BA2	M3	M3	PIN_A26
DDR3_x32_CLK_P	J7	J7	PIN_B22
DDR3_x32_CLK_N	K7	K7	PIN_B21
DDR3_x32_CKE	K7	K7	PIN_A24
DDR3_x32_CS_N	L2	L2	PIN_E22
DDR3_x32_DM0	E7		PIN_E21
DDR3_x32_DM1	D3		PIN_C19
DDR3_x32_DM2		E7	PIN_G18
DDR3_x32_DM3		D3	PIN_E17
DDR3_x32_RAS_N	J3	J3	PIN_B23
DDR3_x32_CAS_N	K3	K3	PIN_D20
DDR3_x32_WE_N	L3	L3	PIN_K18
DDR3_x32_RESET_N	T2	T2	PIN_F19
DDR3_x32_ODT	K1		PIN_B24
DDR3_x32_DQ0	E3		PIN_E25
DDR3_x32_DQ1	F7		PIN_A28
DDR3_x32_DQ2	F2		PIN_G22
DDR3_x32_DQ3	F8		PIN_B26
DDR3_x32_DQ4	H3		PIN_C27
DDR3_x32_DQ5	H8		PIN_C26
DDR3_x32_DQ6	G2		PIN_G23
DDR3_x32_DQ7	H7		PIN_E26
DDR3_x32_DQ8	D7		PIN_A25
DDR3_x32_DQ9	C3		PIN_C20
DDR3_x32_DQ10	C8		PIN_C22
DDR3_x32_DQ11	C2		PIN_C25
DDR3_x32_DQ12	A7		PIN_C21
DDR3_x32_DQ13	A2		PIN_D22
DDR3_x32_DQ14	B8		PIN_D23
DDR3_x32_DQ15	A3		PIN_D25

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Signal name	SDRAM U6	SDRAM U7	FPGA'S PIN NUM
DDR3_x32_DQ13	A2		PIN_D22
DDR3_x32_DQ14	B8		PIN_D23
DDR3_x32_DQ15	A3		PIN_D25
DDR3_x32_DQ16		E3	PIN_A18
DDR3_x32_DQ17		F7	PIN_B19
DDR3_x32_DQ18		F2	PIN_B18
DDR3_x32_DQ19		F8	PIN_B17
DDR3_x32_DQ20		H3	PIN_A16
DDR3_x32_DQ21		H8	PIN_C14
DDR3_x32_DQ22		G2	PIN_C17
DDR3_x32_DQ23		H7	PIN_A19
DDR3_x32_DQ24		D7	PIN_C11
DDR3_x32_DQ25		C3	PIN_D17
DDR3_x32_DQ26		C8	PIN_B14
DDR3_x32_DQ27		C2	PIN_C12
DDR3_x32_DQ28		A7	PIN_C16
DDR3_x32_DQ29		A2	PIN_A14
DDR3_x32_DQ30		B8	PIN_A13
DDR3_x32_DQ31		A3	PIN_D12
DDR3_x32_DQS0_P	F3		PIN_L20
DDR3_x32_DQS1_P	C7		PIN_K20
DDR3_x32_DQS2_P		F3	PIN_K16
DDR3_x32_DQS3_P		C7	PIN_K17
DDR3_x32_DQS0_N	G3		PIN_L19
DDR3_x32_DQS1_N	B7		PIN_J19
DDR3_x32_DQS2_N		G3	PIN_L16
DDR3_x32_DQS3_N		B7	PIN_J17
OCT_RZQIN			PIN_B12

5.5.2 DDR3 64-bit Bottom bank

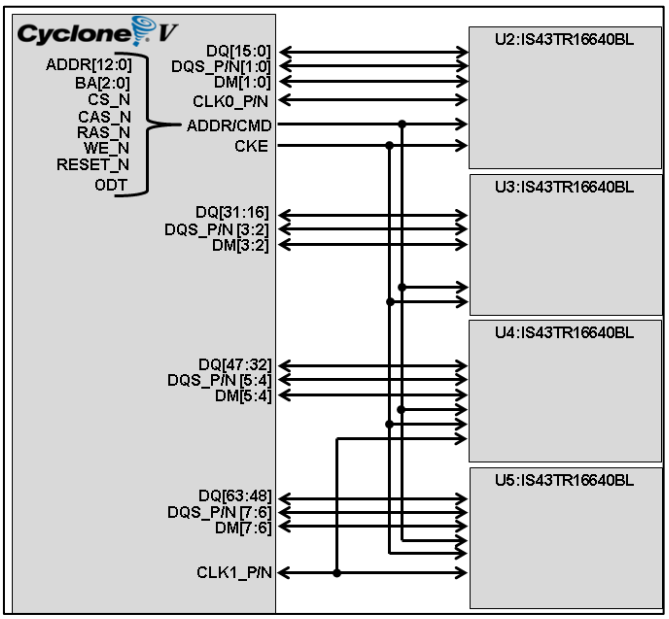


Table 12 shows the pin assignment between DDR3 64-bit (U2, U3, U4, and U5) and the FPGA.

Table 12 Pin assignment between DDR3 64-bit and FPGA

Signal name	SDRAM U2	SDRAM U3	SDRAM U4	SDRAM U5	FPGA'S PIN NUM
DDR3_x64_ADDR0	N3	N3	N3	N3	PIN_AA18
DDR3_x64_ADDR1	P7	P7	P7	P7	PIN_AK20
DDR3_x64_ADDR2	P3	P3	P3	P3	PIN_AK10
DDR3_x64_ADDR3	N2	N2	N2	N2	PIN_AJ10
DDR3_x64_ADDR4	P8	P8	P8	P8	PIN_AJ24
DDR3_x64_ADDR5	P2	P2	P2	P2	PIN_AK6
DDR3_x64_ADDR6	R8	R8	R8	R8	PIN_AJ25
DDR3_x64_ADDR7	R2	R2	R2	R2	PIN_AJ1
DDR3_x64_ADDR8	T8	T8	T8	T8	PIN_AH17
DDR3_x64_ADDR9	R3	R3	R3	R3	PIN_AJ9
DDR3_x64_ADDR10	L7	L7	L7	L7	PIN_AA19
DDR3_x64_ADDR11	R7	R7	R7	R7	PIN_AF19
DDR3_x64_ADDR12	N7	N7	N7	N7	PIN_AF10
DDR3_x64_BA0	M2	M2	M2	M2	PIN_AG11
DDR3_x64_BA1	N8	N8	N8	N8	PIN_AK28
DDR3_x64_BA2	M3	M3	M3	M3	PIN_AG16
DDR3_x64_CLK0_P	J7	J7			PIN_AB12
DDR3_x64_CLK0_N	K7	K7			PIN_AB13
DDR3_x64_CLK1_P			J7	J7	PIN_AB22
DDR3_x64_CLK1_N			K7	K7	PIN_AC22
DDR3_x64_CKE	K7	K7	K7	K7	PIN_AJ17
DDR3_x64_CS_N	L2	L2	L2	L2	PIN_AK21
DDR3_x64_DM0	E7				PIN_AD13
DDR3_x64_DM1	D3				PIN_AF11
DDR3_x64_DM2		E7			PIN_AG13
DDR3_x64_DM3		D3			PIN_AE16

Continued from the previous page

Signal name	SDRAM U2	SDRAM U3	SDRAM U4	SDRAM U5	FPGA'S PIN NUM
DDR3_x64_DM4			E7		PIN_AF16
DDR3_x64_DM5			D3		PIN_AE18
DDR3_x64_DM6				E7	PIN_AE20
DDR3_x64_DM7				D3	PIN_AF20
DDR3_x64_RAS_N	J3	J3	J3	J3	PIN_AE13
DDR3_x64_CAS_N	K3	K3	K3	K3	PIN_AH14
DDR3_x64_WE_N	L3	L3	L3	L3	PIN_AJ7
DDR3_x64_RESET_N	T2	T2	T2	T2	PIN_AG19
DDR3_x64_ODT	K1	K1	K1	K1	PIN_AG26
DDR3_x64_DQ0	E3				PIN_AJ2
DDR3_x64_DQ1	F7				PIN_AK3
DDR3_x64_DQ2	F2				PIN_AJ3
DDR3_x64_DQ3	F8				PIN_AJ4
DDR3_x64_DQ4	H3				PIN_AJ5
DDR3_x64_DQ5	H8				PIN_AE10
DDR3_x64_DQ6	G2				PIN_AE12
DDR3_x64_DQ7	H7				PIN_AD12
DDR3_x64_DQ8	D7				PIN_AK5
DDR3_x64_DQ9	C3				PIN_AK7
DDR3_x64_DQ10	C8				PIN_AK8
DDR3_x64_DQ11	C2				PIN_AJ8
DDR3_x64_DQ12	A7				PIN_AG9
DDR3_x64_DQ13	A2				PIN_AF9
DDR3_x64_DQ14	B8				PIN_AG12
DDR3_x64_DQ15	A3				PIN_AF13
DDR3_x64_DQ16		E3			PIN_AH9
DDR3_x64_DQ17		F7			PIN_AH10
DDR3_x64_DQ18		F2			PIN_AK11
DDR3_x64_DQ19		F8			PIN_AH11
DDR3_x64_DQ20		H3			PIN_AK12
DDR3_x64_DQ21		H8			PIN_AJ12
DDR3_x64_DQ22		G2			PIN_AH12
DDR3_x64_DQ23		H7			PIN_AG14
DDR3_x64_DQ24		D7			PIN_AJ14
DDR3_x64_DQ25		C3			PIN_AF14
DDR3_x64_DQ26		C8			PIN_AK15
DDR3_x64_DQ27		C2			PIN_AJ15
DDR3_x64_DQ28		A7			PIN_AH15
DDR3_x64_DQ29		A2			PIN_AE15
DDR3_x64_DQ30		B8			PIN_AE17
DDR3_x64_DQ31		A3			PIN_AD17
DDR3_x64_DQ32			E3		PIN_AK16
DDR3_x64_DQ33			F7		PIN_AK17
DDR3_x64_DQ34			F2		PIN_AG17
DDR3_x64_DQ35			F8		PIN_AK18
DDR3_x64_DQ36			H3		PIN_AJ18

Continued from the previous page

Signal name	Signal name	Signal name	Signal name	Signal name	Signal name
DDR3_x64_DQ37			H8		PIN_AJ19
DDR3_x64_DQ38			G2		PIN_AH19
DDR3_x64_DQ39			H7		PIN_AH20
DDR3_x64_DQ40			D7		PIN_AF18
DDR3_x64_DQ41			C3		PIN_AD18
DDR3_x64_DQ42			C8		PIN_AJ20
DDR3_x64_DQ43			C2		PIN_AH21
DDR3_x64_DQ44			A7		PIN_AK22
DDR3_x64_DQ45			A2		PIN_AJ22
DDR3_x64_DQ46			B8		PIN_AJ23
DDR3_x64_DQ47			A3		PIN_AK23
DDR3_x64_DQ48				E3	PIN_AG18
DDR3_x64_DQ49				F7	PIN_AD19
DDR3_x64_DQ50				F2	PIN_AG24
DDR3_x64_DQ51				F8	PIN_AH24
DDR3_x64_DQ52				H3	PIN_AH25
DDR3_x64_DQ53				H8	PIN_AK25
DDR3_x64_DQ54				G2	PIN_AK26
DDR3_x64_DQ55				H7	PIN_AJ27
DDR3_x64_DQ56				D7	PIN_AG21
DDR3_x64_DQ57				C3	PIN_AE22
DDR3_x64_DQ58				C8	PIN_AH22
DDR3_x64_DQ59				C2	PIN_AG22
DDR3_x64_DQ60				A7	PIN_AF23
DDR3_x64_DQ61				A2	PIN_AG23
DDR3_x64_DQ62				B8	PIN_AH26
DDR3_x64_DQ63				A3	PIN_AK27
DDR3_x64_DQS0_P	F3				PIN_V12
DDR3_x64_DQS1_P	C7				PIN_Y12
DDR3_x64_DQS2_P		F3			PIN_Y13
DDR3_x64_DQS3_P		C7			PIN_Y16
DDR3_x64_DQS4_P			F3		PIN_Y17
DDR3_x64_DQS5_P			C7		PIN_Y20
DDR3_x64_DQS6_P				F3	PIN_AB19
DDR3_x64_DQS7_P				C7	PIN_AC21
DDR3_x64_DQS0_N	G3				PIN_W12
DDR3_x64_DQS1_N	B7				PIN_AA13
DDR3_x64_DQS2_N		G3			PIN_AA14
DDR3_x64_DQS3_N		B7			PIN_AA16
DDR3_x64_DQS4_N			G3		PIN_Y18
DDR3_x64_DQS5_N			B7		PIN_AA20
DDR3_x64_DQS6_N				G3	PIN_AC19
DDR3_x64_DQS7_N				B7	PIN_AD20
OCT_RZQIN					PIN_AK13

5.6 Power Connector and Switch

The output of the AC adapter for the Nitro Board, which is included in the package, is 12V DC. The maximum voltage that can be input to the Board is 12V. The power circuit on the Board converts it to various voltages and supplies them to each component, HSMC and the test pin header.

Danger	Make sure to use the AC adapter that is included in the package. Using an AC adapter not meeting the specifications described in this Manual may cause the kit to emit heat, explode, or ignite.

Table 13 shows the pin assignment of the DC jack and the slide switch.

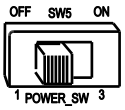


Table 13 Pin assignment of DC jack and slide switch

Board Reference		Legend	Specification
U21		DC_JACK	Center positive 12V input
SW5	1	POWER_SW	Power ON when slid to the "3" pin side. Power OFF when slid to the "1" pin side.
	3		

5.7 Power Connector for the Cooling Fan

The included heatsink has a cooling fan. Connect the fan cable to the J10 pins of this Board. Connect the red wire to the "1" pin and the black wire to the "2" pin.

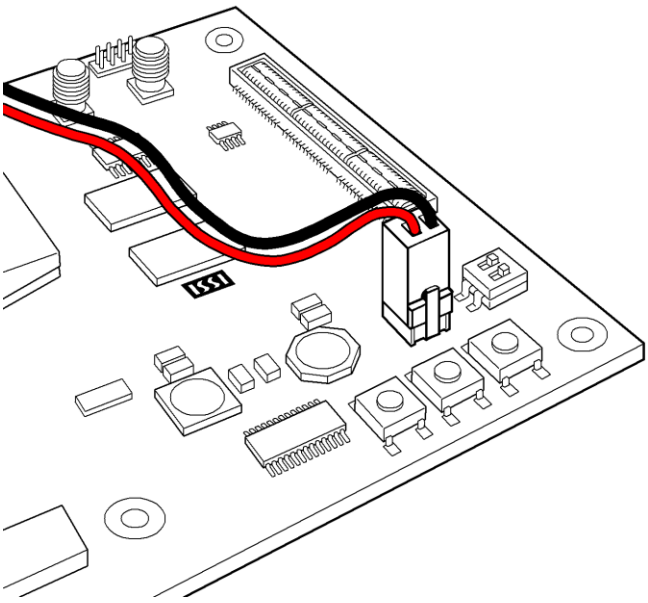


Table 14 shows the pin assignment of the power connector for the cooling fan.

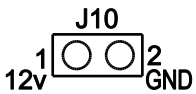
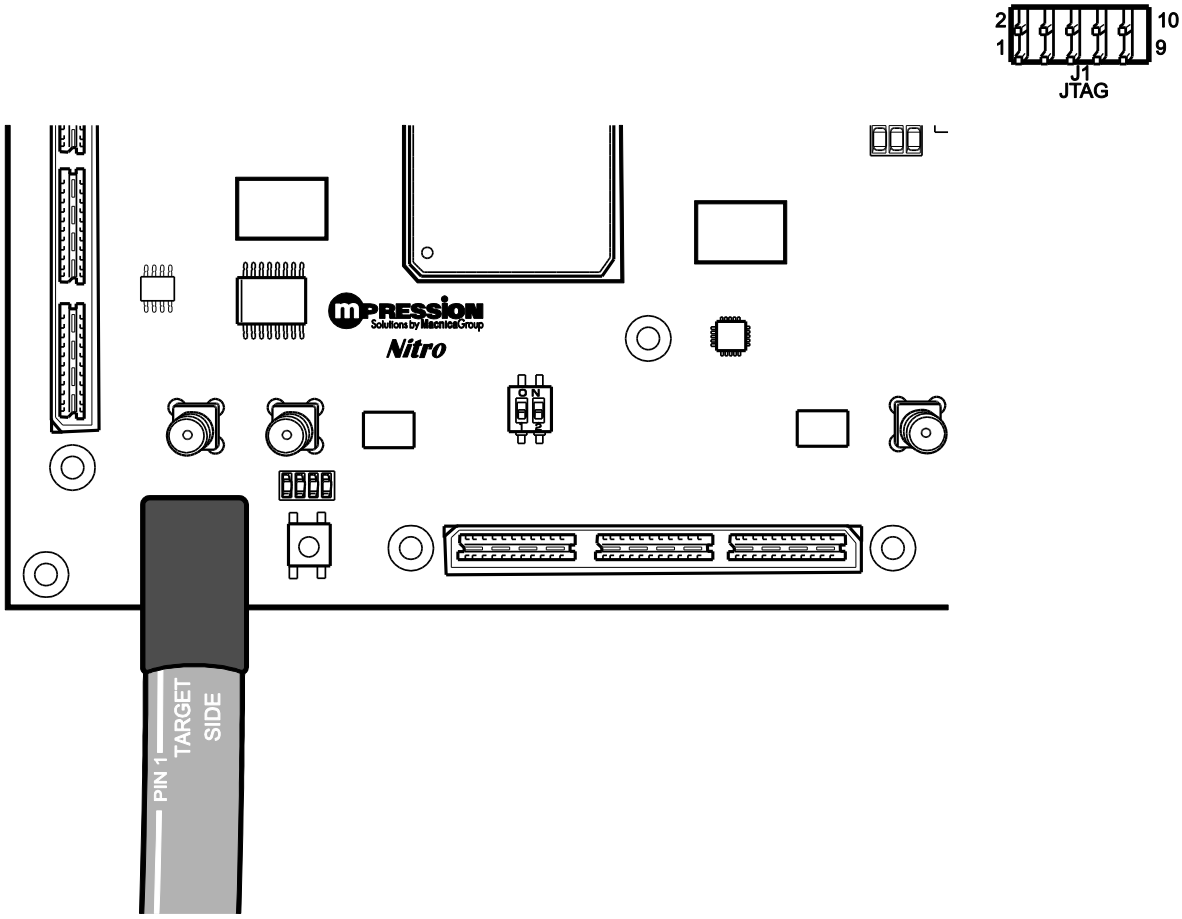


Table 14 Pin assignment of the power connector for the cooling fan

Board Reference		Signal name
J10	1	12V
	2	GND

5.8 JTAG 10-pin Header

Connect a USB-Blaster cable. The white line on the cable must be on the "1" pin side.



Detailed information on the USB-Blaster can be obtained from the following URL:
http://www.altera.com/literature/ug/ug_usb_blstr.pdf

6. Document Revision History

Date	Revision	Changes
August, 2014	1	• Document created
September, 2014	1.1	• FAN's Power Connector picture changed
October, 2014	1.2	• HSMA header fixed
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