# INTEL® FPGA IP

## Maximize System Performance and Design Productivity with IP Solutions

# BROAD PORTFOLIO OF IP

For a system to work, programmable logic devices must be able to communicate with the other devices on the board.

Why is Intel investing in the development, enhancement, and support of a broad intellectual property (IP) portfolio? The reason is simple: for a system to work, programmable logic devices must be able to communicate with the other devices on the board. Therefore, it is imperative for Intel to support various communication interfaces, external memory interfaces, and system building blocks. The capabilities of Intel® FPGAs have gone beyond simple glue logic. They are becoming the heart of many applications, and IP plays a key role in enabling this evolution.

Intel has been developing and licensing IP for over 20 years. From simple arithmetic functions to high-performance communications interfaces, processor subsystems, and application-specific solutions, Intel FPGA IP enables you to create applications on Intel FPGAs for a wide range of markets. The combination of Intel and application-specific IP from a community of trusted partners simplifies your development effort while maximizing design productivity. By utilizing IP, you can implement algorithms and protocol interfaces quickly without needing to know the details.

**FIGURE 1. INTEL AND PARTNER IP OPTIMIZED FOR INTEL FPGAS**


**Intel® FPGA Intellectual Property**

intel FPGA Design Solutions Network

# ACCELERATED DESIGN PRODUCTIVITY

The process of identifying and qualifying IP is often time consuming. Qualifying the supplier can sometimes take as much time as selecting the IP itself. Because of this, Intel has simplified the IP selection process by enabling the use of IP from Intel and its Design Solutions Network (DSN) members throughout the Intel Quartus® Prime software design flow from the time it is installed.

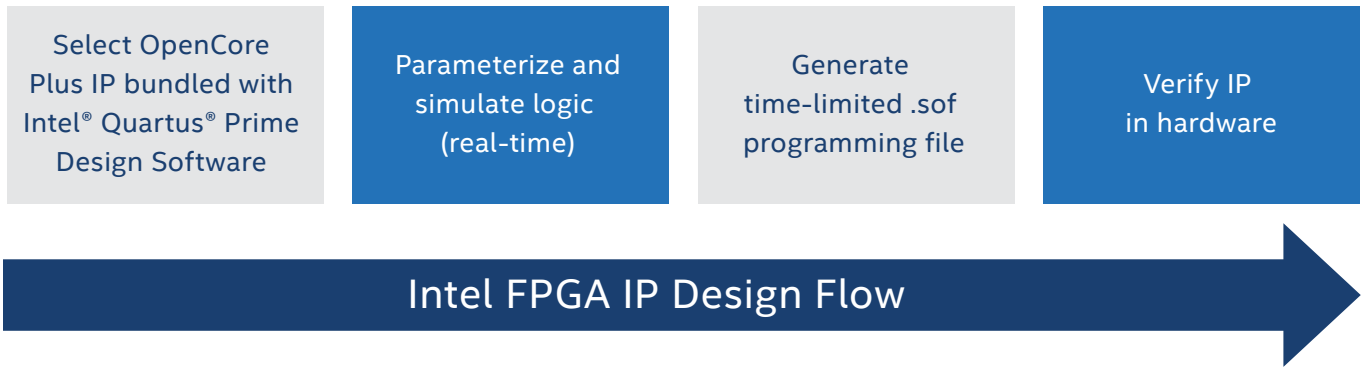
The first step is to download the Quartus Prime design software from our online Download Center. Intel FPGA IP is installed automatically with the Quartus Prime design software and available for immediate use. The IP evaluation flow, called OpenCore Plus, delivers a powerful productivity advantage. With OpenCore Plus, you do not need to acquire a license before evaluating the IP. You can:

- Simulate the core behavior within your system
- Verify the design functionality and quickly evaluate its size and performance
- Generate time-limited device programming files for designs that incorporate the Intel or DSN member IP
- Program a device and verify the design in hardware

The majority of our DSN members also support the OpenCore Plus evaluation feature.

You only need to pay a license fee to obtain production use license rights to the IP when you determine it to be a good fit for your design. No additional product delivery is required. Intel FPGA IP is licensed on a perpetual, royalty-free, per-seat basis, allowing it to be reused in an unlimited number of projects. Once purchased, you can manage your IP licenses via our Self-Service Licensing Center with your myAltera account.

**FIGURE 2. INTEL FPGA IP DESIGN FLOW**



# COMPLETE SOLUTIONS

Intel offers a complete solution that enables you to acquire the FPGAs, IP, and hardware platforms for initial development from a single source.

This complete solution includes:

- IP in soft and hard format
- Design environment
- Development kits
- Reference designs, design examples, and technical documentation

Intel provides IP in soft and hard formats. The key benefit of hardening IP into devices is resource savings. Hardening pre-proven blocks frees up the logic cells in the FPGA, leaving more room for your design.

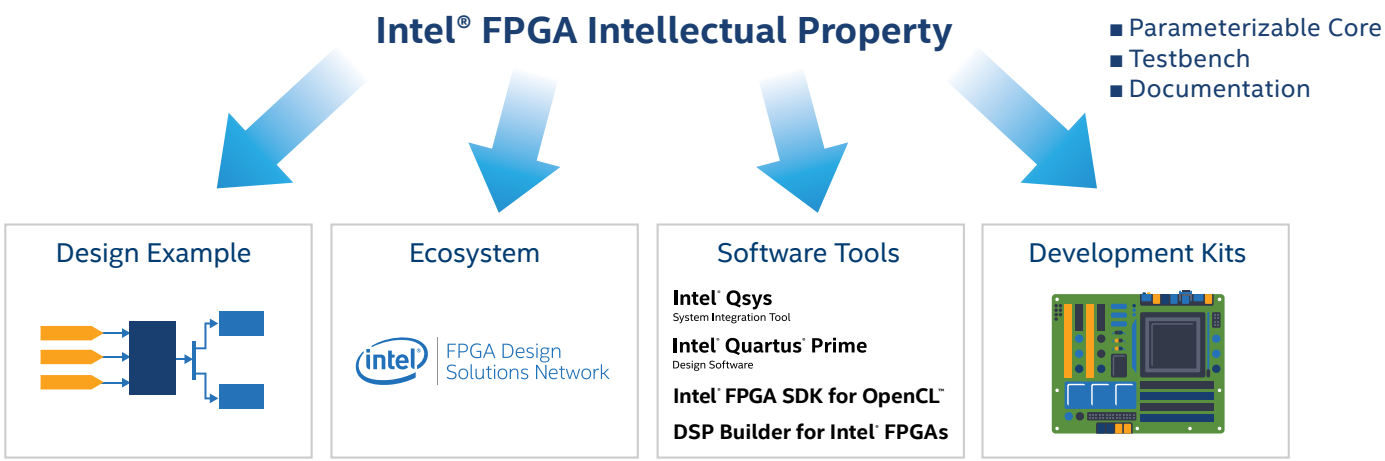
The Intel Quartus Prime design software environment allows you to integrate your own logic with Intel and DSN member IP. With tools such as DSP Builder for Intel FPGAs and Intel FPGA SDK for OpenCL™, your logic does not have to be in a HDL format. The Intel Qsys system integration tool provides an additional productivity advantage by reducing the time needed to integrate the system components.

Intel develops and sells a broad range of development kits for prototype and system design. Application-specific development kits and daughtercards are also available from our DSN member network to improve your design productivity.

Last but not least, Intel and its DSN members offer a wide range of design examples as blueprints to jump start your designs. Some design examples are sample implementations with additional peripherals and interfaces. Others are complete system or sub-system designs for a given application area. Design examples and comprehensive documentation are provided to aid IP integration and initial design verification.



**FIGURE 3. COMPONENTS OF THE INTEL FPGA IP COMPLETE SOLUTIONS**



# MULTIPLE NAMES, COMPARABLE QUALITY

Intel FPGA IP is grouped into different categories to help you understand how the IP can be used. All Intel FPGA IP, whether or not free, undergo the same verification methodology to ensure quality. The IP is developed to allow maximum flexibility and usability across a broad range of applications. A parameterization graphical user interface (GUI) enables you to tailor the IP configuration to meet the performance demands of your application.

**TABLE 1. IP ATTRIBUTES**

| IP CATEGORY | DESCRIPTION | PARAMETERIZATION GUI | FREE | LICENSE |
|---|---|---|---|---|
| Intel FPGA IP function | Encrypted IP | ✓ | | ✓ |
| Hard Intel FPGA IP function | Hard IP | ✓ | ✓ | |
| Megafunction | Ranges from basic arithmetic to transceiver blocks in source code format | ✓ | ✓ | |
| DSN member IP | Encrypted or source code | ✓ | | ✓ |
| Qsys component | IP for use in the Qsys system integration tool | ✓ | ✓ | |
| IP application | Encrypted, full application design (e.g. Optical Transport Network) | | | ✓ |
| Reference design | Subsystem or system blueprints using one or more Intel FPGA IP functions | | ✓[1] | |
| Design example | Ranges from documentation to example implementations of an Intel FPGA IP function | | ✓ | |

Notes:
1. Few exceptions

# PARTNERED WITH EXPERTS

## FPGA Design Solutions Network

Intel has been partnering with leading third-party IP developers for over 10 years. These trusted partners bring complementary products and expertise while extending the range of applications you can implement with Intel FPGAs. Through the Intel FPGA DSN program, members gain access to software, training, hardware platforms, IP packaging tools, and direct support from Intel. Member IP is optimized for Intel FPGAs and pre-verified for use.

Table 2 shows a short list of our DSN partners and their technology expertise. For the complete list, please visit www.altera.com/dsn.

**TABLE 2. SAMPLE DSN MEMBER LIST**

| PARTNER | EXPERTISE |
|---|---|
| Arrive Technologies | SONET SDH, Carrier Ethernet, Pseudowire |
| Bitec | DisplayPort, HDMI, V-by-One IP, Video boards |
| Algo-Logic Systems | Data Center Rack Solutions for 10G / 40G / 100G Networks |
| IntelliProp | SATA and SAS |
| Intilop | 10G TCP offload IP |
| MoreThanIP | Ethernet and Fibre Channel |
| Northwest Logic | Memory controllers, PCI Express* (PCIe*), and MIPI |
| Softing | Industrial Factory Automation |
| System Level Solutions | Computer and Storage (USB, flash memory, and others) |

# INTEL AND DSN MEMBER IP FUNCTIONS

www.altera.com/ip

For a complete list of IP functions from Intel and its DSN members, please visit www.altera.com/ip.

| | PRODUCT NAME | VENDOR NAME |
|---|---|---|
| DSP | **ARITHMETIC** | |
| | Floating Point Megafunctions | Intel |
| | Floating Point Arithmetic Co-Processor | Digital Core Design |
| | Floating Point Arithmetic Unit | Digital Core Design |
| | **ERROR DETECTION/CORRECTION** | |
| | Reed-Solomon Encoder/Decoder II[1] | Intel |
| | Viterbi Compiler, High-Speed Parallel Decoder | Intel |
| | Viterbi Compiler, Low-Speed/ Hybrid Serial Decoder | Intel |
| | Turbo Encoder/Decoder | Intel |
| | High-Speed Reed Solomon Encoder/ Decoder | Intel |
| | BCH Encoder/Decoder | Intel |
| | Low-Density Parity Check Encoder/ Decoder | Intel |
| | Zip-Accel-C: GZIP/ZLIB/Deflate Data Compression Core | CAST, Inc. |
| | Zip-Accel-D: GUNZIP/ZLIP/Inflate Data Decompression Core | CAST, Inc. |
| | **FILTERS AND TRANSFORMS** | |
| | Fast Fourier Transform (FFT)/ Inverse FFT (IFFT) | Intel |
| | Cascaded Integrator Comb (CIC) Compiler | Intel |
| | Finite Impulse Response (FIR) Compiler II | Intel |
| | SHA-1 | CAST, Inc. |
| | SHA-256 | CAST, Inc. |
| | AES CODECs | CAST, Inc. |
| | **MODULATION/DEMODULATION** | |
| | Numerically Controlled Oscillator Compiler | Intel |
| | ATSC and Multi-Channel ATSC 8-VSB Modulators | Commsonic |
| | DVB-T Modulator | Commsonic |
| | DVB-S2 Modulator | Commsonic |
| | Multi-Channel Cable (QAM) Modulator | Commsonic |

| | PRODUCT NAME | VENDOR NAME |
|---|---|---|
| DSP (CONTINUED) | **VIDEO AND IMAGE PROCESSING** | |
| | Video and Image Processing Suite[1] | Intel |
| | HD JPEG 2000 Encoders/ Decoders | IntoPIX |
| | TICO Lightweight Video Compression | IntoPIX |
| | Multi-Channel JPEG 2000 Encoder and Decoder Cores | Barco Silex |
| | VC-2 High Quality Video Decoder | Barco Silex |
| | VC-2 High Quality Video Encoder | Barco Silex |
| | MPEG-2 TS Encapsulator/ Decapsulator for SMPTE2022 1/2 | IntoPIX |
| | JPEG Encoders | CAST, Inc. |
| | Ultra-fast, 4K-compatible, AVC/ H.264 Baseline Profile Encoder | CAST, Inc. |
| | Low-Power AVC / H.264 Baseline Profile Encoder | CAST, Inc. |
| | H.265 Main Profile Video Decoder | CAST, Inc. |
| | H.265 Encoders | Jointwave Group LLC |
| | H.264 Encoders | Jointwave Group LLC |
| | Video Processor and Deinterlacer with Line-Doubled Output | Crucial IP, Inc. |
| | Configurable Cross Converter | Crucial IP, Inc. |
| | Video Scaler with Shrink and Zoom Support | Crucial IP, Inc. |
| | Mosquito / Block Noise Reducer | Crucial IP, Inc. |
| | Adaptive Detail Enhancer | Crucial IP, Inc. |
| PROCESSORS AND PERIPHERALS | **HARD/SOFT PROCESSORS** | |
| | Nios II Embedded Processors[1] | Intel |
| | ARM Cortex-A9 MPCore Processor in Intel SoC | Intel |
| | ARM Cortex-A53 MPCore Processor in Intel SoC | Intel |

Notes:
1. Qsys-compliant licensed core.

| | PRODUCT NAME | VENDOR NAME |
|---|---|---|
| INTERFACE AND PROTOCOLS | **COMMUNICATION** | |
| | Optical Transport Network (OTN) Framers/Deframers | Intel |
| | SFI-5.1 | Intel |
| | SDN CodeChips | Arrive Technologies |
| | SONET/SDH CodeChips | Arrive Technologies |
| | **ETHERNET** | |
| | Low-Latency 10 Gbps Ethernet Media Access Controller (MAC)[1] with 1588 | Intel |
| | Triple-Speed Ethernet (10/100/1000 Mbps) MAC and PHY[1] with 1588 Option | Intel |
| | 1 / 2.5 / 5 / 10G Multi-Rate PHY and Backplane Options | Intel |
| | 10G Base-X (XAUI) PHY | Intel |
| | 40G Ethernet MAC and PHY with 1588 and Backplane Options | Intel |
| | 100G Ethernet MAC and PHY with 1588 and RS-FEC options | Intel |
| | 25G MAC and PHY with RS-FEC option | Intel |
| | 50G MAC and PHY | Intel |
| | 1G/10Gb Ethernet PHY | Intel |
| | Carrier Ethernet CodeChips | Arrive Technologies |
| | Pseudowire CodeChips | Arrive Technologies |
| | High-Performance Gigabit Ethernet MAC[1] | IFI |
| | 10 Gigabit Reduced XAUI PCS Core (RXAUI) | MorethanIP |
| | SPAUI MAC Core | MorethanIP |
| | 20 Gigabit DXAUI PCS Core | MorethanIP |
| | QSGMII PCS Core | MorethanIP |
| | 2.5 Gbps Ethernet MAC | MorethanIP |

| | PRODUCT NAME | VENDOR NAME |
|---|---|---|
| INTERFACE AND PROTOCOLS (CONTINUED) | **HIGH SPEED** | |
| | JESD204B | Intel |
| | RapidIO*[1] Gen1, Gen2 | Intel |
| | Common Public Radio Interface (CPRI) | Intel |
| | Interlaken | Intel |
| | Interlaken Look-Aside | Intel |
| | QuickPath Interconnect (QPI) | Intel |
| | SerialLite II/III | Intel |
| | SATA 1.0/SATA 2.0 | Intelliprop, Inc. |
| | RapidIO Gen3 | Mobiveil |
| | QDR Infiniband Target Channel Adapter | Polybus |
| | **PCIE / PCI** | |
| | PCIe Gen1 x1[1], x4[1] Controller (Soft IP) | Intel |
| | PCIe Gen1, Gen2, Gen3 x1, x2, x4, x8, and x16 Controller (Hardened IP) | Intel |
| | PCI 32/64 bit PCI Master Target 33/66 MHz Controllers | CAST, Inc. |
| | PCI Multifunction Master/ Target Interface | CAST, Inc. |
| | Expresso 3.0 PCI Express Core (Gen 1 - 3) | Northwest Logic, Inc. |
| | PCI Express Multiport Transparent Switch | Mobiveil, Inc. |
| | PCI Express Hybrid Controller | Mobiveil, Inc. |
| | PCI Express to AXI Bridge Controller | Mobiveil, Inc. |
| | PCI-X Core | Northwest Logic, Inc. |
| | PCI Core | Northwest Logic, Inc. |
| | XpressRICH3 PCIe Gen1, Gen2, and Gen3 | PLDA |
| | PCI and PCI-X Master/ Target Cores 32/64 bit | PLDA |

Notes:
1. Qsys-compliant licensed core.

| | PRODUCT NAME | VENDOR NAME |
|---|---|---|
| INTERFACE AND PROTOCOLS (CONTINUED) | **SERIAL** | |
| | Generic QUAD SPI Controller | Intel |
| | Avalon® I²C (Master) | Intel |
| | I²C Slave to Avalon-MM Master Bridge | Intel |
| | Serial Peripheral Interface (SPI)/ Avalon Master Bridge[2] | Intel |
| | UART[2] | Intel |
| | JTAG UART[2] | Intel |
| | 16550 UART | Intel |
| | JTAG/Avalon Master Bridge[2] | Intel |
| | CAN 2.0/FD[1] | CAST, Inc. |
| | Local Interconnect Network (LIN) Controller | CAST, Inc. |
| | H16550S UART | CAST, Inc. |
| | MD5 Message-Digest | CAST, Inc. |
| | Smart Card Reader | CAST, Inc. |
| | DI2CM I²C Bus Interface-Master | Digital Core Design |
| | DI2CSB I²C Bus Interface-Slave | Digital Core Design |
| | D16550 UART with 16-Byte FIFO | Digital Core Design |
| | DSPI Serial Peripheral Interface Master/Slave | Digital Core Design |
| | Secure Digital (SD)/MMC SPI | El Camino GmbH |
| | Secure Digital I/O (SDIO)/SD Memory/Slave Controller | Eureka Technology, Inc. |
| | SDIO/SD Memory/ MMC Host Controller | Eureka Technology, Inc. |
| | Nios II Advanced CAN[1] | IFI |
| | I²C Master/Slave/PIO Controller | Microtronix, Inc. |
| | I²C Master and Slave | SLS |
| | USB High-Speed Function Controller[1] | SLS |
| | USB Full-/Low-Speed Function Controller[1] | SLS |
| | Embedded USB 3.0 / 3.1 Gen 1 Host and Device Controllers | SLS |
| | USB 3.0 SuperSpeed Device Controller | SLS |

| | PRODUCT NAME | VENDOR NAME |
|---|---|---|
| INTERFACE AND PROTOCOLS (CONTINUED) | **AUDIO AND VIDEO** | |
| | Character LCD[2] | Intel |
| | Pixel Converter (BGR0 to BGR)[2] | Intel |
| | Video Sync Generator[2] | Intel |
| | SD/HD/3G-HD Serial Digital Interface (SDI) | Intel |
| | DisplayPort 1.1 and 1.2 | Intel |
| | HDMI 1.4 and 2.0 | Intel |
| | Bitec HDMI 2.0a IP core | Bitec |
| | DisplayPort 1.3 IP Core | Bitec |
| | HDCP IP Core | Bitec |
| | AC'97 Controller | SLS |
| MEMORIES AND MEMORY CONTROLLERS | **DMA** | |
| | Scatter-Gather DMA Controller[2] | Intel |
| | DMA Controller[2] | Intel |
| | DMA Controllers | Eureka Technology, Inc. |
| | Lancero Scatter-Gather DMA Engine for PCI Express | Microtronix, Inc. |
| | AXI* DMA back-End Core | Northwest Logic, Inc. |
| | Expresso DMA Bridge Core | Northwest Logic, Inc. |
| | Express DMA Core | Northwest Logic, Inc. |
| | **FLASH** | |
| | CompactFlash (True IDE)[2] | Intel |
| | EPCS Serial Flash Controller[2] | Intel |
| | Flash Memory[2] | Intel |
| | NAND Flash Controller | Eureka Technology, Inc. |
| | Universal NVM Express Controller (UNEX) | Mobiveil, Inc. |
| | ONFI Controller | SLS |
| | Enhanced ClearNAND Controller | SLS |

Notes:
1. Qsys-compliant licensed core.
2. Qsys component (no license required).

| | PRODUCT NAME | VENDOR NAME |
|---|---|---|
| MEMORIES AND MEMORY CONTROLLERS (CONTINUED) | **SDRAM** | |
| | DDR/DDR2 and DDR3/DDR4 SDRAM Controllers[1] | Intel |
| | LPDDR2 SDRAM Controller | Intel |
| | RLDRAM 2 Controller | Intel |
| | Hybrid Memory Cube Controller | Intel |
| | Streaming Multi-Port SDRAM Memory Controller | Microtronix, Inc. |
| | HyperDrive Multi-Port DDR2 Memory Controller | Microtronix, Inc. |
| | Avalon Multi-Port SDRAM Memory Controller[1] | Microtronix, Inc. |
| | RLDRAM II and III Controllers | Northwest Logic, Inc. |
| | LPDDR2/3 Controllers | Northwest Logic, Inc. |
| | **SRAM** | |
| | SSRAM (Cypress CY7C1380C)[2] | Intel |
| | QDR II/II+/II+Xtreme/IV SRAM Controller | Intel |

Notes:
1. Qsys-compliant licensed core.
2. Qsys component (no license required).



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