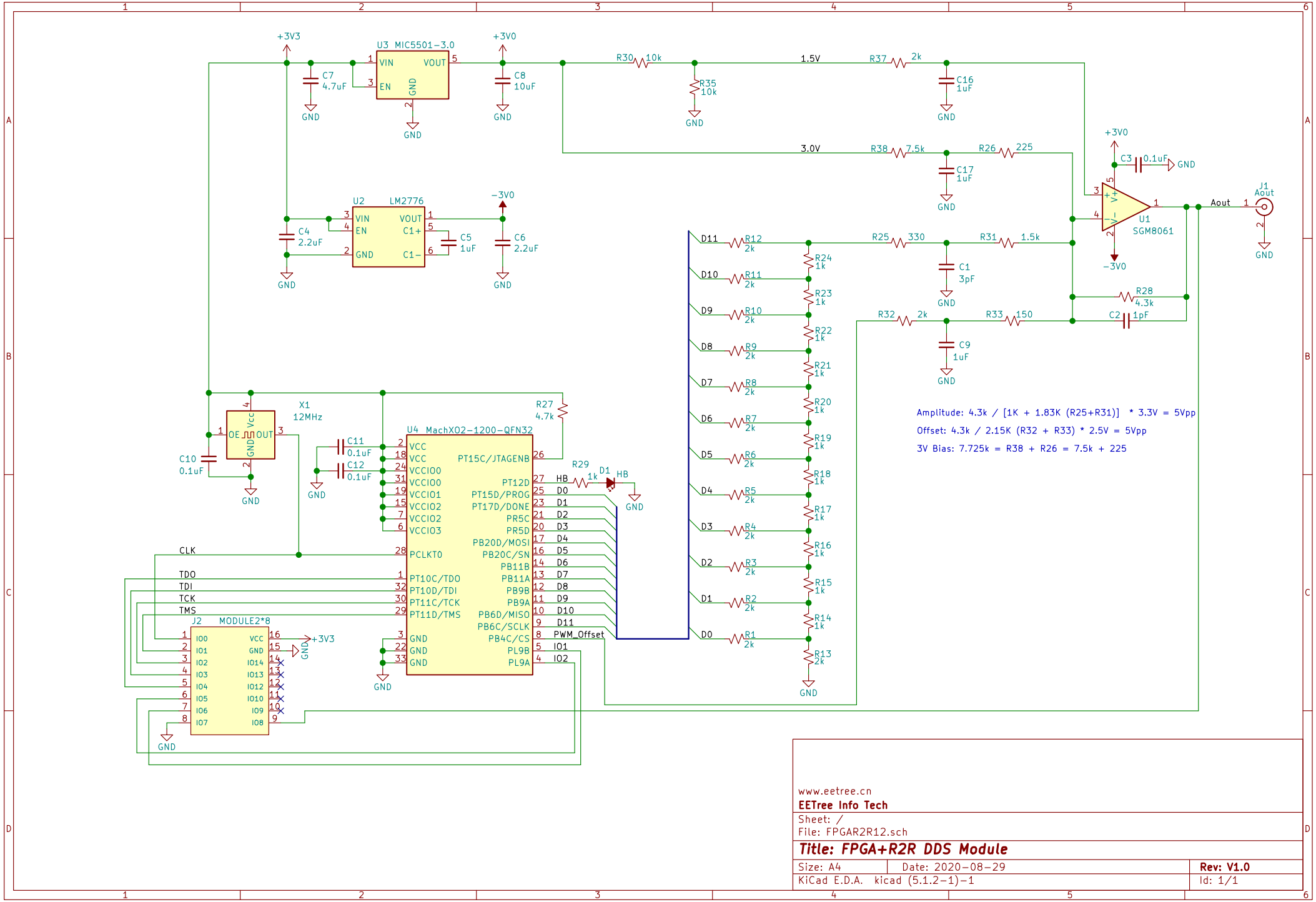
+3V3
U3 MIC5501-3.0
VIN
VOUT
EN
GND
C7
4.7uF
C8
10uF
+3V0
R30 10k
R35
10k
1.5V
R37 2k
C16
1uF
3.0V
R38 7.5k
R26 225
C17
1uF
U2 LM2776
C4
2.2uF
C5
1uF
C6
2.2uF
-3V0
C3
0.1uF
U1
SGM8061
Aout
J1
R25 330
R31 1.5k
C1
3pF
R28
4.3k
R32 2k
R33 150
C2
1pF
C9
1uF
X1
12MHz
C10
0.1uF
C11
0.1uF
C12
0.1uF
R27
4.7k
U4 MachXO2-1200-QFN32
R29 1k
D1
HB
CLK
TDO
TDI
TCK
TMS
J2 MODULE2*8
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
R12 2k
R11 2k
R10 2k
R9 2k
R8 2k
R7 2k
R6 2k
R5 2k
R4 2k
R3 2k
R2 2k
R1 2k
R24 1k
R23 1k
R22 1k
R21 1k
R20 1k
R19 1k
R18 1k
R17 1k
R16 1k
R15 1k
R14 1k
R13 2k
PWM_Offset
Amplitude: 4.3k / [1K + 1.83K (R25+R31)] * 3.3V = 5Vpp
Offset: 4.3k / 2.15K (R32 + R33) * 2.5V = 5Vpp
3V Bias: 7.725k = R38 + R26 = 7.5k + 225
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Sheet: /
File: FPGAR2R12.sch
Title: FPGA+R2R DDS Module
Size: A4
Date: 2020-08-29
Rev: V1.0
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