1st Edition

ANALOG SOLUTIONS FOR ALTERA FPGAs

Product Guide

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Analog Solutions for Altera FPGAs

A message from the Vice President, Product Marketing, Corporate Marketing, and Technical Services, Altera

Dear Customers,

System designs use digital and analog signals to communicate and process information. And most likely, so does your design. But rather than guessing which programmable devices work with which analog ICs, Altera and Maxim are working together to make this decision easy. Our companies have long been focused on efficiency and reducing system cost with one goal in mind: your success.

Over 13,000 customers count on Altera's renowned FPGAs, CPLDs, and ASICs. Maxim's highly integrated analog and mixed-signal semiconductors serve many of the same diverse customers while pushing the boundaries of innovation.

Whether you are designing the latest consumer electronics device or industrial/communications infrastructure equipment, we can meet your need for tens to millions of units. By taking the innovation beyond design into applications and supply chain, we can help you grow to the next level.

Speed is another key component of the Altera-Maxim partnership. We recognize you have stringent deadlines to meet, and we want you to exceed those deadlines. With distribution channels established around the globe, rapid deployment and delivery is assured. Our dedicated field applications engineers are ready to answer any question you present them. And they aren't satisfied until you're satisfied.

Take one step closer to success. Get your products to market faster and easier with support you can trust. Turn the page and find out how Altera and Maxim are building solutions today for tomorrow's integrated world.

Sincerely,

Vince Hu
Vice President,
Product Marketing, Corporate Marketing, and Technical Services
Altera

Introduction

Designing with Programmable Logic in an Analog World

Programmable logic devices (PLDs) revolutionized digital design over 25 years ago, promising designers a blank chip to design literally any function and to program in the field. PLDs can be low-logic density devices that use nonvolatile sea-of-gates cells called complex programmable logic devices (CPLDs) or they can be high-density devices based on SRAM look-up tables (LUTs) called field programmable gate arrays (FPGAs). In addition to implementing Boolean logic and registers in the configurable logic array, you can also use built-in features such as memory, clock management, I/O drivers, high-speed transceivers, Ethernet MACs, DSP building blocks, and embedded processors inside the FPGA.

Using programmable logic devices, data is input, processed, and manipulated, then output. However, this processing is generally limited to the digital domain while most of the signals in the real world are analog in nature (temperature, pressure, sound, vision, voltage, current, frequency, and others). Most data travel on wires or wireless media as analog signals that need to be converted into 0s and 1s for the FPGA to process (**Figure 1**). Making the analog world accessible to the digital world is where Maxim shines. As one of the top three players in nearly every analog function, Maxim has built a reputation for innovation and quality. With a focus on ease of use, our products simplify your system design, allowing you to focus on your unique algorithms.

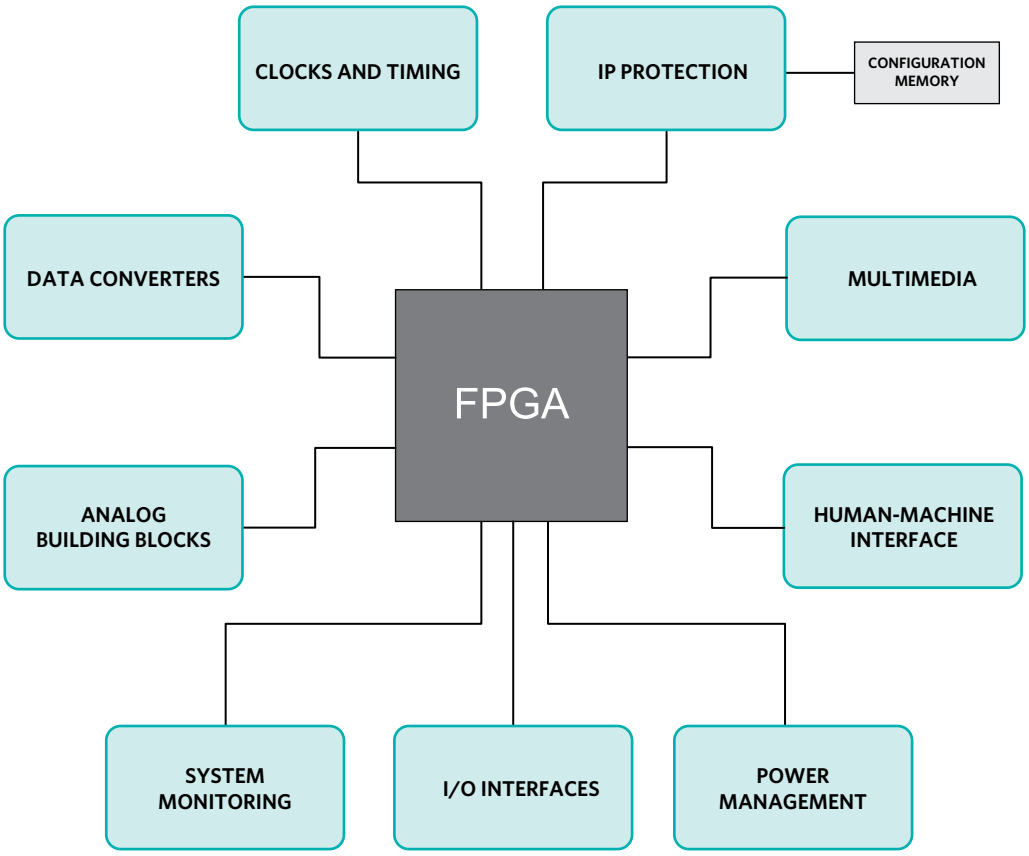


Figure 1. A Typical System Application Showing FPGA Working with Analog Functions

Power Management

FPGAs and CPLDs require anywhere from 3 to 15 or more voltage rails. The logic fabric is usually at the latest process technology node that determines the core supply voltage. Configuration, housekeeping circuitry, various I/Os, SerDes transceivers, clock managers, and other functions have differing requirements for voltage rails, sequencing/tracking, and voltage ripple limits. Learn the best ways to manage this complex challenge starting in the *Powering Altera FPGAs and CPLDs* section.

Data Converters

FPGAs in communications applications typically need high-speed data converters, while those in industrial and medical applications frequently require high precision and resolution. Maxim's data converter portfolio includes a wide variety of devices that serve these applications, including multi-GSPS high-performance and 16-bit to 24-bit precision ADCs and DACs. Turn to the *Signal Conversion Solutions for FPGAs* section for information about high-speed data converters.

IP Protection

While field programmability offers flexibility during the design process, it can also expose your underlying IP to the significant risks of reverse engineering and theft. Maxim provides 1-Wire® secure EEPROMs that use a single pin on the FPGA or CPLD to secure the design implemented. The secure memory uses a challenge-and-response authentication sequence to differentiate between authorized and counterfeit devices, thereby protecting the design investment from copying and cloning. Read about the benefits of our proprietary approach in the *Design Protection Solutions for FPGAs* section. Reference designs with FPGA logic are available.

Multimedia

FPGAs are increasingly used to process audio along with data. In most instances, these systems require audio/video data converters, amplifiers, filters, equalizers, signal conditioners, on-screen display blocks, video decoders, and audio codecs. Maxim offers multimedia subsystem ICs, allowing the FPGA designer to focus on the advanced audio/video processing stages of the design.

Human-Machine Interface

Most systems interact with their human operators and the real world. Maxim provides a wide variety of state-of-the art components to detect touch, temperature, proximity, light, and motion and convert these analog signals to the digital domain for processing within your FPGA. This includes devices suitable for high-volume consumer applications in addition to those built for the rugged industrial environments.

I/O Interfaces

While FPGAs include various I/O drivers such as LVTTL, LVCMOS, LVDS, HSTL/SSTL, and multigigabit serial transceivers, process limitations preclude them from driving the voltage or current levels required by many interface standards. RS-232, RS-485, CAN, IO-Link®, Ethernet, optical, and IrDA® are just a few common examples. Maxim's portfolio provides solutions to these interface problems. Many of these solutions include additional features for ESD and fault protection. In other cases, high-density interface ports like 24+ port SATA and SAS transceivers can be offloaded from the FPGA to a companion chip for optimizing costs.

We provide power-over-Ethernet ICs to power devices such as security cameras, IP phones, WiFi access points, and others through Ethernet. We can help you communicate over power lines using our powerline communication (PLC) ICs.

Building Blocks

Maxim provides building blocks such as level translators, MEMS-based real-time clocks, oscillators, amplifiers, comparators, multiplexers, signal conditioners, filters, potentiometers, ESD/fault protection, and other ICs to make your design robust and reliable.

System Monitoring

FPGAs are used in rack-mounted communications/computing infrastructure or sensitive industrial/medical and defense applications. For these applications, Maxim provides a full spectrum of solutions for enclosure management, thermal management, fan control, and hot-swap controllers, including fault detection/logging and security/authentication.

Powering Altera FPGAs and CPLDs

Overview

Today, programmable logic devices (PLDs) come in two flavors: field programmable gate arrays (FPGAs) and complex programmable logic devices (CPLDs). Both types of PLDs offer immense flexibility, allowing you to implement any digital algorithm, which contributes to their broad industry adoption. While Altera's FPGAs that are based on SRAM technology offer higher logic density and consume higher power, Altera's CPLDs offer lower logic density and consume lower power. Altera also provides HardCopy® ASICs that are a hard ASIC copy of their Stratix® series FPGAs. These devices are similar to Stratix FPGAs, but do not need external configuration memory and associated power supplies. PLD vendors use the latest process technology node in every generation of devices to increase the logic density and integrate more features. Examples include adaptive logic modules, embedded memory blocks, clock managers, DSP functions, Ethernet MACs, PCI Express® controllers, multigigabit transceivers, I/O drivers, and even ARM® processors.

The integration of disparate functions and regular technology node migration results in several power supply rails for a PLD. The benefits of integration and ease of use are questionable if you cannot power these programmable devices in an easy and cost-effective manner. Most digital designers either underestimate the power supply needs of a PLD or are overwhelmed by it. Maxim can help you achieve first-time success with your FPGA power design and meet your time-to-market objectives by following simple guidelines discussed in this chapter.

Power Requirements of PLDs

As PLDs assume the role of a System-on-Chip (SoC) on your board, powering these devices is comparable to powering an entire system. Power is a key topic for PLD vendors. Altera has taken steps to mitigate static power and dynamic power with programmable power architecture in their devices. Still, a typical high-end Stratix series FPGA easily has 10 to 15 unique rails. On the other hand, devices from lower density Arria®, Cyclone®, and MAX® series can have 1 to 10 rails

Table 1. Altera V Series FPGAs, CPLDs, HardCopy ASICs, and SoC FPGAs Power-Supply Requirements

Power Rail	Nominal Voltage (V)	Description
V_{CC}	0.85	Core voltage and peripheral circuitry power supply
V_{CCPT}	1.5	Power supply for programmable power technology
V_{CCAUX}	2.5	Auxiliary supply for programmable power technology; not applicable to HardCopy ASICs
V_{CCPD}	3.0	I/O predriver (3.0V) power supply
	2.5	I/O predriver (2.5V) power supply
V_{CCIO}	3.0	I/O buffers (3.0V) power supply
	2.5	I/O buffers (2.5V) power supply
	1.8	I/O buffers (1.8V) power supply
	1.5	I/O buffers (1.5V) power supply
	1.35	I/O buffers (1.35V) power supply
	1.25	I/O buffers (1.25V) power supply
	1.2	I/O buffers (1.2V) power supply
V_{CCPGM}	3.0	Configuration pins (3.0V) power supply
	2.5	Configuration pins (2.5V) power supply
	1.8	Configuration pins (1.8V) power supply
V_{CCA_FPLL}	2.5	PLL analog voltage-regulator power supply
V_{CCD_FPLL}	1.5	PLL digital voltage-regulator power supply
V_{CCBAT}	—	Battery backup power supply (for design security volatile key register; not applicable to HardCopy ASICs)
Transceiver Power-Supply Rails		
V_{CCA_GXBL}	3.0	Transceiver high-voltage power (left side)
V_{CCA_GXBR}	2.5	Transceiver high-voltage power (right side)
V_{CCHIP_L}	0.85	Transceiver HIP digital power (left side)
V_{CCHIP_R}		Transceiver HIP digital power (right side)
V_{CCHSSI_L}	0.85	Transceiver PCS power (left side)
V_{CCHSSI_R}		Transceiver PCS power (right side)
V_{CCR_GXBL}	0.85	Receiver power (left side)
V_{CCR_GXBR}	1.0	Receiver power (right side)
V_{CCT_GXBL}	0.85	Transmitter power (left side)
V_{CCT_GXBR}	1.0	Transmitter power (right side)
V_{CCH_GXBL}	1.5	Transmitter output buffer power (left side)
V_{CCH_GXBR}		Transmitter output buffer power (right side)

Note: *Taken from the Altera Stratix data sheet (December 2011).*

depending on your application. You need to pick the right set of power regulators based on the overall power level of each of the rails, their sequencing, and their system power management needs. As process technology nodes become smaller in FPGAs, there is a need for tighter tolerances on the voltage supply rails. Maxim provides 1% regulation accuracy across line/load and PVT variations.

Understanding FPGA Power Rails

Modern PLDs have a core supply rail that powers most of the device and consumes the highest power. With every new technology node, there is a new core supply voltage rail. Auxiliary voltage supply rails power supporting circuits on a PLD such as configuration logic, clock managers, and other housekeeping circuits. In addition, FPGAs are typically used to bridge one interface standard to another, and each I/O driver has its unique voltage rail ranging from 1.2V to 3.3V. Examples include LVTTL/LVCMOS, LVDS, bus LVDS, mini LVDS, HSTL, SSTL, and TMDS, among others.

Special care is needed for powering high-speed SerDes transceivers, each of which can consume 1 to several amperes of current and run at speeds of 155Mbps to 28Gbps and beyond. For example, a 100G Ethernet application uses many such transceivers and consumes 10A or more of current. Because of the high speeds involved, a noisy power rail is particularly detrimental to their performance.

Figure 2 illustrates a typical Stratix series FPGA used in a communications application, an Arria series FPGA used in an industrial application, and a Cyclone series FPGA used in a consumer application.

Consider the latest FPGAs from Altera as an example to understand the power needs better. **Table 1** provides a summary of the key voltage rails in the Altera V series FPGAs inclusive of Stratix V, Arria V, Cyclone V, SoC FPGAs, and HardCopy V. While this table shows the latest FPGAs, the power-supply requirements of previous generation FPGAs are quite similar. Altera states that power-supply ramps must all be strictly monotonic and provides power-supply ramp times for various devices.

For most applications, it is impractical to have a separate power supply for each voltage rail. Altera thus provides power-supply sharing guidelines where the same supply can be used to power multiple rails that can share the same voltage. Refer to the relevant Altera data sheet for more information.

Power Architectures

The power architecture that supports a PLD is influenced by the intended application: communications and computing, industrial or automotive,or handheld consumer. Most high-performance/high-power FPGA applications in communications and computing infrastructure applications are built on line cards that are powered by a 48V or 72V backplane in a rack-mounted system. A two-stage intermediate bus architecture (IBA) is typically used in these applications for the individual cards (**Figure 2A**). The first stage is a step-down converter that converts the 48V or 72V to an isolated intermediate voltage such as 12V or 5V. The plug-in cards are often isolated from each other for safety reasons and to eliminate the possibility of current loops and interference between the cards. The second stage of the IBA is to convert the intermediate voltage to multiple lower DC voltages, using nonisolated regulators that are in close proximity to the FPGA and often called point-of-load (POL) regulators. Multiple-output POLs are called PMICs.

FPGAs used in industrial and automotive applications are typically powered by an isolated AC-DC or DC-DC supply followed by a 24V supply that is nonisolated (**Figure 2B**). POL regulators located next to the FPGA generate the specific voltages required by the FPGA.

Consumer and handheld equipment run on 3.6V to 12V batteries. The specific voltages required by an FPGA in such an application can be generated by POLs directly from the battery voltage (**Figure 2C**).

Maxim provides power solutions for every stage of these three architectures:

- Front-end isolated AC-DC and DC-DC power regulators from 5W to hundreds of watts of power with high efficiencies
- 4.5V to 60V (24V nominal) nonisolated DC-DC buck regulators often used in industrial and building automation applications where FPGAs are common
- Primary stage controllers supporting up to 300A
- Secondary stage single- and multirail POL regulators to power FPGAs and CPLDs

System Considerations

System-level design considerations influence the choice of power architecture. Simpler power system designs can use single- and multirail regulators that take a 5V/12V input and supply power to all FPGA rails with built-in sequencing and minimal external components. Ease of use is paramount in such applications. Features that simplify these power designs include internal MOSFETs, internal compensation, digital programmability, and even internal inductors.

Infrastructure equipment uses FPGAs, DSPs, ASICs, and peripherals on the board that are powered by numerous POL regulators controlled by a master controller. PMBus™ protocol or I²C-/SPI-based control with a microcontroller is often used in these applications. It might be necessary to control both the power of the FPGAs on the board and also several other devices along with dynamic power management and monitoring. Also, it is suggested to turn on/off some ICs based on trigger events. Maxim provides advanced system power management ICs (i.e., the MAX34440 and MAX34441) to control multiple POL regulators and fans, enabling dynamic power regulation (hibernate, standby, etc.) and superior monitoring and fault logging.

Applications that run on batteries take advantage of Altera's FPGAs' power saving modes to keep the FPGA circuits in hibernate modes most of the time, except when crunching algorithms. The regulators that power the FPGAs can also save energy and improve efficiency by employing techniques such as pulse-skipping. Many Maxim regulators use such technologies to provide light-load operation mode and control.

Power Regulation Primer

DC-DC power regulators come in two major categories: low dropout (LDO) regulators and switching-mode power supply (SMPS) regulators. LDOs convert the V_{IN} to V_{OUT} at the required current and dissipate the power difference as heat. In most cases, this makes LDOs inefficient for power levels exceeding 100mW. Yet, LDOs are very easy to design and use.

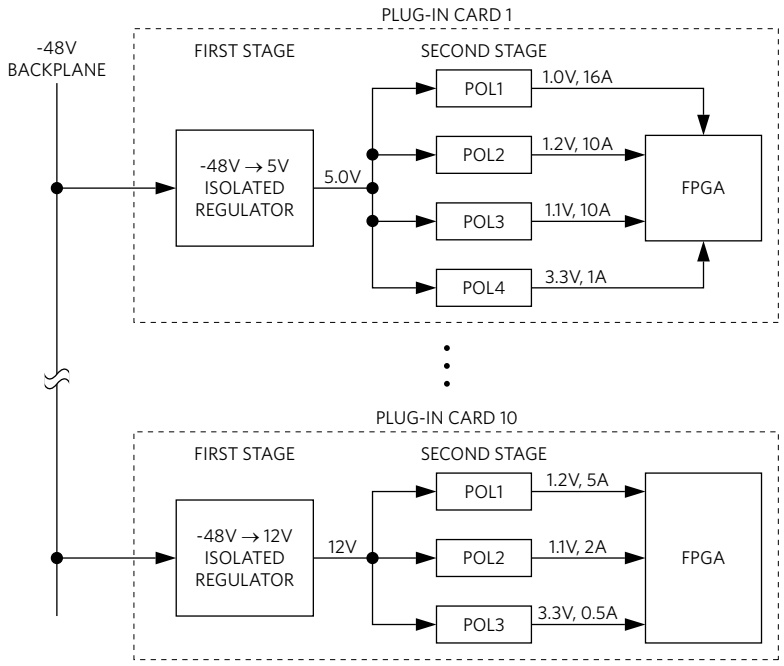
SMPS regulators use a pulse-width modulation (PWM) controller with MOSFETs (internal or external) acting as switches and an inductor acting as an energy storage device. By controlling the duty cycle, an SMPS regulator manages the energy in the inductor, thereby regulating the output voltage despite line and load variations. Efficiencies as high as 90% to 95% are realized, unlike with LDO regulators.

The Four Ps of Power

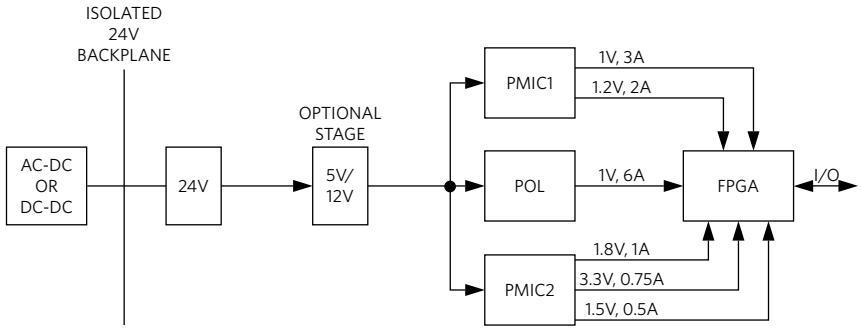
The four Ps of power are: products, process, packaging, and price.

Process technology is a key part of power-supply choice. The process used to develop power regulators determines the performance of the MOSFETs used, and thereby, the efficiency and die area. A MOSFET with low R_{DSON} (drain-source on-resistance) is more efficient dissipating lower power without occupying a larger die area. Similarly, smaller geometries aid in the integration of digital logic, such as sequencing and PMBus control, with power regulators. A careful balance of process technology and cost is required to meet FPGA power requirements. Typically, the top three

A) POWERING A STRATIX SERIES FPGA IN A COMMUNICATIONS APPLICATION



B) POWERING AN ARRIA SERIES FPGA IN AN INDUSTRIAL APPLICATION



C) POWERING A CYCLONE SERIES FPGA OR A MAX SERIES CPLD IN A CONSUMER APPLICATION

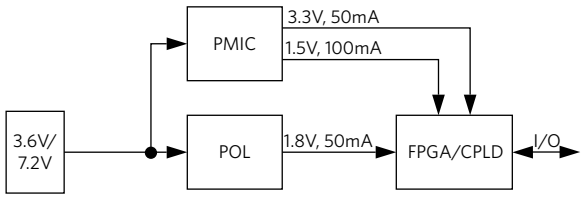


Figure 2. Typical FPGA Power Architecture Used in Communications, Industrial, and Consumer Applications

suppliers have these process capabilities, unlike vendors who cut corners to sell cheap regulators.

Due to the amount of power required from the regulators by the FPGAs, the regulators' ability to manage the heat generated is critical. A superior power regulator can regulate properly over temperature and uses industry-leading packages such as a QFN with an exposed pad.

Price of the regulator is usually a critical factor. The number of regulators used on a board can easily multiply. Therefore, the cost of additional features must be carefully weighed against the benefit provided.

Advanced Features

Power regulators provide several advanced features beyond the input/output voltages and currents. Depending on your application, a feature can be critical for success or completely unnecessary. It is important to understand the types of features available in today's regulators.

Startup Sequencing/Tracking

Three or more voltage rails are typically required to power an FPGA and need sequencing for power-up and power-down. Sequencing limits the inrush current during power-up. If the sequencing is ignored, the devices that require sequencing can be damaged or can latchup. This can cause your FPGA device to malfunction. There are three types of sequencing: coincident tracking, sequential tracking, and ratiometric tracking. An example of sequential tracking is shown in **Figure 3**.

Sequencing and tracking capabilities are integrated into many of Maxim's multi-output power regulators. Stand-alone ICs that perform sequencing and tracking are also available.

Monotonic Startup Voltage Ramp

It is important for the ramping voltage rails to rise monotonically at startup to achieve successful power-up. Altera recommends a strict monotonic voltage ramp, meaning that the rails should rise continuously to their setpoint and not droop. Drooping could result if the POL does not have enough output capacitance (**Figure 4**).

Soft-Start

Altera specifies minimum and maximum startup ramp rates. Power-supply regulators implement soft-start by gradually increasing the current limit at startup. This slows the rate of rise of the voltage rail and reduces the peak inrush current to the FPGA. Maxim's POLs allow soft-start times to be programmed based on the value of a soft-start capacitor connected to one of the POL pins.

Power-Supply Transient Response

FPGAs can implement many functions at different frequencies due to their multiple clock domains. This can result in large step changes in current requirements. Transient response refers to a power supply's ability to respond to abrupt changes in load current. A regulator should respond without significantly overshooting or undershooting its setpoint and without sustained ringing or ripple in the output voltage.

Synchronizing to an External Clock

FPGAs are used in applications that need power regulators to synchronize with common clocks to streamline communication between the system controller and the power supplies. Many POLs provide an external SYNC pin to allow the system designer to synchronize one or multiple regulators to a common system clock.

Multirail Regulators and Multiphase Operation

FPGAs need multiple regulators for regulating all the supply rails. Quite often dual/triple/quad regulators are used for optimal layout. Multirail regulators can often be used in a multiphase configuration operating in parallel to increase the current capability. Their switching frequencies are synchronized and phase shifted by 360/n degrees, where n identifies each phase. Multiphase operation yields lower input ripple current, reduced output ripple voltage, and better thermal management. They are best for V_{CC} and transceiver power rails.

Remote Sensing

There can be a significant voltage drop on a PCB between the power-supply output and the FPGA power-supply pins. This occurs particularly in applications where the load current is high and it is not possible to place the regulator circuit close enough to the FPGA power pins. Remote sensing resolves this issue by using a dedicated pair of traces to accurately measure the voltage at the FPGA's power-supply pins (**Figure 5**) and compensating for the drop. Remote

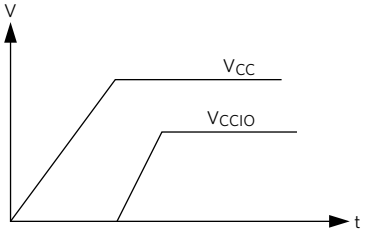


Figure 3. Sequential Tracking

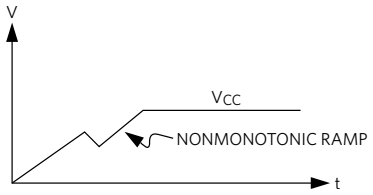


Figure 4. Nonmonotonic Startup Voltage Ramp

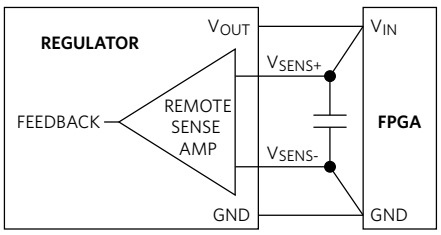


Figure 5. Remote Sensing

sensing is also recommended for voltage rails with very tight tolerances (≤ 3%).

Programming Options

Power regulators can include one or several programming options such as output voltage, switching frequency, and slew rate. A traditional approach is to provide this capability through I/O pins on the regulator that can be tied to a specific resistance value. Depending on the resistance, an appropriate programming option is chosen. This can quickly become complicated and unwieldy depending on the number of programming options. Increasingly, many power regulators provide an I²C or SPI interface to digitally program the options with a tiny register set. Quite often, these options can be changed in the field by a system microcontroller as required.

Choosing Power Regulators

Most power-supply vendors complicate choosing power supply regulators for FPGAs by providing too many tools and web interfaces just to pick a part. Not Maxim. Our goal is to provide you with the right information to evaluate and choose the power supply you need in a few simple steps.

Estimating Your FPGA's Power Needs

First, determine the input voltage. Second, identify the supply rails and load currents needed by the FPGA for your application. And third, use our product selector guide to pick the appropriate part (**Figure 6**).

Once you have determined the input voltage, use Altera's PowerPlay estimator spreadsheets (www.altera.com/power) to get a list of all power supply rails and a rough estimate of the current consumption for each (**Figure 7**).

Maxim recommends that you extract the voltages and currents into a table and determine your power architecture. Every time you add an intermediate regulator, you might be sacrificing system-level power efficiency. This is because you get less than 100% efficiency at each stage. Going from the main system input voltage to all the FPGA rails is an ideal method except when the efficiency loss is so high with one stage (typically when either V_{IN}/V_{OUT} voltage change is high or currents handled are in excess of 50A) that you are better off dividing it into multiple stages. Identify the power requirements of other external components such as memories, processors, data converters, and I/O drivers to determine whether you can regulate them together with the FPGA rails based on total current. Also, note any special sequencing, ramp-up, soft-start, and other requirements. Finally, evaluate cost, efficiency, and size targets. A checklist is provided in **Table 2** to help you.

Which Features Do You Need?

Using Table 2, you should have a thorough understanding of your FPGA's power budget, its supply rails, and other system-level considerations. Let us examine the must-have power regulator features for every FPGA designer, the application-specific optional features, and preferences.

Necessities

Every FPGA design needs power regulators with the ability to select the output voltage, as well as sequencing, adjustable soft-start, monotonic ramp-up, and a good transient response.

User Preferences

Most users have preferences for their power-supply design. On the one hand, some customers want to buy a PWM controller and use external MOSFETs, external compensation, and an external system control. On the other hand, some customers prefer a fully integrated controller and MOSFETs as well as built-in internal compensation, digital programmability, and system control. Maxim provides parts for the entire spectrum of customer choice. Keeping the digital designer in mind, we are developing a family of parts with GUI-based programming facilitated by I²C.

Optional Features

Depending on your application, you might need advanced system control using PMBus or other means. You might need multiphase operation to handle high currents, remote sensing capability, synchronization to an external clock, and power monitoring functions. Or you might need to control the slew rate to mitigate voltage ripple on SerDes channels in high-speed transceiver applications.

Digital Power Control

A new trend in the industry is the use of digital control loop regulators for enhanced automatic compensation to simplify design and reduce cost. Most digital power solutions today use proportional-integral-derivative (PID) controllers, but performance is compromised because of the windowed ADCs used. Maxim's InTune™ digital-control power products are based on state-space or model-predictive control, rather than the PID control used by competitors. The result is a faster transient response. Unlike competing PID controllers, the InTune architecture uses a feedback ADC that digitizes the full output voltage range. Its automatic compensation routine is based on

CHOOSING YOUR FPGA POWER REGULATORS	
1	• USE THE FPGA VENDOR POWER ESTIMATION SPREADSHEET. • IDENTIFY ALL THE REQUIRED VOLTAGE RAILS AND CURRENTS.
2	• USE THE MAXIM POWER REGULATOR CHECKLIST. • IDENTIFY/DECIDE: V_{IN}, V_{OUT}, I_{OUT}, SEQUENCE, I²C/PMBus, PROGRAMMABILITY, SPECIAL NEEDS.
3	• USE THE MAXIM PRODUCT SELECTOR TO CHOOSE PARTS.

Figure 6. Choosing Your FPGA Power Regulators

Table 2. FPGA Power Supply Checklist

Checklist Item	Answer
Basic Requirements	
Identify input voltage rail (e.g., V_{IN} = 5V)	
List all FPGA voltage rails and the current required for each (e.g., V_{CC} = 0.85V at 5A, V_{CCIO} = 1.5V at 2A)	
Sequencing requirements and order (timing diagram), power-on/-off, under fault recovery	
Switching frequency desired	
Soft-start ramp rate (e.g., 5ms)	
Single-/multirail regulators required?	
Internal compensation required?	
Configuration: I^2C or use resistor values?	
Advanced Features and Requirements	
Output voltage ripple targets (mV) for transceivers	
Sink current capability (for DDR)	
Synchronize to external clock?	
Power-up in prebiased load?	
PMBus control or I^2C/SPI required?	
Protection features	
Remote sensing capability needed?	

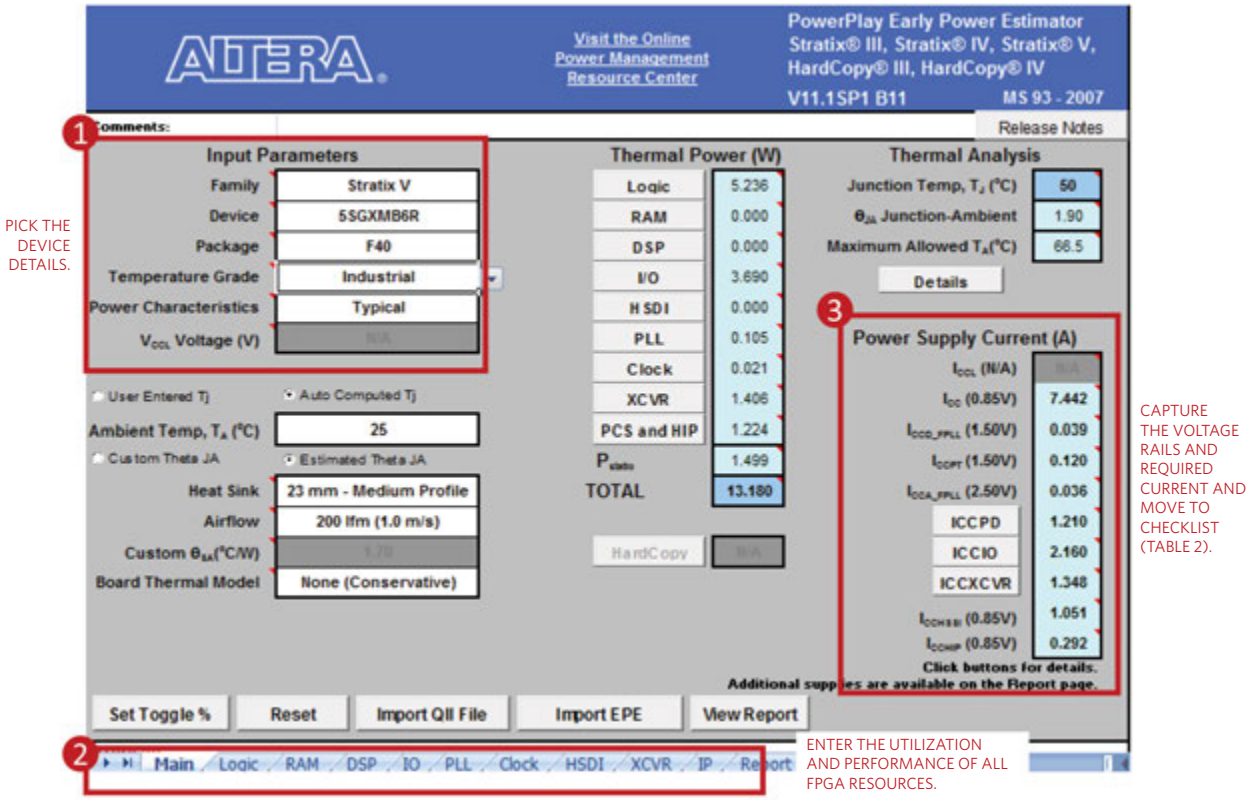


Figure 7. Altera Power Estimator Tool

measured parameters, providing better accuracy, and thus better efficiency.

Design and Simulate the Power Supply

While many power regulators come with built-in compensation, you still need to choose the right inductor value for your unique output current requirement. If the regulator needs external compensation, you need to select the right RC values to compensate for your output voltage in the control loop. Maxim provides a web-based design and simulation tool for power supplies called EE-Sim® (www.maximintegrated.com/eesim). It asks for your design requirements and outputs a complete schematic and bill of materials. You can make changes to the component values on the schematic to fine-tune your power design.

EE-Sim also provides rapid simulation of your power regulator design. Unlike SPICE models that take a long time to converge, making it frustrating to design, EE-Sim relies on advanced SIMPLIS models with a simple web interface that is quick and easy. An EE-Sim example is shown in **Figure 8**, which recommends external component values as well as Bode plots to identify phase margin and efficiency plots. If you want to download the simulation model for additional analysis offline, a free version of EE-Sim is available.

Addressing Your Requirements: Cost, Size, Efficiency, and Ease of Use

In addition to voltages, currents, and features, you will most likely choose your power supply based on few key metrics: cost, size, efficiency, and ease of use. Let us consider both the IC cost and the total solution cost. A good FPGA power regulator should integrate into the IC the necessary features previously discussed. This reduces the overall solution cost and size.

Efficiency is a function of the power architecture of the primary and secondary stage regulators as well as a function of the performance of each individual regulator. Maxim's power regulators are acclaimed as the most efficient for a given power level. Plus, we offer 1% regulation accuracy over PVT, an accuracy that very few vendors can match.

Finally, there is ease of use. Maxim's FPGA power regulators are user-friendly and becoming even easier to use. Almost all our FPGA power regulators have internal MOSFETs. Several have internal compensation circuits for common output voltages. Our thermally efficient QFN and CSP packages simplify PCB design. With GUI-based programming, choosing the power regulator options is as easy as choosing the FPGA programming options in Quartus® II.

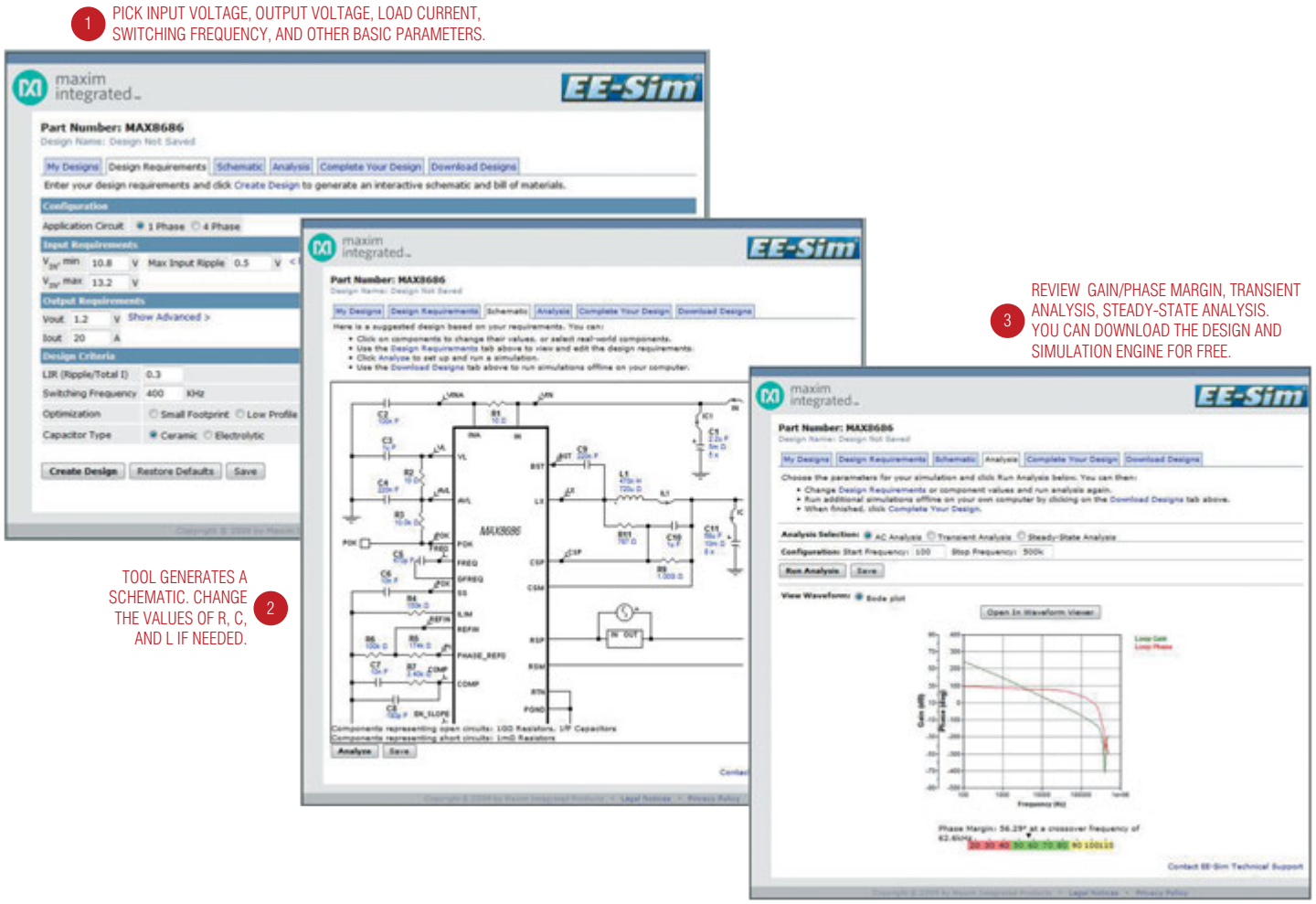


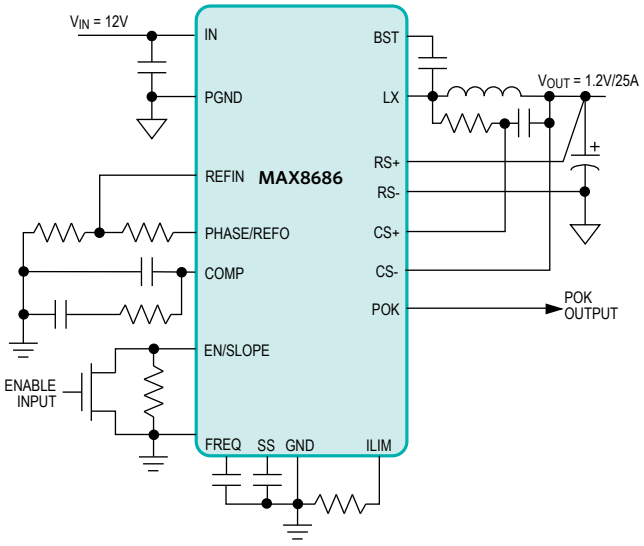
Figure 8. EE-Sim Simulation Tool (MAX8686)

Featured Products

Highly Integrated Step-Down DC-DC Regulator Provides Up to 25A for High Logic Density FPGAs

MAX8686

The MAX8686 current-mode, synchronous PWM step-down regulator with integrated MOSFETs provides the designer with a high-density, flexible solution for a wide range of input voltage and load current requirements. This device combines the benefits of high integration with a thermally efficient TQFN package.



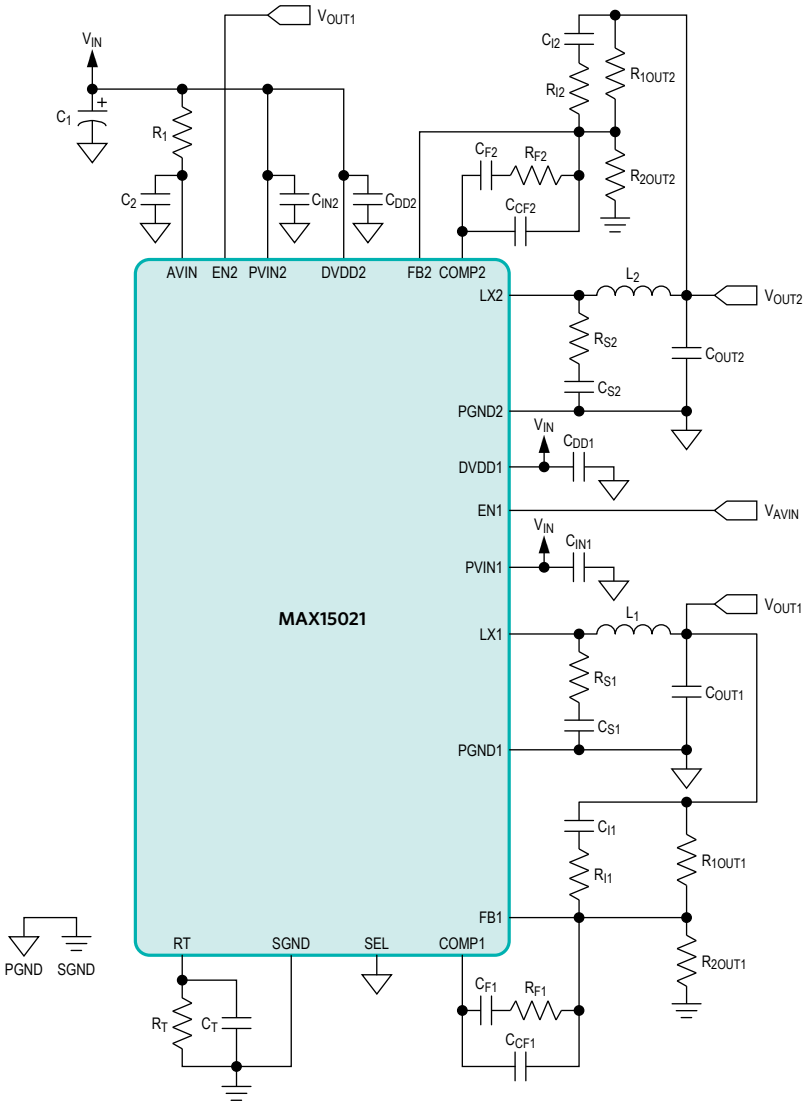
Benefits

- Enough margin to safely power FPGAs from popular 5V/12V inputs
  - Wide 4.5V to 20V input voltage range
  - Adjustable output from 0.7V to 5.5V
  - 25A output capability per phase
  - 300kHz to 1MHz switching frequency
- Enable high voltage regulation accuracy for FPGAs with low core voltages
  - 1% accurate internal reference
  - Differential remote sense
- Designed to simplify powering FPGAs/CPLDs
  - Monotonic startup (prebias)
  - Adjustable soft-start to reduce inrush current
  - Output sink and source current capability
  - Reference input for output tracking
- Integrated protection features enable robust design
  - Thermal overload protection
  - Undervoltage lockout (UVLO)
  - Output overvoltage protection
  - Adjustable current limit supports a wide range of load conditions
- 6mm x 6mm, TQFN-EP package reduces board size

Dual, 4MHz Internal FET Step-Down DC-DC Regulator Reduces Size and Cost

MAX15021

The MAX15021 dual output, synchronous PWM step-down regulator with integrated MOSFETs provides the designer with a high-density solution that maximizes board space and reduces the overall solution cost.



Benefits

- Designed to simplify powering FPGAs/CPLDs
  - Monotonic startup (prebias)
  - Internal digital soft-start to reduce inrush current
  - Sequencing and coincidental/ratiometric tracking
- Reduces solution size
  - Fast 4MHz switching minimizes inductor size
  - 180° out-of-phase switching reduces input ripple current
  - Lead-free, 28-pin, 5mm x 5mm TQFN-EP package
- Flexible and adjustable voltage and power ranges ensure compatibility with a variety of FPGAs
  - Allows easy reuse among multiple FPGA designs
  - Reduces total design time and inventory holding costs
  - 2.5V to 5.5V input voltage range
  - 0.6V to 5.5V adjustable output
  - Output current capabilities of 4A (reg. 1) and 2A (reg. 2)
  - 500kHz to 4MHz switching frequency
- Operates over the -40°C to +125°C temperature range

Example Designs for Altera FPGAs

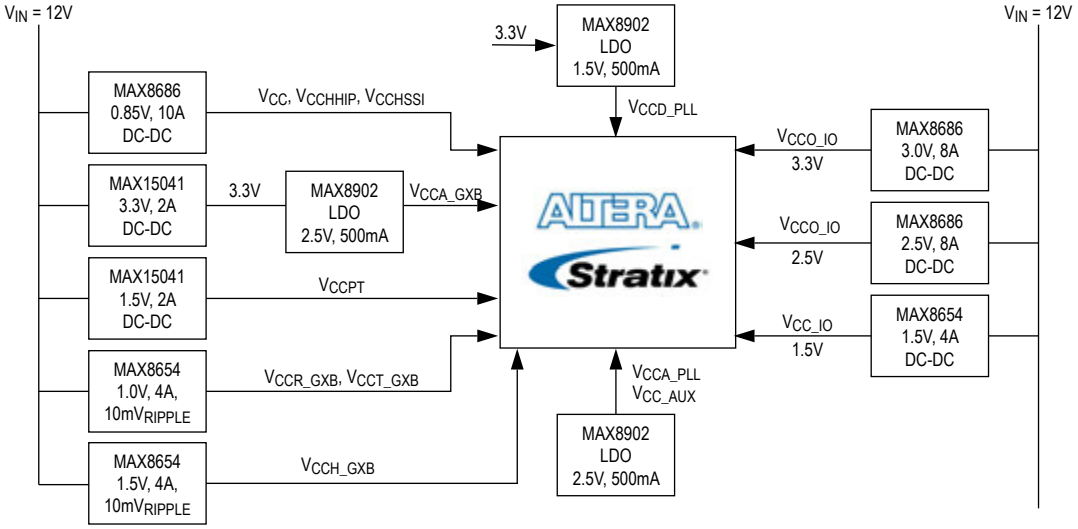


Figure 9. Stratix V FPGA Power Architecture Example

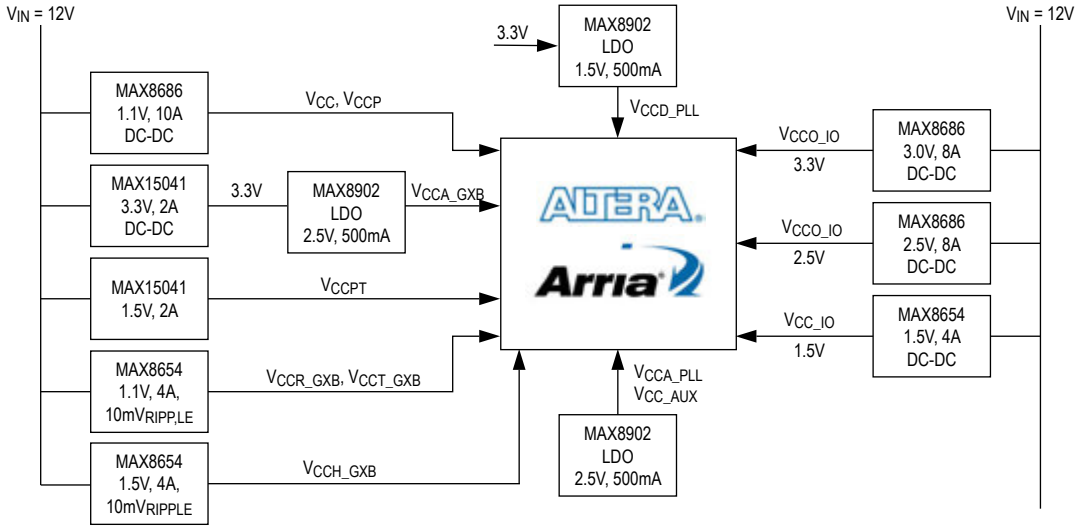


Figure 10. Arria V FPGA Power Architecture Example

Example Designs for Altera FPGAs (continued)

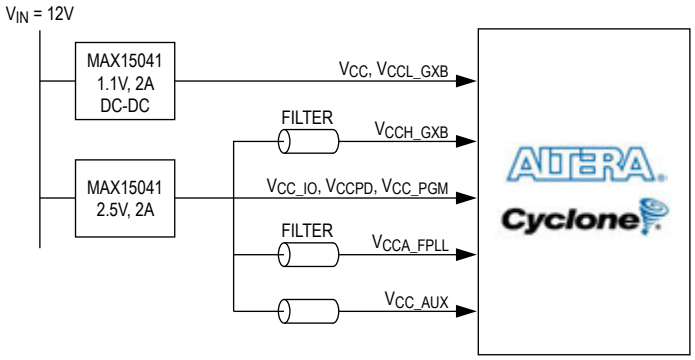


Figure 11. Cyclone V FPGA Power Architecture Example

Selector Guide and Tables

Core Power Regulator, V_{CC} (0.85V to 1.2V Depending on FPGA/CPLD Generation)

Input Voltage (V)	≤ 500mA	≤ 1A to 1.8A	≤ 2A to 5A	≤ 5A to 10A	≤ 30A
1.8	MAX8902 LDO	MAX8516 LDO MAX8517 LDO MAX8518 LDO MAX8526 LDO MAX8527 LDO MAX8528 LDO MAX8794 LDO	MAX8526 LDO MAX8527 LDO MAX8528 LDO MAX8556 LDO MAX8557 LDO MAX8643 Buck	MAX8566 Buck MAX8646 Buck MAX1956 Controller	MAX1956 Controller
2.7 to 5.5	MAX8902 LDO MAX1983 LDO MAX8649 Buck	MAX8516 LDO MAX8517 LDO MAX8518 LDO MAX8649 Buck	MAX8526 LDO MAX8527 LDO MAX8528 LDO MAX15053 Buck MAX8643 Buck MAX15038 Buck MAX15050 Buck MAX15051 Buck MAX17083 Buck	MAX15039 Buck MAX15112 Buck MAX15108 Buck	MAX15118 Buck
4.5 to 14	MAX15036 Buck MAX15037 Buck	MAX15036 Buck MAX15037 Buck	MAX15036 Buck MAX15037 Buck MAX15066 Buck MAX8654 Buck	MAX8654 Buck MAX8686 Buck MAX8598 Controller MAX8599 Controller MAX15026 Controller	MAX8686 Buck MAX8597 Controller MAX8598 Controller MAX8599 Controller MAX15026 Controller
4.5 to 24	MAX15006 LDO MAX15007 LDO MAX17501 Buck MAX15041 Buck MAX1776 Buck	MAX17502 Buck MAX15041 Buck MAX8792 Controller	MAX8792 Controller MAX15041 Buck MAX15026 Controller	MAX8792 Controller MAX15026 Controller	MAX8597 Controller MAX8598 Controller MAX8599 Controller MAX15035 Buck MAX15026 Controller
4.5 to 28	MAX15041 Buck	MAX15041 Buck	MAX15041 Buck MAX15026 Controller MAX15046A/ MAX15046B Controller	MAX15026 Controller MAX15046A/ MAX15046B Controller	MAX8597 Controller MAX8598 Controller MAX8599 Controller MAX15026 Controller MAX15046A/ MAX15046B Controller

Auxiliary, I/O, and SerDes Power Regulators (1.2V, 1.5V, 1.8V, 2.5V, 3.3V)

Input Voltage (V)	≤ 500mA	≤ 1A to 1.8A	≤ 2A to 5A	≤ 5A to 10A	≤ 30A
1.8	MAX8902 LDO	MAX8516 LDO MAX8517 LDO MAX8518 LDO MAX8526 LDO MAX8527 LDO MAX8528 LDO MAX8794 LDO	MAX8556 LDO MAX8557 LDO MAX8794 LDO	MAX17016 Buck MAX15108 Buck MAX1956 Controller MAX8792 Controller	MAX1956 Controller MAX8792 Controller

(Continued on following page)

Auxiliary, I/O, and MGT Power Regulators (1.2V, 1.5V, 1.8V, 2.5V, 3.3V) (continued)

Input Voltage (V)	≤ 500mA	≤ 1A to 1.8A	≤ 2A to 5A	≤ 5A to 10A	≤ 30A
2.7 to 5.5	MAX8902 LDO	MAX15053 Buck MAX15038 Buck	MAX15038 Buck MAX15039 Buck MAX15050 Buck MAX17083 Buck MAX15026 Controller MAX1956 Controller	MAX15039 Buck MAX8654 Buck MAX15108 Buck MAX17016 Buck MAX1956 Controller MAX8792 Controller	MAX15118 Buck MAX15112 Buck MAX17016 Buck MAX1956 Controller MAX15026 Controller MAX8792 Controller MAX8598 Controller MAX8599 Controller
4.5 to 14	MAX8902 LDO MAX1776 Buck	MAX15041 Buck	MAX15041 Buck MAX15036 Buck MAX15037 Buck MAX8654 Buck MAX5089 Buck MAX15026 Controller	MAX15035 Buck MAX8654 Buck MAX17016 Buck MAX8792 Controller MAX15026 Controller	MAX8655 Buck MAX17016 Buck MAX15035 Buck MAX8792 Controller MAX15026 Controller MAX8598 Controller MAX8599 Controller

Multiple Output Power Regulators

Input Voltage (V)	Quad Regulators	≤ 2A to 3A per Output	≤ 5A per Output	≤ 15A per Output	25A per Output
1.8	—	MAX8833 Dual Buck	MAX8833 Dual Buck MAX8855 Dual Buck	—	—
2.7 to 5.5	—	MAX15021 Dual Buck MAX15022 Dual Buck	—	—	—
4.5 to 14	MAX17017 1 Controller, 2 Bucks, 1 LDO MAX17019 1 Controller, 2 Bucks, 1 LDO	—	MAX15002 Dual Controller MAX15048 Triple Controller MAX15049 Triple Controller	MAX15002 Dual Controller MAX15048 Triple Controller MAX15049 Triple Controller	MAX15002 Dual Controller
4.5 to 28	MAX17017 1 Controller, 2 Bucks, 1 LDO MAX17019 1 Controller, 2 Bucks, 1 LDO	MAX15002 Dual Controller MAX15023 Dual Controller MAX17007B Dual Controller MAX15048 Triple Controller MAX15049 Triple Controller	MAX15002 Dual Controller MAX15023 Dual Controller MAX17007B Dual Controller MAX15048 Triple Controller MAX15049 Triple Controller	MAX15002 Dual Controller MAX15023 Dual Controller MAX17007B Dual Controller MAX15048 Triple Controller MAX15049 Triple Controller	MAX15002 Dual Controller MAX15023 Dual Controller MAX15034 Dual Controller MAX17007B Dual Controller

Note: *Some applications can require forced air cooling to achieve full output current. Voltage ranges can vary slightly. Refer to the data sheet for the specific voltage range for each part. Minimum V_{OUT} is 1.25V for the MAX1776.*

Specialty Parts

- MAX1510 DDR termination power regulator that can sink current
- MAX34440 multirail PMBus controller used to control many regulators, fans, and log faults
- Maxim also provides the entire range of supporting power functions such as isolated power regulators, sequencers, supervisors, temperature monitors, and PMBus system monitors

Signal Conversion Solutions for FPGAs

Overview

We live in an analog world. Human sight, hearing, smell, taste, and touch are analog senses. And since real-world signals are analog, they need to be converted into the digital domain by ADCs before they can be processed by an FPGA. After digital processing is completed, digital signals often need to be converted back to the analog domain by DACs. But the analog story does not begin or end with data conversion. Op amps, instrumentation amplifiers (IAs), and programmable gain amplifiers (PGAs) come into play to preprocess analog signals for the ADCs and postprocess analog signals after the DACs.

Maxim makes highly integrated analog and mixed-signal interface semiconductors that serve as the analog interfaces required by FPGAs to make practical systems. Our precision SAR and delta-sigma ADCs and DACs combine with low-power, high-performance, space-efficient op amps, comparators, and precision references to deliver the ever-increasing accuracy and speed needed for your next design.

Signal Conversion and FPGAS Working Together

Using FPGAs in control circuits is common to many applications, including medical, automotive, and consumer electronics. The signal-chain block diagram in **Figure12** shows a generic control system. We sense a parameter, make decisions in the FPGA, and act to produce a physical action.

Different parameters are measured as shown in **Table 3** and processed in the FPGA. Then the system interacts with the environment by the controlling devices shown in **Table 4**. Although the parameters measured and controlled can differ, Figure 12 represents a typical system.

A Practical Signal Chain

The analog input portion of the circuit accepts analog signals from a variety of sensors through factory or field wiring. These sensors are used to convert physical phenomena as shown in Table 3 into electrical representations. Many sensors do not create their own signals, but require an external source for excitation. Once excited, they generate the signal of interest.

The signal chain in Figure 12 starts on the left side with a signal from a sensor entering the analog signal conditioning block. Before the signal is ready to be sampled by the ADC, its gain needs to be matched to the ADC's input requirements.

An analog input module receives many different signals in a tough industrial environment. It is, therefore, essential to filter out as much noise as possible while retaining the signal of interest before converting the signal from the analog-to-digital domain.

Various implementations of the signal chain are possible:

- A mux at the first stage followed by a common amplifying signal path into an ADC
- Individual amplifying channels and a mux prior to the ADC
- With simultaneous-sampling ADCs and independent conditioning amplifiers

The input stage is commonly required to cope with both positive and negative high voltages (e.g., ±30V or higher) to protect the analog input from external fault conditions. For example, sensors can be remotely located from the analog input with large amounts of common-mode voltage that must be rejected. Amplifiers are often used to help condition the signals before processing.

Operational amplifiers (op amps) are an important part of the analog signal-conditioning block. They are used as analog-front-ends (AFEs) to control gain, offset, and anti-alias filtering prior to ADCs. Op amps offer high-voltage protection or current-to-voltage conversion. Depending on the application, some parameters can be more important than others. DC applications require precision with low input offset voltage, low drift, and low bias current if the source impedance is significant. AC applications require bandwidth, low noise, and low distortion. When amplifiers are driving ADCs, settling time becomes a very important parameter.

Low temperature drift and low noise are also critical requirements for the analog signal path. Errors at +25°C are typically calibrated in the software. Drift over temperature might need to be controlled through calibration routines because it can become a critical specification in environments where temperature is not constant.

Analog-to-Digital Conversion

Next in the signal chain is the ADC. The ADC takes the analog signal and converts it to a digital signal. Depending on the application, the ADC requirements vary. For example, the bandwidth of the input signal dictates the ADC's maximum sampling rate so the selected ADC must have a

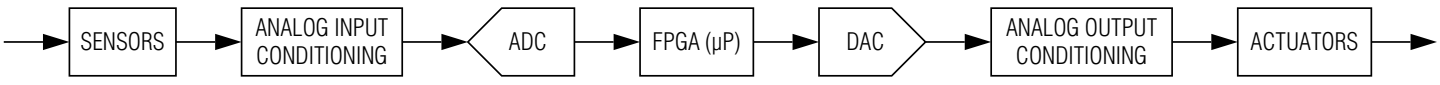


Figure 12. Block Diagram Showing a Common Signal-Chain Flow

sufficiently high sampling rate (greater than twice the input bandwidth). There are some communications applications where this rule does not apply.

The signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) specifications of the system dictate the ADC's resolution, filtering requirements, and gain stages. It is also important to determine how the ADC interfaces to the FPGA. High-bandwidth applications perform better using a parallel or fast serial interface, while in systems requiring easy galvanic isolation, SPI with unidirectional signaling is preferred.

Criteria for ADC Selection

When selecting the right ADC for the application, the engineer must consider, review, and compare very specific device criteria. **Table 5** presents typical ADC selection criteria.

An ADC that is not an ideal match can be used, and analog blocks can be employed to augment its functionality to meet the requirements. Exercise care during selection to ensure that any additional specified components provide performance similar to the ADC. Rather than using discrete components, it is also common to use an integrated AFE to buffer or even replace the ADC.

Once the data is converted, it is processed digitally in the FPGA. In some systems, this is the end of the process as the data is sent to other digital devices in the system, such as a server or PC. In other cases, the system needs to drive an analog output.

Criteria for DAC Selection

Analog output signals are required for situations in which a compatible transducer or instrument needs to be driven. Examples include proportional valves and current-loop-controlled actuators. It can be part of a simple open-loop control system or a complex control loop in a proportional-integral-derivative (PID) system. The result of this output is sensed and fed back for PID processing.

Table 3. Parameters Measured in Many Systems

Dimension	Pitch	Position
Intensity	Energy	Pressure
Impedance	Temperature	Humidity
Density	Speed	Frequency
Viscosity	Time of flight	Phase
Velocity	Distance	Time
Acceleration	Pressure	Salinity
Water purity	Torque	Volume
Weight	State of charge	Gases
Mass	Conductivity	Ph
Resistance	Dissolved oxygen	Voltage
Capacitance	Ion concentration	Current
Inductance	Chemicals	Level
Rotation	Charge (electrons)	

Table 4. Actions that Devices Can Control

Valves	Contrast	Acceleration
Motors	Humidity	Switches
Pressure	Force feedback	Lights
Velocity	Room entry	Weight
Flow	Sequence	Speed
Volume	Authorization	Meters
Torque	Attenuation	Displays
Frequency	Equalization	Calibration
Voltage	Communication	Time
Current	Gain (offset)	Tools
Solenoids	Flux density	Pitch
Position	Temperature	Filters
Power	Galvanometers	
Brightness	Air fuel ratios	

Table 5. Typical ADC Selection Criteria Matrix

Input range: Unipolar Biploar	Resolution: Dynamic range ENOB	Interface: Serial (I^2C, SPI), Parallel (4, 8, 16, N)
Speed: BW	Input type: Single-ended Differential	Channels
Simultaneous	Reference	Power
Filtering: 50Hz/60Hz Rejection	PGA	Other: GPIO FIFO

The analog output begins with digital data from the FPGA (Figure 12). This digital data is converted into an analog voltage or current signal using a digital-to-analog converter (DAC). Signal-conditioning circuitry then provides reconstruction filtering, offset, gain, muxing, sample/hold, and drive amplification as necessary.

As with the analog inputs, various implementations are possible when multiple analog outputs are needed.

Maxim has precision DACs ranging from below 8 bits up to 18 bits of resolution and up to 32 channels. Calibration DACs are available from 4 bits to 16 bits, and our sample/hold amplifiers provide additional ways to maintain constant voltages at many outputs, while the DAC serves other outputs.

Producing discrete, selectable, voltage-output (bipolar and unipolar), or current-output conditioning circuits can be an involved task. This is especially true as one begins to understand the necessity of controlling full-scale gain variations, the multiple reset levels for bipolar and unipolar voltages, or the different output-current levels necessary to provide the system design with the most flexible outputs. For more information about designing with DACs and ADCs, refer to our application note library (www.maximintegrated.com/converter-app-notes).

What is Critical?

The critical parts of the block diagram or chain depend on the specific application. A clean power supply, good filters, and noise-free op amps for signal conditioning are important for a good SNR. Accuracy is greatly dependent on ADC and DAC resolution, linearity, and stable voltage references.

For precise systems, DACs (and ADCs) require an accurate voltage reference. The voltage reference is internal or external to the data converter. In addition to many ADCs and DACs with internal references, Maxim offers stand-alone voltage references with temperature coefficients as low as 1ppm/°C, output voltage as accurate as ±0.02%, and output noise as low as 1.3μV_{P-P} that can be used externally by the data converter for ultimate precision and accuracy.

Along with creating a circuit design that achieves a specified performance, the designer is also usually required to complete the process in a limited amount of time. Easy-to-use development tools, including FMC and plug-in module development cards that directly connect with many FPGA development boards, help integrate Maxim products into FPGA designs. Along with our many EV kits, calculators, and application notes, these tools allow the designer to complete their work more quickly and accurately.

FPGA Challenges Facing a System Designer

Many FPGA designers are accomplished digital engineers; Maxim's expertise is analog interface. These complementary skills optimize system performance and cost. FPGA design has a large affinity with digital designers because FPGAs are configurable digital systems. From simulation to synthesis, everything is done in a digital domain.

However, much uncertainty is introduced when these digital systems are tied to the analog world. Some of the questions that system designers face are:

"How much gain should be applied to a signal?

"What analog filters should be used?

"How to drive the ADC?

"How much resolution is needed?

"What speed is needed?

"What specs are critical?

"How much output drive is required?

"How to lower the noise?"

Answering these questions is where a world-leading analog company such as Maxim excels. With our large product portfolio and expertise in system design, FPGA designers can count on Maxim to have the right solution for their application.

Design requirements often change at the eleventh hour. Maxim products are up to the task.

Four scenarios come to mind:

- The customer changes the specification just before delivery.
- The sales department needs to add a must-have feature at the last minute.
- The design does not fit in the ASIC or FPGA without going to a larger device, thereby increasing cost and requiring the designer to move some circuits outside the device.
- Murphy's Law strikes.

Problems that analog engineers experience are often caused by low signal-to-noise, crosstalk, gain (span), offset (zero), and linearity. External integrated circuits (IC) that resolve these issues are amplifiers, ADCs, DACs, digital potentiometers, filters, multiplexers, and voltage references. Other issues that arise are impedance matching, translation of analog voltages and currents, self-blocking (where a radio transmitter interferes with its own receiver), backlight LED, and touch controls. Analog ICs can be employed to manage these functions, add features, and offload the FPGA.

Other analog ICs partnered with FPGAs in real-world designs include power supplies, margining and calibration, battery chargers, power supervisors, interface devices, temperature controllers and monitors, real-time clocks (RTCs), watchdog timers, and precision resistors.

Maxim offers all of these types of devices. Using such components can save designs from errors and complications due to last minute changes. It can also reduce time-to-market, avoid a spin or redo, and allow a project to succeed where others might fail.

Maxim Makes It Easy

Maxim offers many tools to help the designer create, develop, verify, and complete their designs, including Maxim's very own online calculators (www.maximintegrated.com/tools/calculators).

Choose a calculator and fine-tune it, depending on your particular requirements. For example, use Steve's Analog Design Calculators to pick the ideal converter. Then fine-tune the accuracy and sampling rate using another calculator.

Other great aids are available on the tools, models, and software page (www.maximintegrated.com/design/tools). From here, you have access to the EE-Sim tool (simulations), a constantly updated library of models (SPICE, PSpice®, and IBIS), a selection of BSDL files, and software.

Maxim has long been revered for the quality and variety of our products as well as the ease of use of our evaluation kits (EV kits). Many of our parts have been tailored for specific purposes. Hundreds of Maxim EV kits and reference boards are available through Maxim distributors.

Maxim has a dedicated team of applications engineers ready to answer your questions through email or over the phone. We strive to respond to every customer inquiry within one business day. You can find a selection of links to answer many common inquiries, such as pricing or delivery questions, at our Support Center page (support.maximintegrated.com/center.mvp). Finally, and most importantly, Maxim and our distribution partners' FAEs stand ready to assist you.

Summary

When you partner with Maxim, you have a full-service organization dedicated to supplying everything you need to complete your FPGA design. With a wide selection of lower power, fast, and accurate products in small packages plus easy-to-use design tools and boards, Maxim simplifies your FPGA board development process. In addition, Maxim and our distribution partners' FAEs are here to assist you.

Trapped Between Precision and Noise

In some applications, the designer might feel trapped by noise, precision required, and cost. A good design is one that satisfies the customer's requirements at an affordable price. An FPGA with internal data converters is a great advancement. However, such converters do not meet the requirements for every application.

There are some important considerations about noise to factor in when evaluating one's ADC or DAC needs. By their nature, digital designs add noise into the equation. FPGAs operate at faster speeds (GHz communications are now common), resulting in the creation of more noise.

Let us look at some rules of thumb concerning orders of noise magnitude. Power supplies typically have millivolts (mV) of noise. Noise sources include switching power supplies, power line or mains, radio interference, motors, arc welders, and digital circuits. An ADC or DAC with a 3V full scale has a least significant bit (LSB) at the levels shown in **Table 6**.

It becomes readily apparent why noise is at odds with precision. We recommend sketching the design in block form, as well as estimating noise and signal levels with a fellow designer. Jot down what is known about the project, input and output signals and values, power requirements, and known block contents. See Table 6. If the system needs 8 bits of resolution at the output, are 10 or 12 bits at the input sufficient? If there is 5mV of noise present in the system (56dB down), is a 24-bit converter with a dynamic range of 144dB viable or overkill? See how quickly reality sets in? In just a few minutes, we have defined the parameters of the project. Now the decision to use the internal converter or an external one with a clean power supply is obvious.

Digital noise in particular is typically addressed as follows. First, use an external data converter, meeting your requirements with separate, clean analog supplies and ground to maximize precision and accuracy. Second, oversample and average the signal. You get approximately one extra bit of resolution for each 4x of oversampling.

Not all bits are created equal. We should be wary of marketing bits, which are commonly listed front and center on data sheets. The real bits of converters take into account all nonlinearities and can be extracted by looking at other key parameters. For example, SINAD performance is commonly used to determine the effective number of bits for SAR converters, while noise distribution of captured signal calculates the noise-free bits in sigma-delta converters.

You also need to understand the application's requirement for voltage and temperature stability and construct an error budget for the combination of the data converter and the voltage reference. Maxim has a tool to simplify this task. You can find it in application note 4300: Calculating the Error Budget in Precision Digital-to-Analog Converter (DAC) Applications.

Table 6. Data Converter Resolution and LSB Voltage for 3V Full Scale

No. of Bits	Decimal No. of Levels	LSB
8	256	11.7mV
10	1,024	2.9mV
12	4,096	0.73mV
14	16,384	0.18mV
16	65,536	45.8µV
18	262,144	11.4µV
24	16,777,216	0.18µV

Featured Products

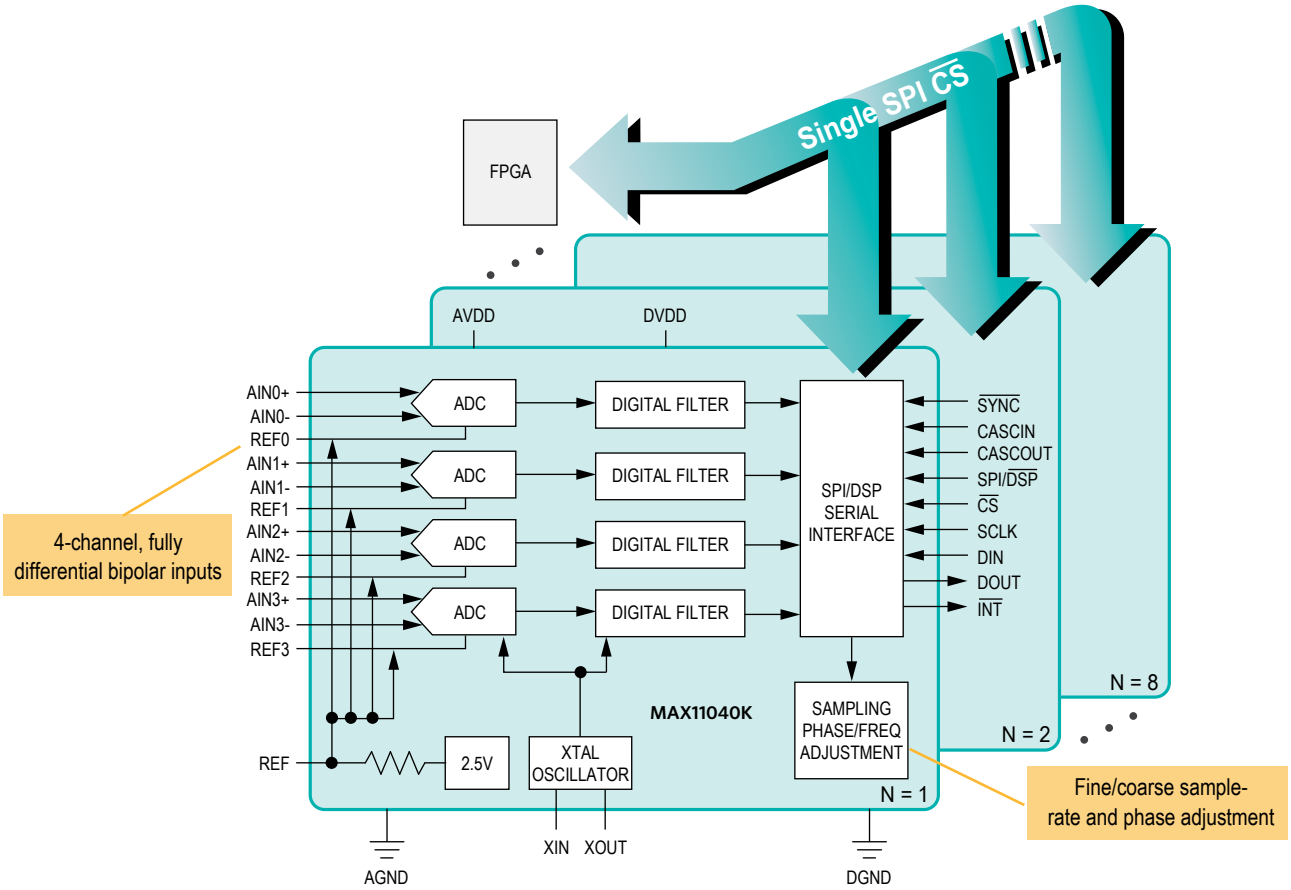
24-/16-Bit Sigma-Delta ADCs Enable 32 Simultaneous Channels

MAX11040K

The MAX11040K sigma-delta ADC offers 117dB SNR, four differential channels, and simultaneous sampling that is expandable to 32 channels (eight MAX11040K ADCs in parallel). A programmable phase and sampling rate make the MAX11040K ideal for high-precision, phase-critical measurements in noisy PLC environments. With a single command, the MAX11040K's SPI-compatible serial interface allows data to be read from all the cascaded devices. Four modulators simultaneously convert each fully differential analog input with a 0.25ksps to 64ksps programmable data-output-rate range. The device achieves 106dB SNR at 16ksps and 117dB SNR at 1ksps.

Benefits

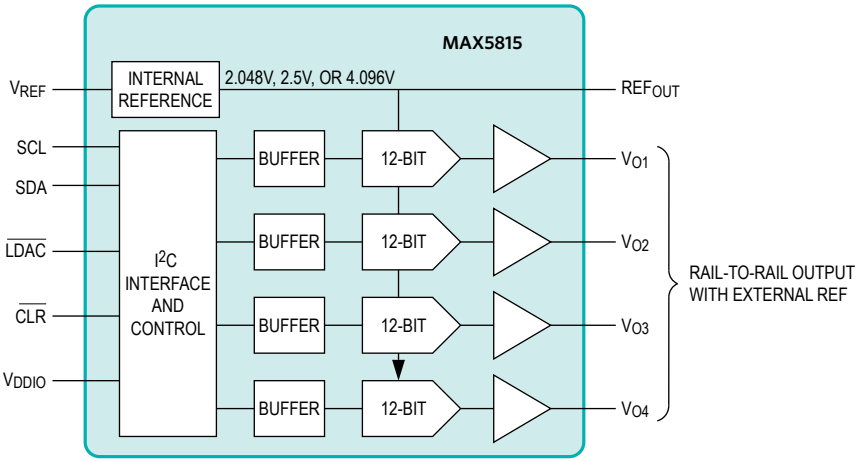
- Simplifies digital interface to an FPGA
  - Eight MAX11040K ADCs can be interfaced
- 106dB SNR allows users to measure both very small and large input voltages
- Easily measures the phase relationship between multiple input channels
  - Simultaneous sampling preserves phase integrity on multiple channels

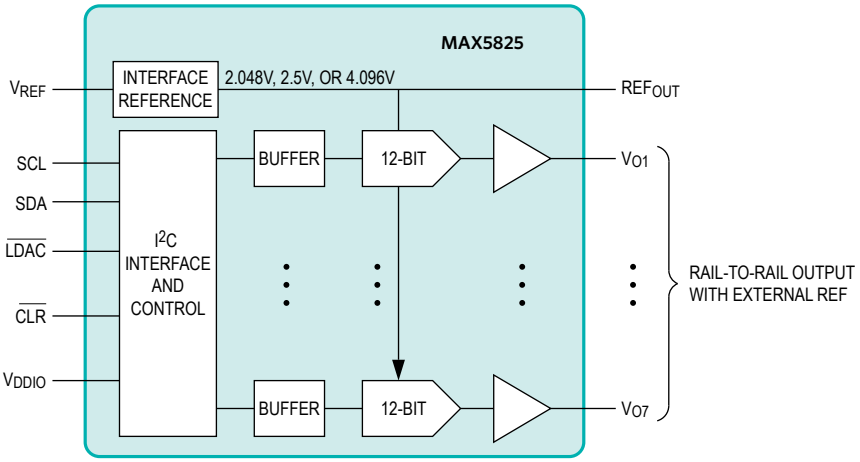


High Integration and a Small Package Create the Industry's Smallest Solution

MAX5815, MAX5825

The MAX5815 and MAX5825 are a 4- and 8-channel, ultra-small, 12-, 10-, and 8-bit family of voltage output, digital-to-analog converters (DACs) with internal reference that are well-suited for process control, data acquisition, and portable instrumentation applications. They accept a wide supply voltage range of 2.7V to 5.5V with extremely low power (3mW) consumption to accommodate most low-voltage applications. A precision external reference input allows rail-to-rail operation and presents a 100kΩ (typ) load to an external reference. A separate V_{DDIO} pin eliminates the need for external voltage translators when connecting to an FPGA, ASIC, DSP, etc.





Benefits

- Reduces cost and simplifies manufacturing
  - Complete single-chip solution
  - Internal output buffer and integrated voltage reference
- Eliminates need to stock multiple voltage references
  - 3 precision selectable internal references: 2.048V, 2.5V, or 4.096V
- Provides industry's smallest PCB area
  - 4-channel available in 12-bump WLP and 14-pin TSSOP packages
  - 8-channel available in 20-bump WLP and 20-pin TSSOP packages

Selector Guide and Tables

Signal Solutions for FPGAs

Part	Description	Features	Benefit
MAX44251/MAX44252	20V, ultra-precision, low-noise, low-drift, dual and quad amplifiers	5.9nV/√Hz input voltage noise; 6µV (max) offset; 20nV/°C offset drift	Maintain system calibration and accuracy over time and temperature; improve system accuracy
MAX9632, MAX9633	36V, high-bandwidth, low-noise single and dual amplifiers	0.94nV/√Hz (MAX9632) and 3nV/√Hz (MAX9633) input voltage noise; less than 750ns settling time	Enable full performance from high-resolution ADCs for more accurate measurement
MAX9943/MAX9944	38V, precision, single and dual op amps	Wide 6V to 38V supply range; low 100µV (max) input offset voltage; drive 1nF loads	Allow operation in a variety of conditions
MAX9945	38V, CMOS-input precision op amp	Wide 4.75V to 38V supply range; low input-bias current; rail-to-rail output swing	High voltage and low femto-amp input-bias current enables easy interfacing with ultra-high omhic sensors
MAX4238/MAX4239	Industry's lowest offset, low-noise rail-to-rail output op amps	2µV (max) offset; 25nV/√Hz; 6.5MHz GBW; no 1/f input-noise component	Ensure precision signal conditioning at low frequencies over time and temperature
MAX5316/MAX5318	1-channel, 16- and 18-bit precision DACs	Internal output buffer and voltage reference buffer; separate V_{DD} I/O voltage; rail-to-rail output buffer; force-sense output	Guarantee full accuracy at the load for precision operation
MAX5815	4-channel, 12-bit DAC with internal reference	Complete single-chip solution; internal output buffer; 3 precision selectable internal references	Eliminates the need for voltage translators and multiple voltage references
MAX5214/MAX5216	Single-channel, low-power, 14- and 16-bit, buffered voltage-output DACs	Low-power consumption (80µA max); 3mm x 3mm, 8-pin µMAX package; ±0.25 LSB INL (MAX5214, 14 bit) or ±1 LSB INL (MAX5216, 16 bit)	Provides better resolution and accuracy while conserving power and saving space
MAX5825	8-channel, low-power, 12-bit, buffered voltage-output DACs	Complete single-chip solution with independent voltage for digital I/O (1.8V to 5V); internal rail-to-rail output buffers; 3 selectable internal or external references	Eliminates voltage level translators to save PCB area
MAX6126	Ultra-low-noise, high-precision, low-dropout voltage reference	Ultra-low 1.3µV_{P-P} noise (0.1Hz to 10Hz, 2.048V output); ultra-low 3ppm/°C (max) temperature coefficient; ±0.02% (max) initial accuracy	Supply current is virtually independent of supply voltage, providing predictable power budget; does not require an external resistor, saving board space and cost
MAX1377, MAX1379, MAX1383	12-bit, 4-channel, simultaneous-sampling ADCs (2 x 2 single-ended or 2 x 1 differential inputs)	Two simultaneous-sampling with two multiplexed inputs (four single-ended inputs total); 1.25Msps per ADC dual or single SPI port; supports ±10V from 5V supply (MAX1383)	Provide a cost-sensitive, high-integration 12-bit solution for power system monitoring and motor control applications
MAX11046	Industry's first single-supply bipolar ADCs with high-impedance input	14-/16-bit, 8-/6-/4-channel simultaneous-sampling SAR ADCs with high-impedance I/O technology that eliminates external buffers; bipolar input with only a single +5V analog supply	No external buffers simplifies circuitry; saves cost and space

(Continued on following page)

Signal Solutions for FPGAs (continued)

Part	Description	Features	Benefit
MAX11040K	24-/16-bit sigma-delta ADCs cascadable up to 32 simultaneous channels	Four fully differential simultaneously sampled channels; 106dB SNR at 16ksps	Easily scalable for up to eight ADCs in parallel; allows monitoring 3 voltages: 3 current plus neutral pair to address power applications
MAX11160/MAX11161, MAX11162/MAX11163, MAX11164/MAX11165, MAX11166/MAX11167, MAX11168	16-bit, 1-channel 500ksps SAR ADCs with integrated reference and bipolar option	> 93dB SNR; integrated 5ppm reference option; available bipolar ±5V input range with 5V supply	High integration and small packages (state package size) give smaller form factor and lower total system cost without compromising high performance
MAX1300/MAX1301, MAX1302/MAX1303	16-bit, 4- and 8-channel SAR ADCs with programmable input ranges up to 3 x V_{REF} (4.096V)	Each channel is programmable to be single-ended or differential and unipolar or bipolar; integrated PGA (gain up to 4) and reference	Allow multiple input sources to be supported in a single device, increasing flexibility and saving cost

Signal Solutions Evaluation Kits

Part	Description	Features
MAX9632EVKIT, MAX9633EVKIT	To evaluate MAX9632 and MAX9633 36V, high-bandwidth, low-noise single and dual amplifiers	Accommodate multiple op amp configurations, +4.5V to +36V wide input supply range, 0805 components
MAX9943EVKIT	To evaluate the MAX9943 and MAX9944 38V, precision, single and dual op amps	Flexible input and output configurations; +6V to +38V single-supply range; ±3V to ±19V dual supply range
MAX9945EVKIT	To evaluate the MAX9945 38V, CMOS-input precision op amp	Accommodates multiple op amp configurations, wide input supply range, 0805 components
MAX5316EVSYS	To evaluate the MAX5316 true accuracy 16-bit, voltage output DAC with digital gain and offset control	Windows® software provides a simple graphical user interface (GUI) for exercising the features of the MAX5316; includes a MAX5316EVKIT with a 16-bit MAX5316GTG+ precision DAC installed (allows a PC to control the SPI interface and GPIOs using its USB port)
MAX5815AEVKIT	Demonstrates the MAX5815 12-bit, 4-channel, low-power DAC with internal reference and buffered voltage output	Windows software provides a simple graphical user interface (GUI) for exercising the features of the device; includes a USB-to-I^2C 400kHz interface circuit
MAX5216EVKIT	Demonstrates the MAX5216 16-bit, low-power, high-performance, buffered digital-to-analog converter (DAC)	Windows software; supports 14- and 16-bit DACs; includes on-board microcontroller to generate SPI commands; USB powered
MAX5825AEVKIT	Demonstrates the MAX5825 12-bit, 8-channel, low-power DAC with internal reference and buffered voltage output	Windows software provides a simple graphical user interface (GUI) for exercising the features of the device; includes a USB-to-I^2C 400kHz interface circuit
MAX5214DACLITE	Demonstrates the MAX5214 true resolution 14-bit, low-power, high-performance, buffered digital-to-analog converter (DAC)	Includes on-board microcontroller to generate SPI commands; Windows software provides a simple graphical user interface (GUI) for exercising the features of the MAX5214; USB powered

(Continued on following page)

Signal Solutions Evaluation Kits (continued)

Part	Description	Features
MAX1379EVKIT	Demonstrates the MAX1379 12-bit, 48-channel, simultaneous-sampling ADCs	Complete evaluation system; convenient test points provided on-board data-logging software with FFT capability; can also be used to evaluate the MAX1377
MAX11046EVKIT	Provides a proven design to evaluate the MAX11046 8-channel, 16-bit, simultaneous-sampling ADC	Eight simultaneous ADC channel inputs; BNC connectors for all signal input channels; 6V to 8V single power-supply operation; USB-to-PC connection compatible with five other MAX1104x family members
MAX11040KEVKIT, MAX11040KDBEVKIT	Fully assembled and tested PCB that evaluates the IC's 4-channel, simultaneous-sampling ADC	Two MAX11040KGUU+s installed on the motherboard; up to three more parts can be connected by cascading up to three daughter boards
MAX11160EVSYS	Proven design for 16-bit, high-speed precision ADC	Windows software provides a simple graphical user interface (GUI) for exercising the features of the MAX11160; includes a companion MAXPRECADCMB serial interface board and the MAX11160DBEVKIT with a 16-bit MAX11160 precision ADC installed (allows a PC to control the SPI interface and GPIOs using its USB port)
MAX1300AEVKIT	Proven design for 16-bit programmable input range precision ADC	On-the-fly programmability of the input ranges based on multiples of the voltage reference; support for single-ended and differential as well as bipolar and unipolar inputs
MAXADCLITE	Demonstrates the industry's smallest SAR ADC in a tiny 12-bump WLP packaging solution	4-channel, 12-bit I^2C SAR ADC with USB connection to a PC; self-powered from the USB port; complete data acquisition system on a tiny EV kit

Design Protection Solutions for FPGAs

Overview

Maxim's secure information and authentication (SIA) products offer low-cost, secure memory solutions that incorporate robust, crypto-industry vetted authentication and encryption schemes with best-in-class countermeasures against invasive (die-level) and side-channel (noninvasive) attacks. These solutions are ideal for protecting design intellectual property, managing licensing, and controlling software feature set upgrades in field-deployed equipment.

Identifying the Problem

Today, designers can select FPGAs that employ various technologies to hold the design configuration data, such as one-time programmable (OTP) antifuses, reprogrammable flash-based storage cells, and reprogrammable SRAM-based configurable logic cells. The configuration data essentially contains the IP related to the design or the end product.

Both antifuse- and flash-based solutions provide relatively secure solutions since the configuration data is stored on the FPGA chip and there are mechanisms that prevent the stored data from being read. Moreover, unless very sophisticated schemes such as depacking, microprobing, voltage contrast electron-beam microscopy, and focused-ion-beam (FIB) probing are used to pry into the silicon and to disable security mechanisms, it is very unlikely that the data can be compromised. However, OEMs need to exercise strict control on licensing as contract manufacturers tasked with FPGA programming can produce more units than authorized and sell them on the gray market. Such unauthorized devices are indistinguishable from the authorized devices and can significantly impact an OEM's profitability.

SRAM FPGAs, however, have fewer safeguards to protect that IP (i.e., the configuration data) against illegal copying and theft. The configuration data is stored on a separate memory chip and is read by the FPGA at power-up. The read data is held in the SRAM memory cells in the FPGA. This arrangement compromises the security of the configuration data at two stages:

- The configuration data bit stream is exposed to eavesdropping during the power-up phase.
- Configuration data stored in SRAM memory cells can easily be probed.

A potential cloner can easily gain access to the configuration data using these techniques and clone the original design, thereby compromising the IP and profitability associated with the genuine product.

Facing the Challenge

Higher-end FPGAs address these security concerns with built-in encryption schemes and identification mechanisms, but these solutions are not cost-efficient for high volume applications such as consumer electronics. However, these applications still require a way to protect their IP from piracy. Furthermore, the security scheme should be robust, easy to implement, and have minimal impact on FPGA resources (i.e., the number of pins and logic elements), power consumption, and the cost of the overall design.

Presenting the Solution: Authentication

The objective of the authentication process is to establish proof of identity between two or more entities. Key-based authentication takes a secret key and the to-be-authenticated data (i.e., the message) as input to compute a message authentication code (MAC). The MAC is then attached to the message. The recipient of the message performs the same computation and compares its version of the MAC to the one received with the message. If both MACs match, the message is authentic. To prevent replay of an intercepted (nonauthentic) message, the MAC computation incorporates a random challenge chosen by the MAC recipient.

Figure 13 illustrates the general concept. The longer the challenge, the more difficult it is to record all possible responses for a potential replay.

To prove the authenticity of the MAC originator, the MAC recipient generates a random number and sends it as a challenge to the originator. The MAC originator must then compute a new MAC based on the secret key, the message, and the recipient's challenge. The originator then sends the computed result back to the recipient. If the originator proves capable of generating a valid MAC for any challenge, it is very certain that it knows the secret key and, therefore, can be considered authentic. This process is called challenge-and-response authentication. See Figure 13.

Numerous algorithms are used to compute MACs, such as Gost-Hash, HAS-160, HAVAL, MDC-2, MD2, MD4, MD5, RIPEMD, SHA family, Tiger, and WHIRLPOOL. A thoroughly scrutinized and internationally-certified, one-way hash algorithm is SHA-1, developed by the National Institute of Standards and Technology (NIST). SHA-1 has evolved into the international standard ISO/IEC 10118-3:2004. Distinctive characteristics of the SHA-1 algorithm are:

- Irreversibility: It is computationally infeasible to determine the input corresponding to a MAC.
- Collision resistance: It is impractical to find more than one input message that produces a given MAC.
- High avalanche effect: Any change in input produces a significant change in the MAC result.

For these reasons, as well as the international scrutiny of the algorithm, SHA-1 is an excellent choice for challenge-and-response authentication of secure memories.

Implementing the Solution

A challenge-and-response authentication scheme can be implemented inexpensively as part of an SRAM-based FPGA system design (**Figure 14**). In this example, the secure memory device uses only a single pin to connect to an FPGA pin configured for bidirectional (open-drain) communication. A resistive connection to V_{DD} delivers power to the secure memory and provides the bias for open-drain communication. Maxim's DS28E01-100 1Kb protected 1-Wire EEPROM with a SHA-1 engine is a good fit for this scheme. The device contains a SHA-1 engine, 128 bytes of user memory, a secret key that can be used for chip-internal operations, but cannot be read from an outside source, and a unique, unchangeable identification number.

The 1-Wire interface of the DS28E01-100 reduces the communications channel to just a single FPGA pin for the challenge-and-response authentication. That minimizes the impact of the security solution since FPGAs are often I/O-pin limited. Alternate implementations can be constructed using a more generic I^2C interface on the FPGA and the DS28CN01 (an I^2C equivalent of the DS28E01-100), or by implementing the SHA-1 engine and other functions in a small ASIC or CPLD. However, if security is the device's only function, using the ASIC approach would probably cost more.

To leverage the security features of the DS28E01-100, a reference authentication core enables the FPGA to do the following steps:

1. Generate random numbers for the challenge. On-chip random number generators usually create pseudorandom numbers, which are not as secure as real random numbers.
2. Know a secret key that can be used for internal operations, but cannot be discovered by an outside source.
3. Compute a SHA-1 MAC that involves the secret key, a random number, and additional data, just like the secure memory.
4. Compare data byte for byte, using the XOR function of the CPU implemented in the FPGA.

For detailed information on the SHA-1 MAC computation, review the Secure Hash Standard. Application note 3675: Protecting the R&D Investment with Secure Authentication provides technical details on the concept of authentication and the architecture of a secure memory.

Microcontroller-like functionality is typically available as a free macro from major FPGA vendors. The Altera microcontroller function occupies 192 logic cells, which represents just 11% of a Cyclone III device.

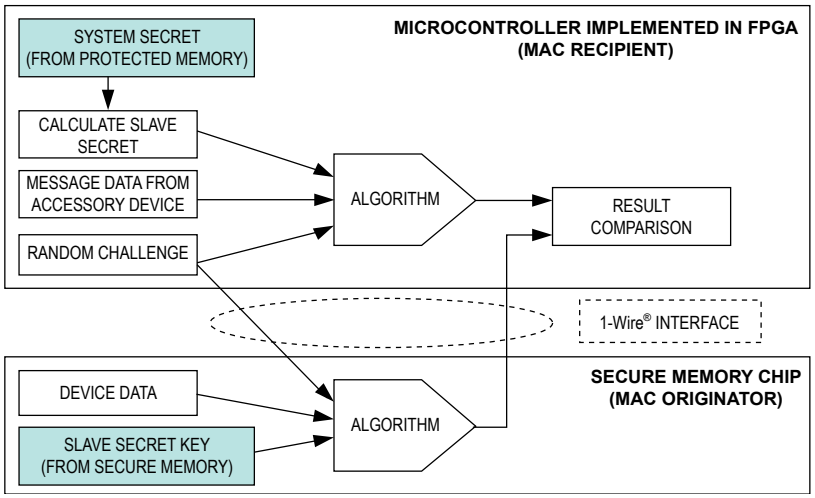


Figure 13. The Challenge-and-Response Authentication Process Proves the Authenticity of a MAC Originator

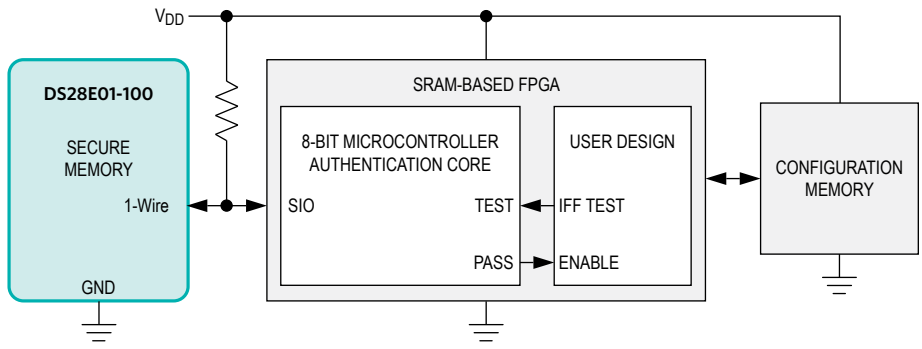


Figure 14. In This Simplified Schematic, a Secure 1-Wire Memory is Used for FPGA Protection

How It Works

The DS28E01-100 is programmed with an OEM-specific secret key and data. Programming can be done by the OEM or, prior to shipment, by Maxim. The DS28E01-100 is effectively the ignition key for the FPGA design. The OEM-specific secret key also resides in the scrambled configuration data that is programmed into the configuration (external) memory.

When power is applied, the FPGA configures itself from its configuration memory. Now the FPGA's microcontroller function activates and performs the challenge-and-response authentication, also known as identification friend or foe (IFF). This identification involves the following steps:

1. The FPGA generates a random number and sends it as a challenge (Q) to the secure memory.
2. The FPGA instructs the secure memory to compute a SHA-1 MAC based on its secret key, the challenge sent, its unique

identification number, and other fixed data, and to transmit the response (MAC2) to the FPGA.

3. The FPGA computes a SHA-1 MAC (MAC1) based on the same input and constants used by the secure memory and the FPGA's secret key.
4. The FPGA compares MAC1 with MAC2. If the MACs match, the FPGA determines that it is working in a licensed environment. The FPGA transitions to normal operation, enabling/performing all of the functions defined in its configuration code. If the MACs differ, however, the environment is considered hostile. In this case, the FPGA takes application-specific action rather than continue with normal operation.

Why the Process Is Secure

Besides the inherent security provided by SHA-1, the principal security element for the above IFF authentication process is the secret key, which is not readable from the secure memory or the FPGA. Furthermore, because the data in the bit stream is scrambled, eavesdropping on the configuration bit stream when the FPGA configures itself does not reveal the secret key. Due to its size, reverse-engineering the bit stream to determine the design with the intent of removing the authentication step is very time-consuming, and thus, is a prohibitively difficult task.

Another critical security component is the randomness of the challenge. A predictable challenge (i.e., a constant) causes a predictable response that can be recorded once and then replayed later by a microcontroller emulating the secure memory. With a predictable challenge, the microcontroller can effectively deceive the FPGA into considering the environment as friendly. The randomness of the challenge in this IFF approach alleviates this concern.

Security can be improved further if the secret key in each secure memory is device-specific: an individual secret key computed from a master secret, the SHA-1 memory's unique identification number, and application-specific constants. If an individual key becomes public, only a single device is affected and not the security of the entire system. To support individual secret keys, the FPGA needs to know the master secret key and compute the 1-Wire SHA-1 memory chip's secret key first before computing the expected response.

For every unit to be built, the owner of the design (OEM) must provide one properly preprogrammed secure memory to the contract manufacturer (CM) that makes the product with the embedded FPGA. This one-to-one relationship limits the number of authorized units that the CM can build. To prevent the CM from tampering with the secure memory (e.g., claiming that additional memories are needed because some were not programmed properly), OEMs are advised to write-protect the secret key.

There is no need to worry about the security of the 1-Wire EEPROM data memory, even if it is not write-protected. By design, this memory data can only be changed by individuals who know the secret key. As a welcome addition, this characteristic lets the application designer implement soft-feature management—the FPGA can enable/disable functions depending on data that it reads from the SHA-1 secured memory.

It is not always practical for the OEM to preprogram memory devices before delivery to the CM. To address this situation, the manufacturer of the secure memory could set up a SHA-1 secret key and a EEPROM-array preprogramming service for the OEM. Maxim provides such a service, where secure memory devices are registered and configured at the factory according to OEM input and then shipped directly to the CM. Key benefits of this service include:

- Eliminates the need for the OEM to disclose the secret key to the CM.
- Eliminates the need for the OEM to implement its own preprogramming system.
- Only OEM-authorized third parties have access to registered devices.
- The vendor maintains records of shipped quantities, if needed for OEM auditing.

Providing Proof of Concept

The FPGA security method featured in Altera's FPGA Design Security Solution Using a Secure Memory Device Reference Design has been tested with Altera products. Altera states: "This reference design provides a solution to help protect FPGA designs from being cloned. Using the 'identification, friend or foe' (IFF) design security approach, this solution disables the design within the FPGA until the hash algorithm computation matches in both the FPGA and a secure memory device, so the design remains secure even if the configuration data bitstream is captured." The simple interface to programming and authentication provided in this reference design makes this copy protection scheme very easy to implement.

In his articles on military cryptography, the 19th century Flemish linguist Auguste Kerckhoffs argues that instead of relying on obscurity, security should depend on the strength of keys. He contends that in the event of a breach, only the keys would need to be replaced instead of the whole system.

Conclusion

IP in FPGA designs can easily be protected by adding just one low-cost chip such as the DS28E01-100 and uploading the FPGA with the free reference core. The 1-Wire interface enables implementation of the security scheme over a single FPGA pin.

Selector Guide and Tables

Secure Information and Authentication Solution for FPGAs

Part	Description	Features	Benefit
DS28E01-100	1-Wire 1Kb SHA-1 secure EEPROM	User-customizable read/write/OTP page modes; ±8kV HBM with ±15kV IEC ESD protection	Communicate and control over a single dedicated contact, minimizing space and pin impact

Interfacing High-Speed DACs and ADCs to FPGAs

Introduction

As the speed and channel count of data converters increase with each new generation, timing and data integrity between these devices and FPGAs become more challenging. Maxim works closely with industry-leading FPGA suppliers to define requirements for digital interfaces between the FPGAs and high-speed data converters. This collaboration to overcome these challenges ensures compatibility, the efficient use of resources, and ease of design.

FPGA/Data Conversion Trends

Data conversion and FPGA technology continue to evolve. Advancements in performance and operating speeds have led many applications to move signal processing from the analog domain to the digital domain. For example, instead of designing wireless transmitters with a dual baseband I/Q DAC, an analog quadrature modulator, and a frequency synthesizer, designers use a fast FPGA and a RF digital-to-analog converter (RF-DAC). A digital quadrature modulator is implemented in the FPGA to upconvert the signal digitally, which is then synthesized by the RF-DAC at the required frequency. Benefits of a digital RF transmitter over an analog RF transmitter include eliminating I/Q imbalance, increased carrier or channel capacity, and the ability to support multiple frequency bands using a common hardware platform. However, to realize these benefits, one must ensure data integrity and proper timing across the digital interface between the RF-DAC and the FPGA.

Similarly, instead of designing wireless receivers with a baseband ADC, an analog quadrature demodulator (or mixer), and a frequency synthesizer, designers use a fast FPGA and a RF analog-to-digital converter (RF-ADC).

Data Converter-to-FPGA Digital Interface Solutions

Maxim has added features to its RF-DACs to simplify the interface to FPGAs. Maxim develops RF-DACs with 2:1 or 4:1 multiplexed LVDS inputs to reduce the RF-DAC input data rate to a level compatible with current FPGA technology. Using the 2:1 multiplexed input mode, one can reduce the I/O pin count requirements, routing complexity, and board space. Alternatively, the 4:1 multiplexed input mode can be employed to increase the timing margins for a more robust design and possible use of slower FPGA.

Newer generations of RF-DAC products include an on-chip delayed-lock loop (DLL) to ease input data synchronization with FPGAs, and a parity function to provide interface failure monitoring. The RF-DAC data interfaces are system synchronous to guarantee deterministic latency. A source synchronous interface generally has a one-clock-cycle latency uncertainty. Maxim's RF-DACs offer a data scrambling feature to whiten the spectral content of the incoming data to eliminate potential data-dependent spurs.

A final consideration in interfacing a data converter to an FPGA is data clock speed. Maxim's RF-DACs and RF-sampling ADCs support a wide variety of interface formats including single data rate (SDR), double date rate (DDR), and quad data rate (QDR) to match the maximum clock rate specifications of different classes of FPGAs.

To meet the high-channel count data conversion demands of applications such as medical imaging, the interface between high-speed ADCs and FPGAs has evolved from parallel to high-speed serial. Benefits of a serial interface include fewer lines that provide a density and cost advantage, as well as relaxed delay-matching specifications that provide simplified design and increased robustness. Maxim offers octal (eight) channel, high-speed ADCs with serial LVDS outputs for high-density/low-power applications such as ultrasound. On some dual-channel, high-speed ADCs and DACs, Maxim offers selectable dual parallel CMOS or single multiplexed parallel CMOS interfaces as a trade-off for I/O pin count and interface speed.

Integrated DLL Simplifies FPGA-to-RF-DAC Synchronization

A functional diagram of the MAX5879 14-bit, 2.3Gsps RF-DAC is shown in **Figure 15**. The RF-DAC is updated on the rising edge of the clock (CLKP/CLKN) and contains selectable 2:1 or 4:1 multiplexed input ports to reduce the I/O pin count or the input data rate of the RF-DAC to either 1150Mwps or 575Mwps on each port.

The integrated MAX5879 DLL circuit ensures robust timing in the interface to the FPGA. This is especially important as the speed of the devices increases and the data window becomes smaller (i.e., data transitions occur more frequently). A simplified block diagram of the clocking scheme using an FPGA and the DLL of the MAX5879 is shown in **Figure 16**. The DLL circuit ensures data synchronization between the FPGA and the DAC by adjusting the phase of the incoming data so the data eye is centered on the internal clock (RCLK) edge that latches the data into the DAC. The DLL adjusts the phase of the incoming data (DATA) to the internal clock (RCLK), making it immune to temperature and power-supply variations.

If a DLL is not present, the designer needs to ensure the digital data being presented to the DAC is stable for a time

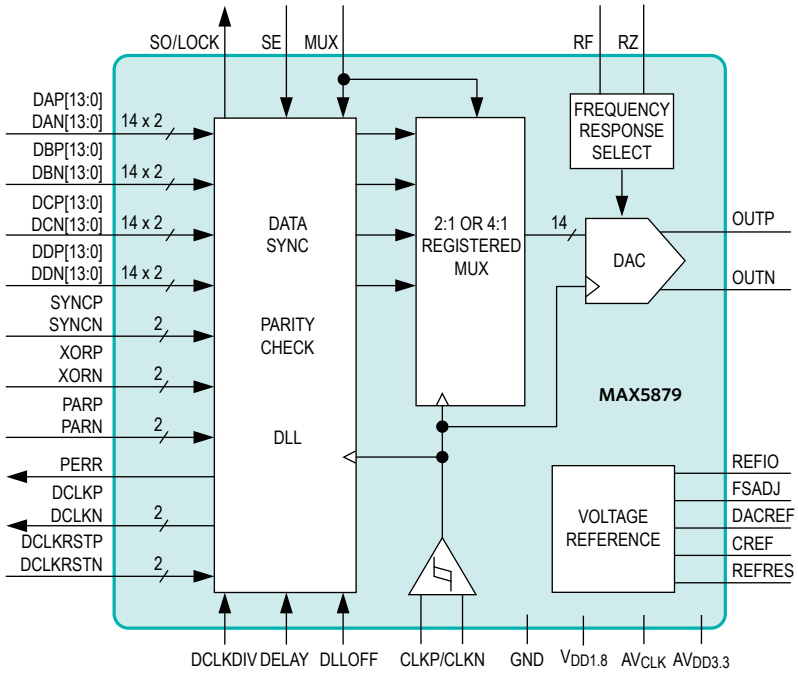


Figure 15. MAX5879 Functional Diagram

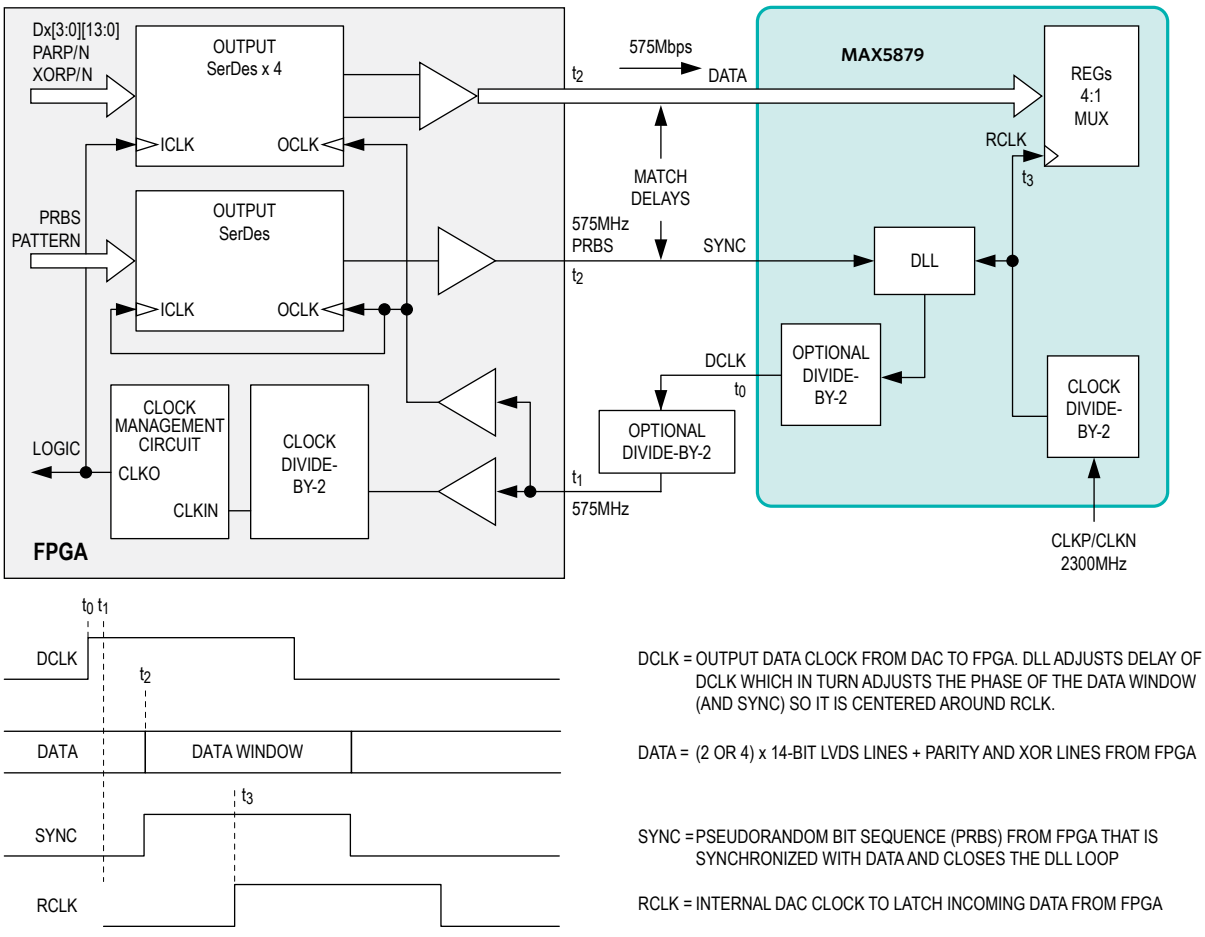


Figure 16. Digital Interface Between the FPGA and the MAX5879 RF-DAC (in 4:1 Mux Mode)

prior to the DCLK transition (t_{SETUP}) and is held for a period of time after the transition (t_{HOLD}). After factoring in temperature variation, the setup and hold times in the product data sheet can consume a large percentage of the valid data window, making it challenging to design a robust high-speed FPGA-to-DAC interface.

Data Scrambling and Parity Check Ensure Reliable System Performance

In some cases, periodic data patterns generated by the FPGA can create data-dependent spurs that affect the overall performance of the system. The MAX5879 RF-DAC contains an XOR data function that can be used to whiten the spectral content of the data bits and prevent this situation from occurring.

In addition, this DAC contains a parity function that is used to detect bits errors between the FPGA data source and the DAC and can be used for system monitoring. The parity calculated by the RF-DAC is compared to the parity received from the FPGA. When the received and calculated parity bits do not match, a parity error flag is set high so the FPGA can detect the fault and trigger a corrective action.

High-Speed Octal ADC has Serial FPGA Interface that Slashes Pin Count and Complexity

For high-channel count applications, a high-speed serial interface between the data converter and the FPGA is preferred over a parallel interface because it simplifies the design and provides a denser and more cost-effective solution. A functional diagram of the MAX19527 octal 12-bit, 50Msps ADC is shown in **Figure 17**. The high-speed interface to the FPGA consists of 10 LVDS pairs (20 pins): 8 high-speed serial outputs (1 for each channel), 1 serial LVDS output clock (CLKOUT), and 1 frame-alignment clock (FRAME). The ADC clock input (CLKIN) or sample clock is multiplied by 6 to determine the serial LVDS output clock (CLKOUT). Serial data on each 12-bit channel is clocked on both the rising and falling edges of CLKOUT. The rising edge of the frame-alignment clock (FRAME) corresponds to the first bit of the 12-bit serial data stream on each of the eight channels.

Implementing an octal 12-bit, 50Msps ADC with parallel CMOS outputs would require 97 pins for the high-speed digital interface to the FPGA (approximately 5 times that of the serial LVDS interface). The significantly higher pin count for a parallel interface implementation would require significantly more FPGA I/O resources to capture the data. Larger packages for both the FPGA and the ADC would also be required, which increase the routing complexity and the number of PCB layers needed for the design.

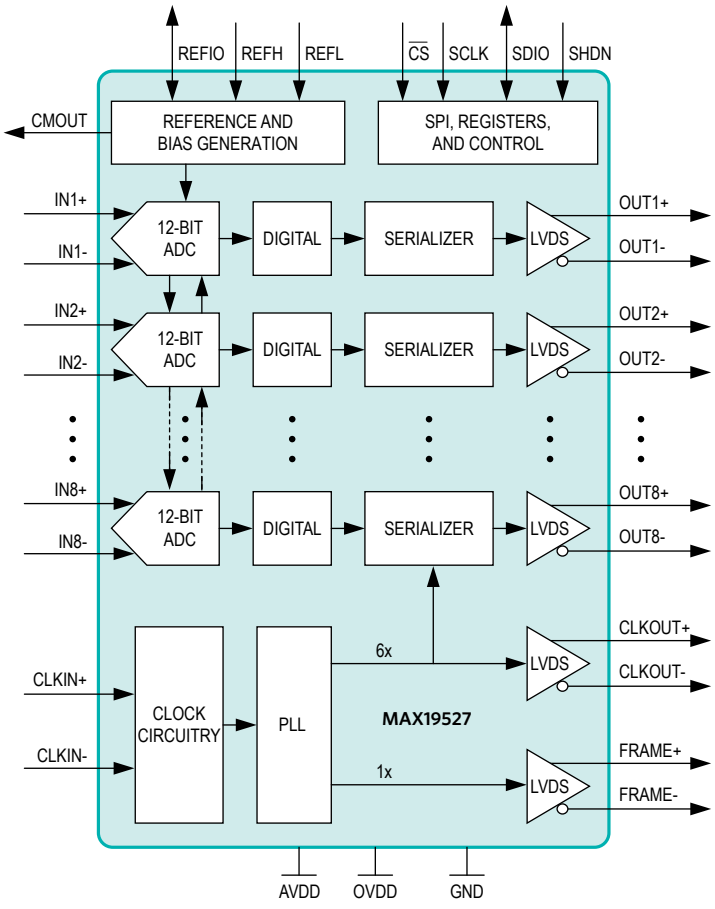


Figure 17. MAX19527 Functional Diagram

Selector Guide and Tables

High-Speed DACs and ADCs

Part	Description	Features	Benefit
MAX5879	14-bit, 2.3Gsps RF-DAC	2:1 or 4:1 multiplexed LVDS Inputs	Optimizes pin count or timing margin
		Delayed-lock loop (DLL)	Ensures data synchronization between the FPGA and the DAC
		Parity check and error flag	More easily ensures data integrity
		Data scrambling	Whitens spectral content to eliminate data-dependent spurs
		SDR, DDR data interface	Increased flexibility to interface to broader set of FPGAs
MAX109	8-bit, 2.2Gsps RF-ADC	1:4 demultiplexed LVDS outputs	Increased timing margin
		SDR, DDR, QDR data interface	Increased flexibility to interface to broader set of FPGAs
MAX19527	12-bit, octal 12-bit 50Msps ADCs with serial LVDS outputs	Serial LVDS outputs with programmable test patterns	Compact ADC/FPGA interface; ensures data timing alignment
		Output drivers with programmable current drive and internal termination	Eliminates reflections to ensure data integrity (open eye diagram)
MAX19517, MAX19507	10-/8-bit, dual 130Msps ADCs	Programmable data output timing; programmable internal termination	Simplifies high-speed FPGA/ADC interface; eliminates reflections to ensure data integrity (open eye diagram)
		Selectable data bus (dual CMOS or single multiplexed CMOS)	Trade-off I/O and interface speed to optimize FPGA resources

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