Reference Manual

Hydra Board

Revision 1.0

2014/02/01

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1. For Ensuring Safe Use

Be sure to follow the instructions given in this Manual, which are intended to prevent harm to the user and others as well as to prevent material damage.

1.1 Legend

Danger	Indicates an imminent hazardous situation which if not avoided will result in death or serious injury.
Warning	Indicates a potentially hazardous situation which if not avoided could result in death or serious injury.
Caution	Indicates a potentially hazardous situation which if not avoided may result in minor or moderate injury or in property damage.

1.2 Cautions

Danger	Make sure to use the AC adapter (if uses or required) that is specified in this Manual or included one in package. Using an AC adapter not meeting the specifications described in this Manual will cause the kit to emit heat, explode, or ignite.
Warning	Do not apply strong impacts or blows to the kit. Doing so may cause the kit to emit heat, explode, or ignite, or the equipment in the kit to fail or malfunction. This may also cause fire.
	Do not put the main unit or the AC adapter in cooking appliances such as microwave ovens, or high-pressure containers. Doing so may cause the main unit or AC adapter to emit heat, explode, ignite, or emit smoke, or its parts to break or warp.
	Do not wrap the main unit, when it is in use, with cloth or other materials that are likely to allow heat to build up inside the wrapping. This will cause heat to build up inside the wrapping, which may cause the main unit to ignite or malfunction.
	When disposing of the main unit, do not dispose of it along with general household waste. Disposing of the main unit by burning it may cause it to explode. Dispose of the main unit following applicable laws, regulations, and ordinances governing waste disposal.
	Do not use the kit in places subject to extremely high or low temperatures or severe temperature changes. Doing so may cause the kit to fail or to malfunction. Always be sure to use the kit in temperatures ranging from 5°C to 35°C and a humidity range of 0% to 85%.
	Do not pull out the power supply cable with excessive force or place heavy items on it. Do not damage, break, bundle, or tamper with the power supply cable. Damage to the power supply cable may cause a short circuit resulting in fire or accidents involving electric shock.
	Do not unplug the power plug with wet or moist hands. This may cause injuries or equipment malfunctions or failures due to electric shock.
	Plug the power plug securely into the outlet. If the power plug is not securely plugged into the outlet, it may cause accidents involving electric shock or fire due to emitted heat.

Warning	Do not connect multiple electrical cords to a single socket or connect an AC adapter to an outlet that is not rated for the specified voltage. Doing so may cause the equipment to malfunction or fail, or lead to accidents involving electric shock or fire due to emitted heat.
	Regularly remove any dust that has accumulated on the power plug and around the outlet (socket). Do not use a power plug upon which dust has accumulated because doing so will lead to insulation failure due to moisture, which may lead to fire. Remove any dust on the power plug and around the outlet with a dry cloth.
	Do not place any containers such as cups or vases filled with water or other liquid on this Board. If this Board is exposed to water or other liquids, it may cause the Board to malfunction or lead to accidents involving electric shock. If water or other liquid has been spilled on this Board, immediately stop using the Board, turn off the power, and unplug the power plug.
Caution	Do not place the kit on unstable or slanted surfaces. Doing so may cause injuries or cause this Board to malfunction if the Board should fall.
	Do not attempt to use or leave the kit in places subject to strong direct sunlight or other places subject to high temperatures, such as in cars during hot weather. Doing so may cause the kit to emit heat, break, ignite, lose control, warp, or malfunction. Also, some parts of the equipment may emit heat, causing burn injuries.
	Unplug the power supply cable when carrying out maintenance of devices in which the main unit is embedded. Failure to do so may lead to accidents involving electric shock.
	Do not place this Board in locations where excessive force may be applied to the Board. Doing so may cause the PC board to warp, leading to breakage of the PC board, loss of parts, or malfunctioning of parts.
	When using the kit together with expansion boards or other peripheral devices, be sure to carefully read each of the manuals for them and to use them correctly. The Manufacturer does not guarantee the operation of specific expansion boards or peripheral devices when used in conjunction with this Board unless they are specifically mentioned in this Manual or their successful operation with this Board has been confirmed in separate documents.
	Do not disassemble, dismantle, modify, alter, or recycle parts unless they are clearly described as customizable in this Manual. Although this kit is customizable, if parts not specified in this Manual as customizable are modified in any way, overall product operation cannot be guaranteed. Please consult with the Manufacturer beforehand if you wish to customize or modify any parts that are not described in this Manual as customizable.

1.3 Developer Information

This Hydra Board is developed by Altima Corporation. Please contact us through the following web site if you have any inquires.

Altima Corporation
1-5-5, Shin-Yokohama, Kouhoku-ku, Yokohama, 222-8563 JAPAN
http://www.m-pression.com/contact

1.4 Inquiries

In case you have any inquiries about the use this product, please contact your local Macnica company or make inquiries through the contact form in the following web site:
http://www.m-pression.com/contact

Macnica companies:

- China & HK: Cytech Technology http://www.cytech.com/
- ASEAN & India: Cytech Global http://www.cytechglobal.com/
- Taiwan: Galaxy Far East Corp. http://www.gfec.com.tw/
- North America: Macnica Americas http://www.macnica-na.com/
- Brazil: Macnica DHW http://www.macnicadhw.com.br/en/
- Japan: Altima http://www.altima.co.jp
  Elsena http://www.elsena.co.jp

2.Important Information

READ FIRST:

- ***Be sure to READ*** this Reference Manual carefully before using this product.
- ***KEEP*** the Reference Manual in a safe place together with the product for future reference.
- ***READ*** this Reference Manual carefully to use this product properly.

Purpose of the Product:

- The purpose of this product is to support the development of Altera Cyclone® V GX.

For Users of This Product:

- Please read this manual carefully and follow the instructions when using this product. Use of this product requires a basic knowledge of electric circuits, logic circuits, and FPGAs.

Precautions to be Taken when Using This Product:

- This product is a development support device for use in your design development support and evaluation stages. When you start mass production after completing design, be sure to decide at your own responsibility whether it can be put to practical use by performing an integration test, evaluation, or some other experiment.
- In no event shall Altima Corp. be liable for any consequence arising from the use of this product, except in cases of intentional or gross negligence on the part of Altima Corp.
- Altima Corp. cannot anticipate every possible circumstance that might involve a potential hazard. The warnings in this Reference Manual and on the product are therefore not all-inclusive. The user is therefore responsible for the safe use of the product at the user's own responsibility.
- This product is to be used for design and development in the evaluation stage. You cannot install the Hydra Board in your product for mass-production use.
- Compatibility with all LAN interfaces is not guaranteed.
- This product does not guarantee device functionality.
- Normal operation after any remodeling of this product by the customer is not guaranteed.
- This product uses lead-free components.
- Generally, the system names and product names listed in this manual are trademarks or registered trademarks of their respective makers.

Improvement Policy:

- Altima Corp. pursues a policy of continuous improvement in the design, performance, and safety of this product. Altima Corp. reserves the right to change, wholly or partially, the specifications, design, reference manual, and other documentation for this product at any time without notice.

Scope of Warranty:

- After you have opened the package, check that it contains all of the items listed and that they are all free of damage. If any of the items are missing or there is any visible damage please contact the company within 30 days of purchase for delivery, Altima Corp offers exchange of this product free of charge only in the event of initial failure. Altima Corp. cannot accept exchange of this product in cases in which failure is due to one of the following reasons:
  (1) Misuse, abuse of the product or use under abnormal conditions
  (2) Remodeling or repair
  (3) A fire or earthquake, or dropping of the product or any other accidents

Figures:

- Some of the figures listed in this Reference Manual may differ from the actual system you develop.

3. Package Components

Before using this product, please make sure that all components listed below are included in the package.

Hydra Board : 1pc	
AC adapter (Output: 12 V/4.0 A) : 1pc	
Bracket : 1pc	
Spacer : 5sets	
Packing List/Directions : 1pc	
Please download the manual and schematics listed on the right from the URL specified in the Packing List/Directions.	- Getting Started - This Reference Manual - Hydra Board schematics

When you open the package, please confirm that all of the above components are included and that none are broken or damaged. If any component is missing, or if there is any visible breakage, please contact our sales representative within 30 days of the package's arrival.

4. Functions and Features of the Hydra Board

4.1 Main Features of the Hydra Board

The Hydra FPGA development kit for car infotainment is an I/O companion board for R-Car H2, the second-generation car infotainment SoC manufactured by Renesas Electronics Corporation.
This development kit has an Altera Cyclone V GX automotive temperature grade FPGA, which enables optimal performance and low power consumption at a minimal system cost, and provides a scalable platform that complements the interface and functionality of car infotainment SoC.
In addition, by using a video interface cable, LVDS daughter card, and configuration board that can be connected to a board equipped with Renesas R-Car H2, this kit allows the user to expand video input and verify various interfaces.
Moreover, evaluation of FPGAs can be performed using only this development kit.

4.2 Basic Specifications of the Hydra Board

The product specifications of this Board are as follows.

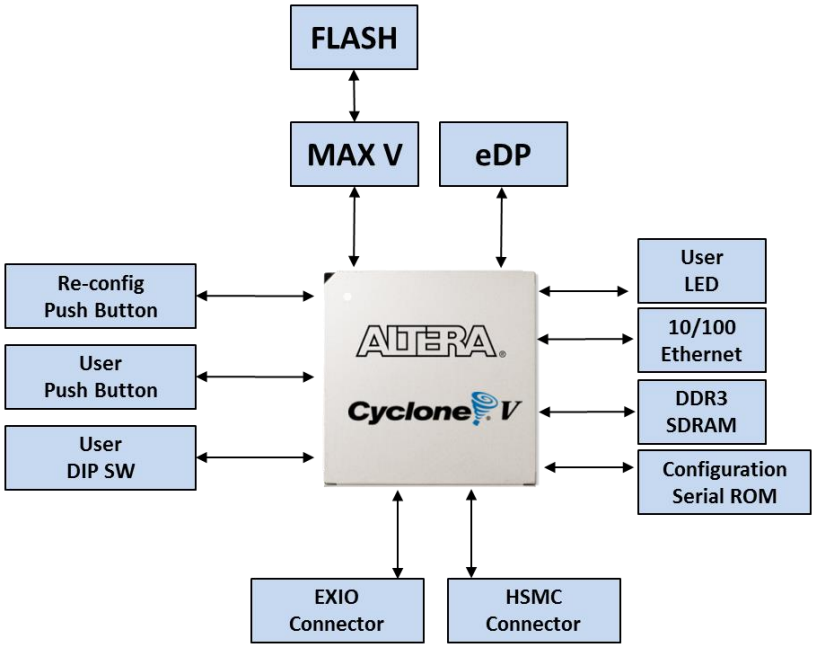
Figure 4-2-1. Main Components

	Maker	Description	Component Name
FPGA	Altera		5CGXFC7C6U19A7N
MAX® V CPLD	Altera	PFL configuration	5M1270ZT144A5N
Serial ROM	Micron	Configuration ROM (8 MByte)	N25Q064A13ESFA0F
DDR-SDRAM	Micron	DDR3-800 (128 MByte × 2)	MT41J64M16JT-15E IT:G
Flash ROM	Micron	Micron NOR Flash (32 MByte)	M29W128GH70N3
Ethernet	TI	10/100 Mbps Ethernet PHY	DP83848HSQ/NOPB
Connectors	Hoshiden	DisplayPort connector (optional)	TCX3250-010187
	Samtec	HSMC	ASP-122953-01
	Samtec	EXIO	QSE-060-01-F-D-A

4.3 Block Diagram

Figure 4-3-1 shows the block diagram of the Hydra Board.

Figure 4-3-1. Hydra Board Block Diagram



4.4 Board Specifications

Table 4.4.1 Board Specifications

Board Size	Height	Width
	115.15 mm	167.65mm
Board Thickness	1.6mm	
Layer number	8 Layers	

5. Hydra Hardware Specifications

5.1 Hydra Board Layout

5.1.1 Hydra Board Main Component Layout

Figure 5.1.1 shows the layout of the connectors used on this Board.

Figure 5-1-1 Hydra Board Main Components

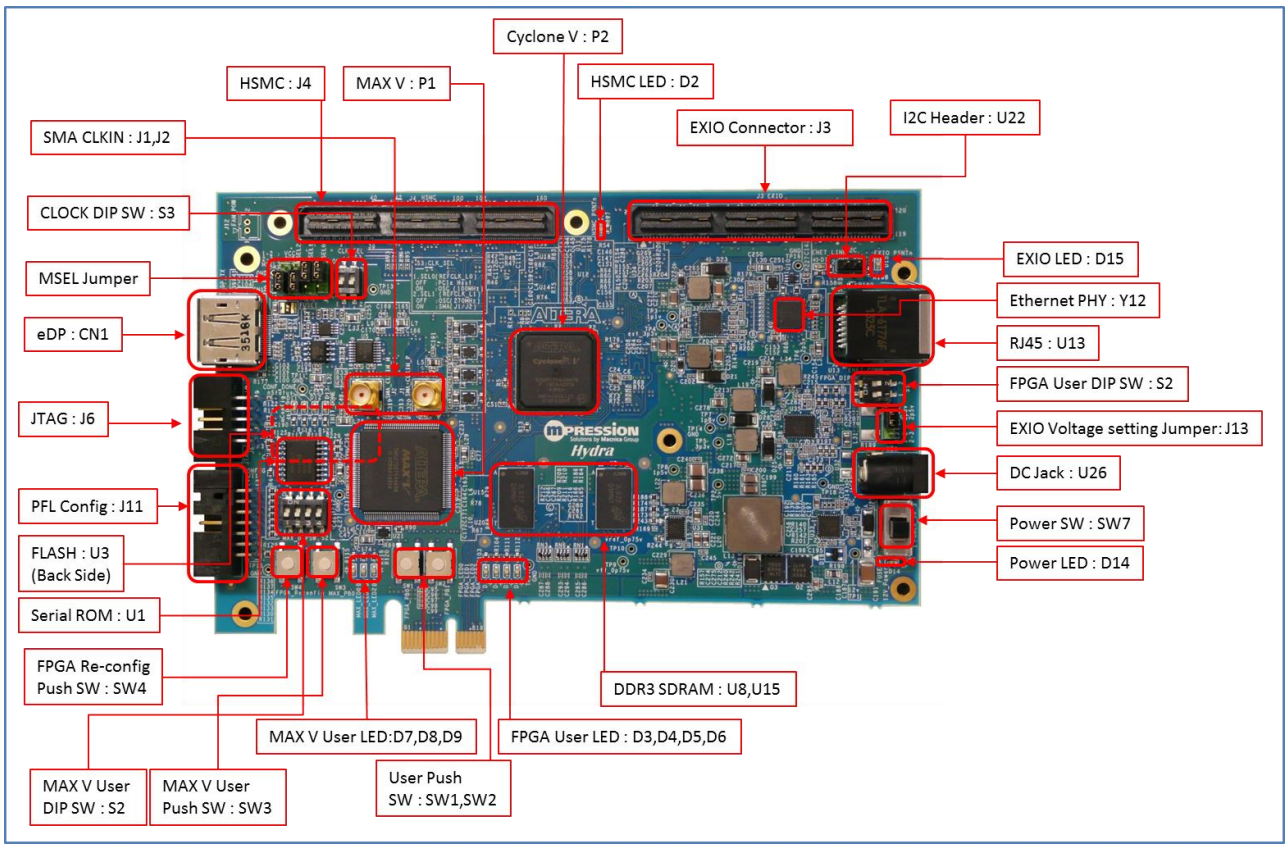


Table 5-1-1 Main Component List

Component No.	Type	Description
FPGA,CPLD		
P2	FPGA	Cyclone V, 5CGXFC7C6U19A7N
P1	CPLD	MAX V, 5M1270ZT144A5N

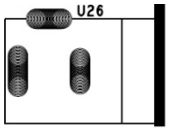
Component No.	Type	Description
J6	JTAG config header	
J11	PFL config header	
J13	EXIO voltage-setting jumper	1-2 short: 3.3 V; 2-3 short: 2.5 V
SW4	FPGA Refconfig SW	
D1	Ethernet Link Led	Lights up when an Ethernet PHY link is established.
D2	HSMC LED	Lights up when the daughter board is connected to the HSMC connector.
D10	FPGA nConfig LED	
D11	FPGA nStatus LED	
D12	FPGA CONF _DONE LED	
D13	FPGA INIT_DONE LED	
D15	EXIO LED	Lights up when a cable or daughter board is connected to the EXIO connector.
General-purpose User I/O		
SW1, SW2	FPGA User Push SW	
SW3	MAX V Uset Push SW	
S1	FPGA DIP SW	
S2	MAX V DIP SW	
D7,D8,D9	MAX V User LED	
D3,D4,D5,D6	FPGA User LED	
Communication Port		
J1	SMA/CLK_IN_P	
J2	SMA/CLK_IN_N	
J3	EXIO	120 pin
J4	HSMC	160 pin
SW7	Power SW	
D14	Power LED	12 V input
CN1	eDP	DisplayPort specification, eDP signals
U1	Serial ROM	For an 8-MByte Active Serial configuration
U3	FLASH	Connected to 32-MByte MAX V
U8,U9	DDR3-SDRAM	256 MBytes, 16 bits x2
U13	Ethernet RJ45	
U22	I2C header	
U26	DC Jack	
U12	Ethernet PHY	10/100 Mbps DP83848HSQ/NOPB

5.2 Connector Pin Assignment

Figure 5.1.1 shows the layout of the connectors on this Board.

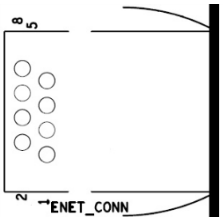
01. U35 (DC Jack)

Pin#	Pin Name	Pin#	Pin Name
1	12V	2	GND
3	GND		



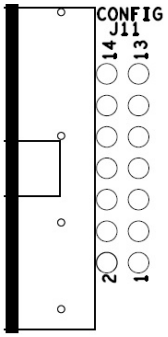
02. U13 (RJ45)

Pin#	Pin Name	Pin#	Pin Name
1	TD+	2	TD-
3	CTT	4	RD+
5	RD-	6	CTR
7	NC	8	GND
9	FG1	10	G2
11	GND_TAB	12	GND_TAB



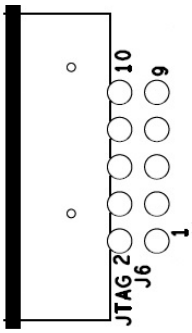
03. J11 (PFL Connector)

Pin#	Pin Name	Pin#	Pin Name
1	FPGA_DCLK	2	GND
3	CONFIG_PIN3	4	FPGA_nCONFIG
5	FPGA_nSTATUS	6	FPGA_CONF_DONE
7	FPGA_DATA0	8	FPGA_DATA1
9	FPGA_DATA2	10	FPGA_DATA0
11	FPGA_DATA4	12	FPGA_DATA3
13	FPGA_DATA6	14	FPGA_DATA0



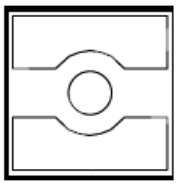
04. J6 (JTAG Connector for FPGA)

Pin#	Pin Name	Pin#	Pin Name
1	JTAG_TCK	2	GND
3	JTAG_MAX_TDO	4	2.5V
5	JTAG_TMS	6	NC
7	NC	8	NC
9	JTAG_TDI	10	GND



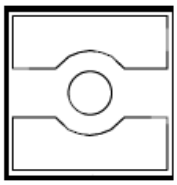
05. J1 (SMA CLKIN_P)

Pin#	Pin Name	Pin#	Pin Name
1	SMA_CLK_IN	2	
3		4	
5			

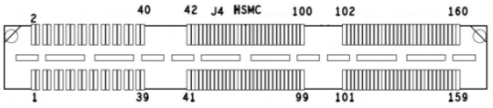


06. J2 (SMA CLKIN_N)

Pin#	Pin Name	Pin#	Pin Name
1	SMA_CLK_IN	2	
3		4	
5			

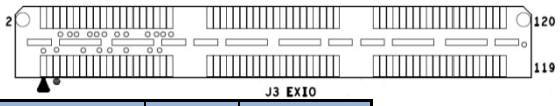


07. J8 (HSMC Connector)



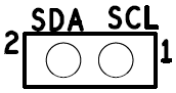
Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1		2		81	3.3V	82	12V
3		4		83	HSMC_TX_D_P5	84	HSMC_RX_D_P5
5		6		85	HSMC_TX_D_N5	86	HSMC_RX_D_N5
7		8		87	3.3V	88	12V
9		10		89	HSMC_TX_D_P6	90	HSMC_RX_D_P6
11		12		91	HSMC_TX_D_N6	92	HSMC_RX_D_N6
13		14		93	3.3V	94	12V
15		16		95	HSMC_CLK_OUT_P1	96	HSMC_CLK_IN_P
17		18		97	HSMC_CLK_OUT_N1	98	HSMC_CLK_IN_N
19		20		99	3.3V	100	12V
21		22		101	HSMC_TX_D_P7	102	HSMC_RX_D_P7
23		24		103	HSMC_TX_D_N7	104	HSMC_RX_D_N7
25	HSMC_TX_P1	26	HSMC_RX_P1	105	3.3V	106	12V
27	HSMC_TX_N1	28	HSMC_RX_N1	107	HSMC_TX_D_P8	108	HSMC_RX_D_P8
29	HSMC_TX_P0	30	HSMC_RX_P0	109	HSMC_TX_D_N8	110	HSMC_RX_D_N8
31	HSMC_TX_N0	32	HSMC_RX_N0	111	3.3V	112	12V
33	HSMC_SDA	34	HSMC_SCL	113	HSMC_TX_D_P9	114	HSMC_RX_D_P9
35		36		115	HSMC_TX_D_N9	116	HSMC_RX_D_N9
37		38		117	3.3V	118	12V
39	HSMC_CLK_OUT0	40	HSMC_CLK_IN0	119	HSMC_TX_D_P10	120	HSMC_RX_D_P10
41	HSMC_D0	42	HSMC_D1	121	HSMC_TX_D_N10	122	HSMC_RX_D_N10
43	HSMC_D2	44	HSMC_D3	123	3.3V	124	12V
45	3.3V	46	12V	125	HSMC_TX_D_P11	126	HSMC_RX_D_P11
47	HSMC_D4	48	HSMC_D5	127	HSMC_TX_D_N11	128	HSMC_RX_D_N11
49	HSMC_D6	50	HSMC_D7	129	3.3V	130	12V
51	3.3V	52	12V	131	HSMC_TX_D_P12	132	HSMC_RX_D_P12
53	HSMC_TX_D_P0	54	HSMC_RX_D_P0	133	HSMC_TX_D_N	134	HSMC_RX_D_N12
55	HSMC_TX_D_N0	56	HSMC_RX_D_N0	135	3.3V	136	12V
57	3.3V	58	12V	137	HSMC_TX_D_P13	138	HSMC_RX_D_P13
59	HSMC_TX_D_P1	60	HSMC_RX_D_P1	139	HSMC_TX_D_N13	140	HSMC_RX_D_N13
61	HSMC_TX_D_N1	62	HSMC_RX_D_N1	141	3.3V	142	12V
63	3.3V	64	12V	143	HSMC_TX_D_P14	144	HSMC_RX_D_P14
65	HSMC_TX_D_P2	66	HSMC_RX_D_P2	145	HSMC_TX_D_N14	146	HSMC_RX_D_N14
67	HSMC_TX_D_N2	68	HSMC_RX_D_N2	147	3.3V	148	12V
69	3.3V	70	12V	149	HSMC_TX_D_P15	150	HSMC_RX_D_P15
71	HSMC_TX_D_P3	72	HSMC_RX_D_P3	151	HSMC_TX_D_N15	152	HSMC_RX_D_N15
73	HSMC_TX_D_N3	74	HSMC_RX_D_N3	153	3.3V	154	12V
75	3.3V	76	12V	155	HSMC_CLK_OUT_P2	156	HSMC_CLK_IN_P25
77	HSMC_TX_D_P4	78	HSMC_RX_D_P4	157	HSMC_CLK_OUT_N2	158	HSMC_CLK_IN_N25
79	HSMC_TX_D_N4	80	HSMC_RX_D_N4	159	3.3V	160	12V

08. J8 (EXIO Connector)



Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
1	GND	2		61		62	
3	EXIO_0	4		63		64	
5	EXIO_1	6		65		66	
7	EXIO_2	8	GND	67		68	
9	EXIO_3	10	EXIO_19	69		70	
11	EXIO_4	12	EXIO_20	71	EXIO_18	72	
13	EXIO_5	14	EXIO_21	73		74	
15	EXIO_6	16	EXIO_22	75		76	
17	EXIO_7	18	EXIO_23	77		78	
19	EXIO_8	20	EXIO_24	79		80	
21	GND	22	EXIO_25	81		82	
23	EXIO_9	24	EXIO_26	83	GND	84	
25	EXIO_10	26	EXIO_27	85	EXIO_PIN85	86	
27	EXIO_11	28	EXIO_28	87		88	
29	EXIO_12	30	EXIO_29	89		90	
31	EXIO_13	32	EXIO_30	91	GND	92	
33	EXIO_14	34	EXIO_31	93		94	
35	EXIO_15	36	EXIO_32	95	GND	96	
37	EXIO_16	38	EXIO_33	97		98	
39	EXIO_17	40		99		100	
41		42		101		102	
43		44		103		104	
45		46		105		106	
47		48		107	GND	108	GND
49		50		109		110	
51		52		111		112	
53		54		113		114	I2C_SCL
55		56		115		116	I2C_SDA
57		58	EXIO_34	117		118	LED
59		60	EXIO_35	119		120	

09. I2C Pin Header



Pin#	Pin Name	Pin#	Pin Name
1	I2C_SCL	2	I2C_SDA

5.3 JTAG Configuration

This section describes the configurations supported by the Hydra Board. The Hydra Board supports the following three configurations.

- JTAG Configuration
  - JTAG configuration is supported by Quartus® II Programmer via Altera USB-Blaster using a JTAG header connection.
- PFL Configuration Mode
  - An FPGA is configured via MAX V by storing configuration data in Flash memory connected to MAX V.
- AS Configuration Mode
  - Configuration data is stored in Micron serial ROM via an FPGA.
  - Started from Micron serial ROM.

Table 5-3-2 JTAG Pin Assignment

Pin#	Pin Name	I/O Standard	FPGA Pin#	MAX V Pin#	Description
1	JTAG_TCK	3.3V	V5	35	Connected to FPGA and MAX
3	JTAG_MAX_TDO	-	-	38	Data output from MAX
5	JTAG_TMS	3.3V	R4	33	Connected to FPGA and MAX
7	NC	-	-	-	-
9	JTAG_TDI	3.3V	P5		Data input to FPGA
2	GND	-	-	-	
4	2.5V	-	-	-	
6	NC	-	-	-	
8	NC	-	-	-	
10	GND	-	-	-	

5.4 Status Display LEDs

The Hydra Board has status display LEDs; Table 5-4-1 describes the meanings that they indicate.

Table 5-4-1. Status LEDs

Board Reference Design	I/O Standard	Description
D1		Ethernet link check LED
D2	3.3V	LED used when an HSMC daughter board is installed
D3-D6		4× general-purpose LED (FPGA LED0-LED3)
D7-D9		MAX LED
D10	3.3V	FPGA nCONFIG check LED
D11	3.3V	FPGA nSTATUS check LED
D12	3.3V	FPGA CONF_DONE check LED
D13	3.3V	FPGA INIT_DONE check LED
D14		+12 V power supply LED
D15	3.3V	LED used when connected to the EXIO connector

5.5 Switches and Jumper Pins

- JTAG Configuration (MSEL) Jumper Pins
- Configuration Push Button

5.5.1 JTAG Configuration (MSEL) Jumper Pins

JTAG configuration is performed with jumpers, MSEL[3], MSEL[2], MSEL[1], and MSE[0]. Table 5-4-1 lists the configuration details.

Table 5-5-1. JTAG Configuration Jumper Pins

MSEL[4:0]	FPP(X8)/AS(X1, x4)	Compression	Security	Delay
10100	FPP	Disabled	Disabled	Fast
11000	FPP	Disabled	Disabled	Standard
10101	FPP	Disabled	Enabled	Fast
11001	FPP	Disabled	Enabled	Standard
10110	FPP	Enabled	-	Fast
11010	FPP	Enabled	-	Standard
10010	AS	-	-	Fast
10011	AS	-	-	Standard
MSEL[4] is fixed at 1. MSEL[3:0] can be configured.				

5.5.2 Configuration Push Button

The SW4 is used as the push button for FPGA reconfiguration.

Table 5-5-5. Reconfiguration Push Button

Board Reference Design	Schematic Pin Name	I/O Standard	Cyclone V Pin#	Description
SW4	FPGA_nCONFIG	3.3-V	A4	Reconfiguration switch. Press this switch when an FPGA needs to be reconfigured.

5.6 Clock

5.6.1 On-board Oscillators

The Hydra Board has oscillators with frequencies of 27, 50, 100, and 270 MHz. The table below lists the on-board oscillators.

Table 5-6-1. On-board Oscillators

Source	Pin Name	Frequency	I/O Standard	Connection Destination
U14	CLK50M	50 MHz	2.5V	Cyclone V: G13
U15	CLK27M	27 MHz	1.5V	Cyclone V: P9
U16	REFCLK_L0	100 MHz	3.3V	Switched with PCIe clock by CLK_SEL DIP SW REFCLK_L0_P Cyclone V:V4 REFCLK_L0_N Cyclone V : U4
U18	CLK50M_DDR	50 MHz	1.8V	Cyclone V:U13
U19	REFCLK_L1	270 MHz	3.3V	Switched with SMA clock by CLK_SEL DIP SW REFCLK_L1_P Cyclone V:F5 REFCLK_L1_N Cyclone V:G4
U20	CLK100M	100 MHz	1.5V	Cyclone V:R10
U21	MAX_CLK100	100 MHz	3.3V	MAX V:91

5.6.2 External Clock Input

The Hydra Board has the following external clock inputs.

Source	Pin Name	I/O Standard	Connection Destination
HSMC	HSMC_CLK_IN0	2.5V	Cyclone V:G10
HSMC	HSMC_CLK_IN_P1	2.5V	Cyclone V:K7
	HSMC_CLK_IN_N1	2.5V	Cyclone V:J7
HSMC	HSMC_CLK_IN_P2	2.5V	Cyclone V:H10
	HSMC_CLK_IN_N2	2.5V	Cyclone V:G11
PCIe	REFCLK_L0	3.3V	Switched with SMA input clock by CLK_SEL DIP SW REFCLK_L0_P Cyclone V:V4 REFCLK_L0_N Cyclone V:U4
SMA Pin	REFCLK_L1	3.3V	Switched with SMA input clock by CLK_SEL DIP SW REFCLK_L1_P Cyclone V:F5 REFCLK_L1_N Cyclone V:G4
HSMC	HSMC_CLK_OUT0	2.5V	Cyclone V:F10
HSMC	HSMC_CLK_OUT_P1	2.5V	Cyclone V:A8
	HSMC_CLK_OUT_N1	2.5V	Cyclone V:A7
HSMC	HSMC_CLK_OUT_P2	2.5V	Cyclone V:A8
	HSMC_CLK_OUT_N2	2.5V	Cyclone V:A7

5.6.3 Clock Input Switching DIP Switches

The Hydra Board has DIP switches to switch between clock input sources. Switch functions are as follows.

CLK_SEL0	ON	REFCLK_L0 uses the PCIe host.
	OFF	REFCLK_L0 uses an on-board oscillator (U16).
CLK_SEL1	ON	REFCLK_L0 uses an on-board oscillator (U19).
	OFF	REFCLK_L0 uses SMA input (J1/J2).

5.7 General-purpose I/O

5.7.1 User-defined Push Buttons

The Hydra Board has user-defined push buttons. The SW1 and SW2 board reference design switches can be used as user-defined push buttons.
Table 5-7-1 lists the push buttons connected to the Hydra Board.

Table 5-7-1. Pin Assignment List for User-defined Push Buttons

Board Reference Design	Pin Name	I/O Standard	FPGA Pin No.	Description
SW1	PUSHSW_N0	3.3V	R22	User-defined push buttons
SW2	PUSHSW_N1	3.3V	W20	

5.7.2 User-defined DIP Switches

The Hydra Board has user-defined DIP switches. When a switch is on, logical low(0) is input to the FPGA, while logical high(1) is input when a switch is off.
Table 5-7-2 lists the Pin Names and pin numbers of the user-defined DIP switches.

Table 5-7-2. User-defined DIP Switch List

Board Reference Design	Pin Name	I/O Standard	FPGA Pin No.	Description
S1-SW1	DIPSW0	3.3 V	T15	User-defined DIP switches
S1-SW2	DIPSW1	3.3 V	R9	

5.7.3 User-defined LEDs

The Hydra Board has user-defined LEDs. The D3 to D6 board reference design LEDs can be used as user-defined LEDs. The LEDs are active on low, and they light up when the FPGA outputs a low(0) signal and turn off when it outputs a high(1) signal. Table 5-6-3 lists the LED Pin Names, I/O standard, and pin numbers.
Table 5-7-3 shows pin assignment information for user-defined LEDs.

Table 5-7-3. User-defined LED List

Board Reference Design	Pin Name	I/O Standard	FPGA Pin No.	Description
D3	LED_N0	3.3 V	G18	User-defined LEDs
D4	LED_N1	3.3 V	R16	
D5	LED_N2	3.3 V	U22	
D6	LED_N3	3.3 V	F14	

5.7.4 User-defined Push Button for MAX V

The Hydra Board has user-defined push buttons for MAX V. The SW3 board reference design switch can be used as a user-defined push button.
Table 5-7-4 lists the push button connected to the Hydra Board.

Table 5-7-4. Pin Assignment List for User-defined Push Button

Board Reference Design	Pin Name	I/O Standard	MAX V Pin No.	Description
SW3	MAX_PUSH_SW0	3.3 V	88	User-defined push buttons

5.7.5 User-defined DIP Switches for MAX V

The Hydra Board has user-defined DIP switches for MAX V. When a switch is on, logical low(0) is input to MAX V, while logical high(1) is input when a switch is off.
Table 5-7-5 lists the Pin Names and pin numbers of user-defined DIP switches.

Table 5-7-5 Pin Names and Pin Numbers of User-defined DIP Switches

Pin Name	I/O Standard	MAX V Pin No.	Description
MAX_DIP_SW0	3.3 V	77	User-defined DIP switches
MAX_DIP_SW1	3.3 V	76	
MAX_DIP_SW2	3.3 V	75	
MAX_DIP_SW3	3.3 V	74	

5.7.6 User-defined LEDs for MAX V

The Hydra Board has user-defined LEDs for MAX V. The D7 to D9 board reference design LEDs can be used as user-defined LEDs. The LEDs are active on low, and they light up when the FPGA outputs a low(0) signal and turn off when it outputs a high(1) signal. Table 5-7-6 lists the Pin Names, I/O standard, and pin numbers of the LEDs.

Table 5-7-6 shows pin assignment information for user-defined LEDs

Board Reference Design	Pin Name	I/O Standard	MAX V Pin #	Description
D7	MAX_LED_N0	3.3 V	86	User-defined LEDs
D8	MAX_LED_N1	3.3 V	85	
D9	MAX_LED_N2	3.3 V	84	

5.8 FPGA/MAX V Pin Assignment List

This section depicts pin assignment for the following connector pins and devices to the FPGA and MAX V.

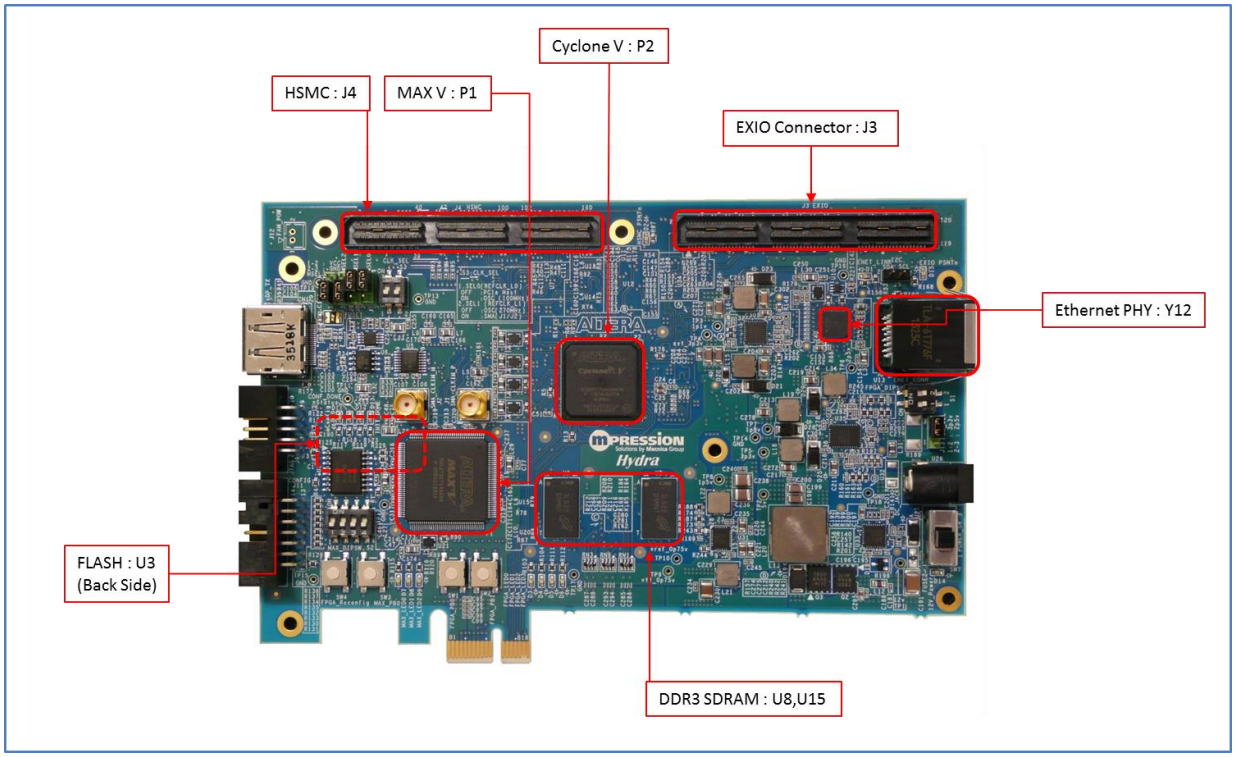


Figure 5-8 Connector and Device List

5.8.1 DDR3 SDRAM

The Hydra Board has two sticks of 667 MHz DDR3 memory (MT41J64M16JT-15EG, 128 Mbytes (64 Mwords × 16 bits)) for a total capacity of 256 Mbytes.
The data sheet for this DDR3 memory can be obtained from the following URL:
http://www.micron.com/parts/dram/ddr3-sdram/mt41j64m16jt-15e-it
Note: The URL above is subject to change without notice.
Note: The DDR3 memory mounted on the Hydra Board may be replaced with an equivalent product that satisfies the requirements for DDR3 performance.
Table 5-8-1 shows pin assignment information for the DDR3 SDRAM.

Table 5-8-1. DDR3 SDRAM Interface Pin Assignment List

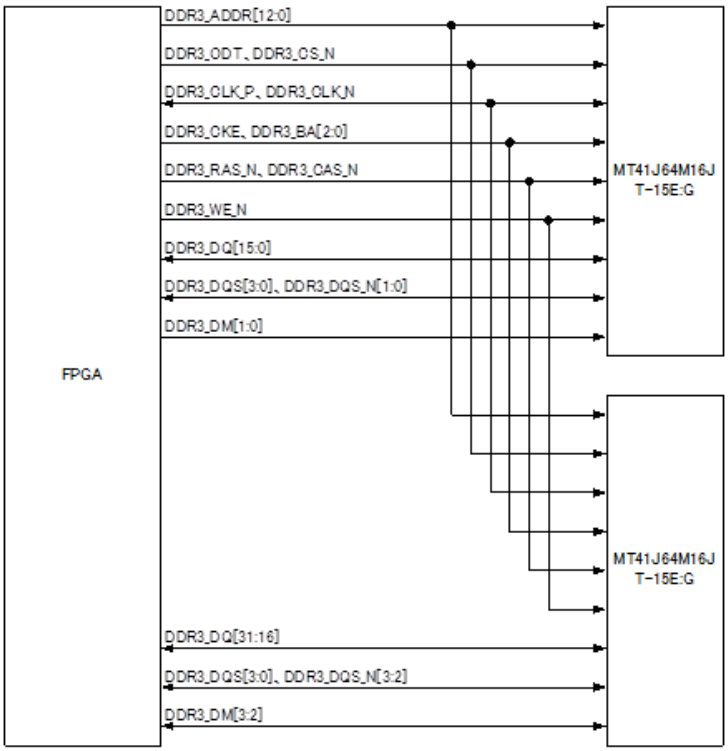
Board Reference Design (U8)	Pin Name	IO Standard	Cyclone V Pin#	Description
N3	DDR3_ADDR0	SSTL-15 Class I	AB18	Address bus
P7	DDR3_ADDR1	SSTL-15 Class I	Y12	Address bus
P3	DDR3_ADDR2	SSTL-15 Class I	Y11	Address bus
N2	DDR3_ADDR3	SSTL-15 Class I	AB13	Address bus
P8	DDR3_ADDR4	SSTL-15 Class I	AA18	Address bus
P2	DDR3_ADDR5	SSTL-15 Class I	V15	Address bus
R8	DDR3_ADDR6	SSTL-15 Class I	AB22	Address bus
R2	DDR3_ADDR7	SSTL-15 Class I	Y20	Address bus
T8	DDR3_ADDR8	SSTL-15 Class I	U8	Address bus
R3	DDR3_ADDR9	SSTL-15 Class I	T13	Address bus
L7	DDR3_ADDR10	SSTL-15 Class I	U12	Address bus
R7	DDR3_ADDR11	SSTL-15 Class I	AB16	Address bus
N7	DDR3_ADDR12	SSTL-15 Class I	V8	Address bus
M2	DDR3_BA0	SSTL-15 Class I	AB17	Bank address bus
N8	DDR3_BA1	SSTL-15 Class I	W13	Bank address bus
M3	DDR3_BA2	SSTL-15 Class I	AA9	Bank address bus
E7	DDR3_DM0	SSTL-15 Class I	Y16	Byte write mask
D3	DDR3_DM1	SSTL-15 Class I	U15	Byte write mask
L2	DDR3_CS_N	SSTL-15 Class I	R12	Chip select
K3	DDR3_CAS_N	SSTL-15 Class I	Y10	Column address select
J3	DDR3_RAS_N	SSTL-15 Class I	AA19	Low address select
L3	DDR3_WE_N	SSTL-15 Class I	V13	Write enable
T2	DDR3_RESET_N	1.5 V	W12	Reset

Board Reference Design (U8)	Pin Name	IO Standard	Cyclone V Pin#	Description
E3	DDR3_DQ0	SSTL-15 Class I	AA22	Data bus
F7	DDR3_DQ1	SSTL-15 Class I	AA17	Data bus
F2	DDR3_DQ2	SSTL-15 Class I	W22	Data bus
F8	DDR3_DQ3	SSTL-15 Class I	Y17	Data bus
H3	DDR3_DQ4	SSTL-15 Class I	Y21	Data bus
H8	DDR3_DQ5	SSTL-15 Class I	Y22	Data bus
G2	DDR3_DQ6	SSTL-15 Class I	W21	Data bus
H7	DDR3_DQ7	SSTL-15 Class I	W18	Data bus
D7	DDR3_DQ8	SSTL-15 Class I	W14	Data bus
C3	DDR3_DQ9	SSTL-15 Class I	AA15	Data bus
C8	DDR3_DQ10	SSTL-15 Class I	AA20	Data bus
C2	DDR3_DQ11	SSTL-15 Class I	AB21	Data bus
A7	DDR3_DQ12	SSTL-15 Class I	Y19	Data bus
A2	DDR3_DQ13	SSTL-15 Class I	Y14	Data bus
B8	DDR3_DQ14	SSTL-15 Class I	AB20	Data bus
A3	DDR3_DQ15	SSTL-15 Class I	Y15	Data bus
C7	DDR3_DQS_P0	Differential 1.5-V SSTL Class I	U17	Data strobe P
B7	DDR3_DQS_N0	Differential 1.5-V SSTL Class I	U16	Data strobe N
F3	DDR3_DQS_P1	Differential 1.5-V SSTL Class I	R14	Data strobe P
G3	DDR3_DQS_N1	Differential 1.5-V SSTL Class I	P14	Data strobe N
J7	DDR3_CLK_P	Differential 1.5-V SSTL Class I	W17	Differential clock
K7	DDR3_CLK_N	Differential 1.5-V SSTL Class I	W16	Differential clock
K9	DDR3_CKE	SSTL-15 Class I	AB7	Clock enable

Board Reference Design (U15)	Pin Name	IO Standard	Cyclone V Pin#	Description
N3	DDR3_ADDR0	SSTL-15 Class I	AB18	Address bus
P7	DDR3_ADDR1	SSTL-15 Class I	Y12	Address bus
P3	DDR3_ADDR2	SSTL-15 Class I	Y11	Address bus
N2	DDR3_ADDR3	SSTL-15 Class I	AB13	Address bus
P8	DDR3_ADDR4	SSTL-15 Class I	AA18	Address bus
P2	DDR3_ADDR5	SSTL-15 Class I	V15	Address bus
R8	DDR3_ADDR6	SSTL-15 Class I	AB22	Address bus
R2	DDR3_ADDR7	SSTL-15 Class I	Y20	Address bus
T8	DDR3_ADDR8	SSTL-15 Class I	U8	Address bus
R3	DDR3_ADDR9	SSTL-15 Class I	T13	Address bus
L7	DDR3_ADDR10	SSTL-15 Class I	U12	Address bus
R7	DDR3_ADDR11	SSTL-15 Class I	AB16	Address bus
N7	DDR3_ADDR12	SSTL-15 Class I	V8	Address bus
M2	DDR3_BA0	SSTL-15 Class I	AB17	Bank address bus
N8	DDR3_BA1	SSTL-15 Class I	W13	Bank address bus
M3	DDR3_BA2	SSTL-15 Class I	AA9	Bank address bus
E7	DDR3_DM2	SSTL-15 Class I	Y9	Byte write mask
D3	DDR3_DM3	SSTL-15 Class I	M8	Byte write mask
L2	DDR3_CS_N	SSTL-15 Class I	R12	Chip select
K3	DDR3_CAS_N	SSTL-15 Class I	AA19	Column address select
J3	DDR3_RAS_N	SSTL-15 Class I	Y10	Low address select
L3	DDR3_WE_N	SSTL-15 Class I	V13	Write enable
T2	DDR3_RESET_N	1.5V	W12	Reset
K1	DDR3_ODT	SSTL-15 Class I	AB15	On-die termination enable
E3	DDR3_DQ16	SSTL-15 Class I	U11	Data bus
F7	DDR3_DQ17	SSTL-15 Class I	R11	Data bus
F2	DDR3_DQ18	SSTL-15 Class I	W11	Data bus
F8	DDR3_DQ19	SSTL-15 Class I	P12	Data bus
H3	DDR3_DQ20	SSTL-15 Class I	AB10	Data bus
H8	DDR3_DQ21	SSTL-15 Class I	U10	Data bus
G2	DDR3_DQ22	SSTL-15 Class I	AB11	Data bus
H7	DDR3_DQ23	SSTL-15 Class I	AA10	Data bus
D7	DDR3_DQ24	SSTL-15 Class I	AA8	Data bus
C3	DDR3_DQ25	SSTL-15 Class I	AA7	Data bus

Board Reference Design (U8)	Pin Name	IO Standard	Cyclone V Pin#	Description
C2	DDR3_DQ27	SSTL-15 Class I	Y7	Data bus
A7	DDR3_DQ28	SSTL-15 Class I	W8	Data bus
A2	DDR3_DQ29	SSTL-15 Class I	W7	Data bus
B8	DDR3_DQ30	SSTL-15 Class I	AB8	Data bus
A3	DDR3_DQ31	SSTL-15 Class I	N8	Data bus
C7	DDR3_DQS_P2	Differential 1.5-V SSTL Class I	M10	Data strobe P
B7	DDR3_DQS_N2	Differential 1.5-V SSTL Class I	L9	Data strobe N
F3	DDR3_DQS_P3	Differential 1.5-V SSTL Class I	N10	Data strobe P
G3	DDR3_DQS_N3	Differential 1.5-V SSTL Class I	N9	Data strobe N
J7	DDR3_CLK_P	Differential 1.5-V SSTL Class I	W17	Differential clock
K7	DDR3_CLK_N	Differential 1.5-V SSTL Class I	W16	Differential clock
K9	DDR3_CKE	SSTL-15 Class I	AB7	Clock enable

The FPGA and DDR3 are connected on the Board as follows.



5.8.2 NOR FLASH

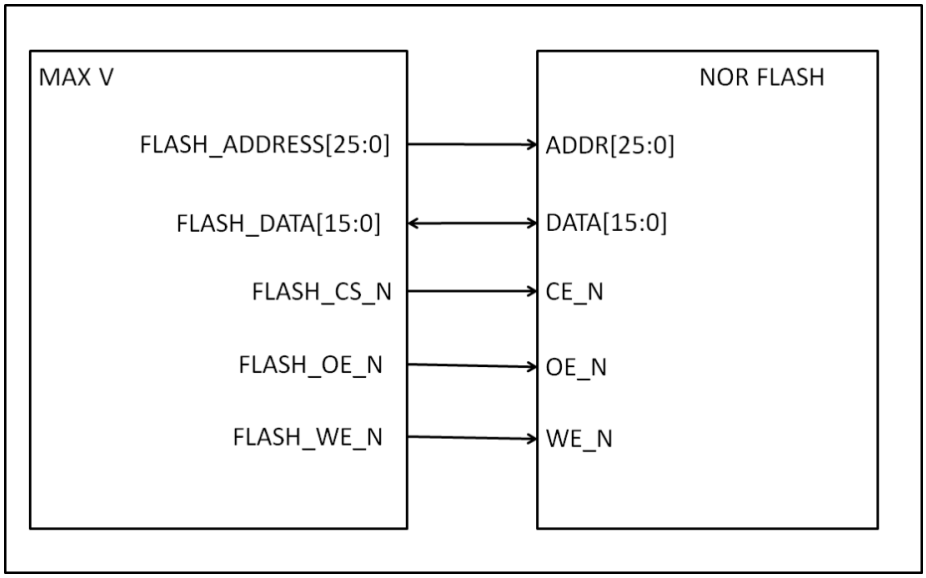
The Hydra Board has a 256 Mbit, 16-bit width Flash ROM (M29W128GH70N3).
This Flash is connected with MAX V.
The data sheet for the Flash ROM can be obtained from the following URL.
http://www.micron.com/parts/nor-flash/parallel-nor-flash/m29w128gh70n3e?source=ps
Note: The URL above is subject to change without notice.

Table 5-8-2 shows pin assignment information for NOR Flash.

Table 5-8-2. NOR Flash Pin Assignment List

Board Reference Design	Pin Name	MAX V Pin#	Board Reference Design	Pin Name	MAX V Pin#
31	FLASH_ADDRESS0	72	1	FLASH_ADDRESS23	137
26	FLASH_ADDRESS1	109	56	FLASH_ADDRESS24	45
25	FLASH_ADDRESS2	110	55	FLASH_ADDRESS25	48
24	FLASH_ADDRESS3	111	35	FLASH_DATA 0	69
23	FLASH_ADDRESS4	112	37	FLASH_DATA1	67
22	FLASH_ADDRESS5	113	39	FLASH_DATA2	63
21	FLASH_ADDRESS6	114	41	FLASH_DATA3	61
20	FLASH_ADDRESS7	117	44	FLASH_DATA4	59
10	FLASH_ADDRESS8	124	46	FLASH_DATA5	57
9	FLASH_ADDRESS9	125	48	FLASH_DATA6	53
8	FLASH_ADDRESS10	127	50	FLASH_DATA7	51
7	FLASH_ADDRESS11	129	36	FLASH_DATA8	68
6	FLASH_ADDRESS12	130	38	FLASH_DATA9	66
5	FLASH_ADDRESS13	131	40	FLASH_DATA10	62
4	FLASH_ADDRESS14	132	42	FLASH_DATA11	60
3	FLASH_ADDRESS15	133	45	FLASH_DATA12	58
54	FLASH_ADDRESS16	49	47	FLASH_DATA13	55
19	FLASH_ADDRESS17	118	49	FLASH_DATA14	52
18	FLASH_ADDRESS18	119	51	FLASH_DATA15	50
11	FLASH_ADDRESS19	123	32	FLASH_CS_N	71
12	FLASH_ADDRESS20	122	34	FLASH_OE_N	70
15	FLASH_ADDRESS21	120	13	FLASH_WE_N	121
2	FLASH_ADDRESS22	134			

The MAX V and Flash are connected on the board as follows.



5.8.3 HSMC

The Hydra Board supports the HSMC (High Speed Mezzanine Card) interface. HSMC supports 17 pairs of LVDS channels for transmitting and receiving signals as well as the SMBus. The LVDS ports can be used at the single-end 2.5-V LVCMOS level. The Hydra Board has one HSMC port located in the upper left part of the board; two transceiver channels are connected to the port.

HSMC is Altera's open standard, and the function can be expanded by connecting a daughter card to the port. For more details on the HSMC standard, visit the following URL.
http://www.altera.com/literature/ds/hsmc_spec.pdf

Table 5-8-3 shows pin assignment information for HSMC.

Table 5-8-3. HSMC Interface Pin Assignment List

Board Reference Design	Pin Name	Cyclone V Pin#	I/O Standard	Description
25	HSMC_TX_P1	D4	2.5 V	Transceiver transmission data
26	HSMC_RX_P1	C2	2.5 V	Transceiver receive data
27	HSMC_TX_N1	D3	2.5 V	Transceiver transmission data
28	HSMC_RX_N1	C1	2.5 V	Transceiver receive data
29	HSMC_TX_P0	N2	2.5 V	Transceiver transmission data
30	HSMC_RX_P0	R2	2.5 V	Transceiver receive data
31	HSMC_TX_N0	N1	2.5 V	Transceiver transmission data
32	HSMC_RX_N0	R1	2.5 V	Transceiver receive data
33	HSMC_SDA	A19	2.5 V	Serial data
34	HSMC_SCL	A20	2.5 V	Serial clock
35	-	-	-	-
36	-	-	-	-
37	-	-	-	-
38	-			
39	HSMC_CLK_OUT0	F10	2.5 V	Single-end clock output
40	HSMC_CLK_IN0	G10	2.5 V	Single-end clock input
41	HSMC_D0	T7	2.5 V	Single-end data
42	HSMC_D1	P8	2.5 V	Single-end data
43	HSMC_D2	R7	2.5 V	Single-end data
44	HSMC_D3	R5	2.5 V	Single-end data
47	HSMC_D4	R6	2.5 V	Single-end data
48	HSMC_D5	P7	2.5 V	Single-end data
49	HSMC_D6	L7	2.5 V	Single-end data
50	HSMC_D7	N6	2.5 V	Single-end data
53	HSMC_TX_D_P0	B16	2.5 V	Differential transmission data
54	HSMC_RX_D_P0	E16	2.5 V	Differential receive data

Board Reference Design	Pin Name	Cyclone V Pin#	I/O Standard	Description
55	HSMC_TX_D_N0	B15	2.5 V	Differential transmission data
56	HSMC_RX_D_N0	D17	2.5 V	Differential receive data
59	HSMC_TX_D_P1	A10	2.5 V	Differential transmission data
60	HSMC_RX_D_P1	D11	2.5 V	Differential receive data
61	HSMC_TX_D_N1	A9	2.5 V	Differential transmission data
62	HSMC_RX_D_N1	E11	2.5 V	Differential receive data
65	HSMC_TX_D_P2	B18	2.5 V	Differential transmission data
66	HSMC_RX_D_P2	F15	2.5 V	Differential receive data
67	HSMC_TX_D_N2	B17	2.5 V	Differential transmission data
68	HSMC_RX_D_N2	E14	2.5 V	Differential receive data
71	HSMC_TX_D_P3	A18	2.5 V	Differential transmission data
72	HSMC_RX_D_P3	J9	2.5 V	Differential receive data
73	HSMC_TX_D_N3	A17	2.5 V	Differential transmission data
74	HSMC_RX_D_N3	J8	2.5 V	Differential receive data
77	HSMC_TX_D_P4	B22	2.5 V	Differential transmission data
78	HSMC_RX_D_P4	H9	2.5 V	Differential receive data
79	HSMC_TX_D_N4	A22	2.5 V	Differential transmission data
80	HSMC_RX_D_N4	G8	2.5 V	Differential receive data
83	HSMC_TX_D_P5	C6	2.5 V	Differential transmission data
84	HSMC_RX_D_P5	C16	2.5 V	Differential receive data
85	HSMC_TX_D_N5	D7	2.5 V	Differential transmission data
86	HSMC_RX_D_N5	C15	2.5 V	Differential receive data
89	HSMC_TX_D_P6	E6	2.5 V	Differential transmission data
90	HSMC_RX_D_P6	H6	2.5 V	Differential receive data
91	HSMC_TX_D_N6	F7	2.5 V	Differential transmission data
92	HSMC_RX_D_N6	G6	2.5 V	Differential receive data
95	HSMC_CLK_OUT_P1	A8	2.5 V	Differential clock output
96	HSMC_CLK_IN_P	K7	2.5 V	Differential clock input
97	HSMC_CLK_OUT_N1	A7	2.5 V	Differential clock output
98	HSMC_CLK_IN_N	J7	2.5 V	Differential clock input
101	HSMC_TX_D_P7	B6	2.5 V	Differential transmission data
102	HSMC_RX_D_P7	E12	2.5 V	Differential receive data
103	HSMC_TX_D_N7	B5	2.5 V	Differential transmission data
104	HSMC_RX_D_N7	F12	2.5 V	Differential receive data
107	HSMC_TX_D_P8	A15	2.5 V	Differential transmission data
108	HSMC_RX_D_P8	G15	2.5 V	Differential receive data
109	HSMC_TX_D_N8	A14	2.5 V	Differential transmission data
110	HSMC_RX_D_N8	G14	2.5 V	Differential receive data
113	HSMC_TX_D_P9	B20	2.5 V	Differential transmission data
114	HSMC_RX_D_P9	D13	2.5 V	Differential receive data
115	HSMC_TX_D_N9	B21	2.5 V	Differential transmission data
116	HSMC_RX_D_N9	C13	2.5 V	Differential receive data

Board Reference Design	Pin Name	Cyclone V Pin#	I/O Standard	Description
119	HSMC_TX_D_P10	C8	2.5V	Differential transmission data
120	HSMC_RX_D_P10	H8	2.5 V	Differential receive data
121	HSMC_TX_D_N10	B8	2.5 V	Differential transmission data
122	HSMC_RX_D_N10	G7	2.5 V	Differential receive data
125	HSMC_TX_D_P11	B12	2.5 V	Differential transmission data
126	HSMC_RX_D_P11	C10	2.5 V	Differential receive data
127	HSMC_TX_D_N11	A12	2.5 V	Differential transmission data
128	HSMC_RX_D_N11	C9	2.5 V	Differential receive data
131	HSMC_TX_D_P12	C14	2.5 V	Differential transmission data
132	HSMC_RX_D_P12	D18	2.5 V	Differential receive data
133	HSMC_TX_D_N12	D14	2.5 V	Differential transmission data
134	HSMC_RX_D_N12	E17	2.5 V	Differential receive data
137	HSMC_TX_D_P13	C21	2.5 V	Differential transmission data
138	HSMC_RX_D_P13	G12	2.5 V	Differential receive data
139	HSMC_TX_D_N13	C20	2.5 V	Differential transmission data
140	HSMC_RX_D_N13	H12	2.5 V	Differential receive data
143	HSMC_TX_D_P14	F8	2.5 V	Differential transmission data
144	HSMC_RX_D_P14	H16	2.5 V	Differential receive data
145	HSMC_TX_D_N14	E7	2.5 V	Differential transmission data
146	HSMC_RX_D_N14	G16	2.5 V	Differential receive data
149	HSMC_TX_D_P15	C11	2.5 V	Differential transmission data
150	HSMC_RX_D_P15	D9	2.5 V	Differential receive data
151	HSMC_TX_D_N15	B11	2.5 V	Differential transmission data
152	HSMC_RX_D_N15	D8	2.5 V	Differential receive data
155	HSMC_CLK_OUT_P2	A13	2.5 V	Differential clock output
156	HSMC_CLK_IN_P2	H10	2.5 V	Differential clock input
157	HSMC_CLK_OUT_N2	B13	2.5 V	Differential clock output
158	HSMC_CLK_IN_N2	G11	2.5 V	Differential clock input

5.8.4 EXIO

The Hydra Board has an EXIO interface connector. EXIO is a connector used to transmit/receive data to/from a Renesas Lager Board. Table 5-8-4 shows pin assignment information for EXIO.

Note that the pin count of this connector differs from that of the HSMC connector, and therefore cards and cables for HSMC cannot be used with this connector. Do not forcibly insert HSMC cards or cables into this connector; doing so may break the connector.

Table 5-8-4 shows the EXIO pin layout.

Board Reference Design	Pin Name	Cyclone V Pin#	I/O Standard	Description
3	EXIO_0	F22	2.5 V	Lager data transfer
5	EXIO_1	E22	2.5 V	Lager data transfer
7	EXIO_2	K22	2.5 V	Lager data transfer
9	EXIO_3	M22	2.5 V	Lager data transfer
10	EXIO_19	L19	2.5 V	Lager data transfer
11	EXIO_4	L22	2.5 V	Lager data transfer
12	EXIO_20	L20	2.5 V	Lager data transfer
13	EXIO_5	E21	2.5 V	Lager data transfer
14	EXIO_21	J22	2.5 V	Lager data transfer
15	EXIO_6	F19	2.5 V	Lager data transfer
16	EXIO_22	L18	2.5 V	Lager data transfer
17	EXIO_7	RF18	2.5 V	Lager data transfer
18	EXIO_23	K19	2.5 V	Lager data transfer
19	EXIO_8	J17	2.5 V	Lager data transfer
20	EXIO_24	E20	2.5 V	Lager data transfer
22	EXIO_25	H20	2.5 V	Lager data transfer
23	EXIO_9	G22	2.5 V	Lager data transfer
24	EXIO_26	P16	2.5 V	Lager data transfer
25	EXIO_10	G21	2.5 V	Lager data transfer
26	EXIO_27	N16	2.5 V	Lager data transfer
27	EXIO_11	K21	2.5 V	Lager data transfer
28	EXIO_28	D22	2.5 V	Lager data transfer
29	EXIO_12	G20	2.5 V	Lager data transfer
30	EXIO_29	P18	2.5 V	Lager data transfer
31	EXIO_13	H21	2.5 V	Lager data transfer
32	EXIO_30	N18	2.5 V	Lager data transfer
33	EXIO_14	J19	2.5 V	Lager data transfer
34	EXIO_31	J21	2.5 V	Lager data transfer
35	EXIO_15	H18	2.5 V	Lager data transfer
36	EXIO_32	L17	2.5 V	Lager data transfer
37	EXIO_16	P21	2.5 V	Lager data transfer
38	EXIO_33	K17	2.5 V	Lager data transfer
39	EXIO_17	P22	2.5 V	Lager data transfer
58	EXIO_34	J16	2.5 V	Lager data transfer
60	EXIO_35	N20	2.5 V	Lager data transfer
62	EXIO_36	F20	2.5 V	Lager data transfer
71	EXIO_18	G17	2.5 V	Lager data transfer
85	EXIO_PIN85	T12	1.5 V/2.5 V	For Lager boot-up
114	I2C_SCL	C19	2.5 V	I2C clock
116	I2C_SDA	C18	2.5 V	I2C data

5.8.5 MAX V

The Hydra Board has MAX V CPLD for FPGA configuration from NOR Flash memory.

Table 5-8-5 shows the pin layout for MAX V.

Table 5-8-5 MAX V Pin Assignment List

Board Reference Design (P1)	Pin Name	IO Standard	FPGA Pin#
33	JTAG_TMS	3.3-V LVTTL	R4
34	JTAG_FPGA_TDO	3.3-V LVTTL	V3
35	JTAG_TCK	3.3-V LVTTL	V5
93	FPGA_DATA7	3.3-V LVTTL	U6
94	FPGA_DATA6	3.3-V LVTTL	P6
95	FPGA_DATA5	3.3-V LVTTL	U7
96	FPGA_DATA4	3.3-V LVTTL	AB6
97	FPGA_DATA3	3.3-V LVTTL	AA5
98	FPGA_DATA2	3.3-V LVTTL	T5
101	FPGA_DATA1	3.3-V LVTTL	W5
102	FPGA_DATA0	3.3-V LVTTL	AB4
103	FPGA_CONF_DONE	3.3-V LVTTL	J6
104	FPGA_nSTATUS	3.3-V LVTTL	G5
105	FPGA_nCONFIG	3.3-V LVTTL	A4
108	FPGA_DCLK	3.3-V LVTTL	M5

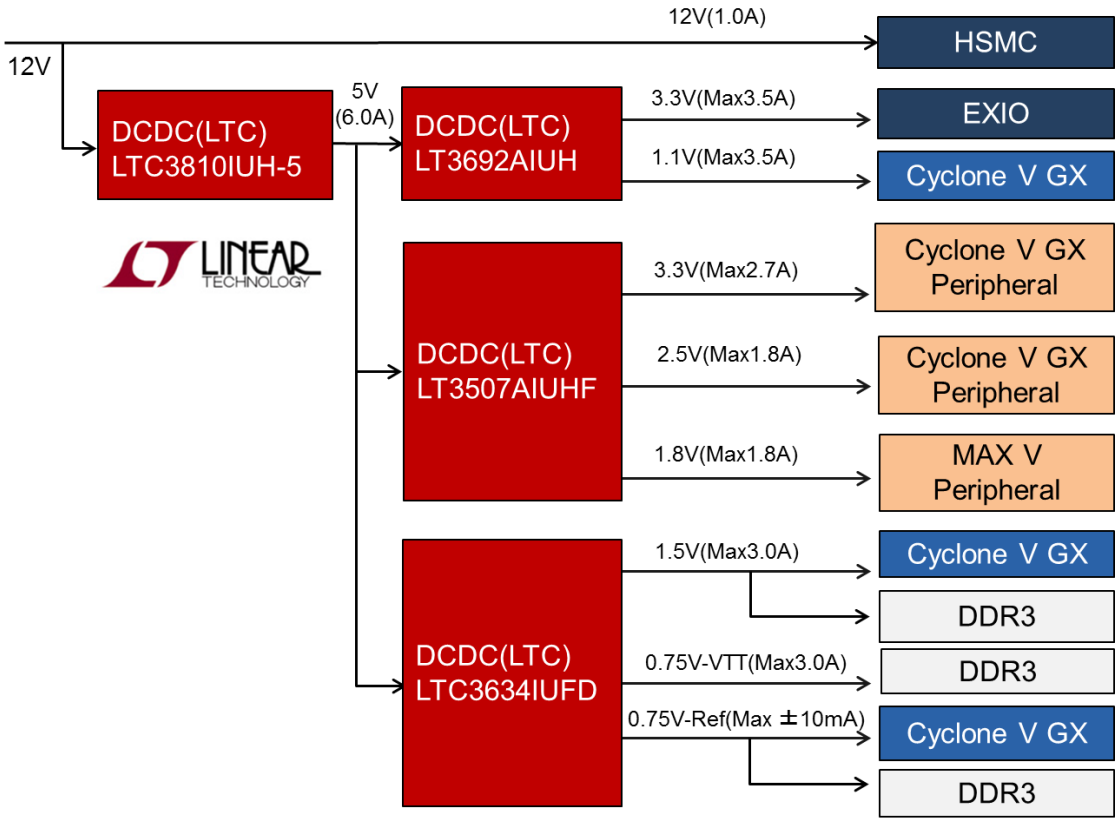
5.8.6 Ethernet

The Hydra Board has DP83848HSQ/NOPB manufactured by Texas Instruments for Ethernet PHY and supports 10/100 Ethernet.
Table 5-8-6 shows the Ethernet pin assignment.

Table 5-8-6 Ethernet Pin Assignment List

Board Reference Design (U12)	Pin Name	I/O Standard	FPGA Pin#
31	ENET_RX_CLK	2.5 V	M17
32	ENET_RX_DV	2.5 V	H19
33	ENET_RX_CRS	2.5 V	M21
34	ENET_RX_ER	2.5 V	M20
35	ENET_RX_COL	2.5 V	L15
36	ENET_RXD0	2.5 V	K16
37	ENET_RXD1	2.5 V	N21
38	ENET_RXD2	2.5 V	J18
39	ENET_RXD3	2.5 V	K15
2	ENET_TX_CLK	2.5 V	M16
3	ENET_TX_EN	3.3 LVTTL	P19
4	ENET_TXD0	3.3 LVTTL	R19
5	ENET_TXD1	3.3 LVTTL	U21
6	ENET_TXD2	3.3 LVTTL	T17
7	ENET_TXD3	3.3 LVTTL	V19
24	ENET_MDIO	3.3 LVTTL	T18
25	ENET_MDC	3.3 LVTTL	T19

5.9 Power Tree



6. Document Revision History

Date	Revision	Changes
2014/02/01	1.0	Document Released