

# Direct digital synthesis enables digital PLLs

Direct digital synthesis, together with a DAC and a high-performance digital phase detector, overcome several fundamental drawbacks in analog PLLs, such as asymmetry in the phase detector or bandwidth limitations and phase noise in the VCO. Furthermore, because the circuitry is digital, feedback-loop parameters are adjusted by changing numerical coefficients in device registers rather than changing electrical parameters in physical components, the latter process being especially difficult for ASIC designs.

By Paul Kern

The performance of analog PLLs has steadily improved, with operating frequencies extending up to 8 GHz and beyond. Industry mainstays for many years, these PLLs are well understood, and offer inexpensive solutions for frequency synthesis and jitter clean up. Recently, digital PLLs based on direct digital synthesis (DDS), have emerged as attractive alternatives in certain applications. This article explores the differences between analog PLLs and DDS-based digital PLLs, and how these differences can be used to guide the designer toward the best option.

A digital PLL implements traditional PLL building blocks using digital logic. While there are many ways to implement a digital PLL, this article will focus on DDS-based digital PLL architectures.

Figure 1 shows a typical analog PLL. The reference divider, which is the first block encountered by an incoming signal, is no different from that of an analog PLL. The reference divider reduces the frequency of the incoming signal before it goes to the phase detector. The reference divider setting plays a key role in PLL behavior. If the designer must use a large reference divider and a low phase-detector frequency to generate the desired output, the maximum loop bandwidth will be constrained.

## The digital phase detector

In an analog PLL, the phase detector generates charge-pump current pulses, whose duration is proportional to the phase difference between the reference and feedback signal. In a digital PLL, on the other hand, the phase detector's output is a digital number proportional to the time difference between the edges of the incoming reference signal and the feedback signal. These digital words are sent to the digital loop filter, which filters and integrates the phase detector output. Because the loop filter parameters are numerical coefficients, however, they can be easily changed, and unlike an analog PLL, there is

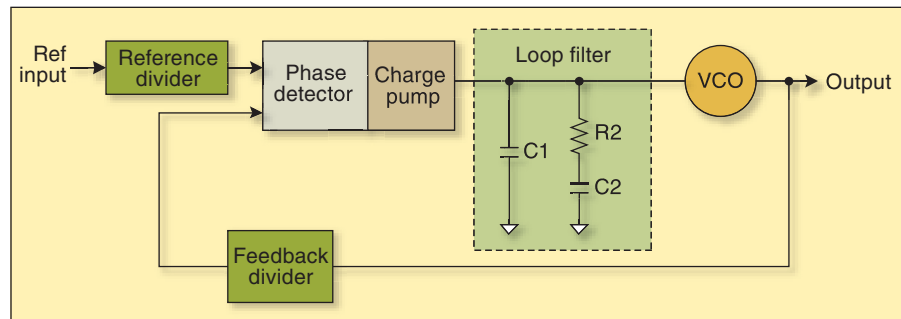


Figure 1. Block diagram of basic analog PLL.

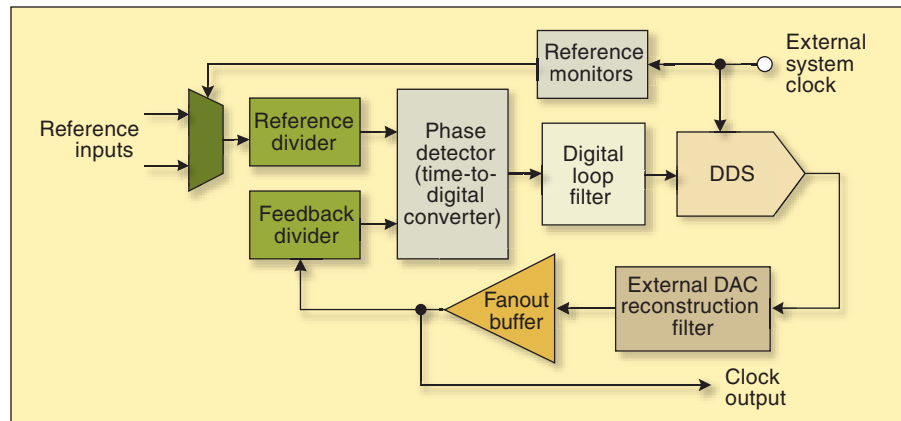


Figure 2. Block diagram of DDS-based digital PLL.

no practical limit to how large they can be. In addition, the digital phase detector doesn't suffer from thermal noise, aging or drift, and charge pump mismatch or leakage. Charge pump leakage occurs when the transistors in the charge pump do not completely turn off, or another leakage path causes unwanted voltage variation at the VCO. The last advantage is particularly important as charge-pump leakage and driver up/down current mismatch are key contributors to spurs that appear in the output spectrum at the phase detector frequency. The digital PLL avoids this by eliminating the charge pumps.

## The digital VCO: DDS plus DAC

In a DDS-based digital PLL, such as the one shown in Figure 2, the DDS block and DAC replace the traditional VCO. The DDS input is a digital-tuning word whose value is proportional to its output frequency. This is similar to a conventional VCO, in which the output frequency is usually proportional to analog input tuning voltage. A typical DDS that runs at 1 GHz will have a fundamental tuning range from dc to about 400 MHz. This range can be extended by using a DAC image above the Nyquist frequency (one-half of the DAC sample rate). The DAC output is sent

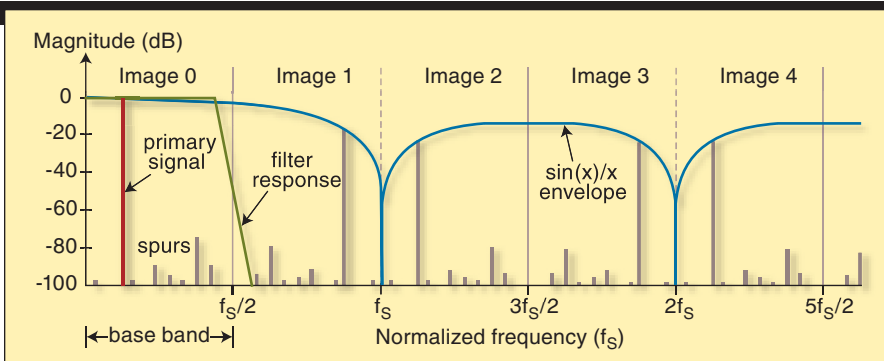


Figure 3. DAC spectrum vs. reconstruction filter response.

to an external low-pass reconstruction filter to remove undesired harmonic content, and then back to the on-chip feedback divider, thus closing the feedback loop.

The external DAC reconstruction filter is one important component not found on an analog PLL. This low-pass filter removes frequency content above the fundamental output frequency, leaving only the desired sine wave. A fifth- or seventh-order low-pass filter is common, depending on the filtering requirement and how close the output frequency is to the Nyquist frequency. This sine wave can then be fed into a fan-out buffer to produce a square wave clock output. A band-pass filter can be used instead of a low-pass filter for additional noise filtering, or to allow the PLL to operate at frequencies well above the Nyquist frequency. It is possible to get an unfiltered spur at or below the output frequency, so the designer must be careful to do frequency planning and run the DAC at a frequency where this is not an issue.

### Digital PLL performance advantages

Once the component blocks used in a digital PLL are understood, the benefits

associated with these digital elements become apparent. For example, the digital PLL excels in frequency translation applications, such as translating the common 19.44 MHz networking clock frequency to 156.25 MHz. This necessitates dividing the incoming signal by 1944, and running the phase detector at 10 kHz. In order to maintain loop stability, the maximum PLL loop bandwidth is typically constrained to about 10% of the phase detector frequency (or 1 kHz in this case). Fractional-N analog PLLs can enhance loop flexibility by keeping the phase-detector frequency high, but this architecture can introduce its own set of problems.

Furthermore, in an analog PLL, low loop bandwidths require bulky loop-filter components, which not only take up board space, but lead to self-resonance and microphonics when ceramic capacitors are used. While digital PLL can also have a reference spur due to finite steps of phase correction, this spur can be suppressed more easily because the digital loop filter makes it easy to implement very narrow loop bandwidths (<1 Hz). More important, because the loop characteristics are determined by digital coefficients, the loop dynamics are much more tightly controlled

than in an analog PLL. This is a key advantage in phase-modulated systems.

In any PLL, reference noise within the PLL loop bandwidth is passed to the output, and reference noise outside the PLL loop bandwidth is attenuated. A key advantage to the dual-loop DDS-based digital PLL architecture is that the output phase noise is dependent on the DAC system clock, as opposed to the analog VCO. This allows designers to choose a system clock source that is tailored for specific jitter requirements. In an analog PLL, replacing one VCO with another will require matching the supply voltage, gain, frequency range, and other VCO parameters, which can be quite difficult. Another difficulty with the analog PLL is that the designer must trade off VCO tuning range for VCO phase noise, with VCO noise going up as the VCO frequency range is increased. The DDS digital PLL removes these constraints. By providing a clean DAC system clock, the designer will have the equivalent of a quiet wideband low-noise VCO. This allows the designer to select a low PLL loop bandwidth for jitter cleanup.

Because the phase detector gain, loop bandwidth, and phase margin are programmable in a digital PLL, the user can maintain the same loop transfer function for various conditions. For example, the user may need to synchronize to an 8 kHz BITS clock on one reference input, and a 19.44 MHz SONET/SDH reference clock on the other input to generate a 125 MHz reference clock for gigabit Ethernet. In a digital PLL, the loop filter can be optimized for constant loop bandwidth and phase margin for both cases. More important, the loop parameters can be adjusted as conditions warrant by programming registers instead of changing components.

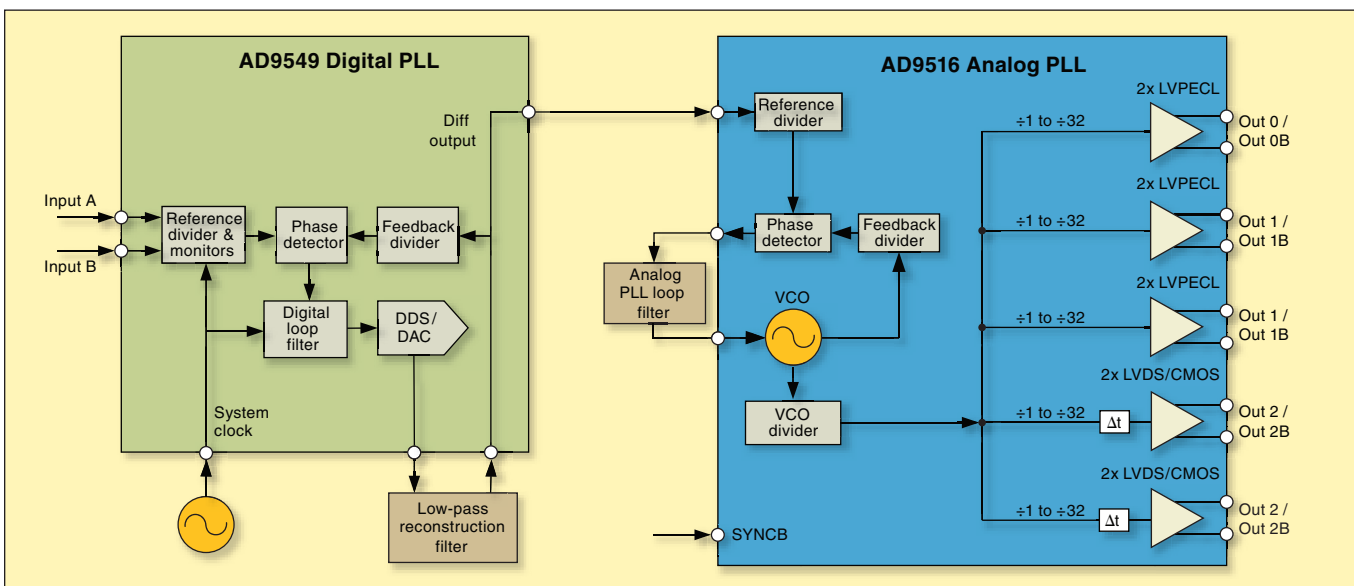


Figure 4. Cascaded architecture where digital PLL feeds analog PLL.



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A DDS-based digital PLL has another key advantage by having a high-speed DAC system clock available for reference monitoring. This clock can be used to oversample the reference inputs, and allows for rapid detection of reference clock drift or failure. Once a failure is detected, the device can automatically switch inputs or go into holdover mode. Hitless clock switching is easily implemented in the digital logic. Clock holdover occurs when both reference clocks fail, and the digital PLL will then act like a DDS frequency synthesizer and continue to output the same frequency for as long as necessary. The stability of the output clock in holdover mode is the same as the stability of the system clock. Accomplishing this with an analog PLL would require either an external oscillator that is a multiple of the reference input, or a voltage on the VCO that is stable to submicrovolt levels over temperature for long periods of time. While the former might be practical, the latter is not.

**Digital PLL drawbacks**

Even an ideal DAC will have harmonics and unwanted spectral energy across the entire band, and these are exacerbated by DAC non-linearities. The standard figure of merit for DAC performance is spurious-free dynamic range (SFDR), measured without a reconstruction filter. SFDR is a measure of the power of the largest spur relative to the carrier from dc to one-half of the DAC sample rate. For a 14-bit DAC, wideband SFDR of -50 dBc to -70 dBc is common. While it is certainly possible to have higher-order DAC spurs at or below the desired output frequency, these spurs often have much lower amplitude (below -70 dBc). The primary means for attenuating DAC spurs is with the reconstruction filter, and a seventh-order low-pass filter will quickly attenuate spurs. Figure 3 shows a typical DAC output spectrum and reconstruction-filter frequency response. The designer should be careful to choose a system clock frequency so that lower-order spurs are not close to the desired output frequency, allowing them to be effectively filtered.

Choosing the correct DAC system clock is an important consideration when using a digital PLL. In the most demanding applications, a high-frequency oscillator can be used to provide the 500 MHz to 1000 MHz DAC system clock directly. However, they can be expensive, and few applications demand them. Many digital PLLs feature an analog PLL clock multiplier that produces phase noise numbers acceptable for many applications. In these cases, the designer can drive the DAC system clock PLL with a common 16 MHz or 25 MHz crystal, or with crystal oscillators in the 16 MHz to 100 MHz range, thus allowing the onboard PLL to generate a 1 GHz system clock. However, the

noise of the onboard PLL must be factored in to any jitter calculations.

When choosing a crystal oscillator, the designer should consider the desired output phase noise and stability requirements. For instance, if Stratum-2 clock stability is required while in holdover, then a Stratum-2-compliant oscillator should be used for the system clock. Output phase noise is not only a function of the phase noise of the oscillator, but also the amount of frequency multiplication supplied by the system clock PLL (if used). Using a third-overtone crystal oscillator at 80 MHz to drive the system clock PLL will deliver better overall phase noise than using a 25 MHz oscillator for the same function.

Another fundamental drawback shared by all digital PLLs is that the output frequencies available are generally lower than those possible when using analog PLLs.

**Digital vs. analog PLL design options**

Of course, whether an analog or digital PLL is the best option depends on the application. In systems where holdover, reference switching, and loop reconfiguration aren't necessary, the analog PLL presents an attractive option, and one that allows for higher output frequencies. On the other hand, the digital PLL excels in redundant clocking applications where smooth switching, holdover, and well-controlled loop dynamics are needed. Their flexibility and dynamic reconfiguration allow different frequencies on the reference inputs, and a DDS-based digital PLL handles low reference frequencies exceptionally well. Therefore, DDS-based digital PLLs can offer solutions that traditional analog PLLs cannot provide. Because digital logic is used to implement the digital PLL building blocks, a new level of performance and flexibility is achieved, giving designers an alternative to analog PLLs.

However, to overcome the limitations of either PLL design, a powerful combination is a digital PLL followed by an analog PLL as shown in Figure 4. The digital PLL can handle clock switching and difficult frequency ratios, while the analog PLL can further attenuate spurs, multiply to higher frequencies, and perform clock distribution. **RFID**

**ABOUT THE AUTHOR**

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