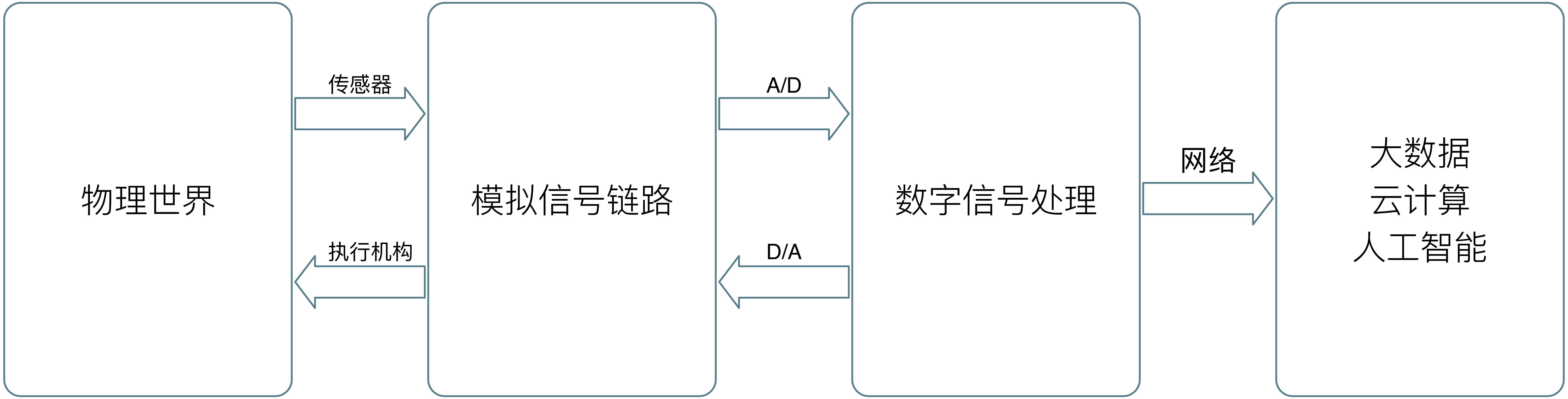
电子产品的系统构成及电路基础

由电流构成的回路，由电压/电流表征的信号

所有电子产品都是用电信号对物理世界进行表征和计算的过程



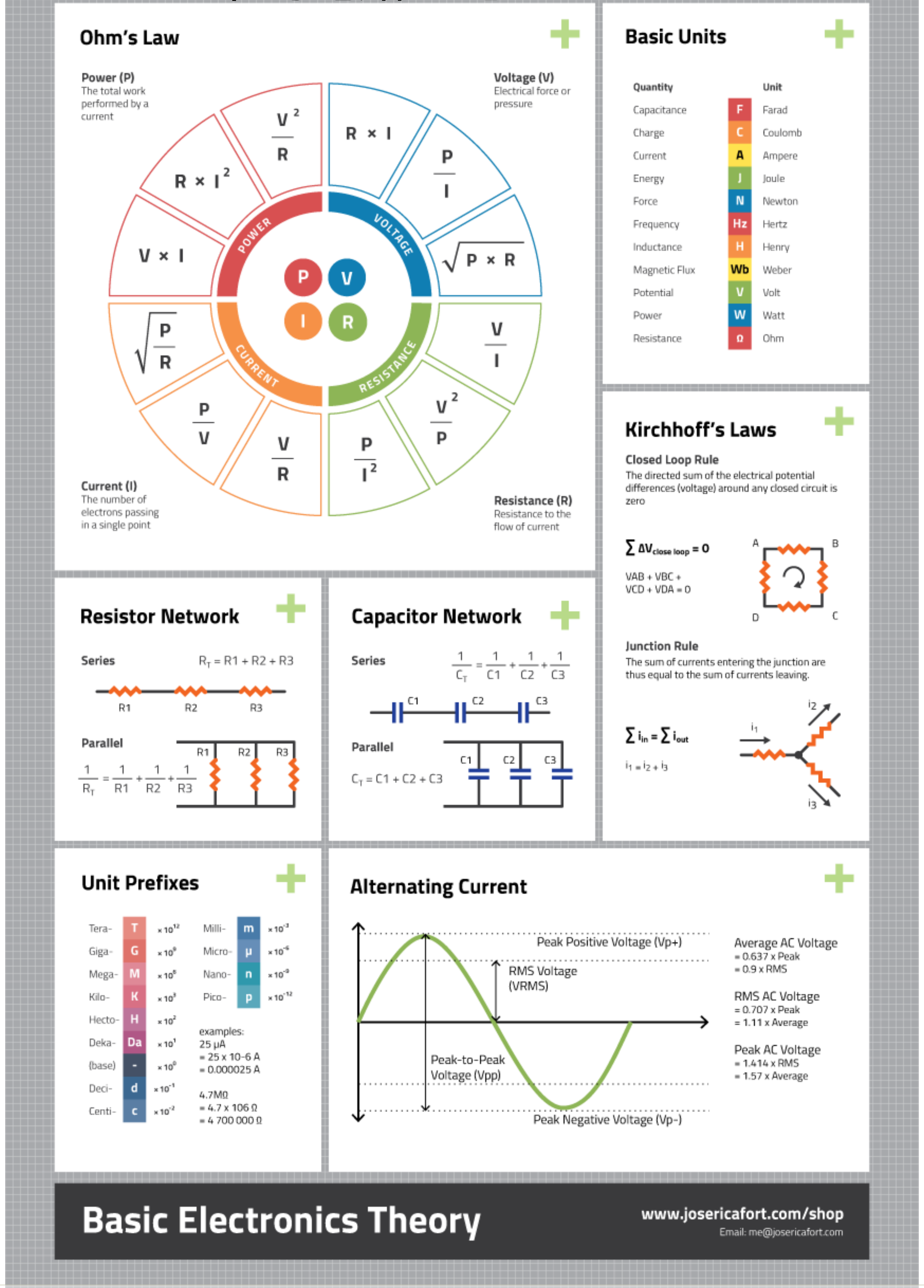
V=I*R

时域

频域

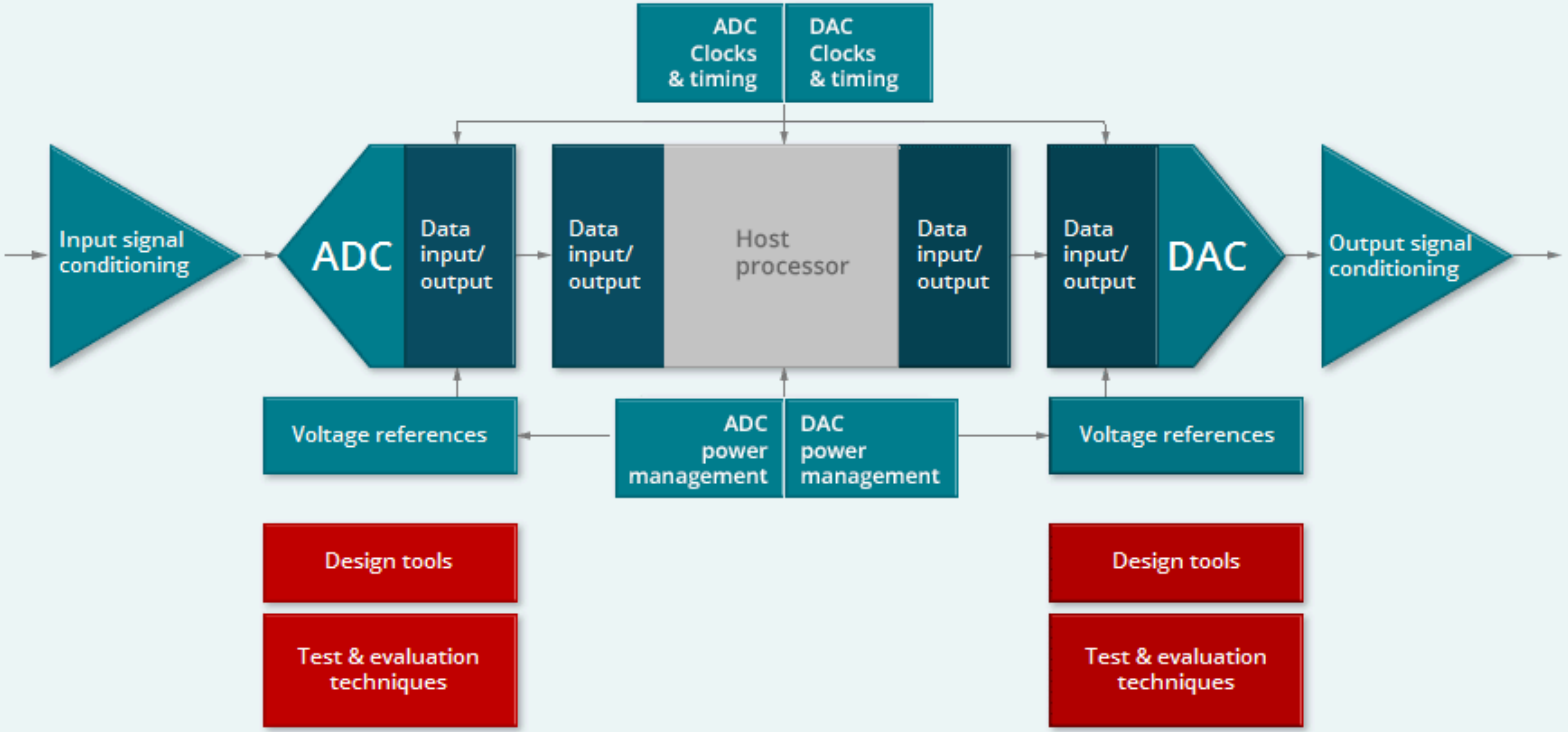
数字域

基本的电路理论

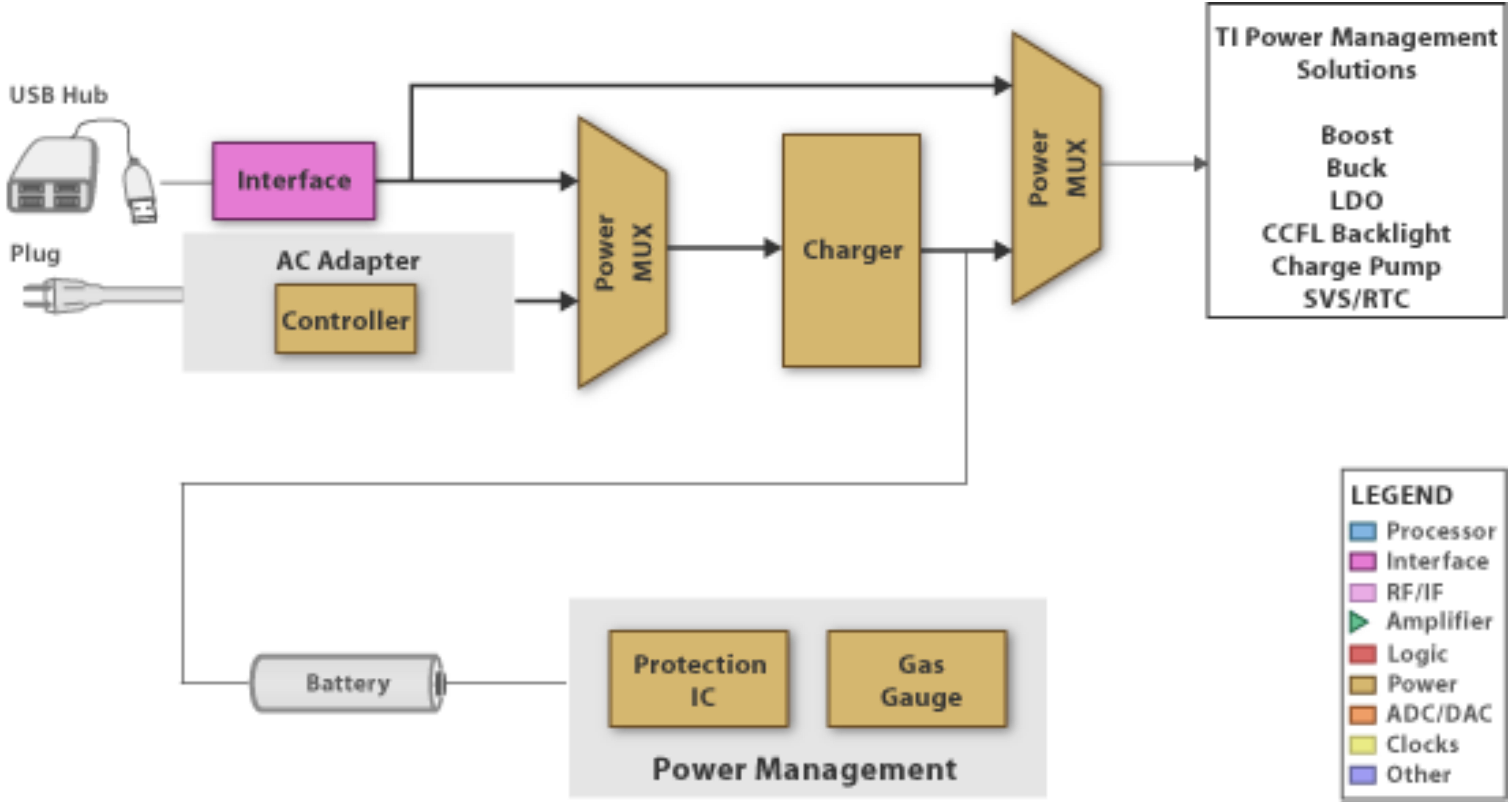


主要公式

Parameter	Symbol	Measuring Unit	Discription
Voltage	Volt	V or E	Unit of Electrical Potential V = I x R
Current	Ampere	I or i	Unit of Electrical Current I = V ÷ R
Resistance	Ohm	R or Ω	Unit of DC Current R = V÷I
Conductance	Siemen or Mho	G or ℧	Unit of Conductance G = 1÷R
Power	Watts	W	Unit of Power P = V x I
Capacitance	Farad	C	Unit of Capacitance C = Q ÷ V
Inductance	Henery	L or H	Unit of Inductance V_L = -L(di ÷dt)
Impedance	Ohm	Z	Unit of AC Resistance $Z^2 = R^2 + X^2$
Charge	Coulomb	Q	Unit of Electrical Charge Q = C x V
Frequency	Hertz	Hz	Unit of Frequency f = 1÷T
Period	sec	s	Unite of Period T = 1 ÷ f

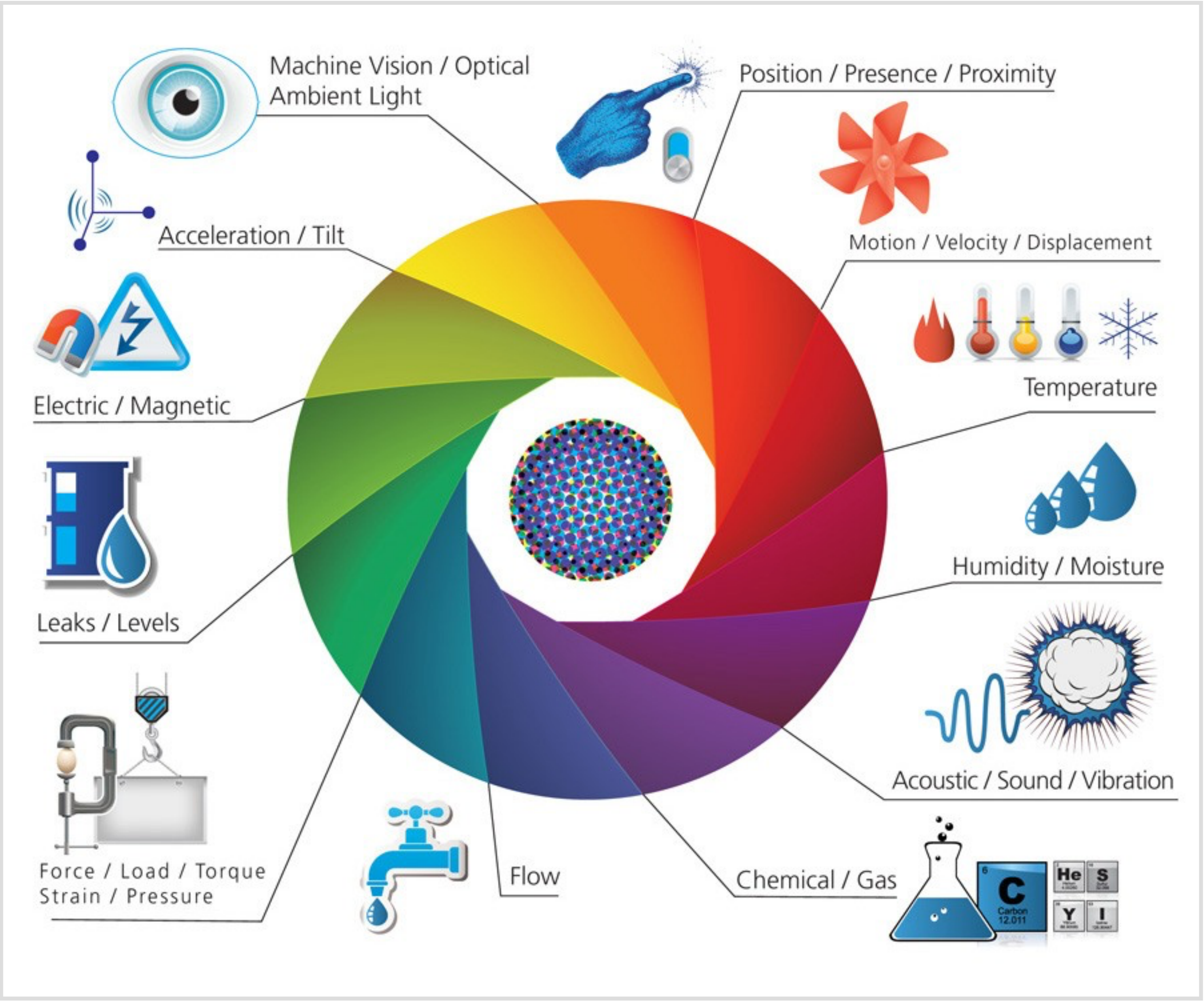


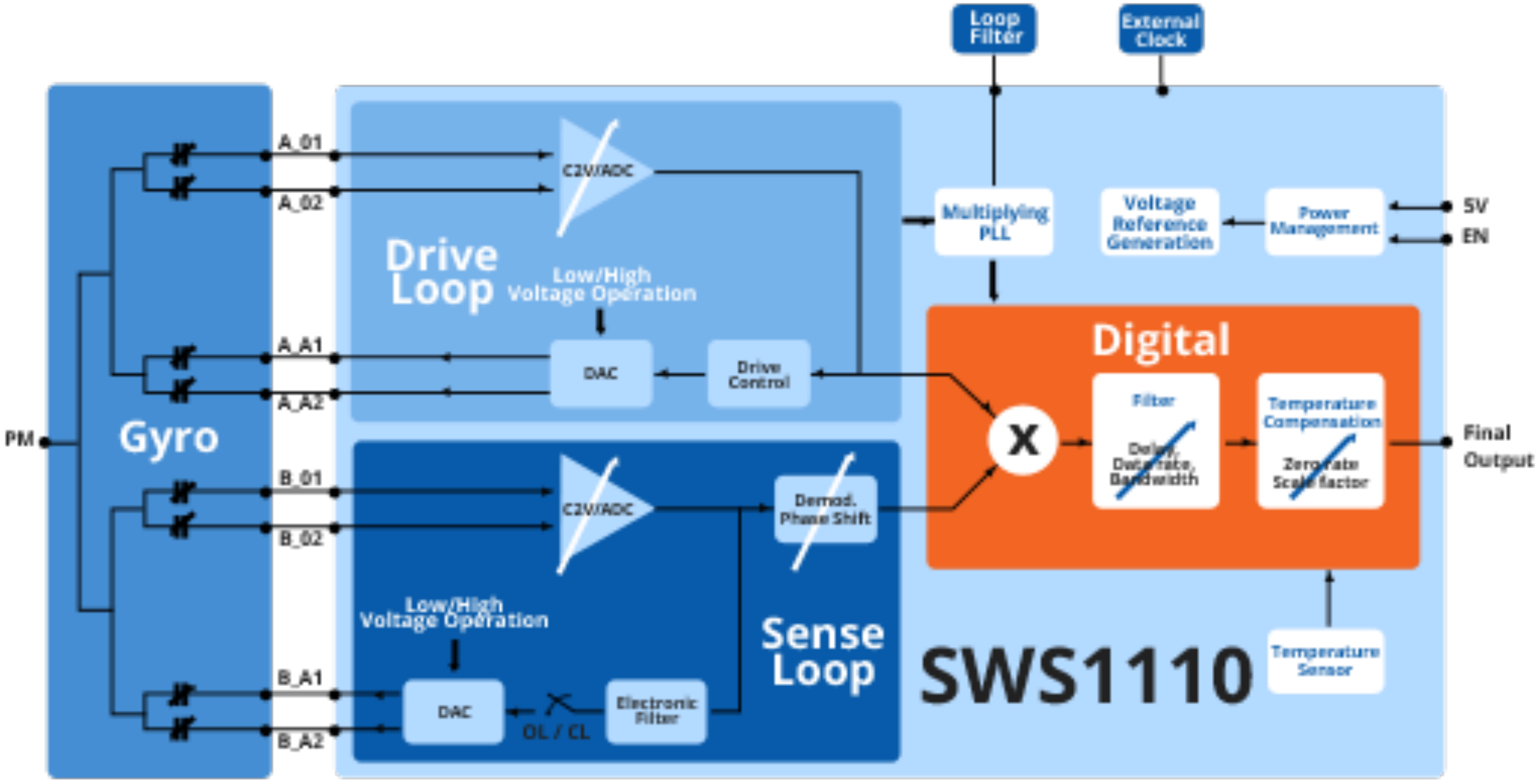
理解电子产品的系统构成及各部分的工作原理



电源部分

所有电子产品都需要供电

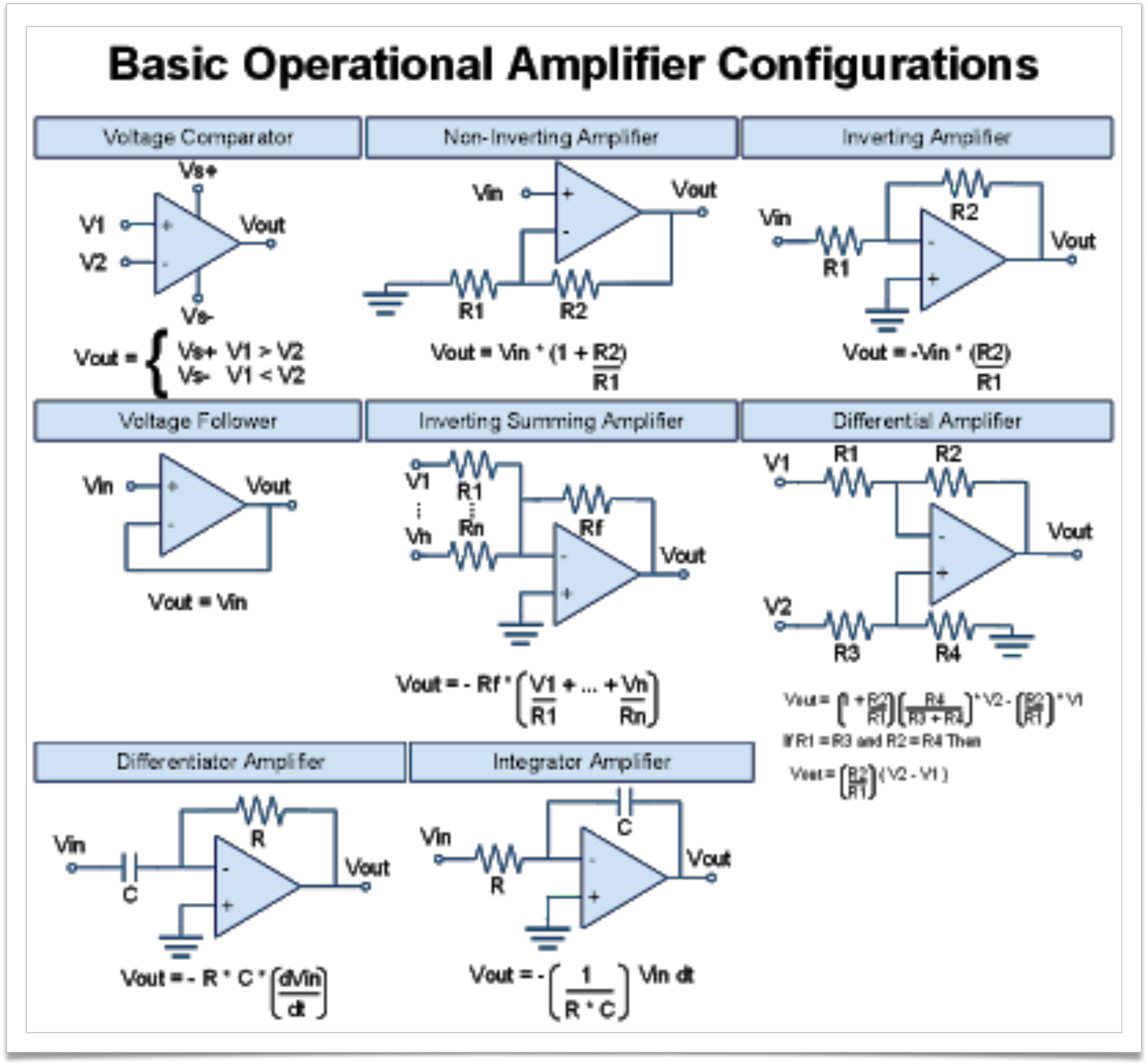


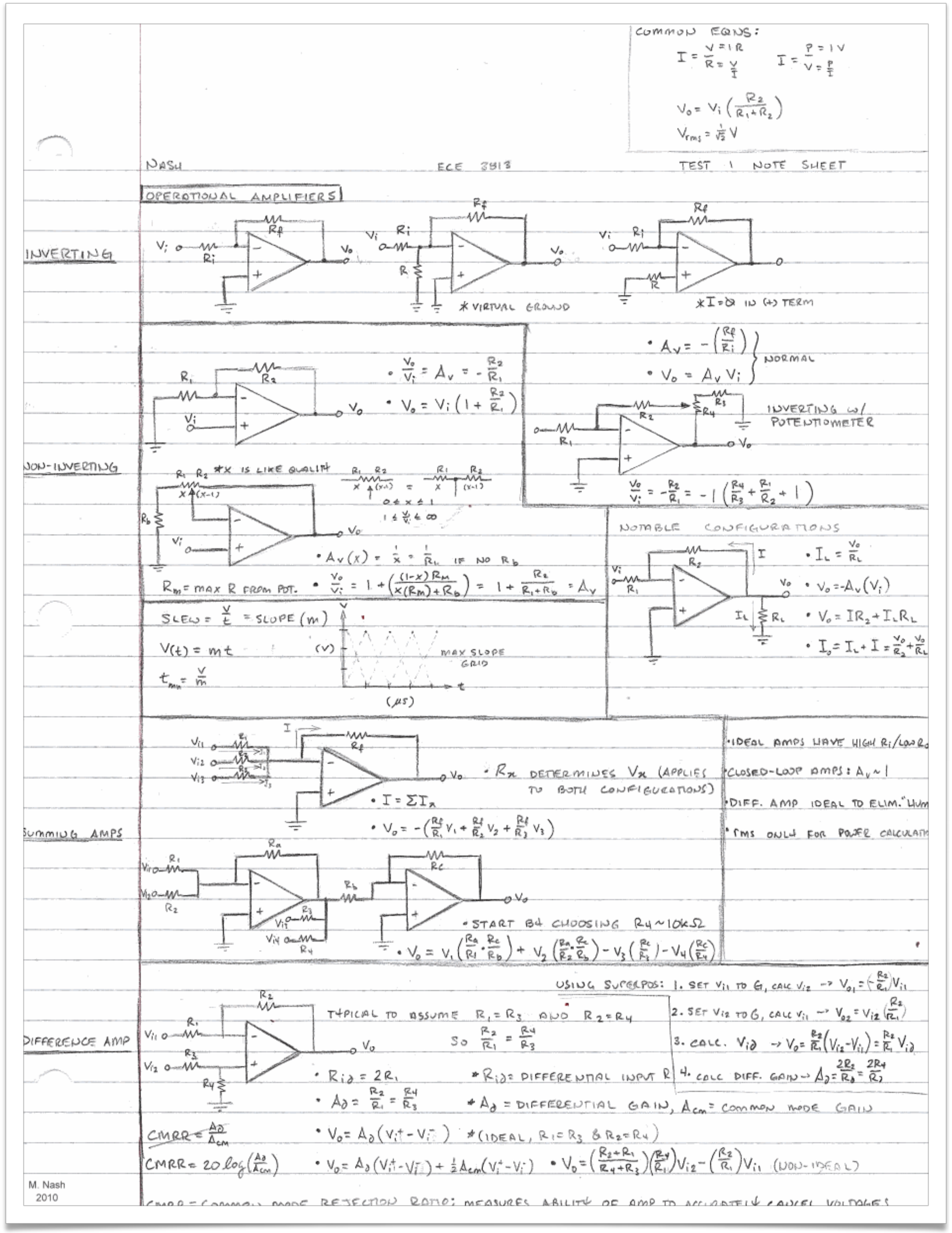


传感器 - 物理信号转变为电信号

对物理世界用电信号进行表征

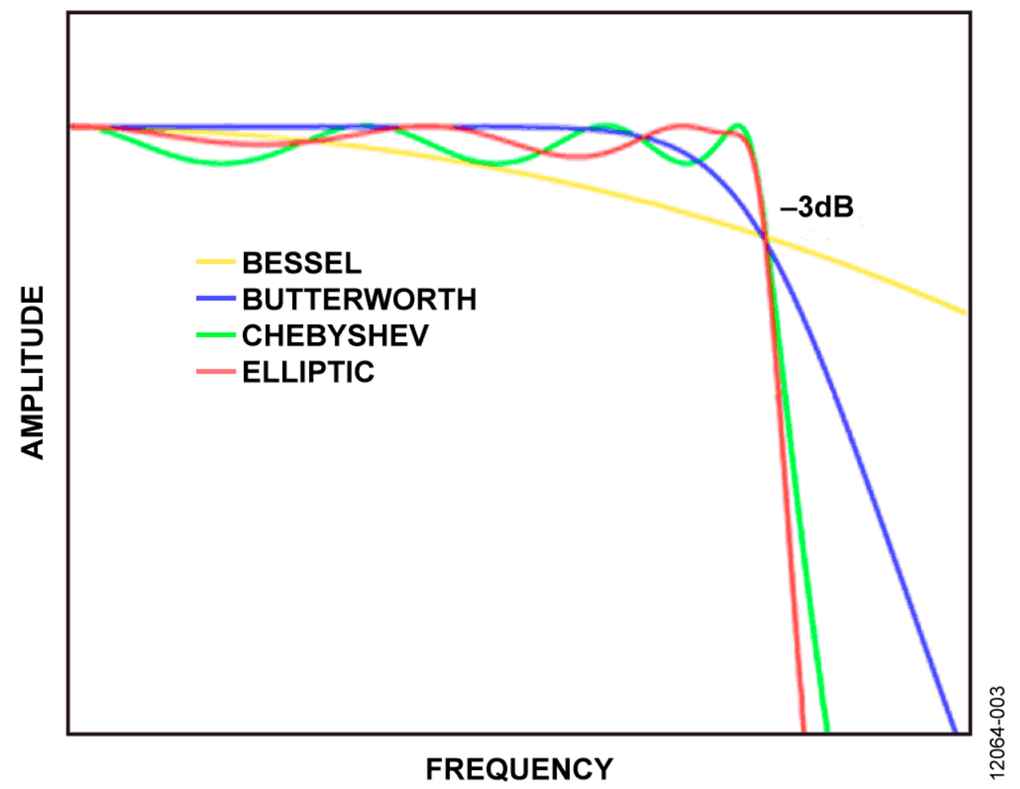
模拟信号调理 - 幅度调节： 放大/衰减

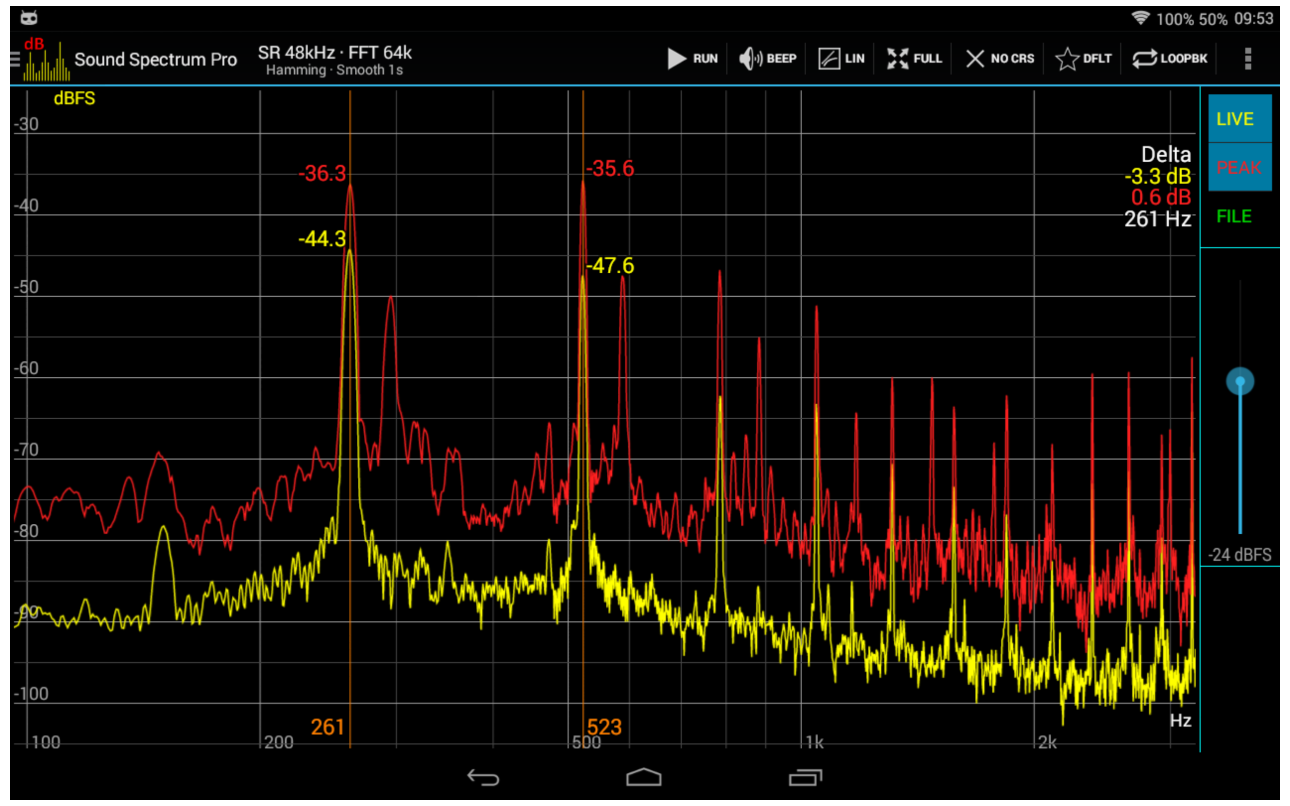




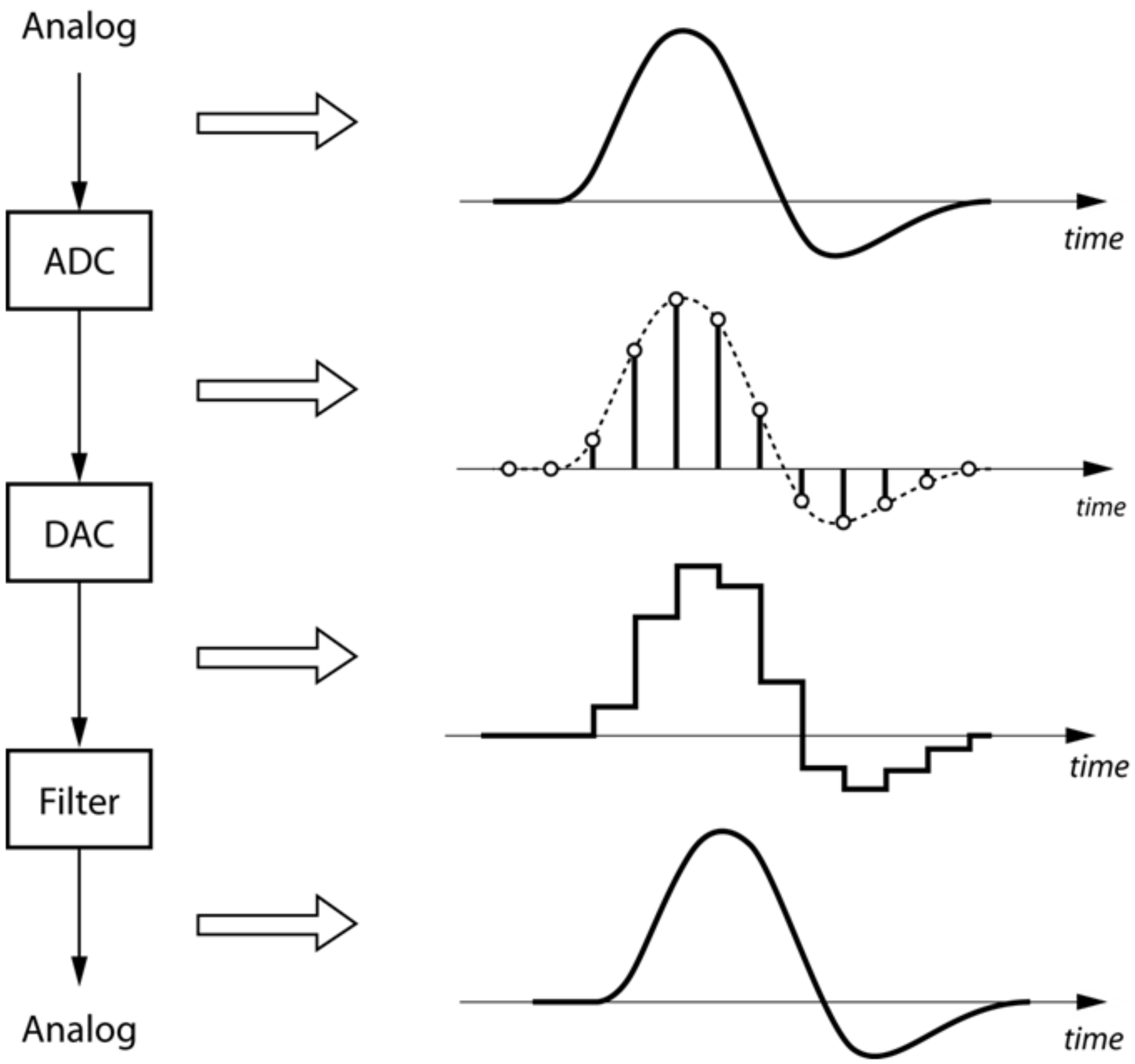
模拟信号调理 - 频域：滤波器

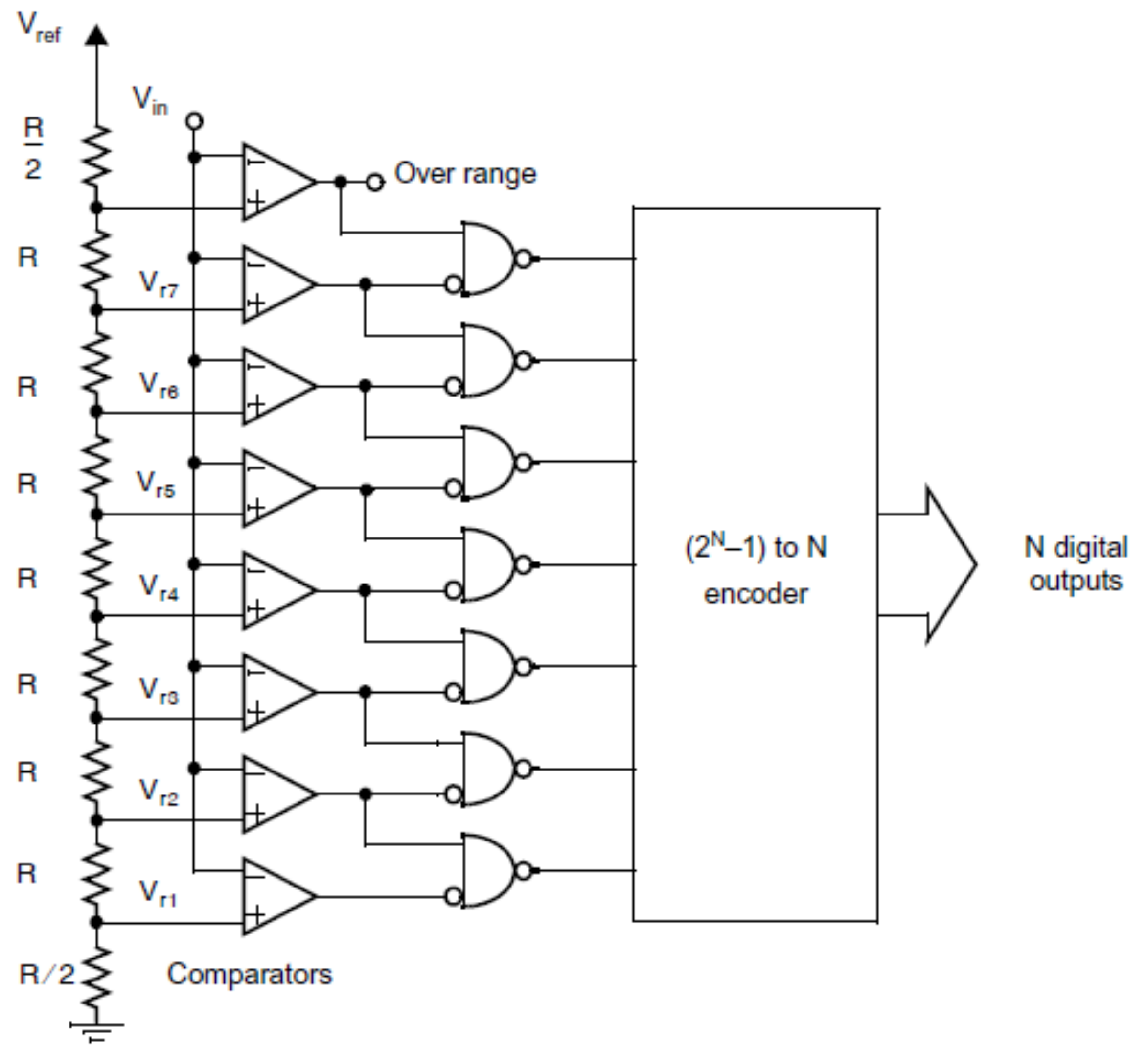
- 主要类型：低通、带通、高通
- 主要指标：
  - 过渡带衰减
  - 抑制度
  - 带内波动
  - 相位特性
- 有源滤波/无源滤波
- 测量仪器 - FFT/频谱仪

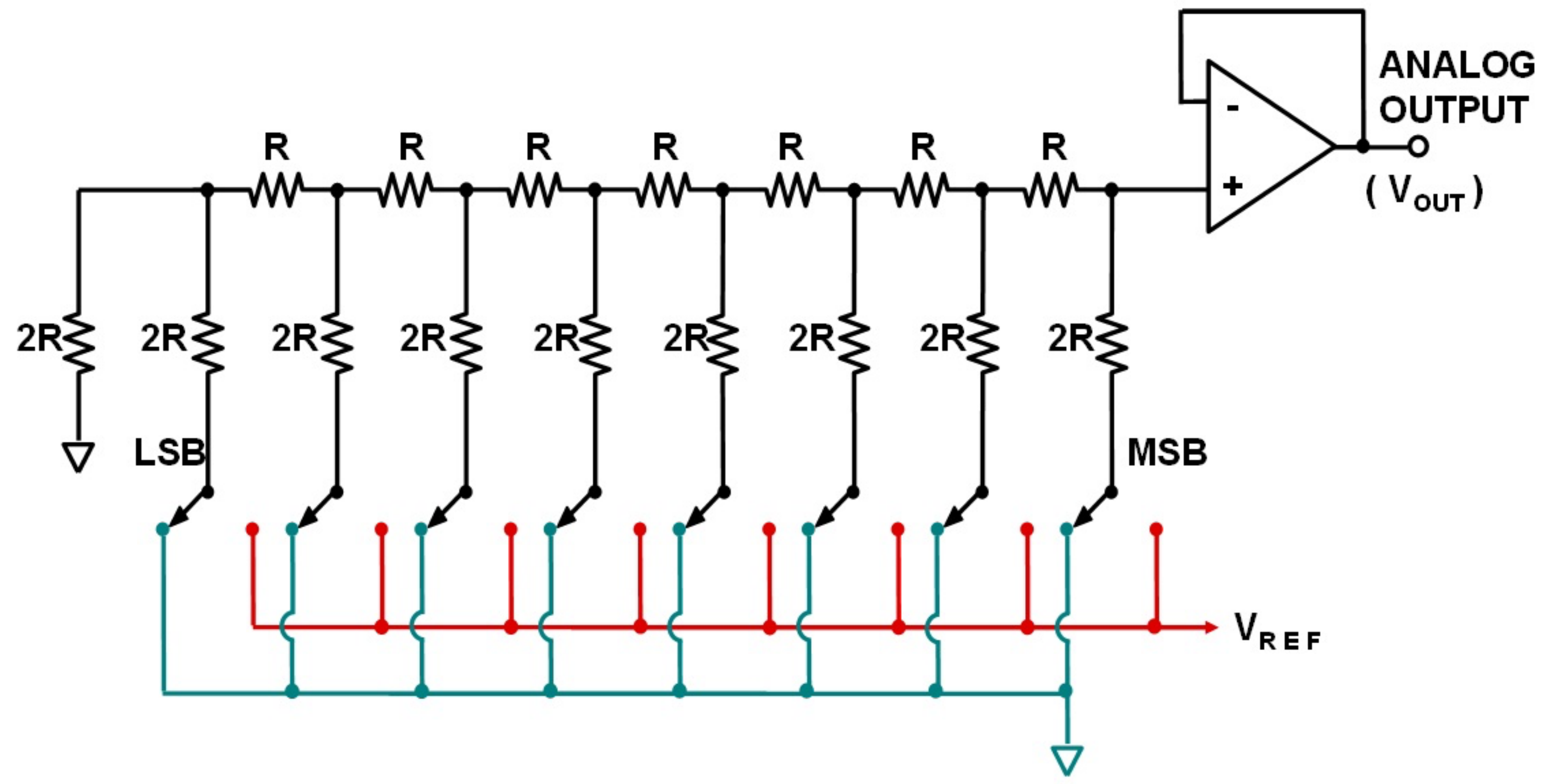




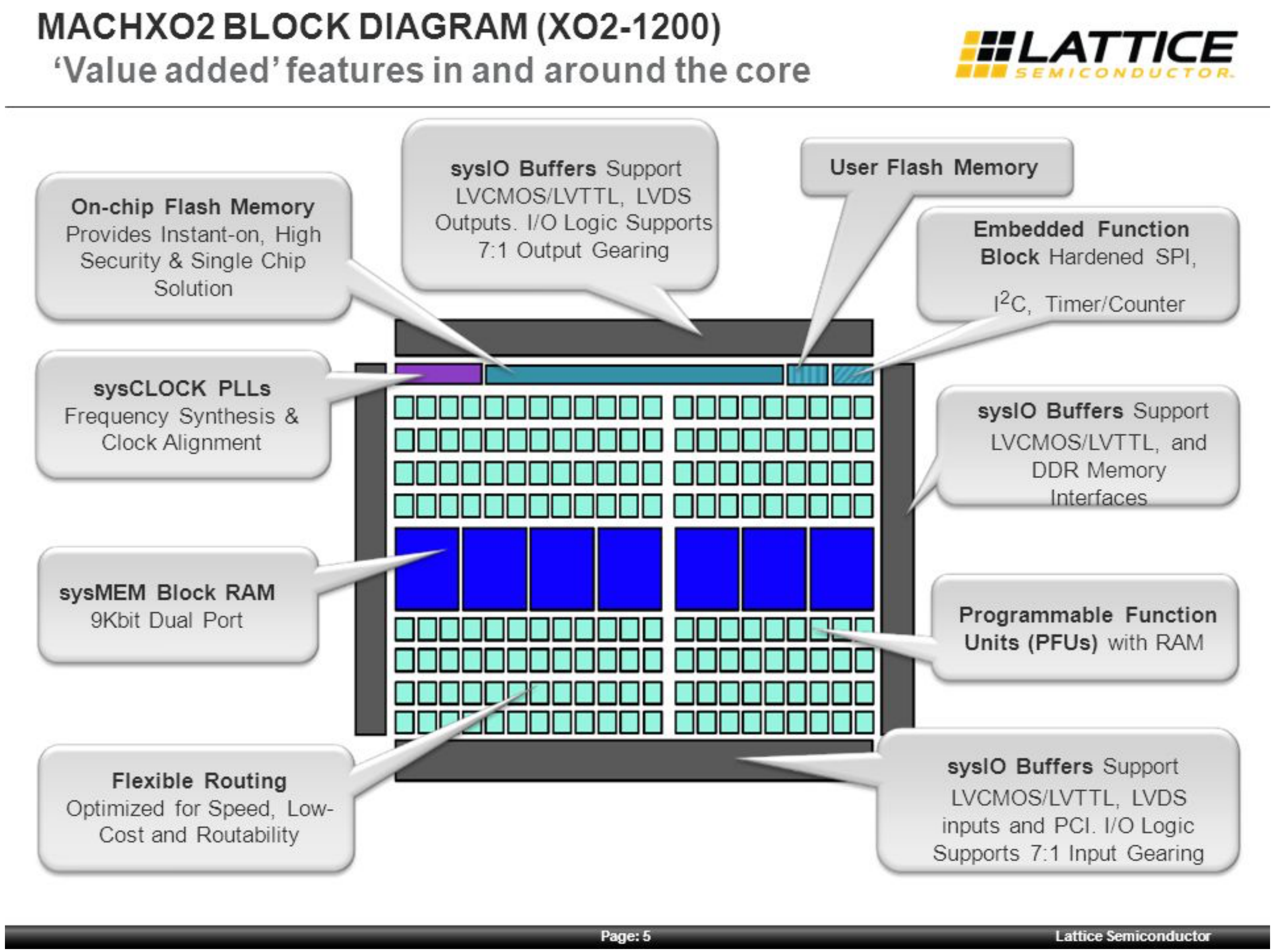
	过度带 衰减速度	通带内起伏	通带外抑制	相位特性
贝塞尔滤波器	非常慢	带内无起伏， 单调衰减	衰减慢	通带内的相 应近乎线性
巴特沃斯滤波器	比较慢	无起伏，最平坦	单调衰减	
切比雪夫滤波器	比较快	有起伏，等波纹	单调衰减	
椭圆滤波器	非常快	有起伏，等波纹	有起伏，等波纹	良好

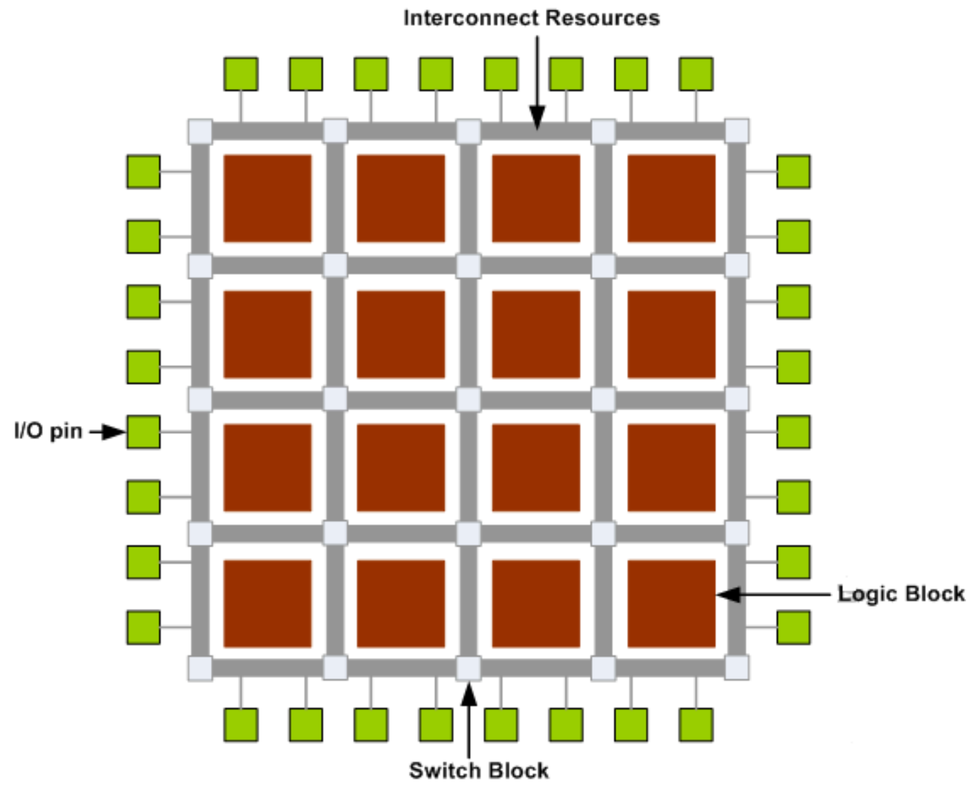


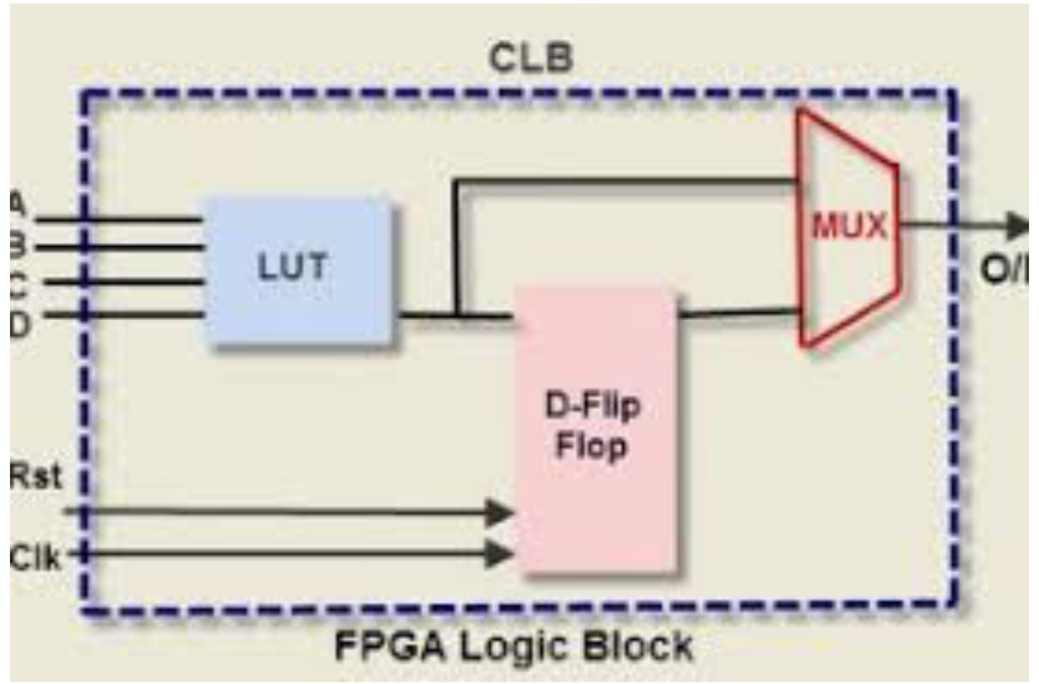


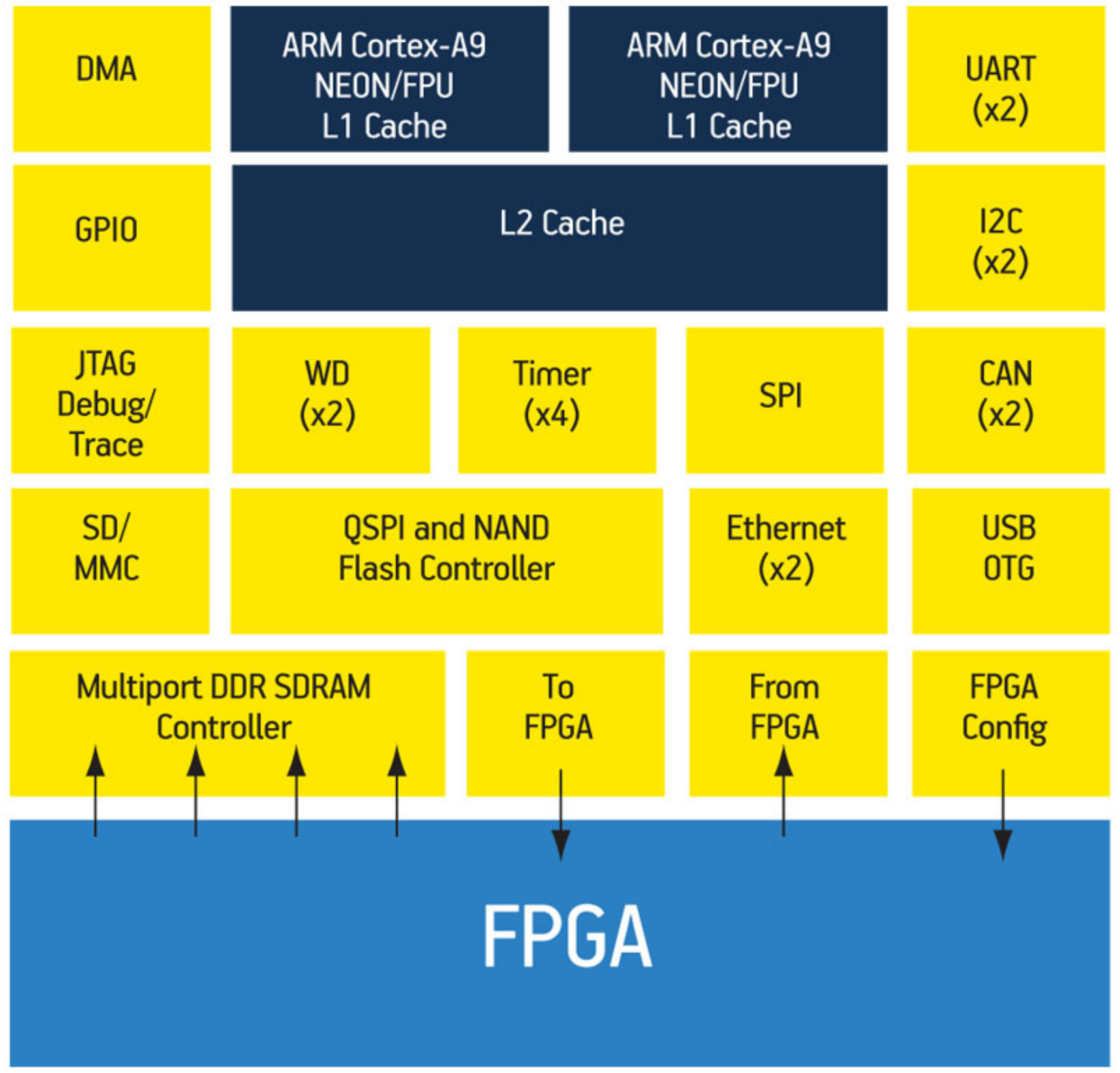


数据转换 - ADC/DAC：连接模拟信号和数字信号的桥梁 - 转换率/分辨率

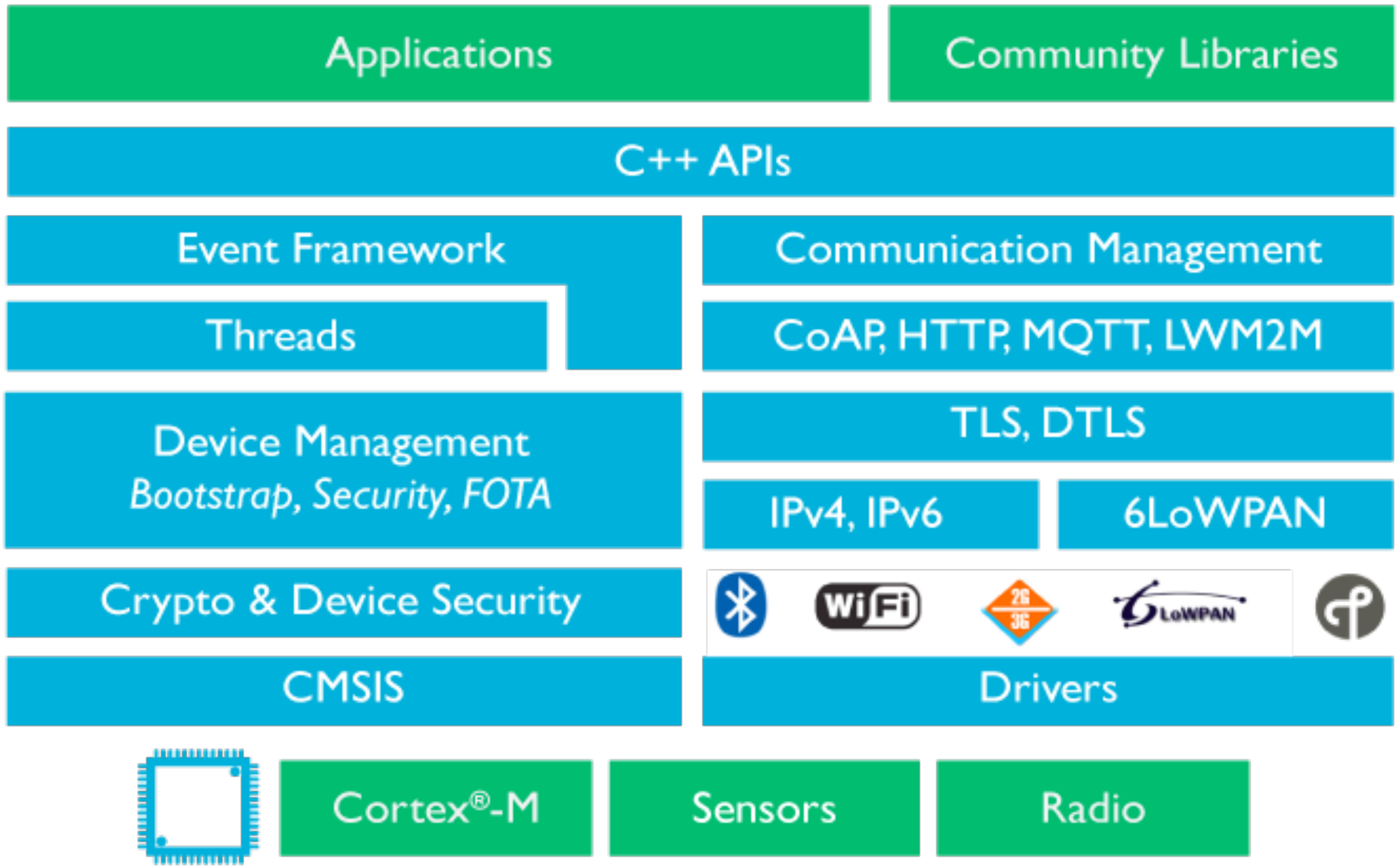

MACHXO2 BLOCK DIAGRAM (XO2-1200)
'Value added' features in and around the core
LATTICE SEMICONDUCTOR
On-chip Flash Memory Provides Instant-on, High Security & Single Chip Solution
sysIO Buffers Support LVCMOS/LVTTL, LVDS Outputs. I/O Logic Supports 7:1 Output Gearing
User Flash Memory
Embedded Function Block Hardened SPI, I2C, Timer/Counter
sysCLOCK PLLs Frequency Synthesis & Clock Alignment
sysIO Buffers Support LVCMOS/LVTTL, and DDR Memory Interfaces
sysMEM Block RAM 9Kbit Dual Port
Programmable Function Units (PFUs) with RAM
Flexible Routing Optimized for Speed, Low-Cost and Routability
sysIO Buffers Support LVCMOS/LVTTL, LVDS inputs and PCI. I/O Logic Supports 7:1 Input Gearing
Page: 5
Lattice Semiconductor

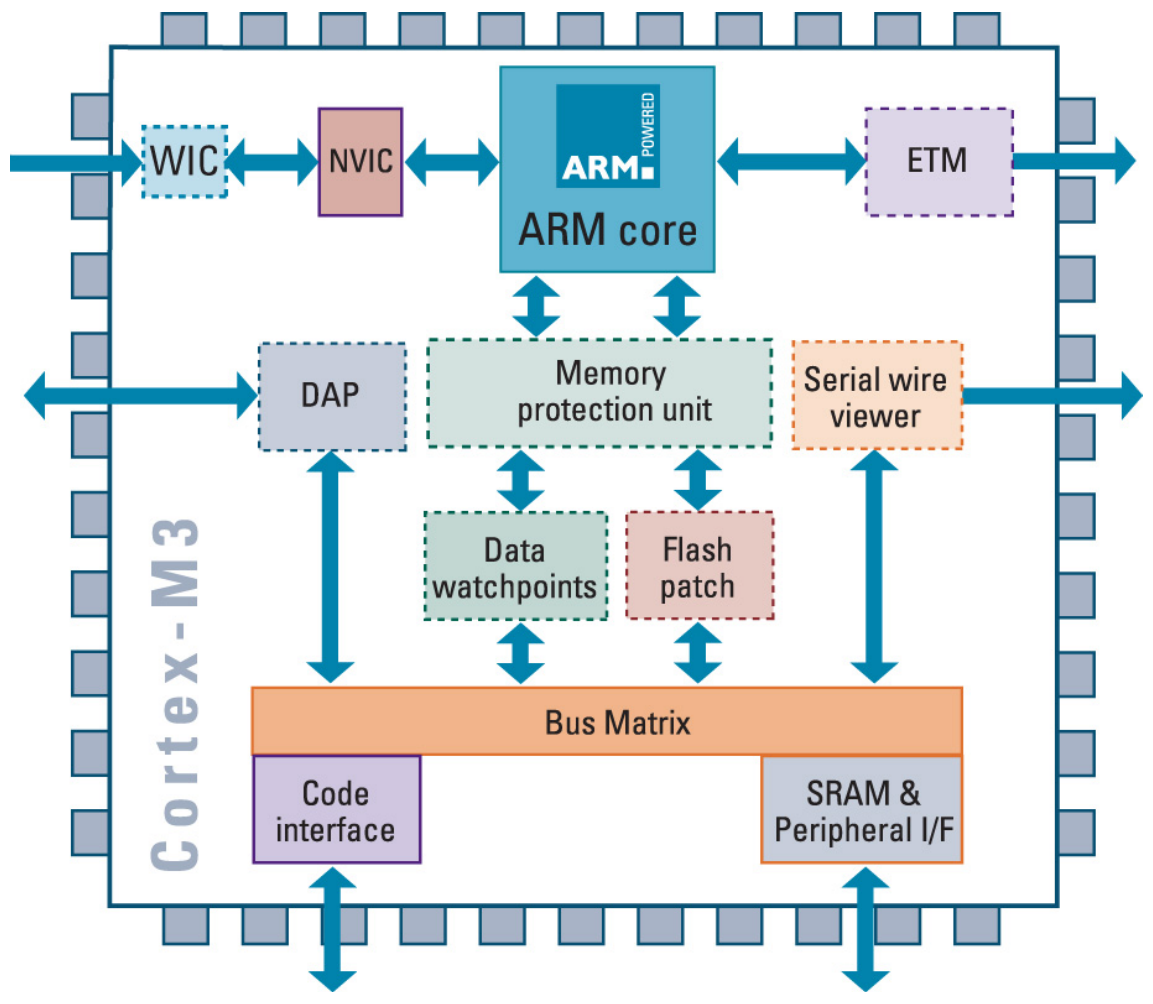

Interconnect Resources
I/O pin
Logic Block
Switch Block

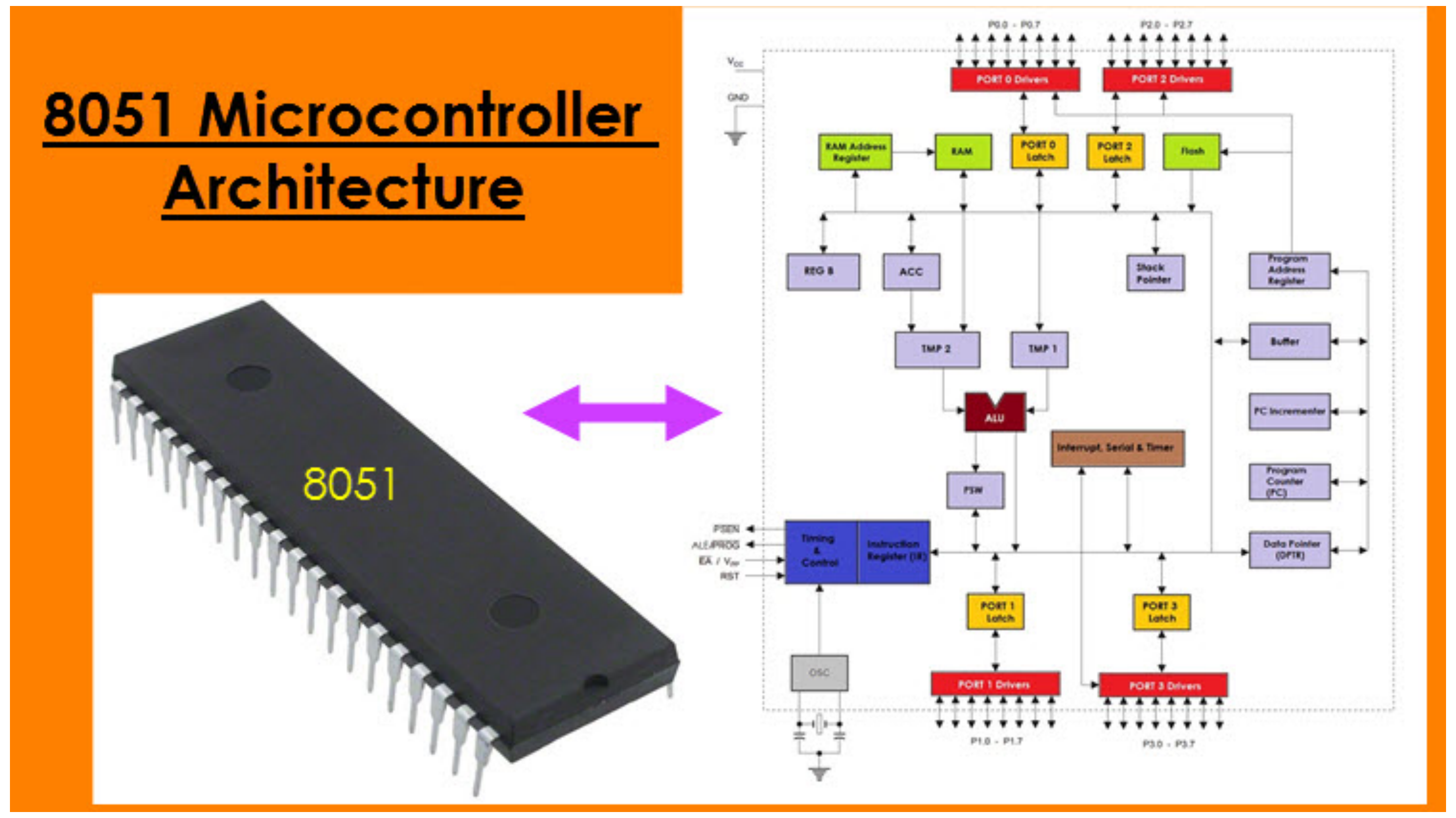

CLB
LUT
MUX
D-Flip Flop
Rst
Clk
FPGA Logic Block


DMA
ARM Cortex-A9 NEON/FPU L1 Cache
ARM Cortex-A9 NEON/FPU L1 Cache
UART (x2)
GPIO
L2 Cache
I2C (x2)
JTAG Debug/ Trace
WD (x2)
Timer (x4)
SPI
CAN (x2)
SD/ MMC
QSPI and NAND Flash Controller
Ethernet (x2)
USB OTG
Multiport DDR SDRAM Controller
To FPGA
From FPGA
FPGA Config
FPGA

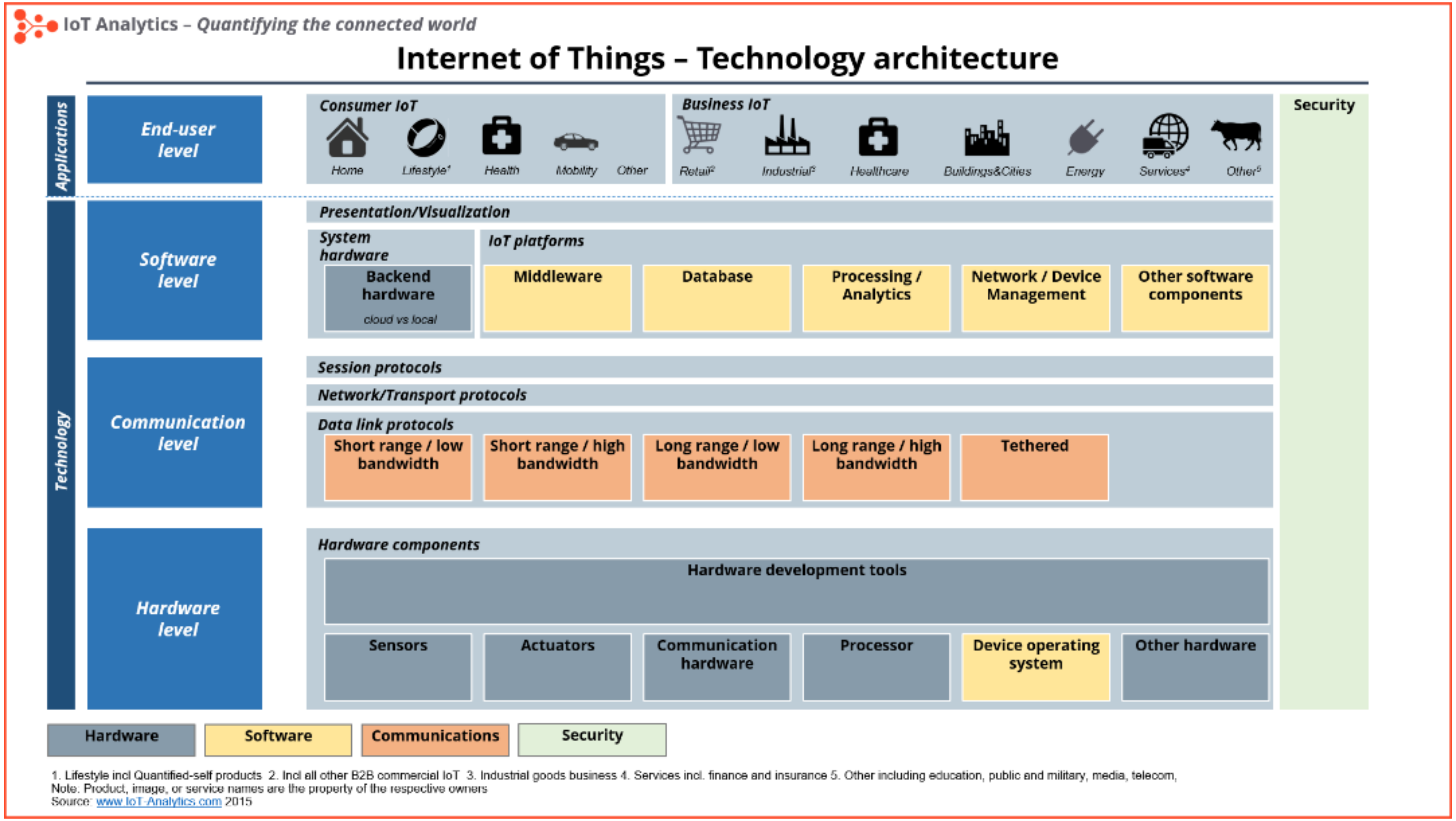
数字信号/逻辑处理

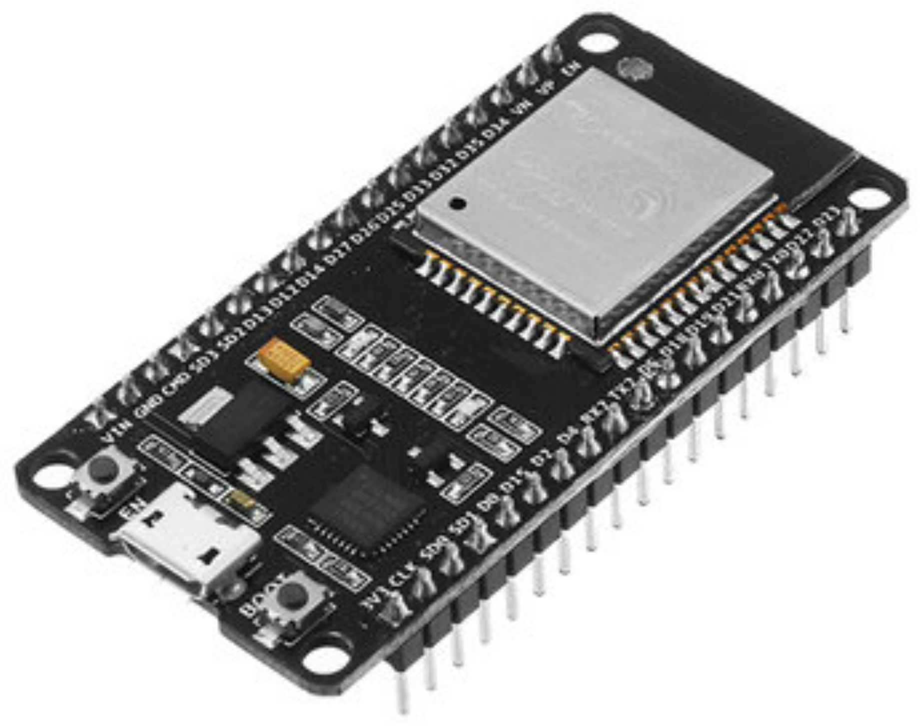






微处理器/微控制器：智能硬件/物联网产品的核心



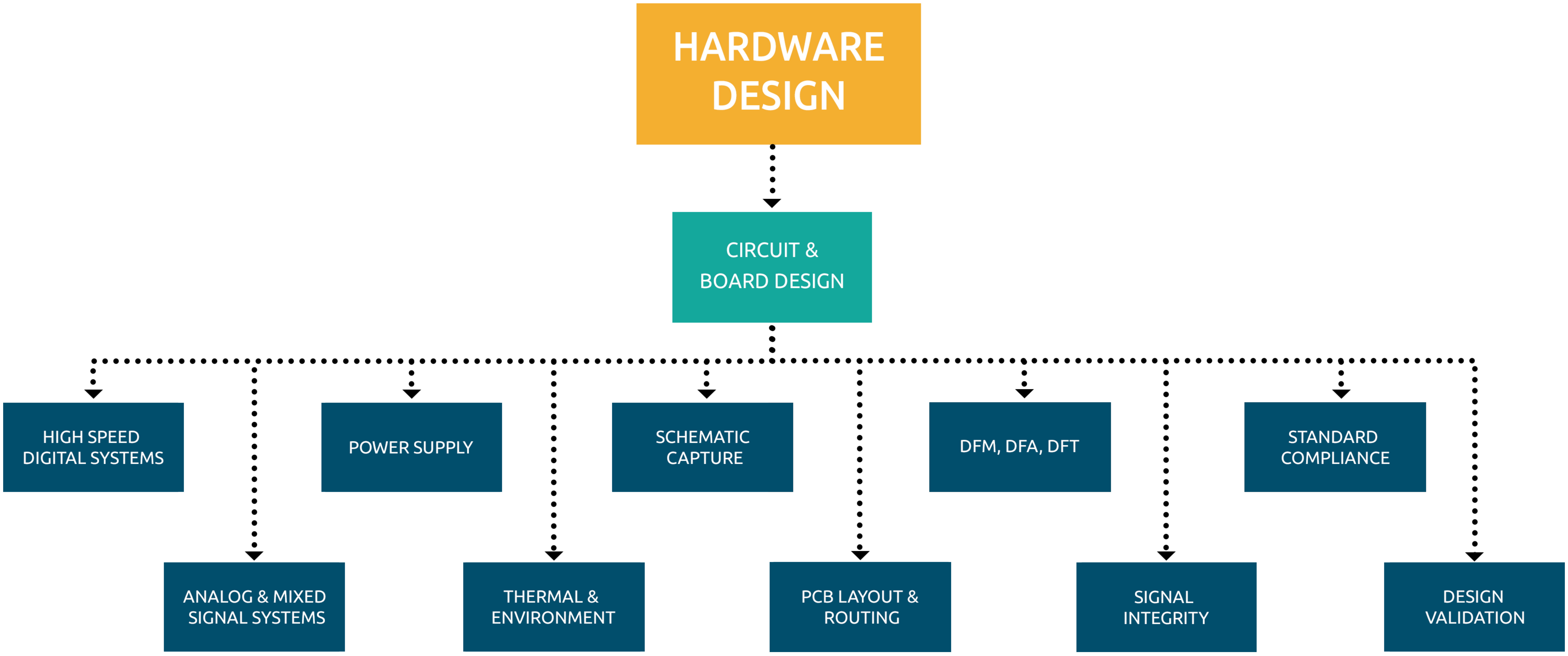


网络通信

物与物之间的连接

各部分的核心参数

电路	关键参数
电源	电压、负载能力、纹波、效率
传感器	灵敏度、接口方式
模拟链路	幅度、频带
A/D、D/A	转换率、分辨率、SFDR、接口方式
数字信号处理/FPGA	逻辑资源、存储资源、IO、速度
MPU/MCU	速度、接口、内部资源、开发环境
网络通信	通信方式、速率、接口、协议



PCB设计流程

从需求到可生产

设计流程本质上是一个将概念变成实际的、能够工作的系统的过程

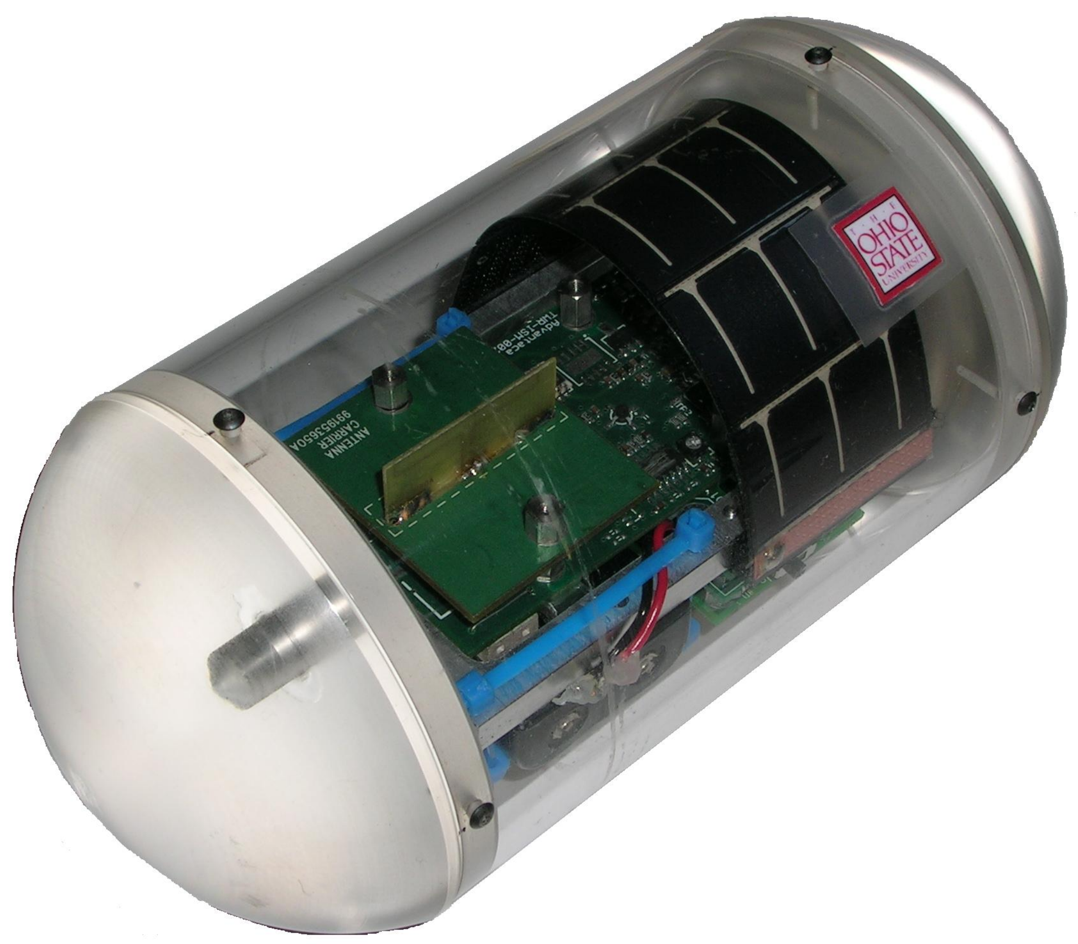
创意

(概念)

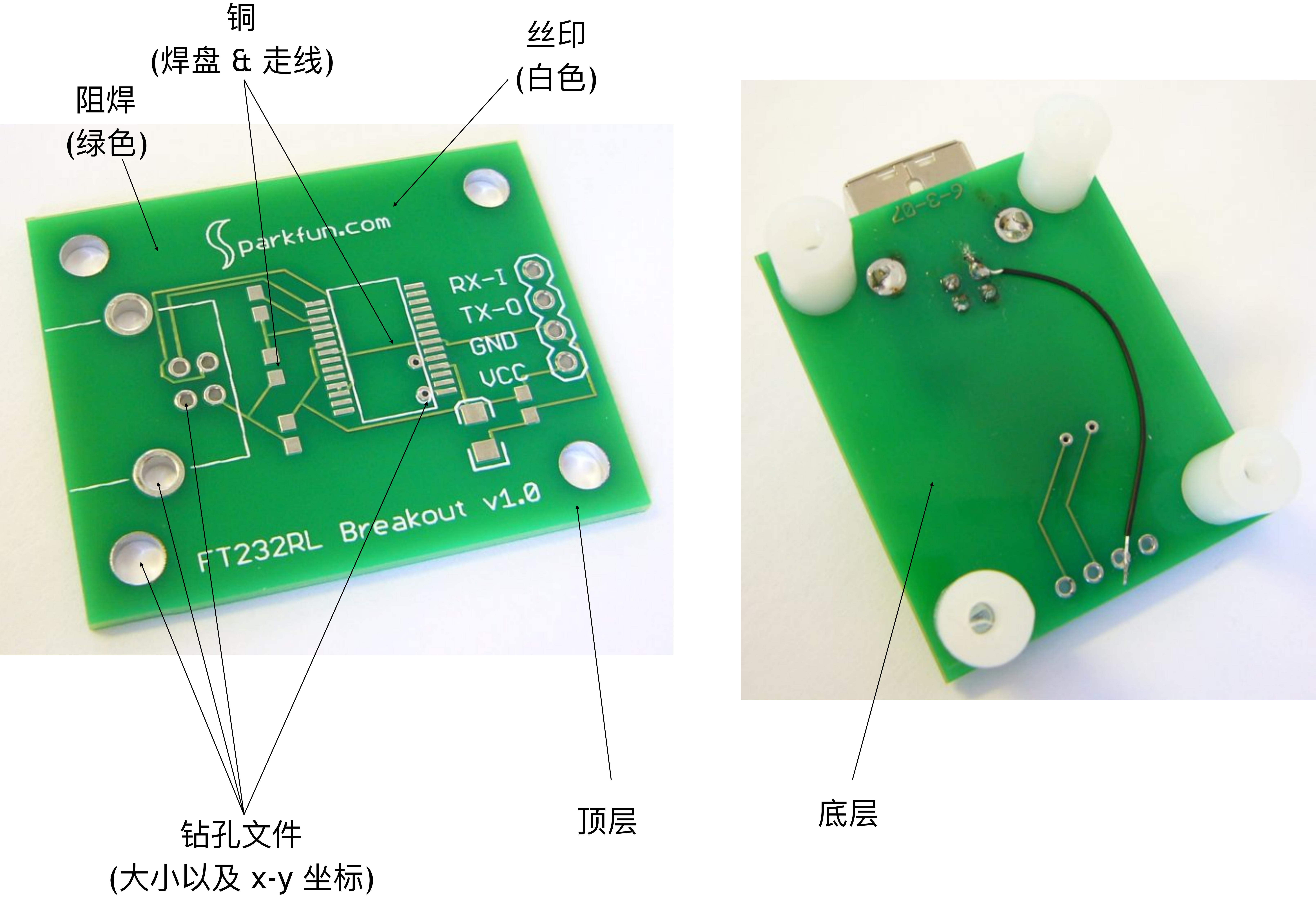
“一个可以空投式运动传感器 - 检测范围为10米，能使用6个月”

实施

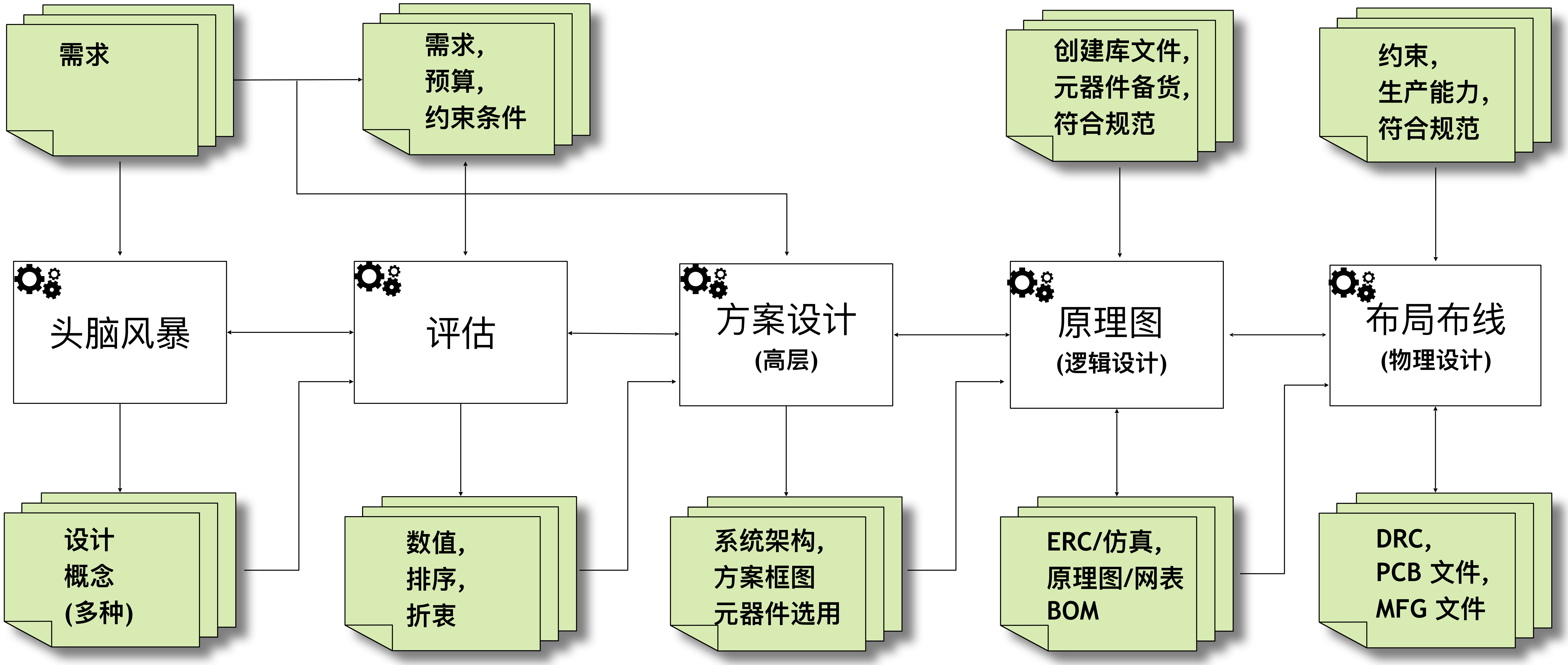
(能够工作的系统)



最终的目标是一个PCB板



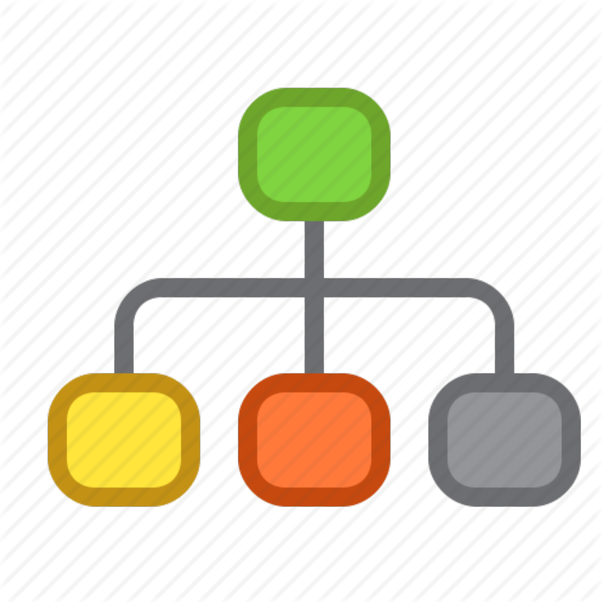
产品设计流程 - 规范化、时间节点



*通过模型、原型样机、讨论进行评估

头脑风暴

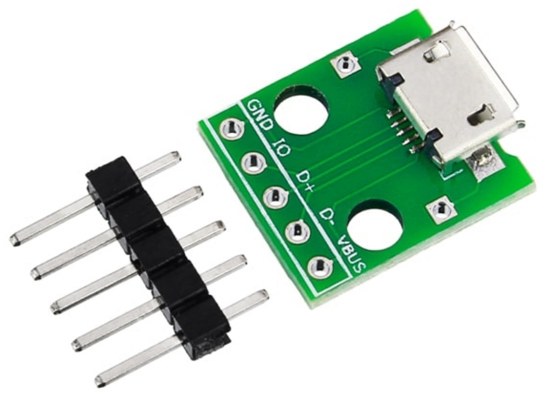
- 目标：越多的主意/方案越好
- 最好多人参与讨论，集思广益
- 根据需求，但不要受约束或正式需求的限制



框图/草稿

元器件

- 无源器件：0805、0603等
- IC封装：QFN、TQFP、BGA等
- 库



连接方式

- 机械连接
- 总线连接
- PC连接

供电和性能

- 功率要求
- 电池性能
- 高速/高灵敏度

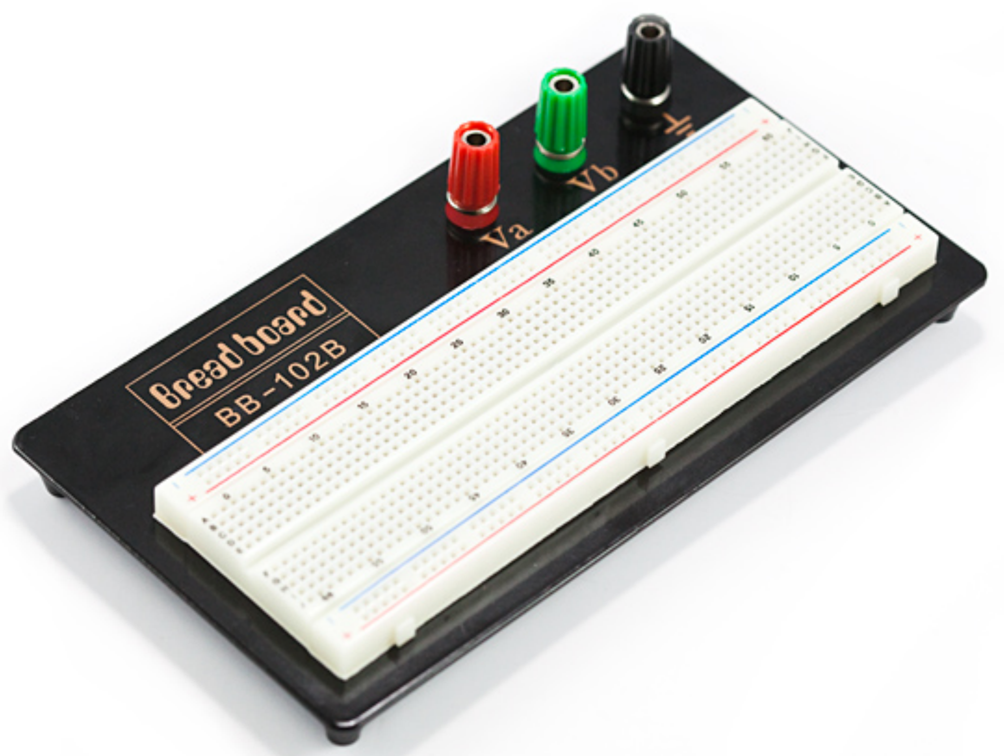
评估

- 目标：选出最佳的方案
- 用“需求”和“限制”来进行评估
- 同时考虑到：
  - 上市时间
  - 性价比 - 开发成本/单价
  - 熟悉程度
  - 备用方案

满足项目的需求：

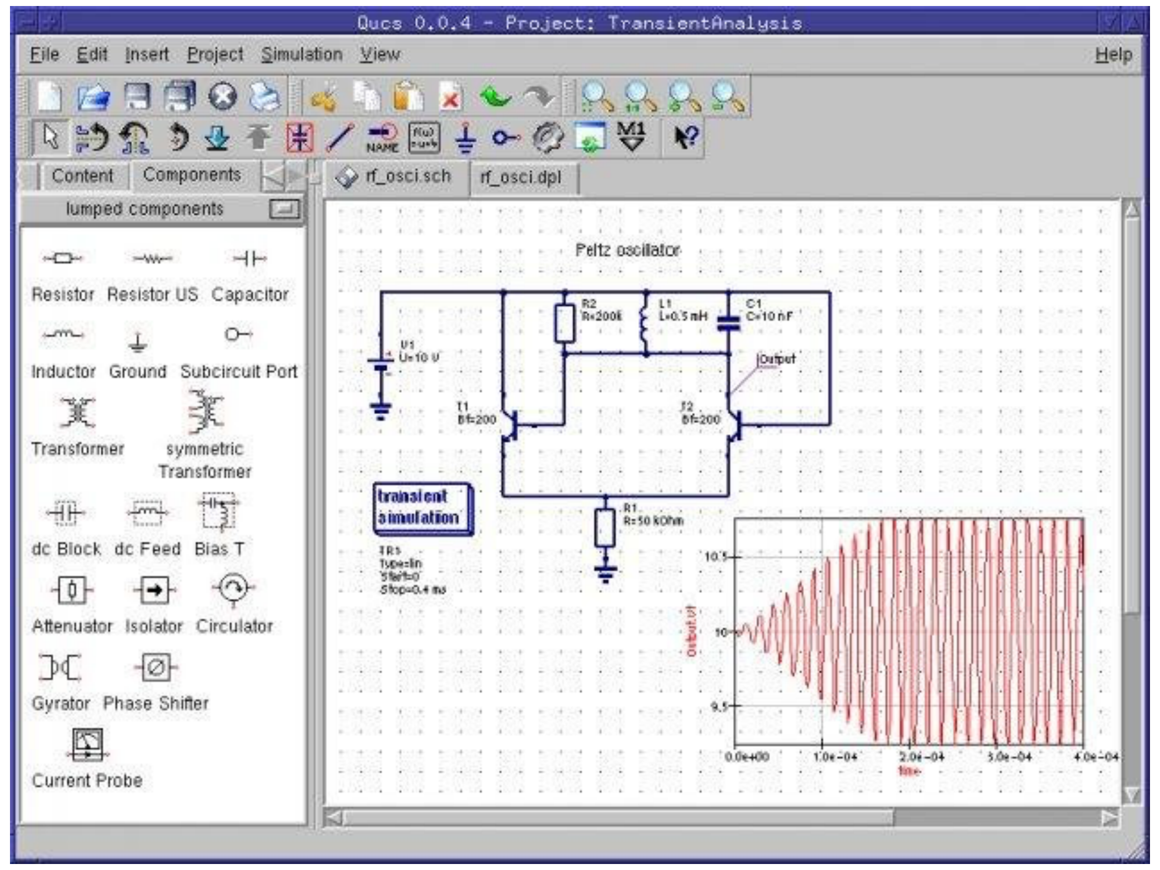
- 功能
- 性能
- 可用性
- 可靠性
- 可维护性
- 预算

电路测试评估



面包板

开发板



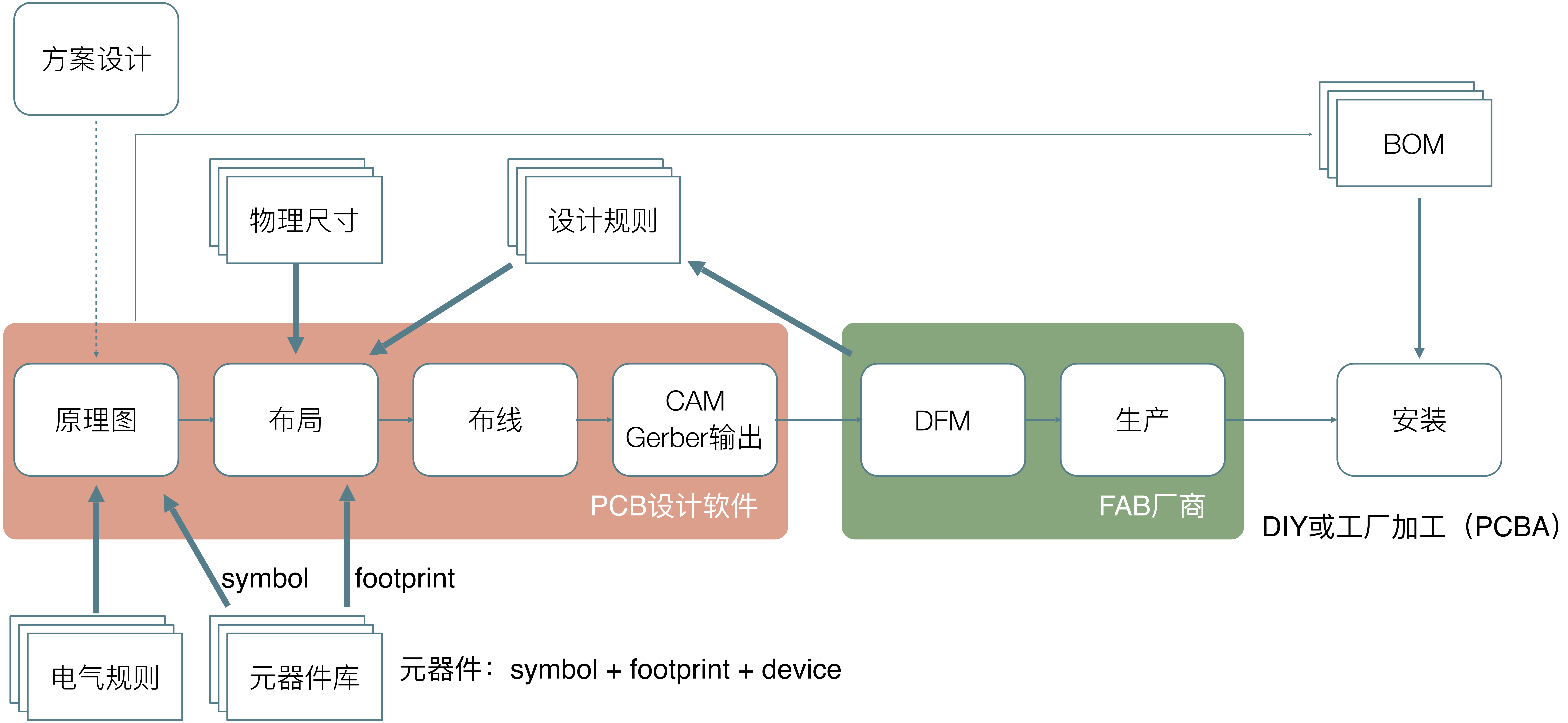
仿真

方案设计

- 将“概念”转变成“框图”
- 将“框图”转变成“元器件”
- Top-down：
  - 从高层次开始设计，逐级分解
  - 明确定义子系统的功能
  - 明确定义子系统的接口
- Bottom-up：
  - 从模块开始进行逐级集成
  - 在模块之间添加“glue logic”进行连接
- 组合：
  - 适用于子系统风险较高的复杂设计

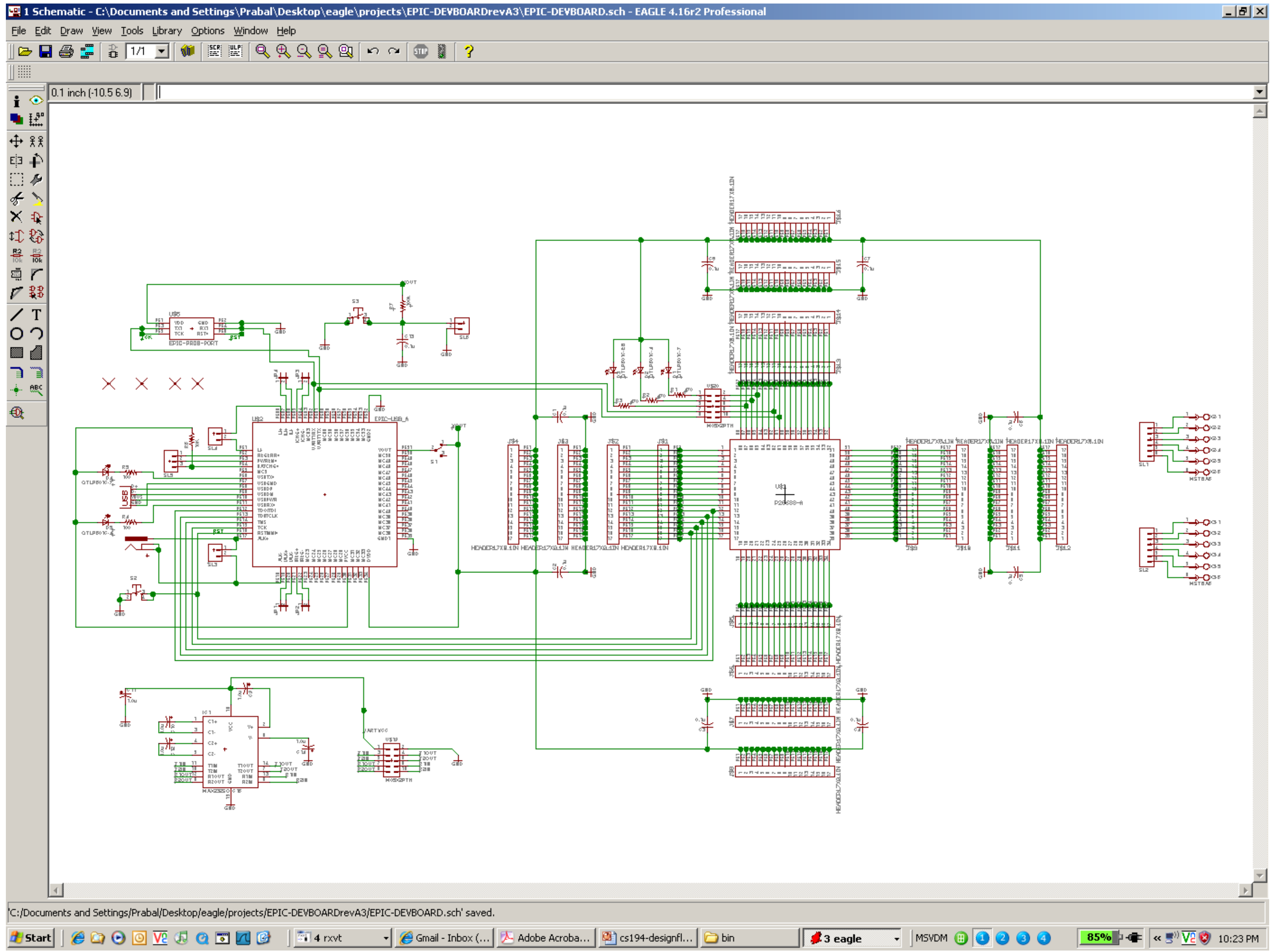
- 需要做很多重要的决定：
  - 模拟还是数字?
  - 3.3V还是5V?
  - 单芯片还是分立器件组合?
- 需要做很多折衷：
  - 高分辨率还是低功耗?
  - 同样的供电系统 - 是较高的数率还是较长的传输距离?
- 一个改变有可能会影响到整个系统的改变
  - 尽可能避免这种设计
  - 在复杂的、高度优化的系统中很难

从原理图到生产文件输出



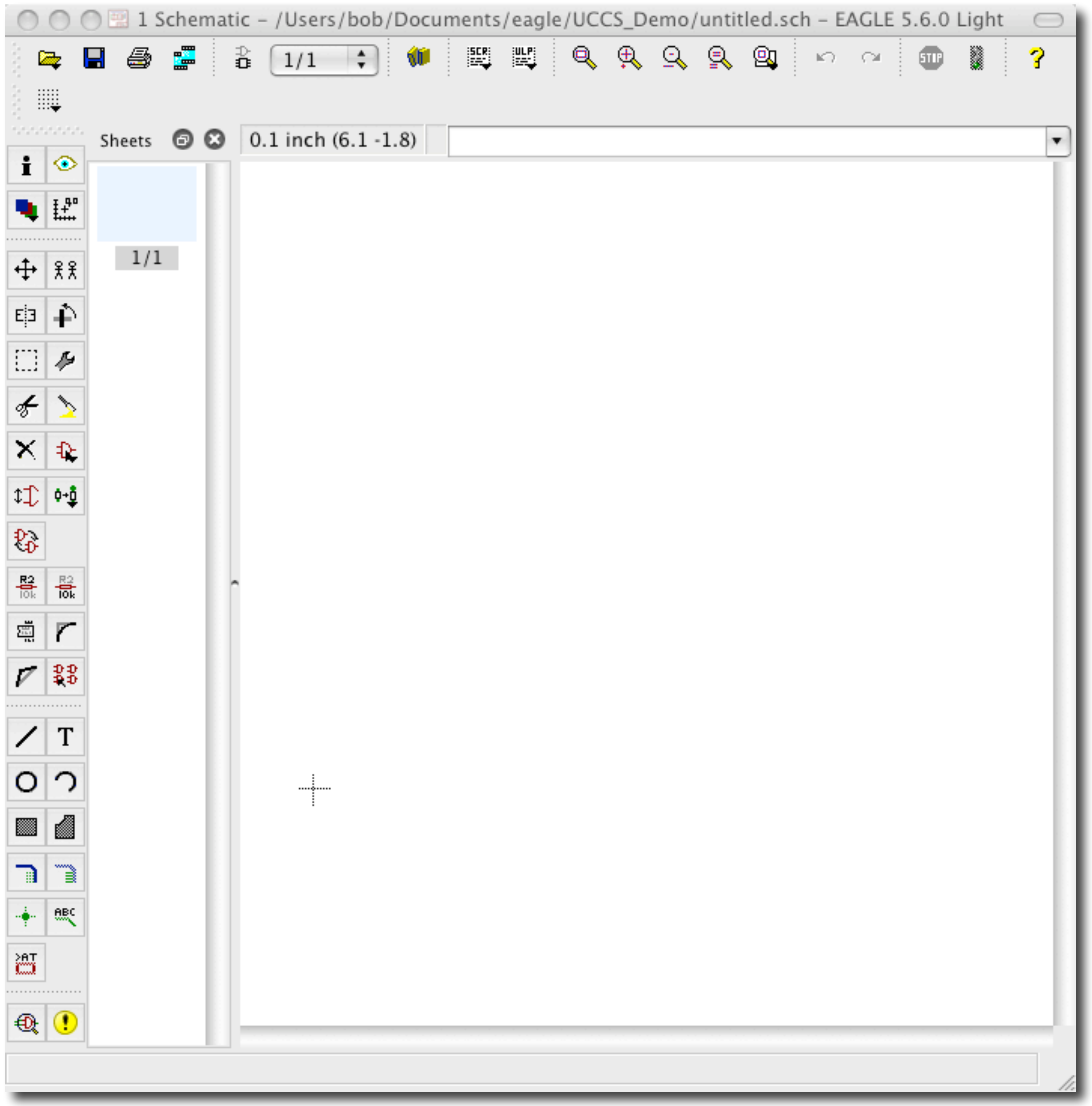
原理图绘制就是将框图转化成详细的设计，是一个逻辑设计的过程

- 器件选择
  - 是不是已经在库里?
    - 是: 好，就用它! (但需要认真确认!)
    - 否: 必须先创建一个原理图符号.
  - 是不是有现货?
    - 是: 好，就用它！ (确认其封装)
    - 否: 挑选不同的器件 (确认供货时间)
  - 是不是符合预算?
  - 电压是否正好合适? 注意: 1.8V, 3.3V, 5.0V
- 粗略的规划一下
- 放置器件
- 连接器件
- 针对布局布线的标注(比如 50 ohm走线,去藕电容的位置等)



画原理图1 - 创建一个新的原理图

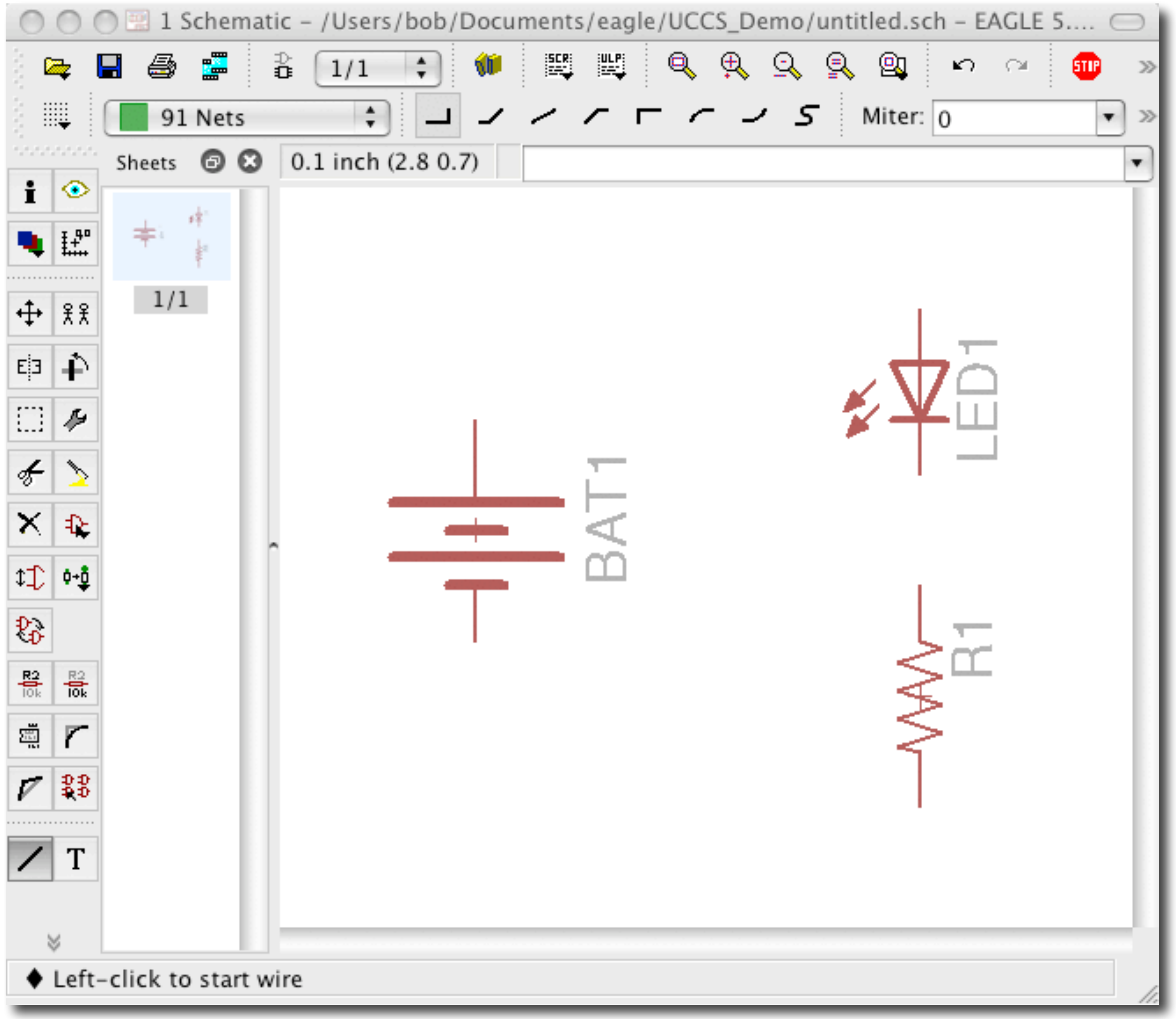
- File -> New -> Schematic
- 随时保存
- 暂时还不需要关心实际的电路板
- 最好设定100-mil的grid.



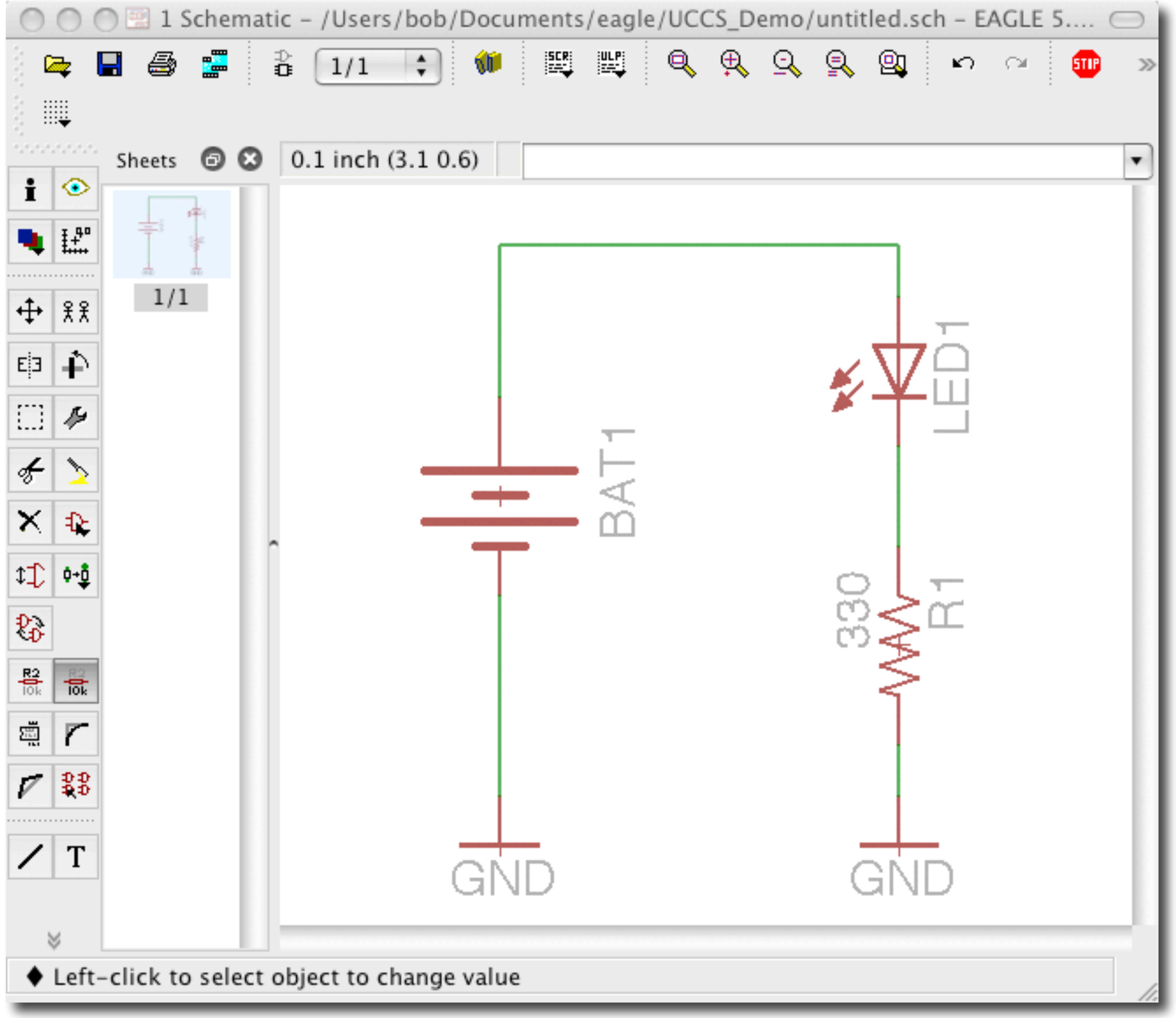
画原理图2 - 添加一个器件

添加一个器件

- 点击添加按钮
- 从库中选择适当的器件
- 设置器件的“值”
- 如果库中没有需要的器件，那就在库中创建一个



画原理图3 - 通过连线（Track又叫Trace）将器件的管脚连接



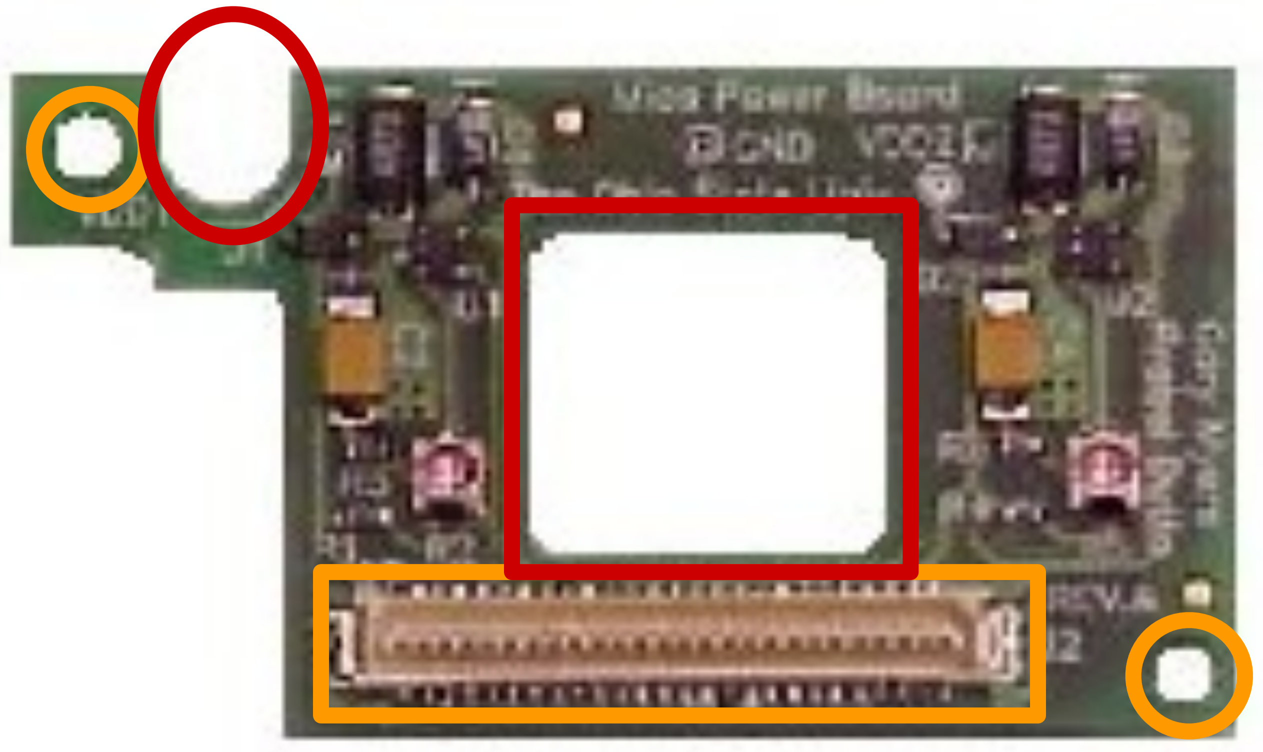
布局布线就是将原理图（通过网表）转换成适合生产加工的一系列Gerber和钻孔文件的过程

- 输入: 原理图 (或网表)
- 使用: 器件库
- 输出
  - Gerbers 光绘文件 (top, bottom, middle layers)
    - Copper
    - Soldermask
    - Silkscreen
  - NC打孔文件
    - 孔径大小
    - X-Y位置
  - 生产图
    - 器件名字和位置
    - Pick & place文件

- 要做的事情
  - 创建器件
  - 设定板子的外形尺寸
  - 布图规划
  - 选择层数并定义各层的功能
  - 放置器件（调用库）
  - 手工布线(地/电源, RF信号等)
  - 自动布线 (非关键的信号)
  - 设计规则检查 (DRC)

在约束条件下的布局和布线

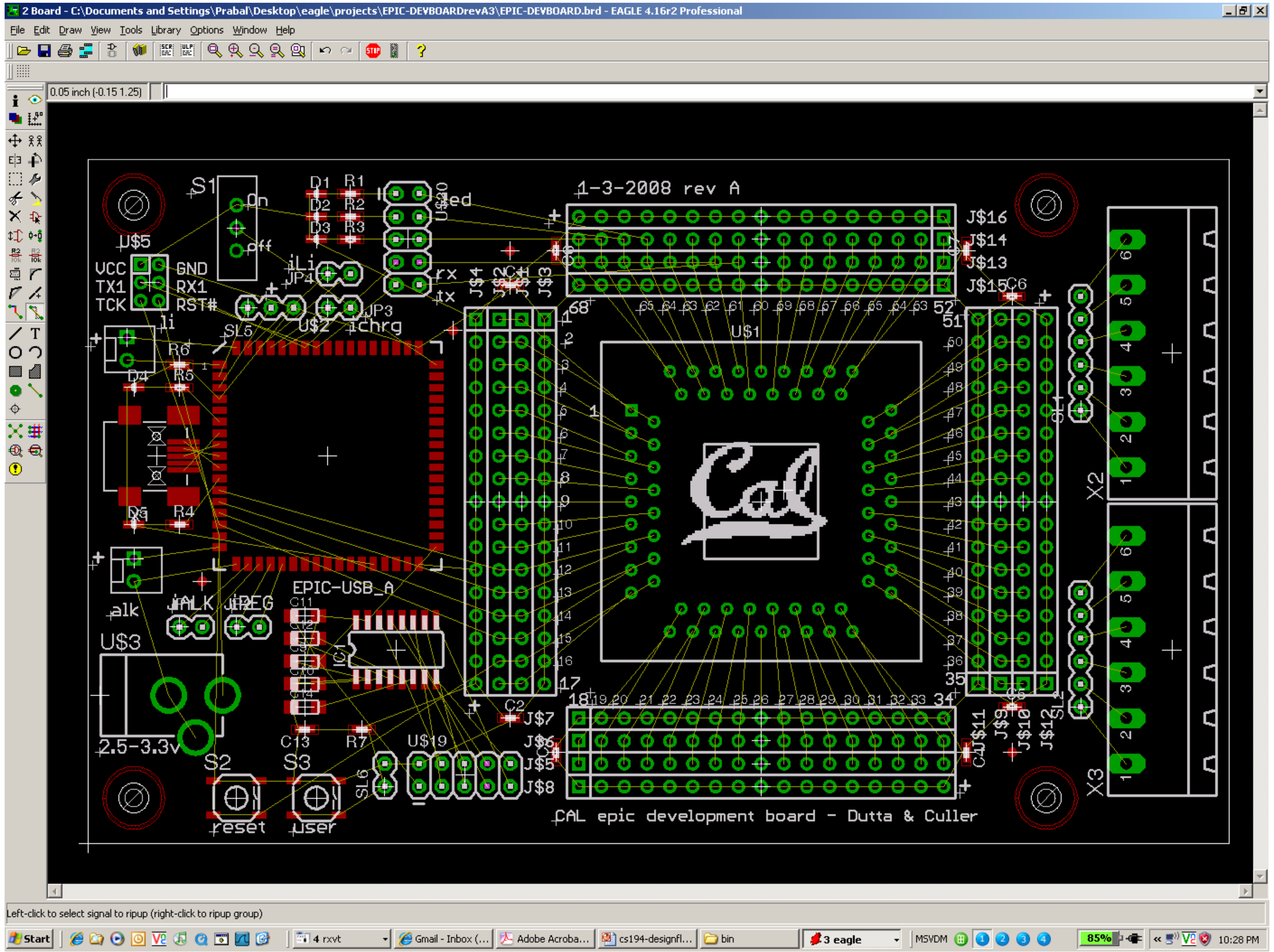
- “约束”会影响到板子的大小、元器件的放置位置、电路板层数的选择等
- 在布局的时候需要先根据“约束条件”设定“规则”来限定板子的布局和布线
  - 同其它板卡或系统连接的要求 - 板卡尺寸、定位孔、接插件位置
  - 制板厂的加工工艺要求 - 线宽、间距、过孔孔径等
  - 成本要求
  - 关键元器件的空间要求， 比如温度传感器附近不能有功率器件（发热）
  - 标准规范 - 无线通信、EMC等



CAPABILITY

Materials	FR4, Rogers4003/4350, GETEK, High Tg FR4
Flammability	UL 94V-0
Minimum Line/Space	4/4 mils
Maximum Board Sizes	18" x 24"
Minimum Hole Size	8 mils(finished PTH)
Minimum Pad Size	18 mils
Copper Weight	1/2 oz, 1 oz , 2 oz, 3 oz, 4 oz
Maximum Layer Count	14 (in production)
Soldermask Color	Green, Yellow, Black, Blue, Red, White
Registration	+/- 5 mils(Max.)
Minimum Board Thickness	0.008" for 2-layer, 0.016" for 4-layer, 0.019" for 6-layer
Impedance Control	+/- 10%(in house TDR tester)
Surface Finish	HAL, Immersion Gold, Immersion Tin, ENTEK
Dimensional Tolerance	+/- 0.005"
Aspect Ratio	< 8 : 1
Annular Ring	0.002"
Blind/Bried Vias	Sequential Lamination
Electroplating Gold	up to 30u" plus

关键元器件的布局


2 Board - C:\Documents and Settings\Prabal\Desktop\eagle\projects\EPIC-DEVBOARDrevA3\EPIC-DEVBOARD.brd - EAGLE 4.16r2 Professional
File Edit Draw View Tools Library Options Window Help
0.05 inch (-0.15 1.25)
1-3-2008 rev A
CAL epic development board - Dutta & Culler
EPIC-USB_A
U$1
U$2
U$3
U$5
U$19
S1
S2
S3
reset
user
VCC
TX1
TCK
GND
RX1
RST#
2.5-3.3v
J$16
J$14
J$13
J$15
J$7
J$6
J$5
J$8
X2
X3
Left-click to select signal to ripup (right-click to ripup group)
Start
3 eagle
10:28 PM

元器件数据手册的利用

- 认真阅读元器件相应的数据手册
- 确定是最终的官方版本的数据手册（www.datasheet5.com）
- 参考原厂提供的参考设计的原理图库、连接方式
- 严格按照数据手册中提供的封装信息进行PCB封装库的构建，一个器件一般会有多个不同的封装，元器件型号（Part number）要对应于器件的正确封装信息
- 尤其注意电源、时钟管脚、差分信号等的连接需求

基本信息汇总 - 第一页

- 型号、基本描述
- 功能、特性
- 应用
- 功能框图
- 封装信息

ANALOG DEVICES

3-Axis, ±2 *g*/±4 *g*/±8 *g*/±16 *g* Digital Accelerometer

Data Sheet **ADXL345**

FEATURES

Ultralow power: as low as 23 μA in measurement mode and 0.1 μA in standby mode at V_S = 2.5 V (typical)
Power consumption scales automatically with bandwidth
User-selectable resolution
Fixed 10-bit resolution
Full resolution, where resolution increases with *g* range, up to 13-bit resolution at ±16 *g* (maintaining 4 mg/LSB scale factor in all *g* ranges)
Embedded memory management system with FIFO technology minimizes host processor load
Single tap/double tap detection
Activity/inactivity monitoring
Free-fall detection
Supply voltage range: 2.0 V to 3.6 V
I/O voltage range: 1.7 V to V_S
SPI (3- and 4-wire) and I²C digital interfaces
Flexible interrupt modes mappable to either interrupt pin
Measurement ranges selectable via serial command
Bandwidth selectable via serial command
Wide temperature range (−40°C to +85°C)
10,000 *g* shock survival
Pb free/RoHS compliant
Small and thin: 3 mm × 5 mm × 1 mm LGA package

APPLICATIONS

Handsets
Medical instrumentation
Gaming and pointing devices
Industrial instrumentation
Personal navigation devices
Hard disk drive (HDD) protection

GENERAL DESCRIPTION

The ADXL345 is a small, thin, ultralow power, 3-axis accelerometer with high resolution (13-bit) measurement at up to ±16 *g*. Digital output data is formatted as 16-bit twos complement and is accessible through either a SPI (3- or 4-wire) or I²C digital interface.

The ADXL345 is well suited for mobile device applications. It measures the static acceleration of gravity in tilt-sensing applications, as well as dynamic acceleration resulting from motion or shock. Its high resolution (3.9 mg/LSB) enables measurement of inclination changes less than 1.0°.

Several special sensing functions are provided. Activity and inactivity sensing detect the presence or lack of motion by comparing the acceleration on any axis with user-set thresholds. Tap sensing detects single and double taps in any direction. Free-fall sensing detects if the device is falling. These functions can be mapped individually to either of two interrupt output pins. An integrated memory management system with a 32-level first in, first out (FIFO) buffer can be used to store data to minimize host processor activity and lower overall system power consumption.

Low power modes enable intelligent motion-based power management with threshold sensing and active acceleration measurement at extremely low power dissipation.

The ADXL345 is supplied in a small, thin, 3 mm × 5 mm × 1 mm, 14-lead, plastic package.

FUNCTIONAL BLOCK DIAGRAM

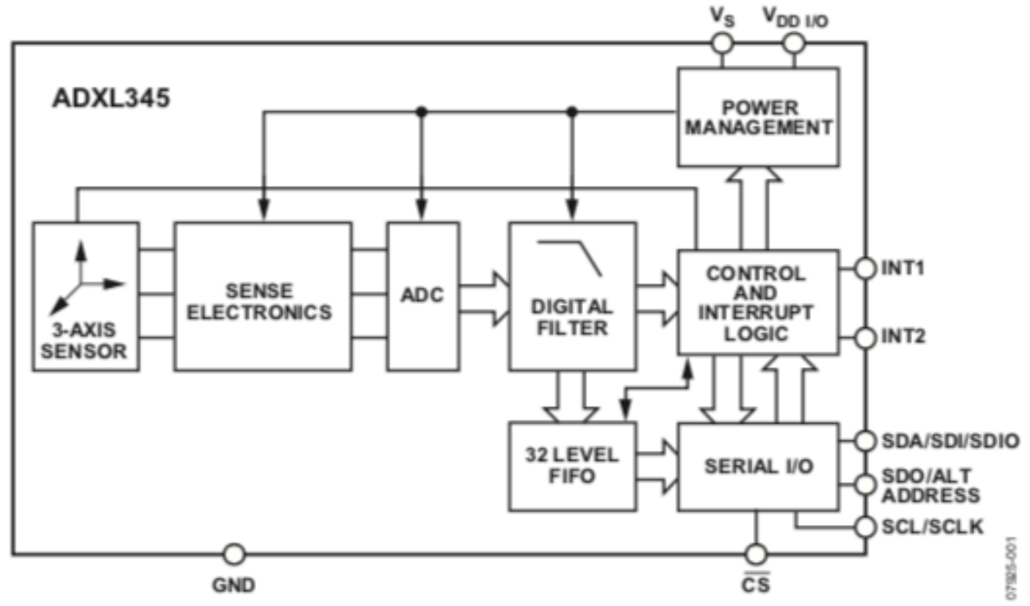


Figure 1.

Rev. E Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

管脚定义

- 管脚编号
- 每个管脚的功能
- 物理上的排列方式
- 注意不同的封装其定义不同
- 管脚1的位置
- 散热/接地管脚
- Vcc、Vdd、Vs、CLK、CLR、NC
- 低电平有效

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

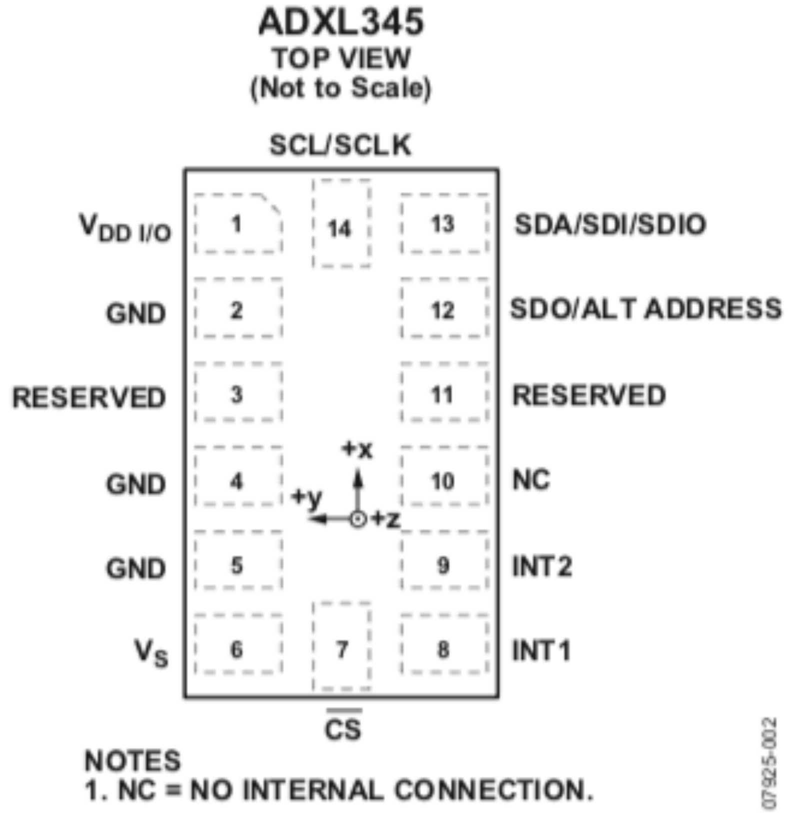


Figure 3. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{DD\ I/O}$	Digital Interface Supply Voltage.
2	GND	This pin must be connected to ground.
3	RESERVED	Reserved. This pin must be connected to V_S or left open.
4	GND	This pin must be connected to ground.
5	GND	This pin must be connected to ground.
6	V_S	Supply Voltage.
7	$\overline{CS}$	Chip Select.
8	INT1	Interrupt 1 Output.
9	INT2	Interrupt 2 Output.
10	NC	Not Internally Connected.
11	RESERVED	Reserved. This pin must be connected to ground or left open.
12	SDO/ALT ADDRESS	Serial Data Output (SPI 4-Wire)/Alternate I^2C Address Select (I^2C).
13	SDA/SDI/SDIO	Serial Data (I^2C)/Serial Data Input (SPI 4-Wire)/Serial Data Input and Output (SPI 3-Wire).
14	SCL/SCLK	Serial Communications Clock. SCL is the clock for I^2C, and SCLK is the clock for SPI.

极限工作和推荐工作条件

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	10,000 *g*
Any Axis, Powered	10,000 *g*
V_S	−0.3 V to +3.9 V
$V_{DD\ I/O}$	−0.3 V to +3.9 V
Digital Pins	−0.3 V to $V_{DD\ I/O}$ + 0.3 V or 3.9 V, whichever is less
All Other Pins	−0.3 V to +3.9 V
Output Short-Circuit Duration (Any Pin to Ground)	Indefinite
Temperature Range	
Powered	−40°C to +105°C
Storage	−40°C to +105°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

SPECIFICATIONS

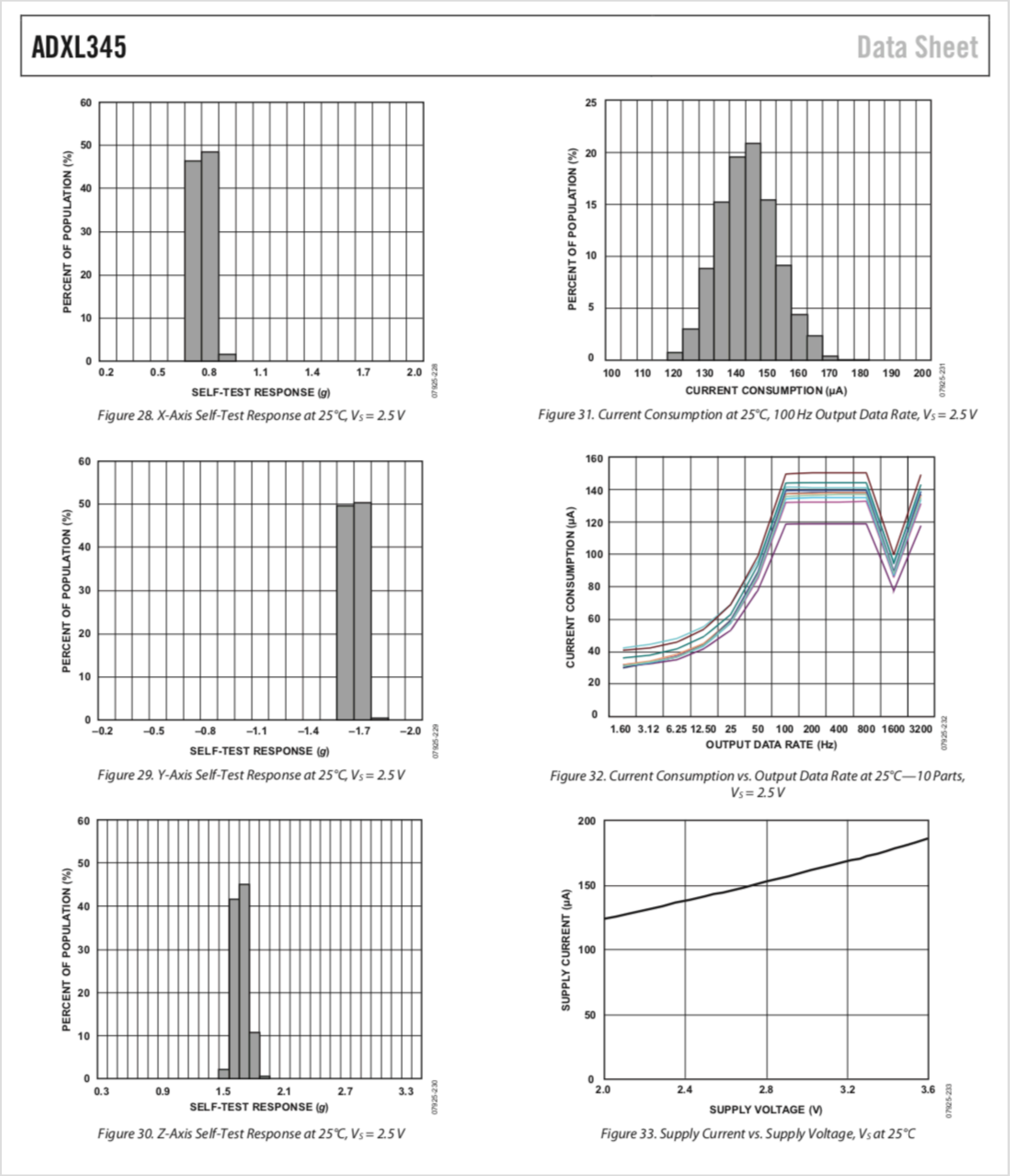
T_A = 25°C, V_S = 2.5 V, $V_{DD\ I/O}$ = 1.8 V, acceleration = 0 *g*, C_S = 10 µF tantalum, $C_{I/O}$ = 0.1 µF, output data rate (ODR) = 800 Hz, unless otherwise noted. All minimum and maximum specifications are guaranteed. Typical specifications are not guaranteed.

Table 1.

Parameter	Test Conditions	Min	Typ[1]	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range	User selectable		±2, ±4, ±8, ±16		*g*
Nonlinearity	Percentage of full scale		±0.5		%
Inter-Axis Alignment Error			±0.1		Degrees
Cross-Axis Sensitivity[2]			±1		%
OUTPUT RESOLUTION	Each axis				
All *g* Ranges	10-bit resolution		10		Bits
±2 *g* Range	Full resolution		10		Bits
±4 *g* Range	Full resolution		11		Bits
±8 *g* Range	Full resolution		12		Bits
±16 *g* Range	Full resolution		13		Bits
SENSITIVITY	Each axis				
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	All *g*-ranges, full resolution	230	256	282	LSB/*g*
	±2 *g*, 10-bit resolution	230	256	282	LSB/*g*
	±4 *g*, 10-bit resolution	115	128	141	LSB/*g*
	±8 *g*, 10-bit resolution	57	64	71	LSB/*g*
	±16 *g*, 10-bit resolution	29	32	35	LSB/*g*
Sensitivity Deviation from Ideal	All *g*-ranges		±1.0		%
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	All *g*-ranges, full resolution	3.5	3.9	4.3	m*g*/LSB
	±2 *g*, 10-bit resolution	3.5	3.9	4.3	m*g*/LSB
	±4 *g*, 10-bit resolution	7.1	7.8	8.7	m*g*/LSB
	±8 *g*, 10-bit resolution	14.1	15.6	17.5	m*g*/LSB
	±16 *g*, 10-bit resolution	28.6	31.2	34.5	m*g*/LSB
Sensitivity Change Due to Temperature			±0.01		%/°C
0 *g* OFFSET	Each axis				
0 *g* Output for X_{OUT}, Y_{OUT}		−150	0	+150	m*g*
0 *g* Output for Z_{OUT}		−250	0	+250	m*g*
0 *g* Output Deviation from Ideal, X_{OUT}, Y_{OUT}			±35		m*g*
0 *g* Output Deviation from Ideal, Z_{OUT}			±40		m*g*
0 *g* Offset vs. Temperature for X-, Y-Axes			±0.4		m*g*/°C
0 *g* Offset vs. Temperature for Z-Axis			±1.2		m*g*/°C
NOISE					
X-, Y-Axes	ODR = 100 Hz for ±2 *g*, 10-bit resolution or all *g*-ranges, full resolution		0.75		LSB rms
Z-Axis	ODR = 100 Hz for ±2 *g*, 10-bit resolution or all *g*-ranges, full resolution		1.1		LSB rms
OUTPUT DATA RATE AND BANDWIDTH	User selectable				
Output Data Rate (ODR)[3,4,5]		0.1		3200	Hz
SELF-TEST[6]					
Output Change in X-Axis		0.20		2.10	*g*
Output Change in Y-Axis		−2.10		−0.20	*g*
Output Change in Z-Axis		0.30		3.40	*g*
POWER SUPPLY					
Operating Voltage Range (V_S)		2.0	2.5	3.6	V
Interface Voltage Range ($V_{DD\ I/O}$)		1.7	1.8	V_S	V
Supply Current	ODR ≥ 100 Hz		140		µA
	ODR < 10 Hz		30		µA
Standby Mode Leakage Current			0.1		µA
Turn-On and Wake-Up Time[7]	ODR = 3200 Hz		1.4		ms

关键性能和各参数之间的曲线

- 参数变量之间的关系
- 电流 vs 电压
- 灵敏度 vs 温度
- 要让器件工作在“安全区”



应用中要特别注意的地方

- 供电
- 接地
- 时钟
- 物理连接

APPLICATIONS INFORMATION

POWER SUPPLY DECOUPLING

A 1 μF tantalum capacitor (C_S) at V_S and a 0.1 μF ceramic capacitor ($C_{I/O}$) at $V_{DD\ I/O}$ placed close to the ADXL345 supply pins is recommended to adequately decouple the accelerometer from noise on the power supply. If additional decoupling is necessary, a resistor or ferrite bead, no larger than 100 Ω, in series with V_S may be helpful. Additionally, increasing the bypass capacitance on V_S to a 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor may also improve noise.

Care should be taken to ensure that the connection from the ADXL345 ground to the power supply ground has low impedance because noise transmitted through ground has an effect similar to noise transmitted through V_S. It is recommended that V_S and $V_{DD\ I/O}$ be separate supplies to minimize digital clocking noise on the V_S supply. If this is not possible, additional filtering of the supplies, as previously mentioned, may be necessary.

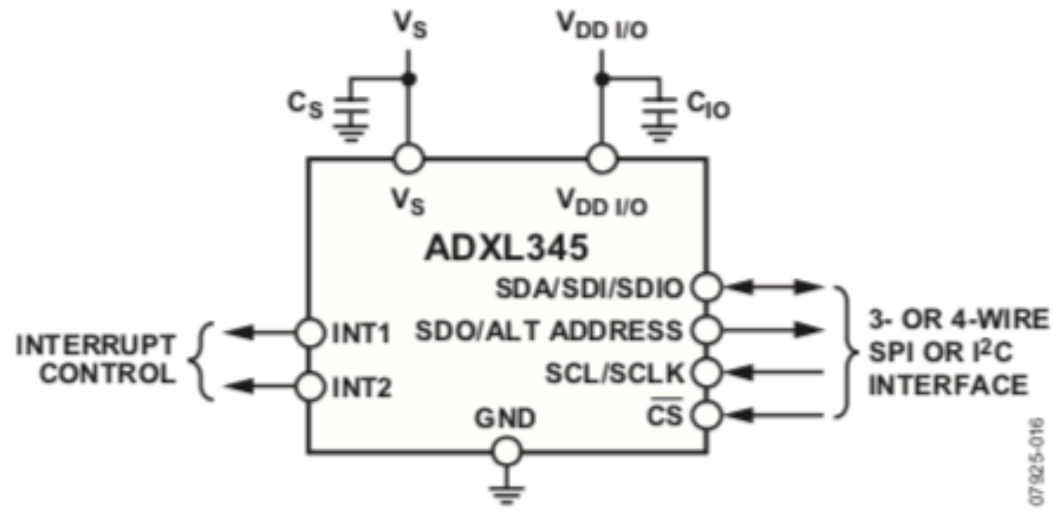


Figure 44. Application Diagram

MECHANICAL CONSIDERATIONS FOR MOUNTING

The ADXL345 should be mounted on the PCB in a location close to a hard mounting point of the PCB to the case. Mounting the ADXL345 at an unsupported PCB location, as shown in Figure 45, may result in large, apparent measurement errors due to undampened PCB vibration. Locating the accelerometer near a hard mounting point ensures that any PCB vibration at the accelerometer is above the accelerometer's mechanical sensor resonant frequency and, therefore, effectively invisible to the accelerometer. Multiple mounting points, close to the sensor, and/or a thicker PCB also help to reduce the effect of system resonance on the performance of the sensor.

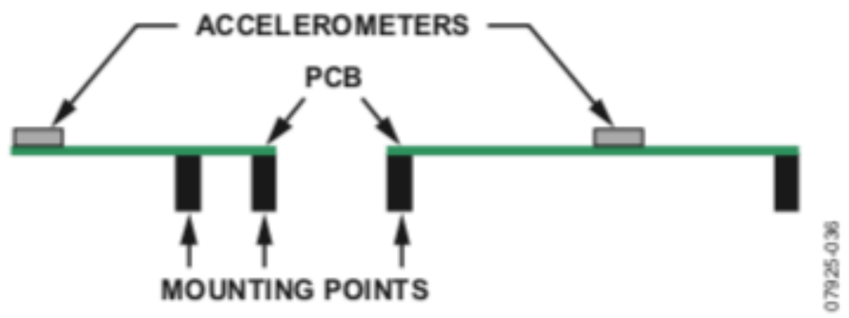


Figure 45. Incorrectly Placed Accelerometers

TAP DETECTION

The tap interrupt function is capable of detecting either single or double taps. The following parameters are shown in Figure 46 for a valid single and valid double tap event:

- The tap detection threshold is defined by the THRESH_TAP register (Address 0x1D).
- The maximum tap duration time is defined by the DUR register (Address 0x21).
- The tap latency time is defined by the latent register (Address 0x22) and is the waiting period from the end of the first tap until the start of the time window, when a second tap can be detected, which is determined by the value in the window register (Address 0x23).
- The interval after the latency time (set by the latent register) is defined by the window register. Although a second tap must begin after the latency time has expired, it need not finish before the end of the time defined by the window register.

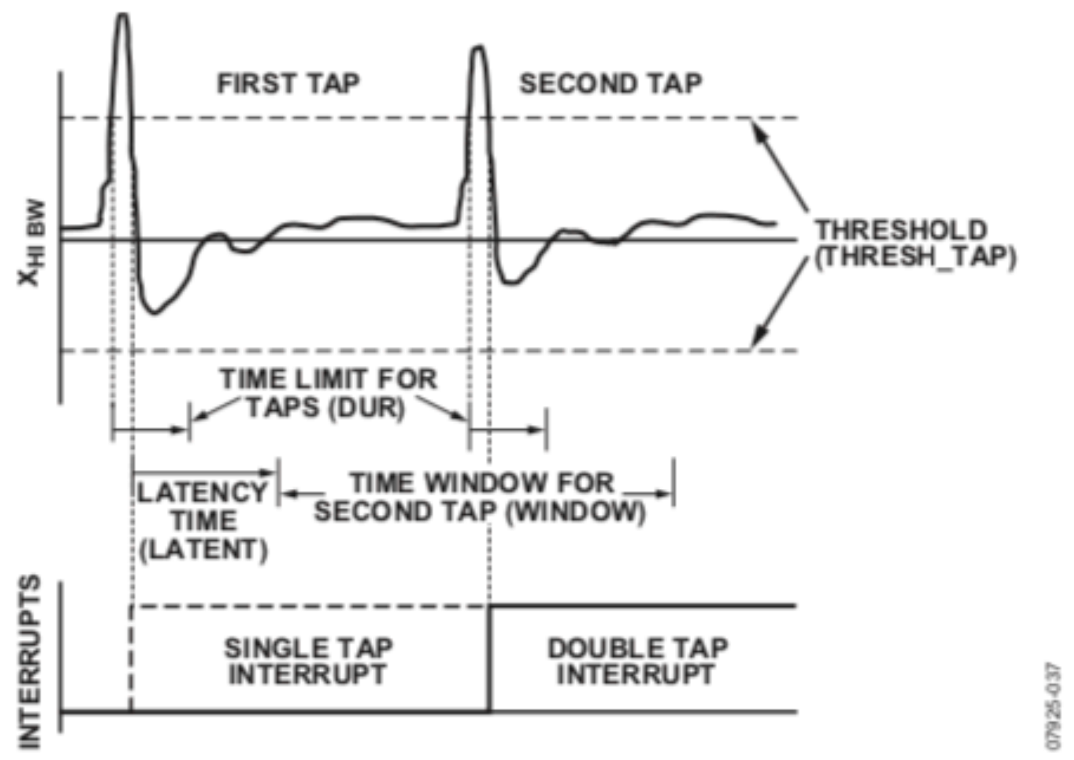


Figure 46. Tap Interrupt Function with Valid Single and Double Taps

If only the single tap function is in use, the single tap interrupt is triggered when the acceleration goes below the threshold, as long as DUR has not been exceeded. If both single and double tap functions are in use, the single tap interrupt is triggered when the double tap event has been either validated or invalidated.

封装信息

- 制作PCB封装库的重要参考
- 注意Pin1的位置
- 注意其焊盘的大小
- 一般在Datasheet的最后面
- 不同的封装对应不同的型号尾标
- 不同的温度范围/应用级别也对应不同的型号尾标

OUTLINE DIMENSIONS

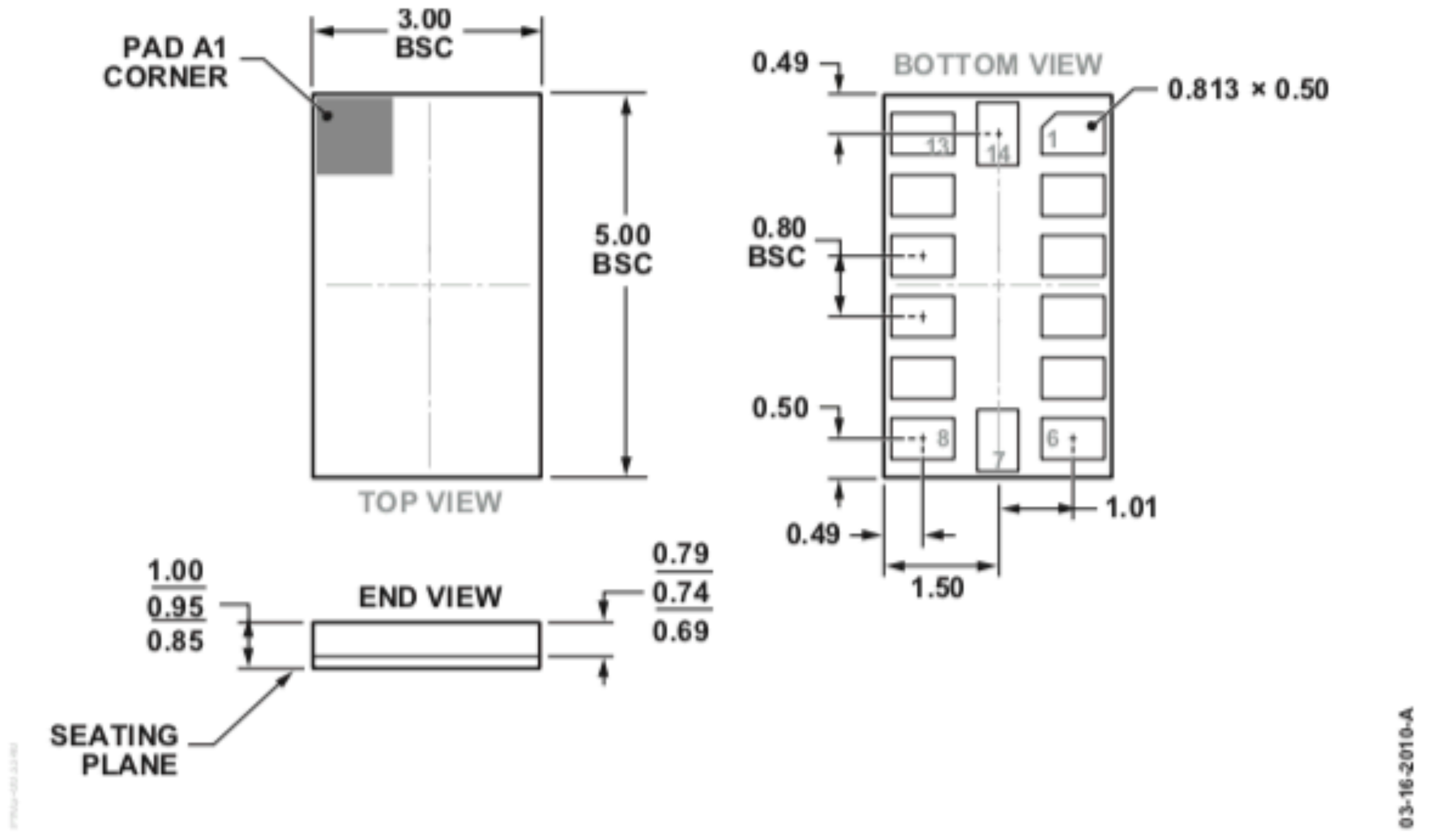


Figure 61. 14-Terminal Land Grid Array [LGA]
(CC-14-1)
Solder Terminations Finish Is Au over Ni
Dimensions shown in millimeters

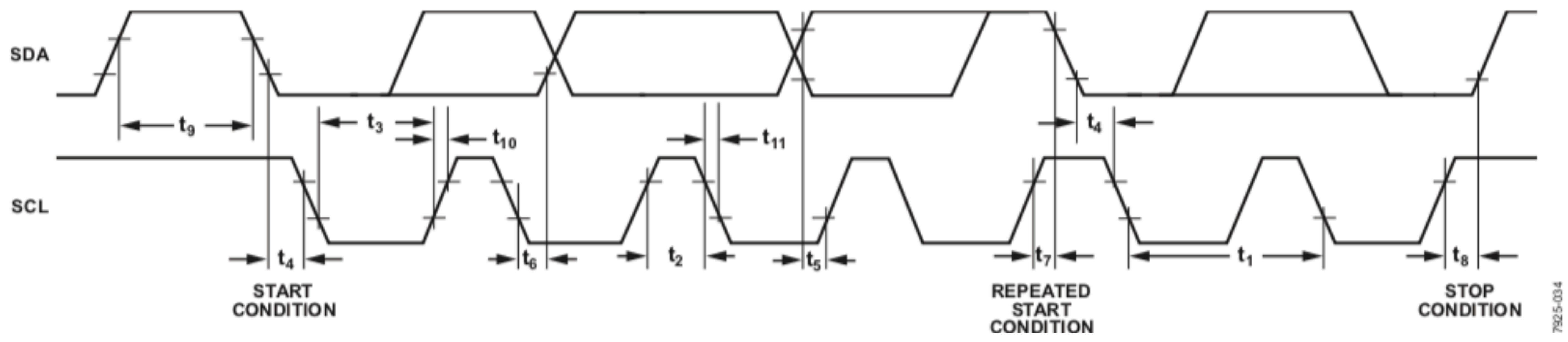
ORDERING GUIDE

Model[1]	Measurement Range (*g*)	Specified Voltage (V)	Temperature Range	Package Description	Package Option
ADXL345BCCZ	±2, ±4, ±8, ±16	2.5	−40°C to +85°C	14-Terminal Land Grid Array [LGA]	CC-14-1
ADXL345BCCZ-RL	±2, ±4, ±8, ±16	2.5	−40°C to +85°C	14-Terminal Land Grid Array [LGA]	CC-14-1
ADXL345BCCZ-RL7	±2, ±4, ±8, ±16	2.5	−40°C to +85°C	14-Terminal Land Grid Array [LGA]	CC-14-1
EVAL-ADXL345Z				Evaluation Board	
EVAL-ADXL345Z-DB				Evaluation Board	
EVAL-ADXL345Z-M				Analog Devices Inertial Sensor Evaluation System, Includes ADXL345 Satellite	
EVAL-ADXL345Z-S				ADXL345 Satellite, Standalone	

[1] Z = RoHS Compliant Part.

Parameter	Limit[1,2] Min	Max	Unit	Description
f_{SCL}		400	kHz	SCL clock frequency
t_1	2.5		µs	SCL cycle time
t_2	0.6		µs	t_{HIGH}, SCL high time
t_3	1.3		µs	t_{LOW}, SCL low time
t_4	0.6		µs	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100		ns	$t_{SU, DAT}$, data setup time
t_6[3, 4, 5, 6]	0	0.9	µs	$t_{HD, DAT}$, data hold time
t_7	0.6		µs	$t_{SU, STA}$, setup time for repeated start
t_8	0.6		µs	$t_{SU, STO}$, stop condition setup time
t_9	1.3		µs	t_{BUF}, bus-free time between a stop condition and a start condition
t_{10}		300	ns	t_R, rise time of both SCL and SDA when receiving
	0		ns	t_R, rise time of both SCL and SDA when receiving or transmitting
t_{11}		300	ns	t_F, fall time of SDA when receiving
		250	ns	t_F, fall time of both SCL and SDA when transmitting
C_b		400	pF	Capacitive load for each bus line

[1] Limits based on characterization results, with f_{SCL} = 400 kHz and a 3 mA sink current; not production tested.
[2] All values referred to the V_{IH} and the V_{IL} levels given in Table 11.
[3] t_6 is the data hold time that is measured from the falling edge of SCL. It applies to data in transmission and acknowledge.
[4] A transmitting device must internally provide an output hold time of at least 300 ns for the SDA signal (with respect to $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[5] The maximum t_6 value must be met only if the device does not stretch the low period (t_3) of the SCL signal.
[6] The maximum value for t_6 is a function of the clock low time (t_3), the clock rise time (t_{10}), and the minimum data setup time ($t_{5(min)}$). This value is calculated as $t_{6(max)} = t_3 - t_{10} - t_{5(min)}$.



参考连接方式及相应的时序要求

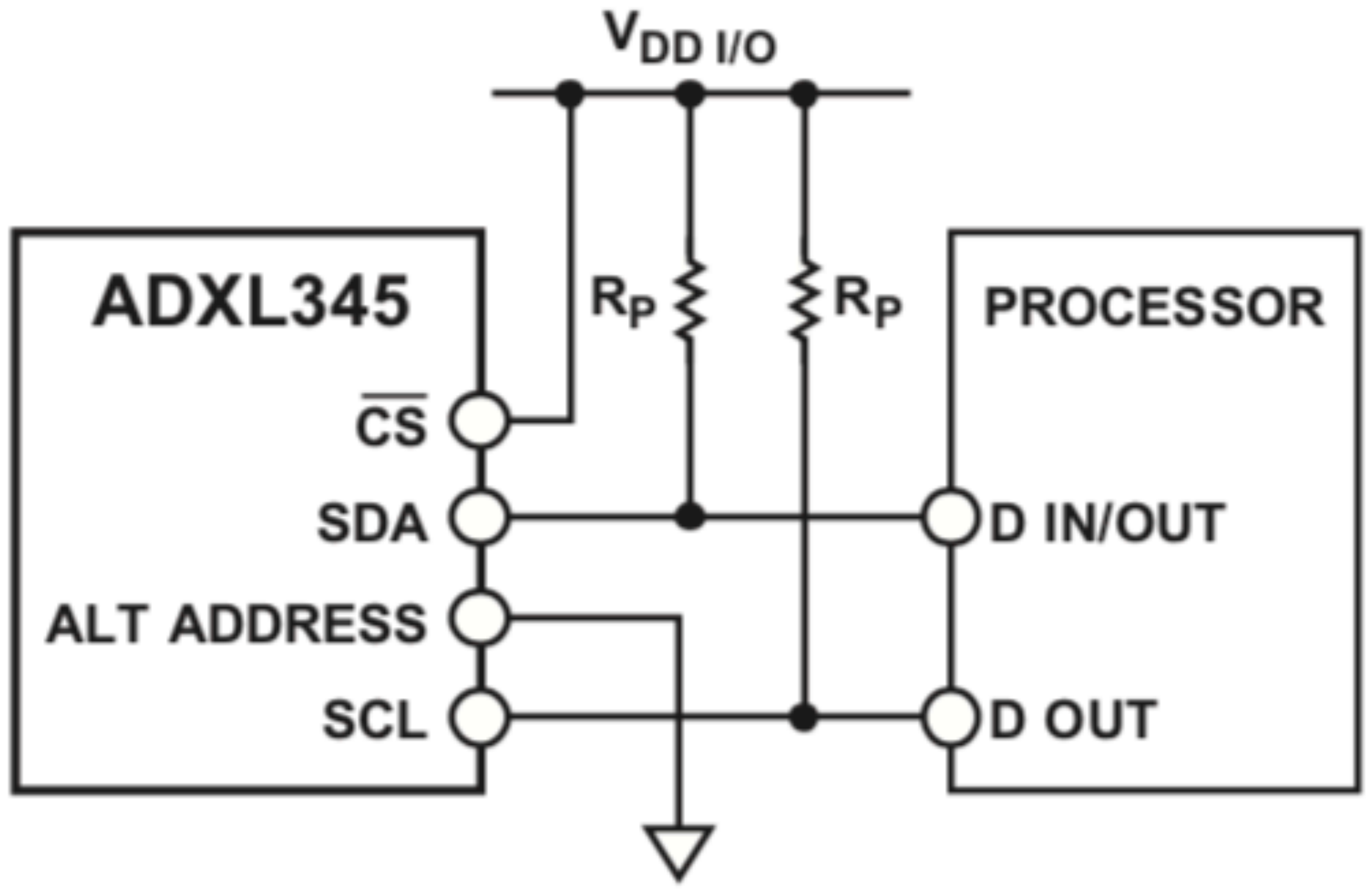


Figure 40. I^{2}C Connection Diagram (Address 0x5

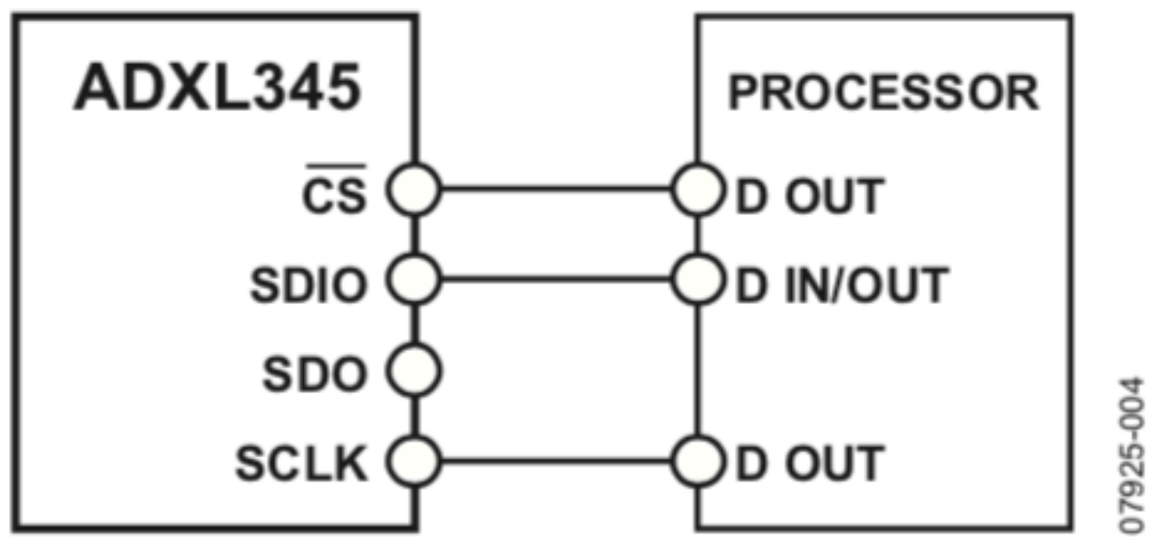


Figure 34. 3-Wire SPI Connection Diagram

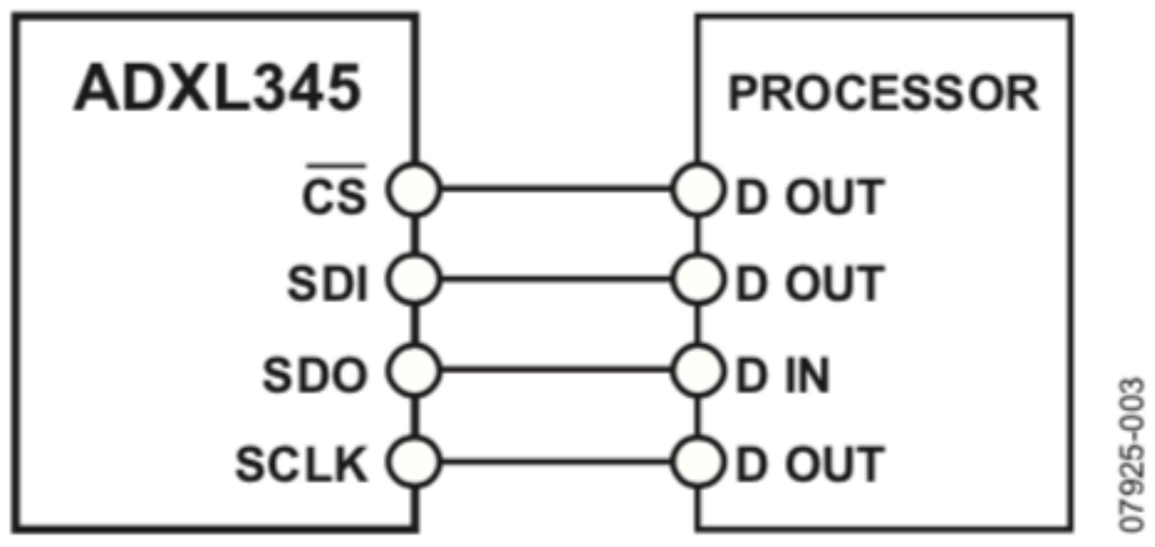


Figure 35. 4-Wire SPI Connection Diagram

参考设计 - 借鉴其符号及电路连接方式

- EVKit和DevKit的区别
- 一般在器件数据手册后面
- 有些参考设计有独立的文档
- 参考设计主要用于用户进行评估用的，因此有很多用于测试的接口，在实际的设计中需要简化掉

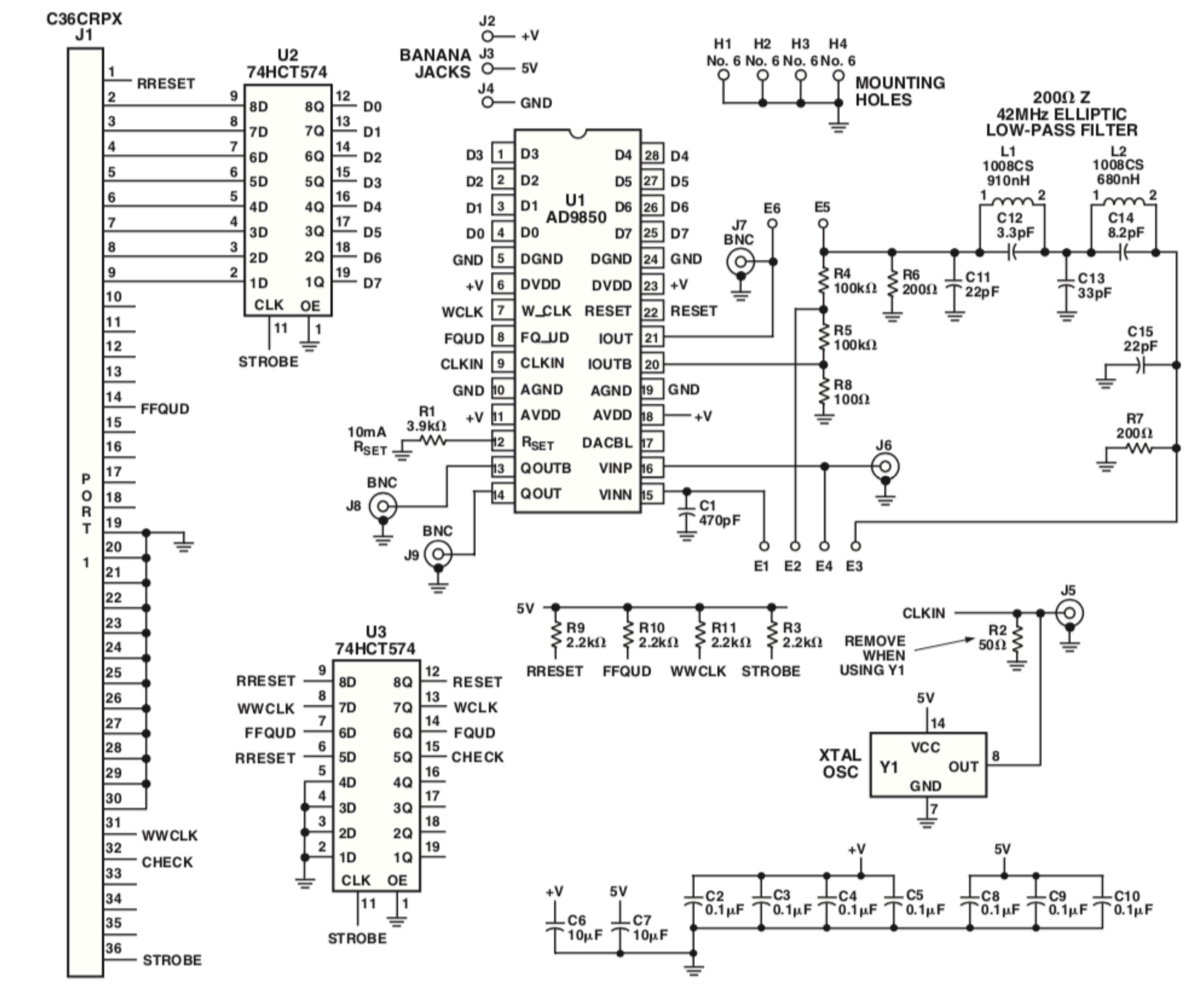


Figure 17. AD9850/CGPCB Electrical Schematic

COMPONENT LIST

Integrated Circuits

U1	AD9850BRS (28-Lead SSOP)
U2, U3	74HCT574 H-CMOS Octal Flip-Flop

Capacitors

C1	470 pF Ceramic Chip Capacitor
C2 to C5, C8 to C10	0.1 µF Ceramic Chip Capacitor
C6, C7	10 µF Tantalum Chip Capacitor
C11	22 pF Ceramic Chip Capacitor
C12	3.3 pF Ceramic Chip Capacitor
C13	33 pF Ceramic Chip Capacitor
C14	8.2 pF Ceramic Chip Capacitor
C15	22 pF Ceramic Chip Capacitor

Resistors

R1	3.9 kΩ Resistor
R2	50 Ω Resistor
R3, R9, R10, R11	2.2 kΩ Resistor
R4, R5	100 kΩ Resistor
R6, R7	200 Ω Resistor
R8	100 Ω Resistor

Connectors

J2, J3, J4	Banana Jack
J5 to J9	BNC Connector

Inductors

L1	910 nH Surface Mount
L2	680 nH Surface Mount