# 使用 Quartus 和 ModelSim 仿真 OC8051

该手册中使用软件版本 Quartus Prime Lite Edition 17.0, ModelSim-altera

### 1.新建 Quartus 工程

(1) 新建工程名为"oc8051 ", 保存路径 "..\8051\trunk\syn\synplify"

| 🕞 New Project Wizard   | >                 |
|--|-------------------|
| Directory, Name, Top-Level Entity  |                   |
| What is the working directory for this project?  |                   |
| D:/STEP_FPGA/SOC/OC8051/8051/trunk/syn/synplify  |                   |
| What is the name of this project?  |                   |
| oc8051   |                   |
| What is the name of the top-level design entity for this project? This name and must exactly match the entity name in the design file. | is case sensitive |
| oc8051   |                   |
| Use Existing Project Settings  |                   |
|  |                   |
|  |                   |
|  |                   |
|  |                   |
|  |                   |
|  |                   |
|  |                   |
|  |                   |

(2) 将目录 "8051\_latest (源码) \8051\trunk\rtl\verilog "下,除

oc8051\_alu\_test.v 文件外的所有文件添加到工程中。

(3) 选择小脚丫 MAX10 开发板芯片 10M08SAM153C8G

🕥 New Project Wizard

| Device Board  |   |   |   |              |   |  |  |
|---|---|---|---|--------------|---|--|--|
| Select the family and devic   | e you want to target for  | compilatio  | n.  |              |   |  |  |
| ou can install additional c   | levice support with the li  | nstall Devic  | es com  | mand on t    | the Tools me                                    | enu.   |  |
| To determine the version of   | of the Quartus Prime sof  | tware in wh   | nich you  | ir target de | evice is supp                                   | orted, refer to the De   | evice Support List webpa   |
| Device family   |   |   |   | Show ir      | n 'Available d                                  | levices' list  |  |
| Family: MAX 10 (DA/DF/  | /DC/SA/SC)  |   | •   | Packag       | ·••   | MRGA   |  |
| Device: All   |   |   | •   | n ackag      |   | 150  |  |
|   |   |   |   | Pin cou      | int:  | 153  |  |
| Target device   |   |   |   | Core s       | beed grade:                                     | Any  |  |
| <ul> <li>Auto device selected</li> </ul>  | by the Fitter   |   |   | Name f       | ilter:  |  |  |
| Specific device select  | ted in 'Available devices'  | list  |   | L Sh         | wadvancod                                       | Idovicos   |  |
| Othor: n/a  |   |   |   | v siit       | Jw auvanceu                                     | i devices  |  |
|   |   |   |   |              |   |  |  |
|   |   |   |   |              |   |  |  |
| Available devices:  |   |   |   |              |   |  |  |
| Available devices:  | Core Voltage  | LEs   | То  | tal I/Os     | GPIOs   | Memory Bits  | Embedded multipl   |
| Available devices:<br>Name<br>10M085AM153C8G  | Core Voltage<br>3.3V  | <b>LEs</b><br>8064                                  | <b>To</b><br>112                                    | tal I/Os     | GPIOs   | Memory Bits<br>387072  | Embedded multipl   |
| Available devices:<br>Name<br>10M08SAM153C8G<br>10M08SAM153C8GES  | Core Voltage<br>3.3V<br>3.3V  | LEs<br>8064<br>8064                                 | <b>To</b><br>112<br>112                             | tal I/Os     | GPIOs<br>112<br>112                             | Memory Bits<br>387072<br>387072  | Embedded multipl<br>48<br>48                                     |
| Available devices:<br>Name<br>10M08SAM153C8G<br>10M08SAM153C8GES<br>10M08SAM153I7G  | Core Voltage<br>3.3V<br>3.3V<br>3.3V  | LEs<br>8064<br>8064<br>8064                         | <b>To</b><br>112<br>112<br>112                      | tal I/Os     | GPIOs<br>112<br>112<br>112                      | Memory Bits           387072           387072           387072   | Embedded multipl<br>48<br>48<br>48                               |
| Available devices:<br>Name<br>10M08SAM153C8G<br>10M08SAM153C8GES<br>10M08SAM153I7G<br>10M08SCM153C8G                        | Core Voltage<br>3.3V<br>3.3V<br>3.3V<br>3.3V<br>3.3V  | LEs<br>8064<br>8064<br>8064<br>8064                 | <b>To</b><br>112<br>112<br>112<br>112               | tal I/Os     | GPIOs<br>112<br>112<br>112<br>112<br>112        | Memory Bits           387072           387072           387072           387072           387072                                   | Embedded multipl<br>48<br>48<br>48<br>48<br>48                   |
| Available devices:<br>Name<br>10M08SAM153C8G<br>10M08SAM153C8GES<br>10M08SAM153I7G<br>10M08SCM153I7G<br>10M08SCM153I7G      | Core Voltage<br>3.3V<br>3.3V<br>3.3V<br>3.3V<br>3.3V<br>3.3V<br>3.3V  | LEs<br>8064<br>8064<br>8064<br>8064<br>8064         | <b>To</b><br>112<br>112<br>112<br>112<br>112<br>112 | tal I/Os     | GPIOs<br>112<br>112<br>112<br>112<br>112<br>112 | Memory Bits           387072           387072           387072           387072           387072           387072           387072 | Embedded multipl<br>48<br>48<br>48<br>48<br>48<br>48             |
| Available devices:<br>Name<br>10M08SAM153C8G<br>10M08SAM153C8GES<br>10M08SAM153I7G<br>10M08SCM153I7G<br>10M08SCM153I7G<br>4 | Core Voltage 3.3V 3.3V 3.3V 3.3V 3.3V 3.3V 3.3V   | LEs<br>8064<br>8064<br>8064<br>8064<br>8064<br>8064 | <b>To</b><br>112<br>112<br>112<br>112<br>112<br>112 | tal I/Os     | GPIOs<br>112<br>112<br>112<br>112<br>112<br>112 | Memory Bits           387072           387072           387072           387072           387072           387072           387072 | Embedded multipl<br>48<br>48<br>48<br>48<br>48<br>48<br>48       |
| Available devices:<br>Name<br>10M08SAM153C8G<br>10M08SAM153C8GES<br>10M08SAM153I7G<br>10M08SCM153I7G<br>10M08SCM153I7G<br>4 | Core Voltage           3.3V           3.3V           3.3V           3.3V           3.3V           3.3V           3.3V | LEs<br>8064<br>8064<br>8064<br>8064<br>8064         | <b>To</b><br>112<br>112<br>112<br>112<br>112        | tal I/Os     | GPIOs<br>112<br>112<br>112<br>112<br>112<br>112 | Memory Bits           387072           387072           387072           387072           387072           387072                  | Embedded multipl<br>48<br>48<br>48<br>48<br>48<br>48<br>48<br>48 |
| Available devices:<br>Name<br>10M08SAM153C8G<br>10M08SAM153C8GES<br>10M08SAM153I7G<br>10M08SCM153I7G<br>10M08SCM153I7G<br>( | Core Voltage           3.3V           3.3V           3.3V           3.3V           3.3V           3.3V           3.3V | LEs<br>8064<br>8064<br>8064<br>8064<br>8064         | <b>To</b><br>112<br>112<br>112<br>112<br>112<br>112 | tal I/Os     | GPIOs<br>112<br>112<br>112<br>112<br>112<br>112 | Memory Bits           387072           387072           387072           387072           387072           387072                  | Embedded multipl<br>48<br>48<br>48<br>48<br>48<br>48<br>48<br>48 |
| Available devices:<br>Name<br>10M08SAM153C8G<br>10M08SAM153C8GES<br>10M08SAM153I7G<br>10M08SCM153I7G<br>10M08SCM153I7G<br>< | Core Voltage 3.3V 3.3V 3.3V 3.3V 3.3V 3.3V 3.3V   | LEs<br>8064<br>8064<br>8064<br>8064<br>8064         | <b>To</b><br>112<br>112<br>112<br>112<br>112        | tal I/Os     | GPIOs<br>112<br>112<br>112<br>112<br>112<br>112 | Memory Bits           387072           387072           387072           387072           387072           387072                  | Embedded multipl<br>48<br>48<br>48<br>48<br>48<br>48<br>48<br>5  |

### (4) 仿真工具设置为 ModelSim-Altera, 格式选择是 Verilog-HDL, 这是为仿真设置的,

#### 其他默认即可,如下图所示:

| 🕤 New Project  | Wizard                  |                   |  | ×  |
|----------------|-------------------------|-------------------|--|----|
| EDA Tool       | Settings                |                   |  |    |
| Specify the ot | ner EDA tools used with | the Quartus Prime | software to develop your project.                            |    |
| EDA tools:     |                         |                   |  |    |
| Tool Type      | Tool Name               | Format(s)         | Run Tool Automatically                                       |    |
| Design Entr    | <none></none>           | <none></none>     | Run this tool automatically to synthesize the current design |    |
| Simulation     | ModelSim-Altera         | Verilog HDL       | Run gate-level simulation automatically after compilation    |    |
| Board-Level    | Timing                  | <none></none>     | -  |    |
|                | Symbol                  | <none></none>     | -  |    |
|                | Signal Integrity        | <none></none>     | •  |    |
|                | Boundary Scan           | <none></none>     | ·  |    |
|                |                         |                   |  |    |
|                |                         |                   |  |    |
|                |                         |                   |  |    |
|                |                         |                   | < Back Next > Finish Cancel He                               | lp |

(5) 确定后工程信息如下,工程创建完成

 $\times$ 

| 🕥 New Project Wizard  | ×   |
|---|---|
| Summary   |   |
| When you click Finish, the project will be created with the following set | tings:  |
| Project directory:  | D:/STEP_FPGA/SOC/OC8051/8051/trunk/syn/synplify |
| Project name:   | oc8051  |
| Top-level design entity:  | oc8051  |
| Number of files added:  | 31  |
| Number of user libraries added:   | 0   |
| Device assignments:   |   |
| Design template:  | n/a   |
| Family name:  | MAX 10 (DA/DF/DC/SA/SC)                         |
| Device:   | 10M08SAM153C8G                                  |
| Board:  | n/a   |
| EDA tools:  |   |
| Design entry/synthesis:   | <none> (<none>)</none></none>                   |
| Simulation:   | ModelSim-Altera (Verilog HDL)                   |
| Timing analysis:  | 0   |
| Operating conditions:   |   |
| Core voltage:   | 3.3V  |
| Junction temperature range:   | 0-85 °C   |
|   |   |
|   | < Back Next > Finish Cancel Help                |

# 2.新建 mem 初始化文件

新建一个 Memory Init File, 文件名可以设置为 oc8051\_altera\_rom.mif 设置如下, 注意

数据宽度是 32 位:

| 🕥 New   | $\times$ |  |  |  |  |
|---|----------|--|--|--|--|
| State Machine File<br>SystemVerilog HDL File<br>Tcl Script File   | ^        |  |  |  |  |
| Verilog HDL File<br>VHDL File<br>✔ Memory Files   |          |  |  |  |  |
| Hexadecimal (Intel-Format) File<br>Memory Initialization File<br>Verification/Debugging Files<br>In-System Sources and Probes F |          |  |  |  |  |
| Logic Analyzer Interface File<br>SignalTap II Logic Analyzer File<br>University Program VWF                                     |          |  |  |  |  |
| V Other Files   | ~        |  |  |  |  |
| OK Cancel Help  |          |  |  |  |  |



内容如下,只在第一个存储位置填入数据 00559075,这里的 75 是指令 mov, 90 是 P1

的地址,55是移入的立即数,所以该指令的作用就是向P1端口输出数0x55

| 5 | p   |          | oc8051_  | altera_rom | .mif     | ×        |         |          |          |       |
|---|-----|----------|----------|------------|----------|----------|---------|----------|----------|-------|
| ۵ | ddi | +0       | +1       | +2         | +3       | +4       | +5      | +6       | +7       | ASCII |
|   | 0   | 00559075 | 00000000 | 0000000    | 00000000 | 00000000 | 0000000 | 00000000 | 00000000 |       |
|   | 8   | 0000000  | 0000000  | 0000000    | 0000000  | 0000000  | 0000000 | 0000000  | 0000000  |       |
|   | 16  | 0000000  | 0000000  | 0000000    | 0000000  | 0000000  | 0000000 | 0000000  | 0000000  |       |

## 3.创建 onchiprom

使用 Quartus 中的 IP Catalog 工具创建 ROM, 配置过程如下:



此处数据宽度是 32 位,设置如下:

| K MegaWizard Plug-In Manager [page 1 of 5] ? |  |   |  |                       |   |
|--|--|---|--|-----------------------|---|
| Parameter EDA 3<br>Settings                  | 1 Summary  |   |  |                       | ^ |
| General Regs/Clken/Ac                        | clrs > Men   | n Init >  |  |                       | _ |
| General Regs/Clken/Ac                        | Clrs Men<br>DI<br>How w<br>How m<br>Note: '<br>What<br>Mat<br>Se<br>What<br>Se | Currently selected device family:<br>vide should the 'q' output bus be?<br>nany 32-bit words of memory?<br>You could enter arbitrary values for width and de<br>should the memory block type be?<br>Auto MLAB<br>1144K LCs<br>et the maximum block depth to Auto vec<br>clocking method would you like to use?<br>Single clock<br>Dual clock: use separate 'input' and 'output' clock | MAX 10<br>Match project/de<br>32<br>b<br>4096<br>w<br>epth<br>M9K<br>Options<br>ords | fault<br>its<br>vords |   |
|  |  |   |  |                       |   |
|  |  |   |  |                       | Y |

| 下面将'q' output port 复选框中取消选中, | 也就是输出没有锁存 |
|------------------------------|-----------|
|------------------------------|-----------|

| ☆ MegaWizard Plug-In Manager [page 2 of 5]  | ? | × |
|---|---|---|
| I Parameter<br>Settings     I Summary       General     Regs/Clken/Adrs   |   | ^ |
| Image: Signature       Which ports should be registered?         Image: Signature       Image: Signature         Image: |   |   |
| Resource Usage  |   | Y |

#### 选择初始化文件是上面创建的 mif 文件,同时设置一个 Instance ID,这样就可以在代码

运行时从 Quartus 中查看修改 ROM 内容。

| 🔨 MegaWizard Plug-In Manager [page 3 of 5]   | ? | $\times$ |
|--|---|----------|
| ROM: 1-PORT  |   | ^        |
| I Parameter<br>Settings     I EDA     I Summary       Caparal     Page/Clikon (A dire     More Lait  |   |          |
| General       Regs/Clken/Adrs       Mem Init         address1       Do you want to specify the initial content of the memory?         Image: Second Sec |   |          |
| Resource Usage   |   | ×        |

ROM 创建完成。

## 4.创建 onchipram

使用 Quartus 中的 IP Catalog 工具创建双端口 RAM,配置过程同上一节中 ROM 的过程

类似,不过没有 mem 初始化文件,配置过程如下:



| 🛪 MegaWizard Plug-In Manager | [page 1 of 10]  | ? | $\times$ |
|------------------------------|---|---|----------|
| General Widths/Bik Type Clk  | s/Rd, Byte En Regs/Clkens/Aclrs Output1 Mem Init Currently selected device family: MAX 10   |   | ^        |
| Wraddress[40]                | Match project/default     More adjusted by the dual port RAM?     With one read port and one write port     With two read/write ports |   |          |
|                              |   |   |          |
|                              | How do you want to specify the memory size?   |   |          |
|                              | <ul> <li>As a number of words</li> <li>As a number of bits</li> </ul>   |   |          |
|                              |   |   |          |
|                              |   |   |          |
| Resource Usage –<br>1 M9K    | Cancel Sack Next > Finish   |   | ×        |

| 🛪 MegaWizard Plug-In Man  | ager [page 2 of 10]  |   |                          | ?                        | $\times$ |
|---|--|---|--------------------------|--------------------------|----------|
| 🍓 RAM: 2-POR  | T  |   | About                    | <u>D</u> ocumentatio     | on       |
| Image: Parameter Settings     Image: Parameter Settings     Image: Parameter Settings       General     Widths/Blk Type | nary<br>≻ Clks/Rd, Byte En >   | Regs/Clkens/Adrs  | Output1 > Men            | n Init                   |          |
| data 7.068051_altera_ram<br>wraddress[7.00_gevee<br>rdaddress[7.00_gevee<br>clock<br>Block Type: AUTO                   | How many 8-bit we<br>Use different da<br>Read/Write Ports<br>How wide should<br>How wide should<br>How wide should<br>Note: You could do<br>What should the r<br>O Auto<br>M144K | ords of memory?<br>ata widths on different port<br>the 'q_a' output bus be?<br>the 'data_a' input bus be?<br>the 'q' output bus be?<br>enter arbitrary values for w<br>nemory block type be?<br>MLAB<br>O LCs | ridth and depth<br>O M9K | 256<br>8 ~<br>8 ~<br>8 ~ | 5        |
| Resource Usage  | Set the maxim  | um block depth to Auto  | ✓ words                  |                          |          |
| 1 M9K   |  | [   | Cancel < <u>B</u> ack N  | lext > Einis             | h        |

| 🛪 MegaWizard Plug-In Manager         | [page 3 of 10]  | ?  | $\times$ |
|--------------------------------------|---|--|----------|
| a RAM: 2-PORT                        |   | About Documenta                          | tion     |
| IParameter   IParameter     Settings |   | <pre></pre>                              |          |
| General Widths/Blk Type Cl           | ks/Rd, Byte En Regs/Clkens/AcIrs Mem Init   | >  |          |
| data (7.0)                           | <ul> <li>Single clock</li> <li>Dual clock: use separate 'read' and 'write' clocks</li> <li>Dual clock: use separate 'input' and 'output' clocks</li> <li>No clock (fully asynchronous)</li> <li>Customize clocks for A and B ports</li> </ul> | 5  |          |
|                                      | <ul> <li>Create a 'rden' read enable signal</li> <li>Byte Enable Ports</li> <li>Create byte enable for port A</li> <li>Create byte enable for port B</li> <li>What is the width of a byte for byte enables? 8</li> </ul>                      | <ul><li>✓ bits</li></ul>                 |          |
|                                      | Enable error checking and correcting (ECC) to check<br>single bit errors and detect double errors<br>Enable ECC pipeline registers before the output de<br>achieve the same performance as non-ECC mode<br>expense of one cycle of latency    | k and correct<br>ecoder to<br>at the     |          |
| Resource Usage<br>1 M9K + 1 reg      | Cancel  | < <u>B</u> ack <u>N</u> ext > <u>Fin</u> | ish      |

| 🔌 MegaWizard Plug-In Manag   | ger [page 5 of 10]   | ? ×   |
|--|--|---|
| a RAM: 2-POR   | Г  | <u>About</u> <u>D</u> ocumentation                          |
| Parameter   Image: Settings  | ary  |   |
| General > Widths/Blk Type >  | Clks/Rd, Byte En Regs/Clkens/Aclrs Mem Ini   | t >   |
| data 7 c 8051 altera ram<br>wraddress 7.01 9 4 ar a ram<br>wren rdaddress 7.01 9 4 ar a ram<br>wrclock<br>wrclock rdclock 5 ar a ram<br>Block Type: AUTO 5 | <ul> <li>Which ports should be registered?</li> <li>Write input ports 'data', 'wraddress', and 'wren'</li> <li>Read input ports 'rdaddress' and 'rden'</li> <li>Read output port(s) 'q'</li> <li>Create one clock enable signal for each clock signal</li> <li>Use different clock enables for 'rdaddress' and 'q</li> <li>Create an 'aclr' asynchronous clear for the registered ports</li> </ul> | More Options<br>More Options<br>' registers<br>More Options |
| Resource Usage<br>1 M9K + 1 reg  | Cancel   | < Back Next > Einish  |

| 🛪 MegaWizard Plug-In Manager  | [page 8 of 10]   | ? ×  |  |
|---|--|--|--|
| a RAM: 2-PORT   |  | About Documentation  |  |
| Parameter   Parameter     Settings   Settings   |  |  |  |
| General $>$ Widths/Blk Type $>$ Clk   | s/Rd, Byte En > Regs/Clkens/Aclrs > Mem Init   |  |  |
| data[7.0]     altera_ram       wraddress[7.0]     yraddress[7.0]       wren     yraddress[7.0]       rden     yraddress[7.0]       wrclock     in       wrclock     in       Block Type: AUTO     g | <ul> <li>Do you want to specify the initial content of the memory</li> <li>No, leave it blank</li> <li>Initialize memory content data to XXX on power-up in simulation</li> <li>Yes, use this file for the memory content data (You can use a Hexadecimal (Intel-format) File [.he Initialization File [.mif])</li> <li>Note: The configuration scheme of your device is I In order to use memory initialization, you must sel configuration mode with memory initialization for Compressed Image with Memory Initialization page of the configuration page of the configurating page of the configuration page of the configurating page of</li></ul> | ry?<br>∞x] or a Memory<br>internal Configuration.<br>lect a single image<br>example the Single<br>on. You can set the<br>he Device and Pin |  |
|   | File name:<br>The initial content file should conform to which port's dimensions?  | Browse<br>PORT_B ~   |  |
| Resource Usage<br>1 M9K + 1 reg   | Cancel [   | < <u>Back</u> <u>Next &gt;</u> Einish  |  |

# 5.修改源代码

(1) 修改 oc8051\_rom.v,使用刚刚创建的 ROM 做为 CPU 内部 ROM。将其内容替换

为如下:

```
63 'include "oc8051_timescale.v"
     'include "oc8051 defines.v"
64
65
66
     module oc8051_rom (rst, clk, addr, ea_int, data_o);
67
68
     //parameter INT_ROM_WID= 15;
69
     input rst, clk;
71
     input [15:0] addr;
      //input [22:0] addr;
     output ea_int;
73
74
     output [31:0] data_o;
75
76
     wire ea;
77
78
     reg ea_int;
79
90
81
    G'ifdef OC8051_Altera_ROM
82
8.3
      parameter INT_ROM_WID= 12;
84
85
      assign ea = | addr[15:INT_ROM_WID];
86
87
88
     always @ (posedge clk or posedge rst)
89
       if (rst)
90
        ea int <= #1 1'b1;
        else ea_int <= #1 !ea;</pre>
91
92
93
     oc8051_altera_rom oc8051_altera_rom1
94
   E(
95
      .address(addr[11:0]),
96
      .clock(clk),
97
     .q(data_o)
98
     -);
99
      'else
```

(2) 修改 defines.v 添加`define OC8051\_Altera\_RAM, `define OC8051\_Altera\_ROM,

取消掉`define OC8051\_ROM 前面的注释,将`define OC8051\_RAM\_GENERIC 注释掉。

| oc 🧇                       | 8051_rom.v 🛛  | 🔶 oc8051_defines.v 🛛   | 🧇 oc8051_ram_256x8_two_bist.v 🛽 |   |
|----------------------------|---|--|---------------------------------|---|
| <b>F</b>                   | 📅   🕮 🕮   🖪 🗗   | 🎦 🛛 👅 🔀 📴 🧮  |                                 |   |
| 61<br>62<br>63             | //<br>// oc8051 1                                       | ITERNAL ROM  |                                 | ^ |
| 64<br>65<br>66             | define OC8  | 3051_ROM   |                                 |   |
| 67<br>68<br>69             | //<br>// oc8051 m                                       | nemory   |                                 |   |
| 70<br>71<br>72             | //`define (<br>//`define (                              | DC8051_CACHE<br>DC8051_WB  |                                 |   |
| 73<br>74<br>75<br>76<br>77 | define 008<br>//`define 0<br>//`define 0<br>//`define 0 | <mark>8051_Altera_RAM</mark><br>DC8051_RAM_XILINX<br>DC8051_RAM_VIRTUALSIL<br>DC8051_RAM_GENERIC | ICON                            |   |
| 79<br>80                   | define OC8  | 8051_Altera_ROM  |                                 |   |
| 81<br>82<br>83             | //<br>// oc8051 s                                       | simulation defines   |                                 |   |
| 84<br>85<br>86             | // define (   | DC8051_SIMULATION<br>DC8051_SERIAL   |                                 |   |
| 87<br>88<br>89             | // oc8051 k   | Dist   |                                 | ~ |
| <                          | // detine (   |  |                                 | > |

(3) 修改 oc8051\_ram\_256x8\_two\_bist, 将 126-146 行使用下列代码替换:



### 6.添加 TestBench 文件

(1) 新建一个 Verilog HDL 文件, 文件名为 oc8051\_tb.v, 这是一个测试文件, 内容如

ጉ፡

上面的测试代码定义了时钟周期是 20ns, 注意的是要给 ack\_i、iack\_i、wbd\_err\_i、

wbi\_err\_i 赋初值,否则会导致时序仿真出现异常。

| (2) ŗ | 点击 Assignments->Setting, | 选择 EDA Tool | s Setting->Simulation, | 如下设置: |
|-------|--------------------------|-------------|------------------------|-------|
|-------|--------------------------|-------------|------------------------|-------|

| 🖌 Settings - oc8051  | - 🗆 X   |
|--|---|
| Category:  | Device/Board  |
| Category:<br>General<br>Files<br>Libraries<br>V IP Settings<br>IP Catalog Search Location<br>Design Templates<br>V Operating Settings and Conc<br>Voltage<br>Temperature<br>Compilation Process Setting<br>Incremental Compilation<br>VEDA Tool Settings<br>Design Entry/Synthesis<br>Simulation<br>Board-Level<br>V Compiler Settings<br>VHDL Input<br>Verilog HDL Input<br>Default Parameters<br>TimeQuest Timing Analyzer<br>Assembler<br>Design Assistant<br>SignalTap II Logic Analyzer<br>Logic Analyzer Interface<br>PowerPlay Power Analyzer S | Device/Board         Simulation         Specify options for generating output files for use with other EDA tools.         Tool name:       ModelSim-Altera         Run gate-level simulation automatically after compilation         EDA Netlist Writer settings         Format for output netlist:       Verilog HDL         Output directory:       simulation/modelsim         Map illegal HDL characters       Enable glitch filtering         Options for Power Estimation       Generate Value Change Dump (VCD) file script         Script Settings       Design instance name:         More EDA Netlist Writer Settings       NativeLink settings         None       Compile test bench:       oc8051_tb         Use script to set up simulation: |
|  | O Script to compile test bench:        More NativeLink Settings     Reset   |
| < >>   | Buy SoftwareOKCancelApplyHelp   |

# 7.功能仿真

(1) 仿真软件设置

Tools ——Options

| S Options                           |                      |  |         |        | ×    |
|-------------------------------------|----------------------|--|---------|--------|------|
| Category:                           |                      |  |         |        |      |
| ✓ General                           | EDA Tool Options     |  |         |        |      |
| EDA Tool Options                    | Specify the director | y that contains the tool executable for each third-party ED/ | A tool: |        |      |
| Fonts<br>Headers & Footers Settings | EDA Tool             | Directory Containing Tool Executable                         |         |        |      |
| ✓ Internet Connectivity             | Precision Synthesis  | 5  |         |        |      |
| Libraries                           | Synplify             |  |         |        |      |
| ✓ IP Settings                       | Synplify Pro         |  |         |        |      |
| IP Catalog Search Locations         | Active-HDL           |  |         |        |      |
| Design Templates                    | Riviera-PRO          |  |         |        |      |
| Preferred Text Editor               | ModelSim             |  |         |        |      |
| Processing                          | QuestaSim            |  |         |        |      |
| I ooltip Settings                   | ModelSim-Altera      | C:\intelFPGA_lite\17.0\modelsim_ase\win32aloem               |         |        |      |
| Colors<br>Fonts                     | Use NativeLink       | with a Synplify/Synplify Pro node-locked license             |         |        |      |
|                                     |                      |  | 014     |        |      |
| 1                                   |                      |  | ОК      | Cancel | Help |

### Assignments——Settings

| 🖌 Settings - oc8051   | - 🗆 X   |
|---|---|
| Category:   | Device/Board  |
| General   | Simulation  |
| Files   | Specify options for generating output files for use with other EDA tools. |
| Libraries<br>VIP Settings                                   | Tool name: ModelSim-Altera  |
| IP Catalog Search Location                                  |   |
| Design Templates  |   |
| <ul> <li>Operating Settings and Conc<br/>Voltage</li> </ul> | EDA Netlist Writer settings   |
| Temperature   | Format for output netlist: Verilog HDL   Time scale: 1 ps                 |
| <ul> <li>Compilation Process Setting</li> </ul>             | Output directory: simulation/modelsim                                     |
| ✓ EDA Tool Settings   | Map illegal HDL characters Enable glitch filtering                        |
| Design Entry/Synthesis                                      | Options for Power Estimation  |
| Simulation  | Concernts Value Changes During (VCD) file agrint                          |
| Board-Level   | Generate value change bump (VCD) file script Script Settings              |
| VHDL Input  | Design instance name:   |
| Verilog HDL Input   |   |
| Default Parameters  | More EDA Netlist Writer Settings  |
| TimeQuest Timing Analyzer                                   | Nativel ink settings  |
| Assembler   |   |
| SignalTan II Logic Analyzer                                 | ( ) None  |
| Logic Analyzer Interface                                    | Compile test bench: oc8051_tb     Test Benches                            |
| PowerPlay Power Analyzer S                                  | Use script to set up simulation:  |
| SSN Analyzer  | O Script to compile test bench:   |
|   | More NativeLink Settings Reset  |
| < >>  | Buy Software         OK         Cancel         Apply         Help         |

(2) Analysis&Synthesis

| Task | s Compilation *                        |          |  |  |  |  |  |
|------|--|----------|--|--|--|--|--|
|      | Task                                   | т ^      |  |  |  |  |  |
|      | 🗸 🕨 Compile Design                     |          |  |  |  |  |  |
| 4%   | Analysis & Synthesis                   | 00:0     |  |  |  |  |  |
|      | Fitter (Place & Route)                 |          |  |  |  |  |  |
|      | > 🕨 Assembler (Generate programmin     | g files) |  |  |  |  |  |
|      | > TimeQuest Timing Analysis            |          |  |  |  |  |  |
|      | > 🕨 EDA Netlist Writer                 | ~        |  |  |  |  |  |
|      | <ul> <li>EDA Netlist Writer</li> </ul> | ~        |  |  |  |  |  |

### 注意:如果报如下错误,需要修改 Device 属性

|     | _    |  |         |                |           | Total regis        | sters                    | N/A     | until Partition Merge |               |         | Altera On-C |
|-----|------|--|---------|----------------|-----------|--------------------|--------------------------|---------|-----------------------|---------------|---------|-------------|
|     |      | Task                                   | т ^     |                |           | Total pins         |                          | N/A     | until Partition Merge |               |         | FIFO        |
|     | ~ >  | <ul> <li>Compile Design</li> </ul>     |         |                |           | Total virtu        | al pins                  | N/A     | until Partition Merge |               |         | RAM: 1-POI  |
| ×   | >    | Analysis & Synthesis                   | 00:0    |                |           | Total men          | nory bits                | N/A     | until Partition Merge |               |         | RAM: 2-POI  |
|     | >    | Fitter (Place & Route)                 |         |                |           | Embedde            | d Multiplier 9-bit eleme | nts N/A | until Partition Merge |               |         | ROM: 1-PO   |
|     | >    | Assembler (Generate programming files) | s) ~    |                |           | Total PLLs         | 5                        | N/A     | until Partition Merge |               | <       |             |
| <   |      |  | >       | <              | >         | UFM block          | ks                       | N/A     | until Partition Merge |               |         | id          |
| × 6 | All  |  |         | <b>60</b> E    | ind 😽 F   | Find Ne <u>x</u> t |                          |         |                       |               |         |             |
| =   | Evne | TD Message                             |         |                |           |                    |                          |         |                       |               |         |             |
|     | > 0  | 16010 Generating hard_block p          | artitio | on "hard_block | c:auto_ge | nerated_           | inst"                    |         |                       |               |         |             |
|     | 0    | 16031 Current Internal Config          | uration | mode does no   | ot suppor | t memory           | initialization           | or ROM  | . Select Internal     | Configuration | mode w1 | th ERAM.    |
|     | 0    | 16031 Current Internal Config          | uration | mode does no   | ot suppor | t memory           | initialization           | OF ROM  | . Select Internal     | Configuration | mode wi | ER ERAM.    |
|     |      | 16031 Current Internal Config          | uration | mode does no   | ot suppor | t memory           | initialization           | or ROM  | Select Internal       | Configuration | mode wi | TH ERAM.    |
|     | ŏ    | 16031 Current Internal Config          | uration | mode does no   | ot suppor | t memory           | initialization           | or ROM  | . Select Internal     | Configuration | mode wi | th ERAM.    |
|     | ō    | 16031 Current Internal Config          | uration | mode does no   | ot suppor | t memory           | initialization           | or ROM  | . Select Internal     | Configuration | mode wi | th ERAM.    |
|     | 0    | 16031 Current Internal Config          | uration | mode does no   | ot suppor | t memory           | initialization           | or ROM  | . Select Internal     | Configuration | mode wi | th ERAM.    |
|     | 0    | 16031 Current Internal Config          | uration | mode does no   | ot suppor | t memory           | initialization           | or ROM  | . Select Internal     | Configuration | mode wi | th ERAM.    |
| ges | 0    | 16031 Current Internal Config          | uration | mode does no   | ot suppor | t memory           | initialization           | or ROM  | . Select Internal     | Configuration | mode wi | th ERAM.    |

#### 修改 Device 属性

| Quartus Prime      | Lite Edition - D:/STEP_FPGA/SOC  | S Device                 |  |              |                  |                  |                      |                                     |
|--------------------|--|--------------------------|--|--------------|------------------|------------------|----------------------|-------------------------------------|
|                    | 2 C oc8051 ·   | Device Board             |  |              |                  |                  |                      |                                     |
| Project Navigator  | A Hierarchy 🔹  | Select the family and d  | evice you want to ta                             | arget for co | mpilation.       |                  |                      |                                     |
| , ,                | EntiticInstance  | You can install addition | al device support w                              | ith the Ins  | tall Devices com | mand on the T    | ools menu.           |                                     |
| MAX 10: 10M08      | SAM153C8G  | To determine the versi   | on of the Quartus P                              | rime softw   | are in which you | ir target device | is supported, refer  | to the Device Support List webpage. |
| > 👎 oc8051_top 🕯   | 6  | Device family            |  |              |                  | Show in 'Ava     | ilable devices' list | ~                                   |
|                    |  | Family: MAX TO (DA)      | DF/DC/SA/SC)                                     |              | •                | Package:         | MBGA                 | •                                   |
|                    |  | Device: All              | Device: All                                      |              |                  |                  | 153                  | •                                   |
|                    |  | Target device            | Target device Core speed grade: Any Name filter: |              |                  |                  |                      | -                                   |
|                    |  |                          |  |              |                  |                  |                      |                                     |
|                    |  | Auto device selec        | ted by the Fitter                                |              |                  | Show an          | lyancod dovicor      |                                     |
|                    |  | Specific device se       | lected in 'Available                             | devices' lis | t r              | - Show ac        | vanced devices       |                                     |
|                    |  | O Other: n/a             |  |              |                  | Device and P     | in Options           |                                     |
| lasks 🛛            | Compilation •  | Available devices:       |  |              |                  |                  |                      |                                     |
|                    | Task   | Name                     | Core Voltage                                     | LES          | Total I/Os       | GPIOs            | Memory Bits          | Embedded multiplier 9-bit ^         |
| 🗸 🕨 Compile        | e Design   | 10M04SAM153I7G           | 3.3V   | 4032         | 112              | 112              | 193536               | 40                                  |
| × > > Analy        | ysis & Synthesis   | 10M04SCM153C8G           | 3.3V   | 4032         | 112              | 112              | 193536               | 40                                  |
| > Fitter           | (Place & Route)  | 10M04SCM153I7G           | 3.3V   | 4032         | 112              | 112              | 193536               | 40                                  |
| > Asser            | mbler (Generate programming files)   | 10M08SAM153C8G           | 3.3V   | 8064         | 112              | 112              | 387072               | 48                                  |
| > > Time           | Quest Timing Analysis  | 10M08SAM153C8GES         | 3.3V   | 8064         | 112              | 112              | 387072               | 48                                  |
| > EDA N            | Netlist Writer   | 10M08SAM153I7G           | 3.3V   | 8064         | 112              | 112              | 387072               | 48                                  |
| <                  |  | 10M08SCM153C8G           | 3.3V   | 8064         | 112              | 112              | 387072               | 48                                  |
| All O A            | Image: A state of the state | 10M08SCM153I7G           | 3 3V   | 8064         | 112              | 112              | 387072               | 48 >                                |
| TVDF TD<br>0 16031 | Message<br>Current Internal Configu<br>Quartus Prime Analysis &  | Migration Devices 0      | migration devices                                | selected     |                  |                  |                      |                                     |
| sages              |  |                          |  |              |                  | ₩ Bi             | y Software           | OK Cancel Help                      |

| General   | Configuration  |  |
|---|--|--|
| Configuration   | Specify the device configuration scheme a  | nd the configuration device.   |
| Programming Files<br>Unused Pins<br>Dual-Purpose Pins<br>Capacitive Loading<br>Board Trace Model<br>I/O Timing<br>Voltage<br>Pin Placement<br>Error Detection CRC | Configuration scheme: Internal Configurat<br>Configuration mode: Single Uncompress<br>Configuration device Dual Compressed<br>Single Compresses<br>Single Compresses<br>Single Uncompress<br>Single Uncompresses | tion<br>ssed Image with Memory Initialization (256Kbits UFM)<br>Images (256Kbits UFM)<br>d Image (1376Kbits UFM)<br>d Image with Memory Initialization (256Kbits UFM)<br>ssed Image (912Kbits UFM)<br>ssed Image with Memory Initialization (256Kbits UFM) |
| CvP Settings  | Configuration device I/O voltage:  |  |
| Partial Reconfiguration   | Force VCCIO to be compatible with co   | onfiguration I/O voltage   |
|   | VID Operation mode   |  |
|   | Configuration pin:   | Configuration Pin Options  |
|   | Generate compressed bitstreams   |  |
|   | Active serial clock source:  |  |
|   | Enable input tri-state on active configur  | ration pins in user mode   |
|   | Description:   |  |
|   | Specifies the configuration mode used wit  | h the configuration scheme for configuring the device.   |
|   |  | Reset  |
|   |  | OK Cancel Help   |

#### (3) RTL 仿真

|   | <u>T</u> ools | <u>W</u> indow <u>H</u> elp               |          |                        |
|---|---------------|---|----------|------------------------|
|   | R             | un Sim <u>u</u> lation Tool               | N.       | <u>R</u> TL Simulation |
| 1 | ሔ L           | aunch Simulation Library <u>C</u> ompiler | <b>R</b> | Gate Level Simulation  |

| Wave            |          |          |  |  |  | 1.000 |          |  |  |  |  |  |  |
|-----------------|----------|----------|--|--|--|-------|----------|--|--|--|--|--|--|
| <b>\$</b> 1.    | Msgs     |          |  |  |  |       |          |  |  |  |  |  |  |
| 4/oc8051_tb/rst | 1        |          |  |  |  |       |          |  |  |  |  |  |  |
|                 | 1        |          |  |  |  |       |          |  |  |  |  |  |  |
|                 | 11111111 | 11111111 |  |  |  |       | 01010101 |  |  |  |  |  |  |

参考来源:网友 leishangwen 的《DE2 上使用 OC8051 运行点灯程序》:

https://download.csdn.net/download/leishangwen/5173363